- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Operating Temperature Ranges:**
  - **Military (M) −55°C to 125°C**
- **High-Performance Floating-Point Digital Signal Processor (DSP):**
  - **SM320LC31-40EP (3.3 V)**
    **50-ns Instruction Cycle Time**
    **220 MOPS, 40 MFLOPS, 20 MIPS**
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **32-Bit Instruction and Data Words, 24-Bit Addresses**
- **Two 1K Word × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks**
- **Boot-Program Loader**
- **64-Word × 32-Bit Instruction Cache**
- **Eight Extended-Precision Registers**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two Low-Power Modes**
- **On-Chip Memory-Mapped Peripherals:**
  - **One Serial Port Supporting 8-/16-/24-/32-Bit Transfers**
  - **Two 32-Bit Timers**
  - **One-Channel Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation**
- **Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI)**
- **Two- and Three-Operand Instructions**
- **40 / 32-Bit Floating-Point / Integer Multiplier and Arithmetic Logic Unit (ALU)**
- **Parallel ALU and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **Bus-Control Registers Configure Strobe-Control Wait-State Generation**
- **Validated Ada Compiler**
- **Integer, Floating-Point, and Logical Operations**
- **32-Bit Barrel Shifter**
- **One 32-Bit Data Bus (24-Bit Address)**
- **Packaging**
  - **132-Lead Plastic Quad Flatpack (PQ Suffix)**

## description

The SM320LC31-EP digital signal processor (DSP) is a 32-bit, floating-point processor manufactured in 0.6-µm triple-level-metal CMOS technology. The device is part of the SMJ320C3x generation of DSPs from Texas Instruments.

The SM320LC31-EP internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 60 MFLOPS. The SM320LC31-EP optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## description (continued)

The SM320LC31-EP can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The SM320LC31-EP supports a wide variety of system applications from host processor to dedicated coprocessor.

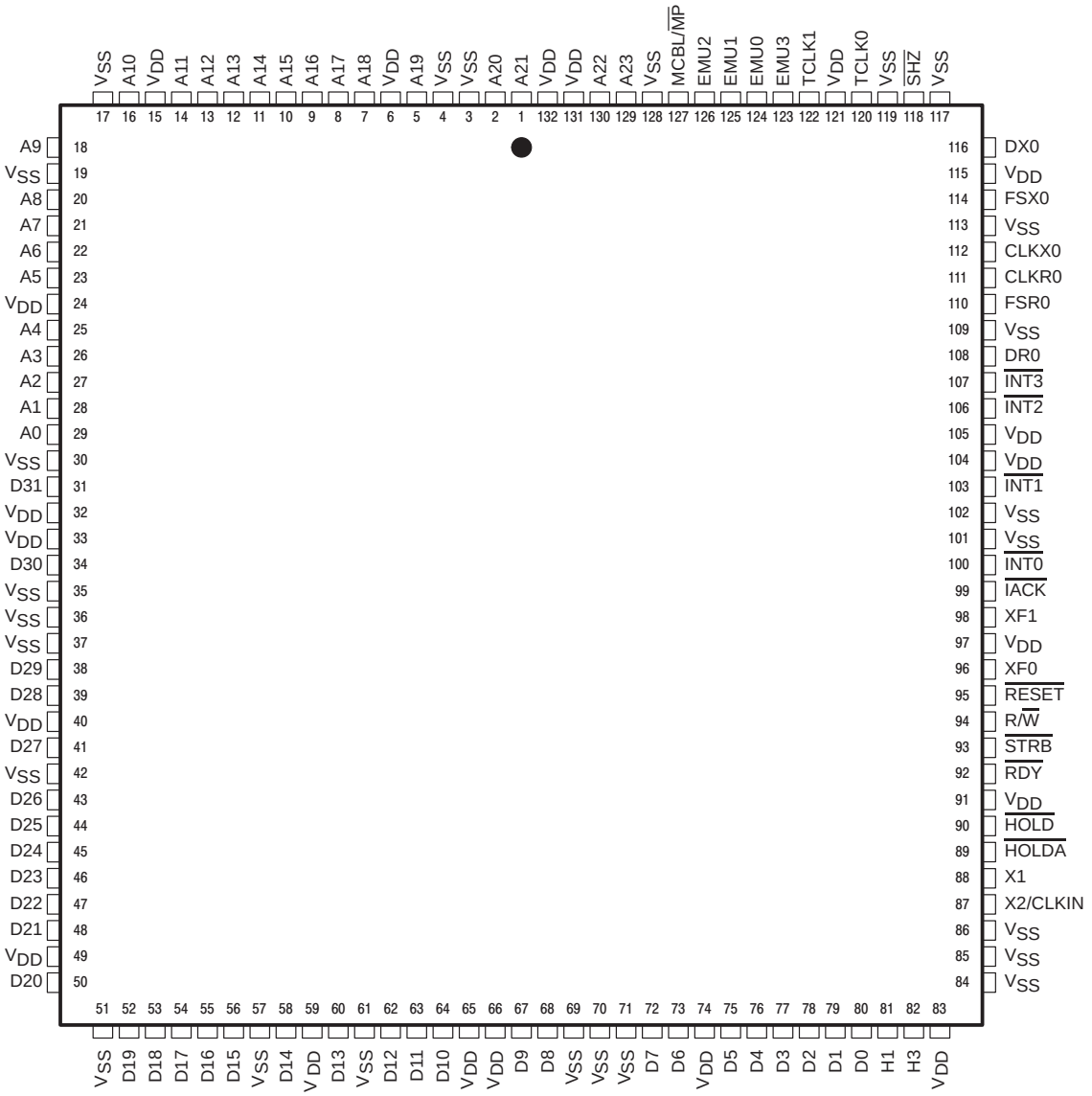
High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

For additional information when designing for cold temperature operation, please see Texas Instruments application report *320C3x, 320C4x and 320MCM42x Power-up Sensitivity at Cold Temperature*, literature number SGUA001.

## SM320LC31-EP pinout (top view)

The SM320LC31-EP device is packaged in a132-pin plastic quad flatpack (PQ Suffix). The full part number is SM320LC31PQM40EP.

**PQ PACKAGE**
**(TOP VIEW)**



## Terminal Assignments (PQ Package)

| PIN NUMBER | PIN NAME | PIN NUMBER | PIN NAME | PIN NUMBER | PIN NAME | PIN NUMBER | PIN NAME |
|---|---|---|---|---|---|---|---|
| 29 | A0 | 64 | D10 | 103 | $\overline{\text{INT1}}$ | 30 | $V_{SSL}$† |
| 28 | A1 | 63 | D11 | 106 | $\overline{\text{INT2}}$ | 35 | $V_{SSL}$† |
| 27 | A2 | 62 | D12 | 107 | $\overline{\text{INT3}}$ | 36 | $DV_{SS}$ |
| 26 | A3 | 60 | D13 | 127 | MCBL/$\overline{\text{MP}}$ | 37 | $IV_{SS}$† |
| 25 | A4 | 58 | D14 | 92 | R/$\overline{\text{W}}$ | 42 | $DV_{SS}$ |
| 23 | A5 | 56 | D15 | 95 | $\overline{\text{RDY}}$ | 51 | $CV_{SS}$† |
| 22 | A6 | 55 | D16 | 94 | $\overline{\text{RESET}}$ | 57 | $IV_{SS}$† |
| 21 | A7 | 54 | D17 | 118 | $\overline{\text{SHZ}}$ | 61 | $DV_{SS}$ |
| 20 | A8 | 53 | D18 | 93 | $\overline{\text{STRB}}$ | 69 | $V_{SSL}$† |
| 18 | A9 | 52 | D19 | 120 | TCLK0 | 70 | $V_{SSL}$† |
| 16 | A10 | 50 | D20 | | | 71 | $DV_{SS}$ |
| 14 | A11 | 48 | D21 | | | 84 | $CV_{SS}$† |
| 13 | A12 | 47 | D22 | 6 | $AV_{DD}$‡ | 85 | $IV_{SS}$† |
| 12 | A13 | 46 | D23 | 15 | $AV_{DD}$‡ | 86 | $DV_{SS}$ |
| 11 | A14 | 45 | D24 | 24 | $V_{DDL}$ | 101 | $V_{SSL}$† |
| 10 | A15 | 44 | D25 | 32 | $V_{DDL}$ | 102 | $CV_{SS}$† |
| 9 | A16 | 43 | D26 | 33 | $DV_{DD}$‡ | 109 | $IV_{SS}$† |
| 8 | A17 | 41 | D27 | 40 | $DV_{DD}$‡ | 113 | $V_{SUBS}$§ |
| 7 | A18 | 39 | D28 | 49 | $DV_{DD}$‡ | 117 | $DV_{SS}$ |
| 5 | A19 | 38 | D29 | 59 | $V_{DDL}$ | 119 | $CV_{SS}$† |
| 2 | A20 | 34 | D30 | 65 | $V_{DDL}$ | 128 | X1 |
| 1 | A21 | 31 | D31 | 66 | $DV_{DD}$‡ | 88 | X2/CLKIN |
| 130 | A22 | 108 | DR0 | 74 | $DV_{DD}$‡ | 87 | XF0 |
| 129 | A23 | 116 | DX0 | 83 | $CV_{DD}$‡ | 96 | XF1 |
| 111 | CLKR0 | 124 | EMU0 | 91 | $CV_{DD}$‡ | 98 | No Connect |
| 112 | CLKX0 | 125 | EMU1 | 97 | $V_{DDL}$ | | |
| 80 | D0 | 126 | EMU2 | 104 | $V_{DDL}$ | | |
| 79 | D1 | 123 | EMU3 | 105 | $PV_{DD}$‡ | | |
| 78 | D2 | 110 | FSR0 | 115 | $PV_{DD}$‡ | | |
| 77 | D3 | 114 | FSX0 | 121 | $V_{DDL}$ | | |
| 76 | D4 | 81 | $\overline{\text{HOLD}}$ | 131 | $V_{DDL}$ | | |
| 75 | D5 | 82 | $\overline{\text{HOLDA}}$ | 132 | $V_{SSL}$† | | |
| 73 | D6 | 90 | H1 | 3 | $DV_{SS}$ | | |
| 72 | D7 | 89 | H3 | 4 | $CV_{SS}$† | | |
| 68 | D8 | 99 | $\overline{\text{IACK}}$ | 17 | $DV_{SS}$ | | |
| 67 | D9 | 100 | $\overline{\text{INT0}}$ | 19 | $CV_{SS}$† | | |

† $CV_{SS}$, $V_{SSL}$, and $IV_{SS}$ are on the same plane.
‡ $AV_{DD}$, $DV_{DD}$, $CV_{DD}$, and $PV_{DD}$ are on the same plane.
§ $V_{SUBS}$ connects to die metallization. Tie this pin to clean ground.

## Terminal Functions

| TERMINAL NAME | QTY | TYPE† | DESCRIPTION | CONDITIONS WHEN SIGNAL IS Z TYPE‡ | | |
|---|---|---|---|---|---|---|
| **PRIMARY-BUS INTERFACE** | | | | | | |
| D31−D0 | 32 | I/O/Z | 32-bit data port | S | H | R |
| A23−A0 | 24 | O/Z | 24-bit address port | S | H | R |
| R/$\overline{W}$ | 1 | O/Z | Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface. | S | H | R |
| $\overline{STRB}$ | 1 | O/Z | External-access strobe | S | H | |
| $\overline{RDY}$ | 1 | I | Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion. | | | |
| $\overline{HOLD}$ | 1 | I | Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23−A0, D31−D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set. | | | |
| $\overline{HOLDA}$ | 1 | O/Z | Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23−A0, D31−D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set. | S | | |
| **CONTROL SIGNALS** | | | | | | |
| $\overline{RESET}$ | 1 | I | Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector. | | | |
| $\overline{INT3}$−$\overline{INT0}$ | 4 | I | External interrupts | | | |
| $\overline{IACK}$ | 1 | O/Z | Interrupt acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate the beginning or the end of an interrupt-service routine. | S | | |
| MCBL/$\overline{MP}$ | 1 | I | Microcomputer boot-loader/microprocessor mode-select | | | |
| $\overline{SHZ}$ | 1 | I | Shutdown high impedance. When active, $\overline{SHZ}$ shuts down the device and places all pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition. | | | |
| XF1, XF0 | 2 | I/O/Z | External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction. | S | | R |
| **SERIAL PORT 0 SIGNALS** | | | | | | |
| CLKR0 | 1 | I/O/Z | Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver. | S | | R |
| CLKX0 | 1 | I/O/Z | Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter. | S | | R |
| DR0 | 1 | I/O/Z | Data-receive. Serial port 0 receives serial data on DR0. | S | | R |
| DX0 | 1 | I/O/Z | Data-transmit output. Serial port 0 transmits serial data on DX0. | S | | R |
| FSR0 | 1 | I/O/Z | Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0. | S | | R |
| FSX0 | 1 | I/O/Z | Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0. | S | | R |
| **TIMER SIGNALS** | | | | | | |
| TCLK0 | 1 | I/O/Z | Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0. | S | | |
| TCLK1 | 1 | I/O/Z | Timer clock 1. As an input, TCLK0 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1. | S | | |

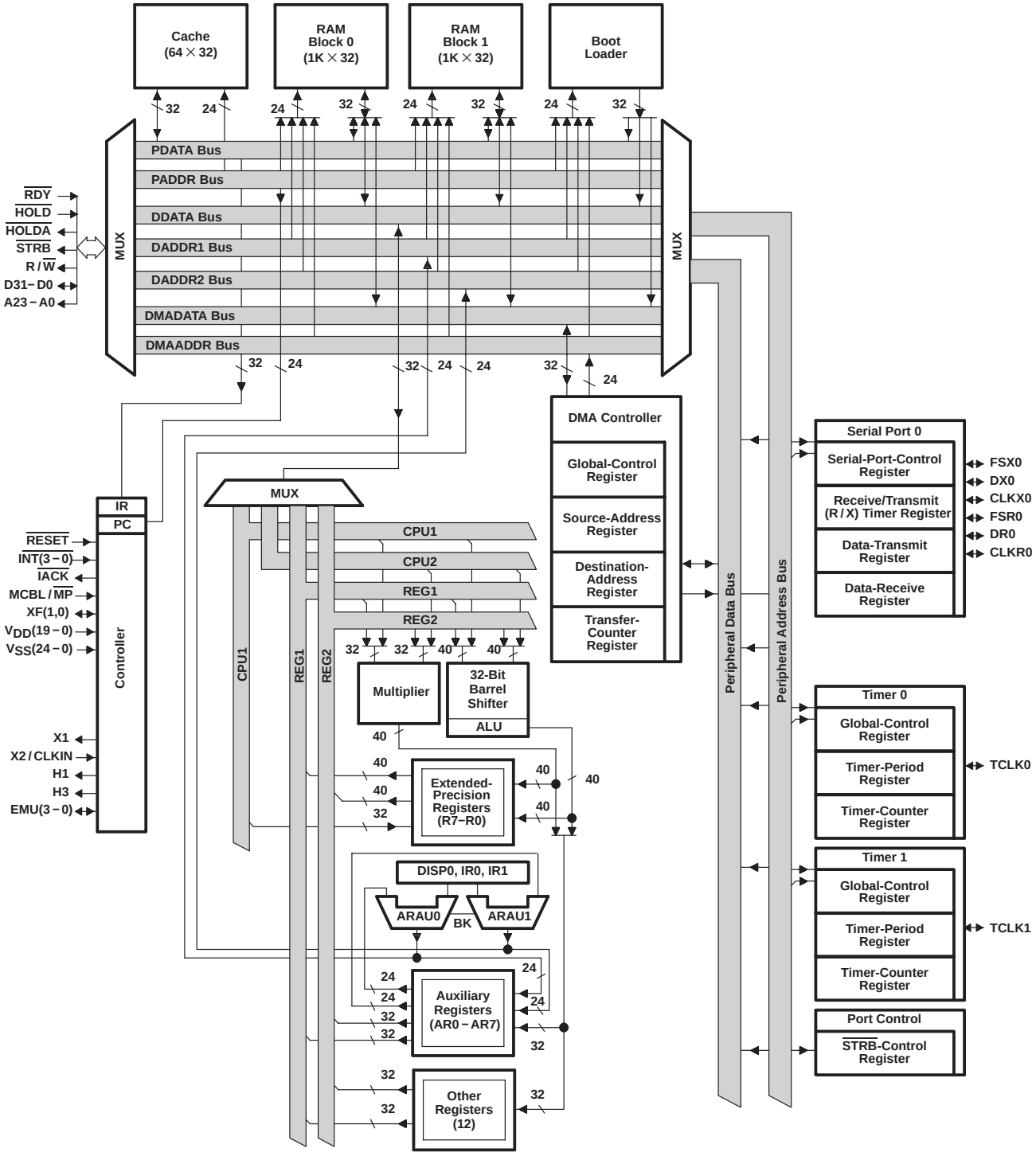
† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

## Terminal Functions (Continued)

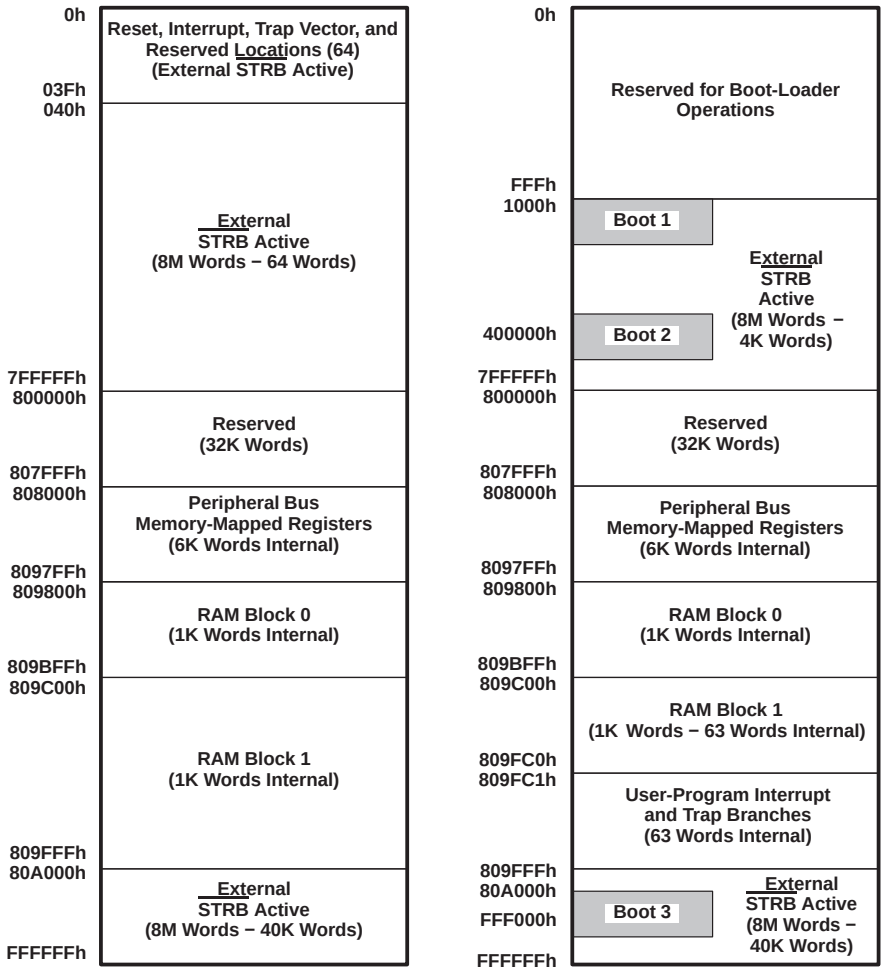
| TERMINAL NAME | TERMINAL QTY | TYPE† | DESCRIPTION | CONDITIONS WHEN SIGNAL IS Z TYPE‡ |
|---|---|---|---|---|
| **SUPPLY AND OSCILLATOR SIGNALS** | | | | |
| H1 | 1 | O/Z | External H1 clock. H1 has a period equal to twice CLKIN. | S |
| H3 | 1 | O/Z | External H3 clock. H3 has a period equal to twice CLKIN. | S |
| $V_{DD}$ | 20 | I | 5-V supply for C31 devices and 3.3-V supply for LC31 devices. All must be connected to a common supply plane.§ | |
| $V_{SS}$ | 25 | I | Ground. All grounds must be connected to a common ground plane. | |
| X1 | 1 | O | Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected. | |
| X2/CLKIN | 1 | I | Internal-oscillator input from a crystal or a clock | |
| **RESERVED¶** | | | | |
| EMU2−EMU0 | 3 | I | Reserved for emulation. Use pullup resistors to $V_{DD}$ | |
| EMU3 | 1 | O/Z | Reserved for emulation | S |

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = HOLD active, R = $\overline{RESET}$ active
§ Recommended decoupling capacitor value is 0.1 μF.
¶ Follow the connections specified for the reserved pins. Use 18-kΩ−22-kΩ pullup resistors for best results. All $V_{DD}$ supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

## functional block diagram



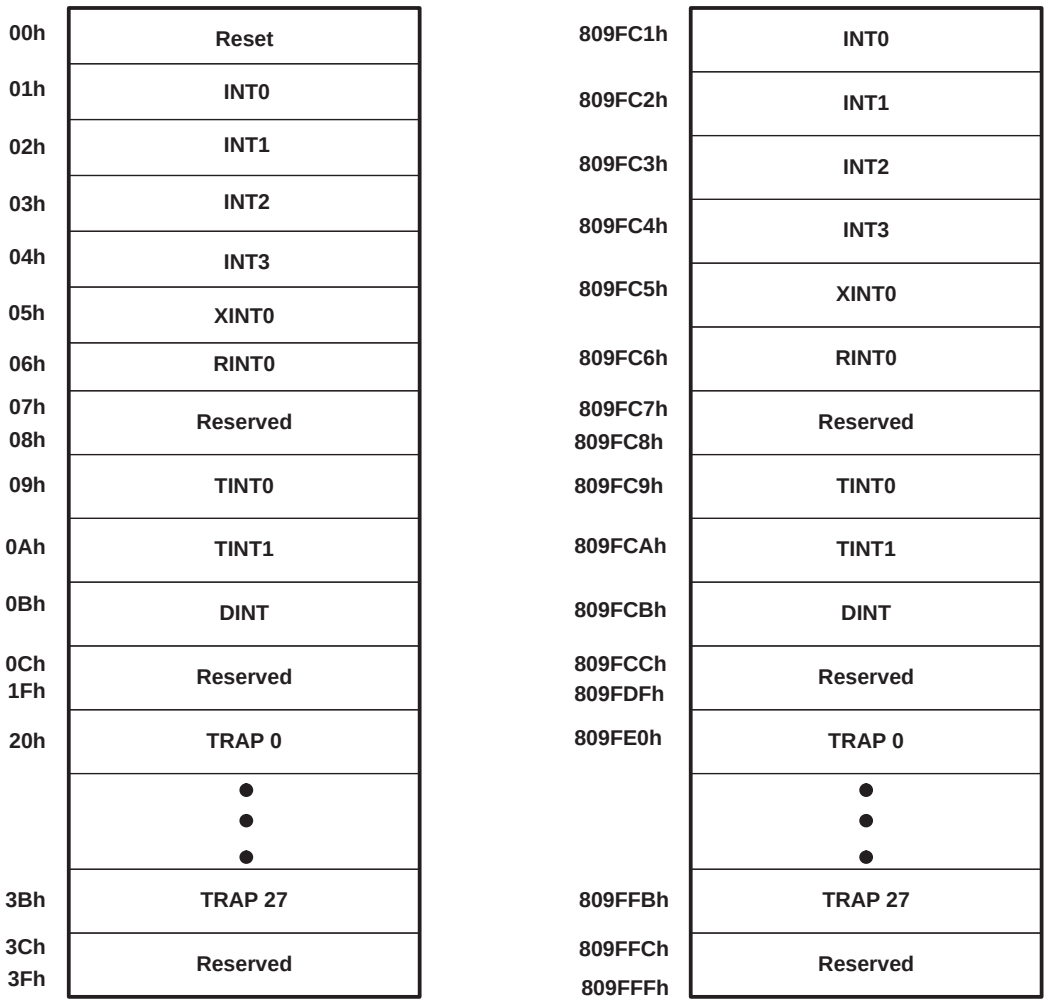
## memory map†




† Figure 1 depicts the memory map for the SMJ320C31. See the *TMS320C3x Users Guide* (literature number SPRU031) for a detailed description of this memory mapping.

**Figure 1. SM320C31-EP Memory Map**

## memory map (continued)




(a) Microprocessor Mode

(b) Microcomputer / Boot-Loader Mode

**Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations**

## memory map (continued)

| | |
|---|---|
| 808000h | DMA Global Control |
| | |
| 808004h | DMA Source Address |
| | |
| 808006h | DMA Destination Address |
| | |
| 808008h | DMA Transfer Counter |
| | |
| 808020h | Timer 0 Global Control |
| | |
| 808024h | Timer 0 Counter |
| | |
| 808028h | Timer 0 Period Register |
| | |
| 808030h | Timer 1 Global Control |
| | |
| 808034h | Timer 1 Counter |
| | |
| 808038h | Timer 1 Period Register |
| | |
| 808040h | Serial Global Control |
| | |
| 808042h | FSX/DX/CLKX Serial Port Control |
| 808043h | FSR/DR/CLKR Serial Port Control |
| 808044h | Serial R/X Timer Control |
| 808045h | Serial R/X Timer Counter |
| 808046h | Serial R/X Timer Period Register |
| | |
| 808048h | Data-Transmit |
| | |
| 80804Ch | Data-Receive |
| | |
| 808064h | Primary-Bus Control |
| | |

†Shading denotes reserved address locations

**Figure 3. Peripheral Bus Memory-Mapped Registers†**

## absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . . . −0.3 V to 5 V
Input voltage, $V_I$ . . . . . −0.3 V to 5 V
Output voltage, $V_O$ . . . . . −0.3 V to 5 V
Continuous power dissipation (worst case) (see Note 2) . . . . . 850 mW
Operating case temperature, $T_C$ . . . . . −55°C to 125°C
Storage temperature, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to $V_{SS}$.
2. Actual operating power is less. This value was obtained under specially produced worst-case test conditions for the TMS320C31-33 and the TMS320LC31-40, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal ($I_{CC}$) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

## recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage ($DV_{DD}$, etc.) | 3.13 | 3.3 | 3.47 | V |
| $V_{SS}$ | Supply voltage ($CV_{SS}$, etc.) | | 0 | | V |
| $V_{IH}$ | High-level input voltage (except $\overline{\text{RESET}}$) | 1.8 | | $V_{DD}$ + 0.3* | V |
| | High-level input voltage ($\overline{\text{RESET}}$) | 2.2 | | $V_{DD}$ + 0.3* | V |
| $V_{IL}$ | Low-level input voltage | − 0.3* | | 0.6 | V |
| $I_{OH}$ | High-level output current | | | − 300 | µA |
| $I_{OL}$ | Low-level output current | | | 2 | mA |
| $T_C$ | Operating case temperature | −55 | | 125 | °C |
| $V_{TH}$ | High-level input voltage for CLKIN | 2.5 | | $V_{DD}$ + 0.3* | V |

* This parameter is not production tested.

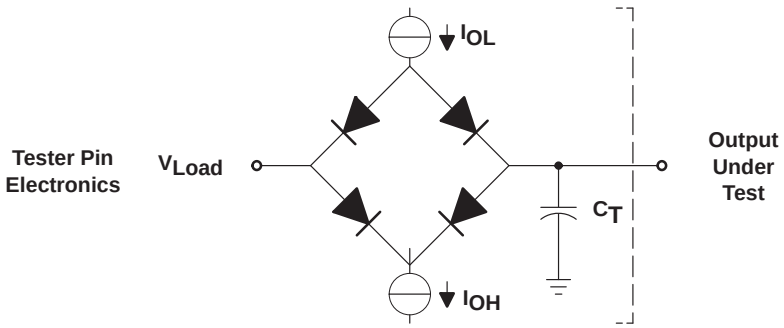
NOTE 3: All voltage values are with respect to $V_{SS}$. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

## electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 3)†

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{DD}$ = MIN, $I_{OH}$ = MAX | | 2 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$ = MIN, $I_{OH}$ = MAX | | | | 0.4 | V |
| $I_Z$ | High-impedance current | $V_{DD}$ = MAX | | − 20 | | + 20 | µA |
| $I_I$ | Input current | $V_I$ = $V_{SS}$ to $V_{DD}$ | | − 10 | | + 10 | µA |
| $I_{IP}$ | Input current (with internal pullup) | Inputs with internal pullups§ | | − 600 | | 10 | µA |
| $I_{CC}$ | Supply current¶# | $T_A$ = 25°C, $V_{DD}$ = MAX | $f_x$ = 40 MHz | | 150 | 300 | mA |
| $I_{DD}$ | Supply current | Standby, IDLE2, Clocks shut off | | | 20 | | µA |
| $C_i$ | Input capacitance | All inputs except CLKIN | | | | 15* | pF |
| | | CLKIN | | | | 25 | |
| $C_o$ | Output capacitance | | | | | 20* | pF |

† All input and output voltage levels are TTL compatible.
‡ For LC31, all typical values are at $V_{DD}$ = 3.3 V, $T_A$ = 25°C.
§ Pins with internal pullup devices: INT3–INT0, MCBL/MP.
¶ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).
# $f_x$ is the input clock frequency.
* This parameter is not production tested.
NOTE 3: All voltage values are with respect to $V_{SS}$. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

## PARAMETER MEASUREMENT INFORMATION




Where: $I_{OL}$ = 2 mA (all outputs)
$I_{OH}$ = 300 µA (all outputs)
$V_{LOAD}$ = 2.15 V
$C_T$ = 80-pF typical load-circuit capacitance

**Figure 4. SM320LC31-EP Test Load Circuit**

## PARAMETER MEASUREMENT INFORMATION

### signal transition levels for LC31 (see Figure 5 and Figure 6)

Outputs are driven to a minimum logic-high level of 2 V and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows:

- For a high-to-low transition on an output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

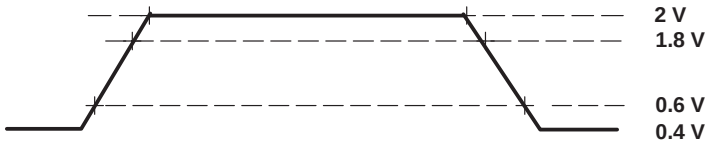



**Figure 5. LC31 Output Levels**

Transition times for inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.8 V and the level at which the input is said to be low is 0.6 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.6 V and the level at which the input is said to be high is 1.8 V.

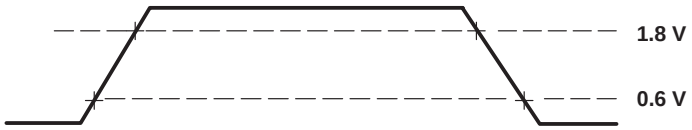



**Figure 6. LC31 Input Levels**

## PARAMETER MEASUREMENT INFORMATION

### timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

| | | | |
|---|---|---|---|
| A | A23−A0 | H | H1 and H3 |
| ASYNCH | Asynchronous reset signals | HOLD | $\overline{\text{HOLD}}$ |
| C | CLKX0 | HOLDA | $\overline{\text{HOLDA}}$ |
| CI | CLKIN | IACK | $\overline{\text{IACK}}$ |
| CLKR | CLKR0 | INT | $\overline{\text{INT3}}$−$\overline{\text{INT0}}$ |
| CONTROL | Control signals | RDY | $\overline{\text{RDY}}$ |
| D | D31−D0 | RW | R/$\overline{\text{W}}$ |
| DR | DR | RESET | $\overline{\text{RESET}}$ |
| DX | DX | S | $\overline{\text{STRB}}$ |
| FS | FSX/R | SCK | CLKX/R |
| FSX | FSX0 | SHZ | $\overline{\text{SHZ}}$ |
| FSR | FSR0 | TCLK | TCLK0, TCLK1, or TCLKx |
| GPI | General-purpose input | XF | XF0, XF1, or XFx |
| GPIO | General-purpose input/output; peripheral pin | XFIO | XFx switching from input to output |
| GPO | General-purpose output | | |

## timing

Timing specifications apply to the SM320LC31-EP.

### X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals.

**timing parameters for X2/CLKIN, H1, H3 (see Figure 7, Figure 8, and Figure 9)**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{f(CI)}$ | Fall time, CLKIN | | 5* | ns |
| 2 | $t_{w(CIL)}$ | Pulse duration, CLKIN low $t_{c(CI)}$ = min | 9 | | ns |
| 3 | $t_{w(CIH)}$ | Pulse duration, CLKIN high $t_{c(CI)}$ = min | 9 | | ns |
| 4 | $t_{r(CI)}$ | Rise time, CLKIN | | 5* | ns |
| 5 | $t_{c(CI)}$ | Cycle time, CLKIN | 25 | 303 | ns |
| 6 | $t_{f(H)}$ | Fall time, H1 and H3 | | 3 | ns |
| 7 | $t_{w(HL)}$ | Pulse duration, H1 and H3 low | P−5† | | ns |
| 8 | $t_{w(HH)}$ | Pulse duration, H1 and H3 high | P−6† | | ns |
| 9 | $t_{r(H)}$ | Rise time, H1 and H3 | | 3 | ns |
| 10 | $t_{d(HL-HH)}$ | Delay time. from H1 low to H3 high or from H3 low to H1 high | 0 | 4 | ns |
| 11 | $t_{c(H)}$ | Cycle time, H1 and H3 | 50 | 606 | ns |

† P = $t_{c(CI)}$
* This parameter is not production tested.

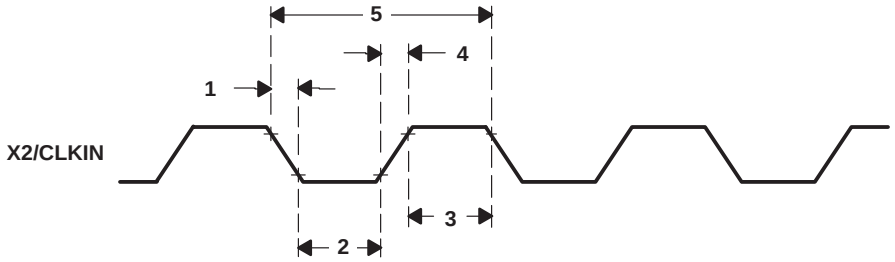



**Figure 7. Timing for X2/CLKIN**

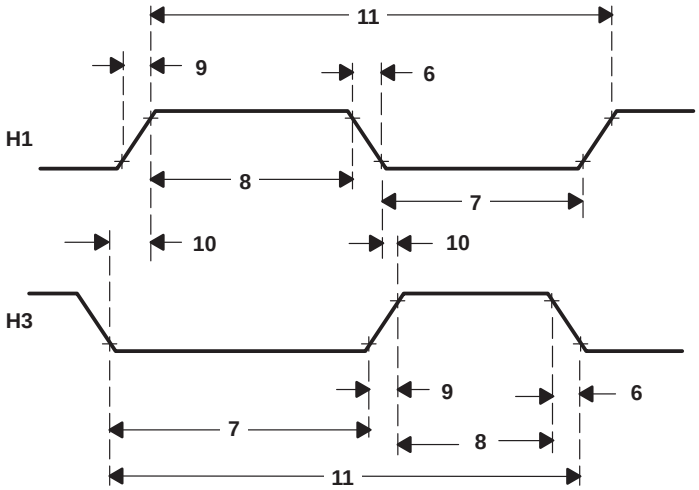



**Figure 8. Timing for H1 and H3**

## X2/CLKIN, H1, and H3 timing (continued)

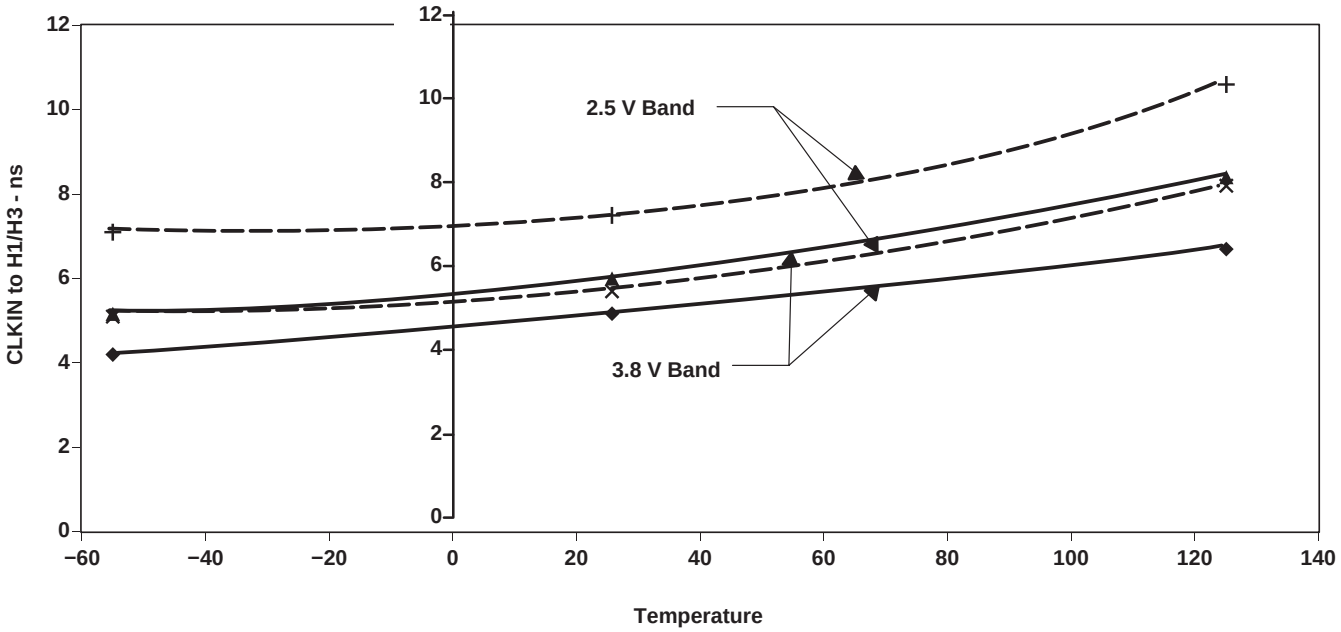



**Figure 9. SM320LC31-EP CLKIN to H1/H3 as a Function of Temperature (Typical)**

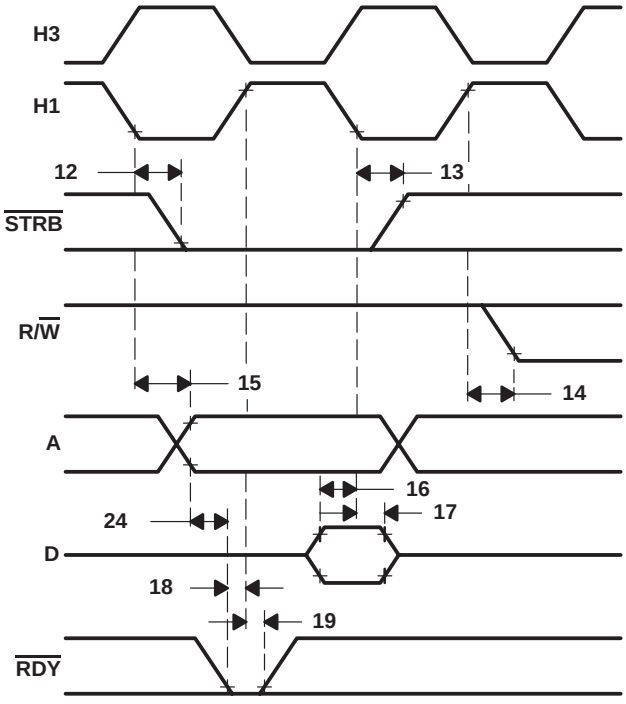
### memory read/write timing

The following table defines memory read/write timing parameters for $\overline{\text{STRB}}$.

### timing parameters for memory ($\overline{\text{STRB}}$ = 0) read/write (see Figure 10 and Figure 11)†

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 12 | $t_{d(H1L-SL)}$ | Delay time, H1 low to $\overline{\text{STRB}}$ low | 0* | 6 | ns |
| 13 | $t_{d(H1L-SH)}$ | Delay time, H1 low to $\overline{\text{STRB}}$ high | 0* | 6 | ns |
| 14 | $t_{d(H1H-RWL)R}$ | Delay time, H1 high to R/$\overline{\text{W}}$ low (read) | 0* | 9 | ns |
| 15 | $t_{d(H1L-A)}$ | Delay time, H1 low to A valid | 0* | 10 | ns |
| 16 | $t_{su(D-H1L)R}$ | Setup time, D before H1 low (read) | 14 | | ns |
| 17 | $t_{h(H1L-D)R}$ | Hold time, D after H1 low (read) | 0 | | ns |
| 18 | $t_{su(RDY-H1H)}$ | Setup time, $\overline{\text{RDY}}$ before H1 high | 8 | | ns |
| 19 | $t_{h(H1H-RDY)}$ | Hold time, $\overline{\text{RDY}}$ after H1 high | 0 | | ns |
| 20 | $t_{d(H1H-RWH)W}$ | Delay time, H1 high to R/$\overline{\text{W}}$ high (write) | | 9 | ns |
| 21 | $t_{v(H1L-D)W}$ | Valid time, D after H1 low (write) | | 17 | ns |
| 22 | $t_{h(H1H-D)W}$ | Hold time, D after H1 high (write) | 0 | | ns |
| 23 | $t_{d(H1H-A)W}$ | Delay time, H1 high to A valid on back-to-back write cycles (write) | | 15 | ns |
| 24 | $t_{d(A-RDY)}$ | Delay time, $\overline{\text{RDY}}$ from A valid | | 7* | ns |

† See Figure 12 for address bus timing variation with load capacitance greater than typical load-circuit capacitance ($C_T$ = 80 pF).
* This parameter is not production tested.




NOTE A: $\overline{\text{STRB}}$ remains low during back-to-back read operations.

**Figure 10. Timing for Memory ($\overline{\text{STRB}}$ = 0) Read**

**memory read/write timing (continued)**

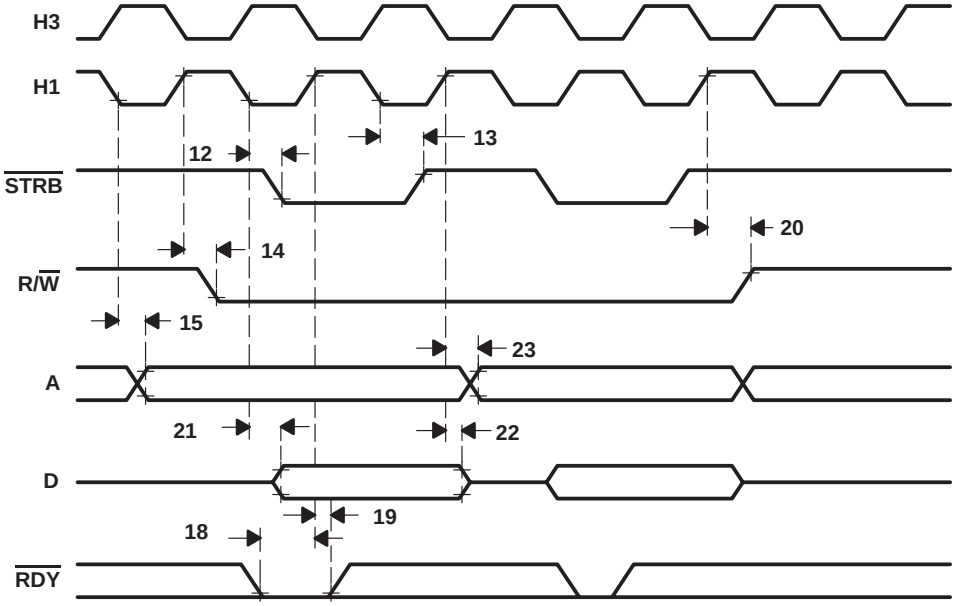
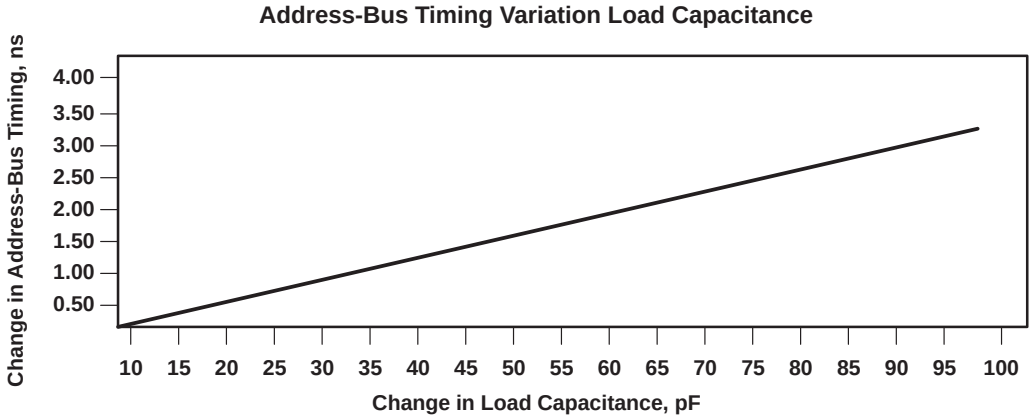



**Figure 11. Timing for Memory ($\overline{\text{STRB}}$ = 0) Write**




NOTE A: 30 pF/ns slope

**Figure 12. Address-Bus Timing Variation With Load Capacitance (see Note A)**

### XF0 and XF1 timing when executing LDFI or LDII

The following table defines the timing parameters for XF0 and XF1 during execution of LDFI or LDII.

### timing for XF0 and XF1 when executing LDFI or LDII (see Figure 13)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 25 | $t_{d(H3H-XF0L)}$ | Delay time, H3 high to XF0 low | | 13 | ns |
| 26 | $t_{su(XF1-H1L)}$ | Setup time, XF1 before H1 low | 10 | | ns |
| 27 | $t_{h(H1L-XF1)}$ | Hold time, XF1 after H1 low | 0 | | ns |

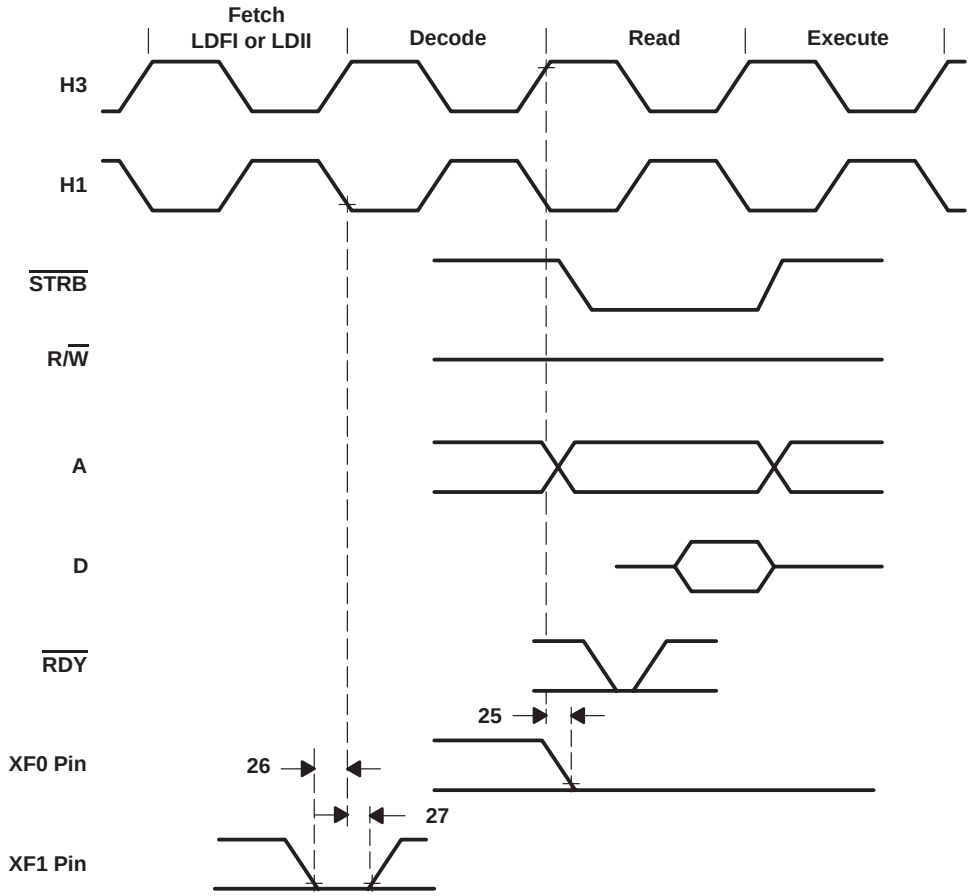



**Figure 13. Timing for XF0 and XF1 When Executing LDFI or LDII**

### XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII.

### timing for XF0 when executing STFI or STII (see Figure 14)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 28 | $t_{d(H3H-XF0H)}$ | Delay time, H3 high to XF0 high | | 13 | ns |

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

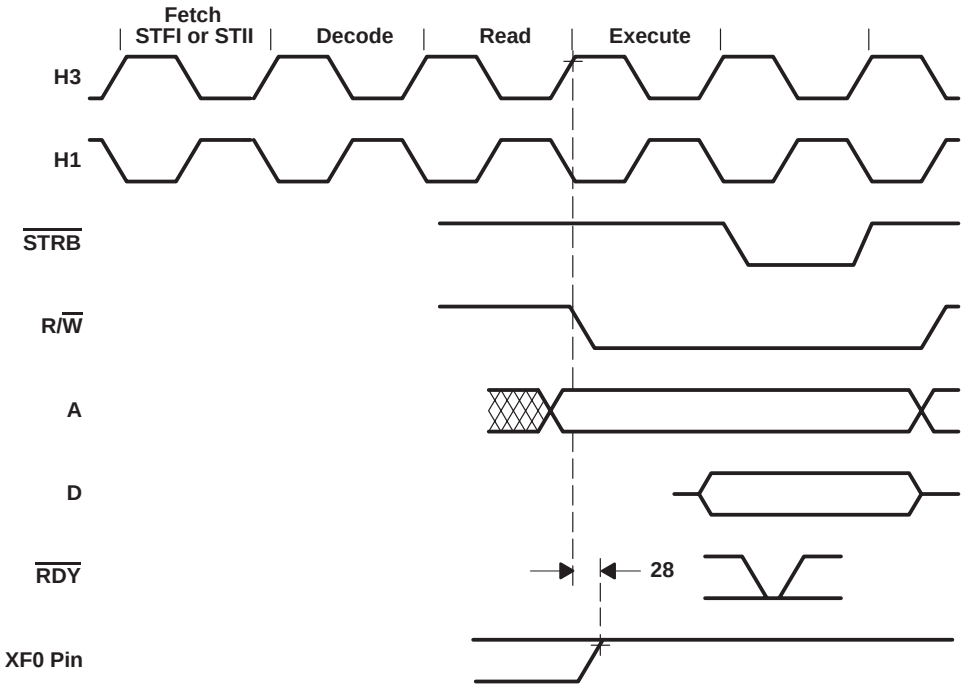



**Figure 14. Timing for XF0 When Executing an STFI or STII**

### XF0 and XF1 timing when executing SIGI

The following table defines the timing parameters for the XF0 and XF1 pins during execution of SIGI.

### timing for XF0 and XF1 when executing SIGI (see Figure 15)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 29 | $t_{d(H3H-XF0L)}$ | Delay time, H3 high to XF0 low | | 13 | ns |
| 30 | $t_{d(H3H-XF0H)}$ | Delay time, H3 high to XF0 high | | 13 | ns |
| 31 | $t_{su(XF1-H1L)}$ | Setup time, XF1 before H1 low | 10 | | ns |
| 32 | $t_{h(H1L-XF1)}$ | Hold time, XF1 after H1 low | 0 | | ns |

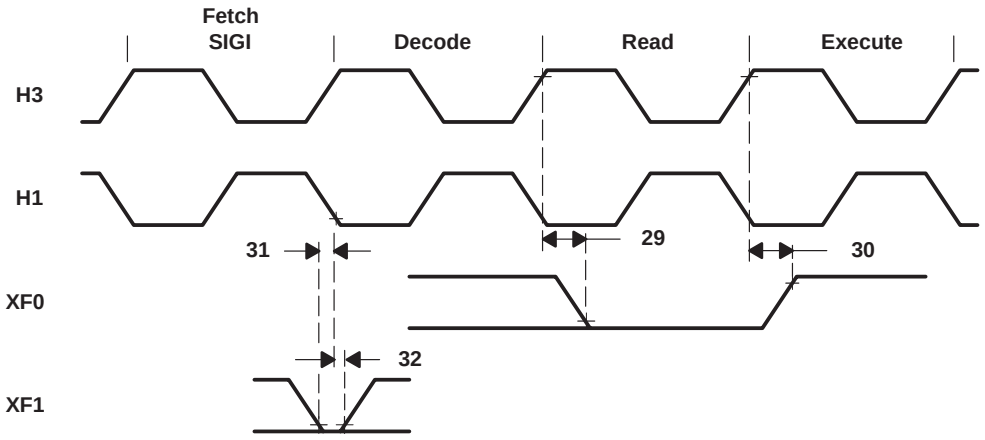


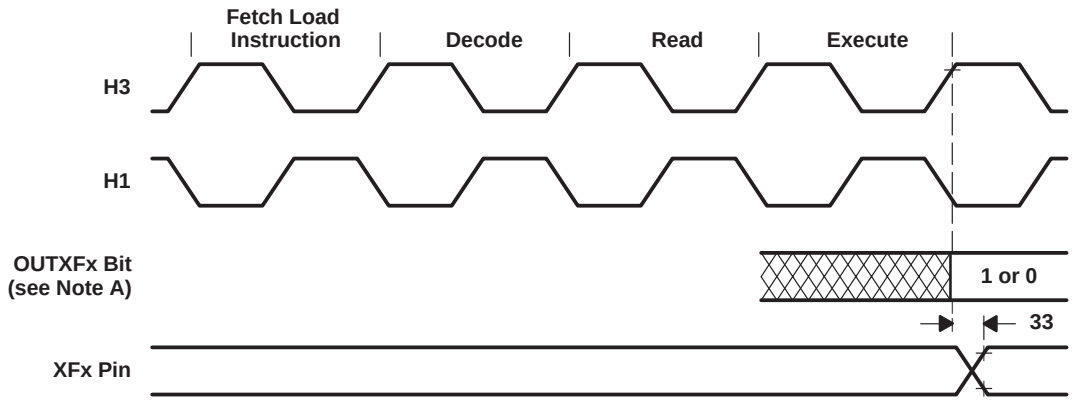

**Figure 15. Timing for XF0 and XF1 When Executing SIGI**

### loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output.

### timing for loading the XF register when configured as an output pin (see Figure 16)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 33 | $t_{v(H3H-XF)}$ | Valid time, H3 high to XFx | | 13 | ns |




NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

**Figure 16. Timing for Loading XF Register When Configured as an Output Pin**

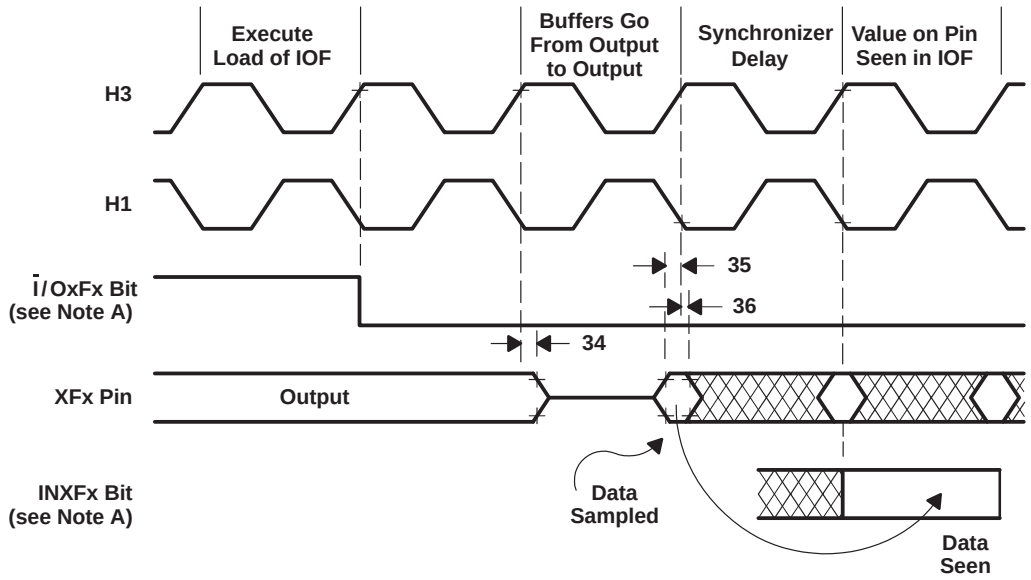
### changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin.

### timing of XFx changing from output to input mode (see Figure 17)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 34 | $t_{h(H3H-XF)}$ | Hold time, XFx after H3 high | | 13* | ns |
| 35 | $t_{su(XF-H1L)}$ | Setup time, XFx before H1 low | 10 | | ns |
| 36 | $t_{h(H1L-XF)}$ | Hold time, XFx after H1 low | 0 | | ns |

* This parameter is not production tested.




NOTE A: $\overline{I}$/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

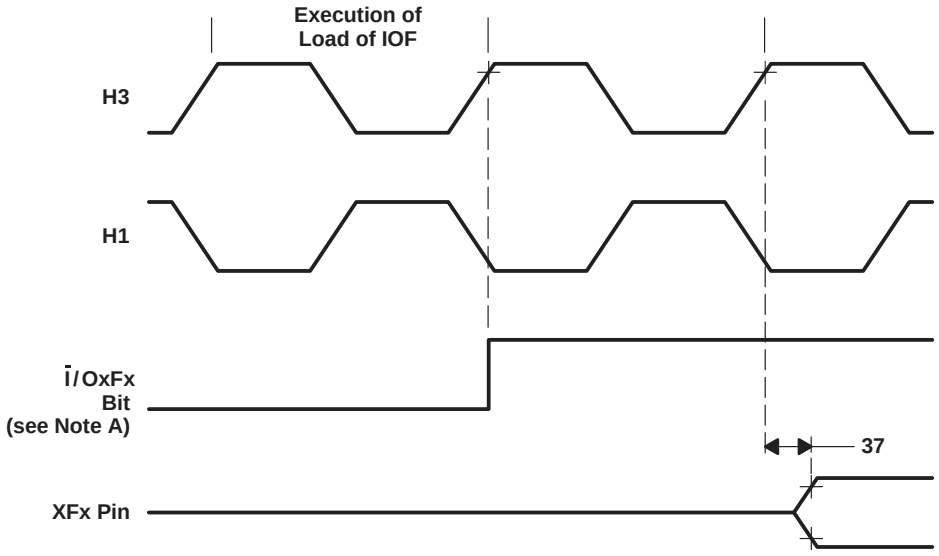
**Figure 17. Timing for Change of XFx From Output to Input Mode**

### changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin.

### timing for XFx changing from input to output mode (see Figure 18)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 37 | $t_{d(H3H-XFIO)}$ | Delay time, H3 high to XFx switching from input to output | | 17 | ns |




NOTE A: I/OxFx represents either bit 1 or bit 5 of the IOF register.

**Figure 18. Timing for Change of XFx From Input to Output Mode**

### reset timing

RESET is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 19 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

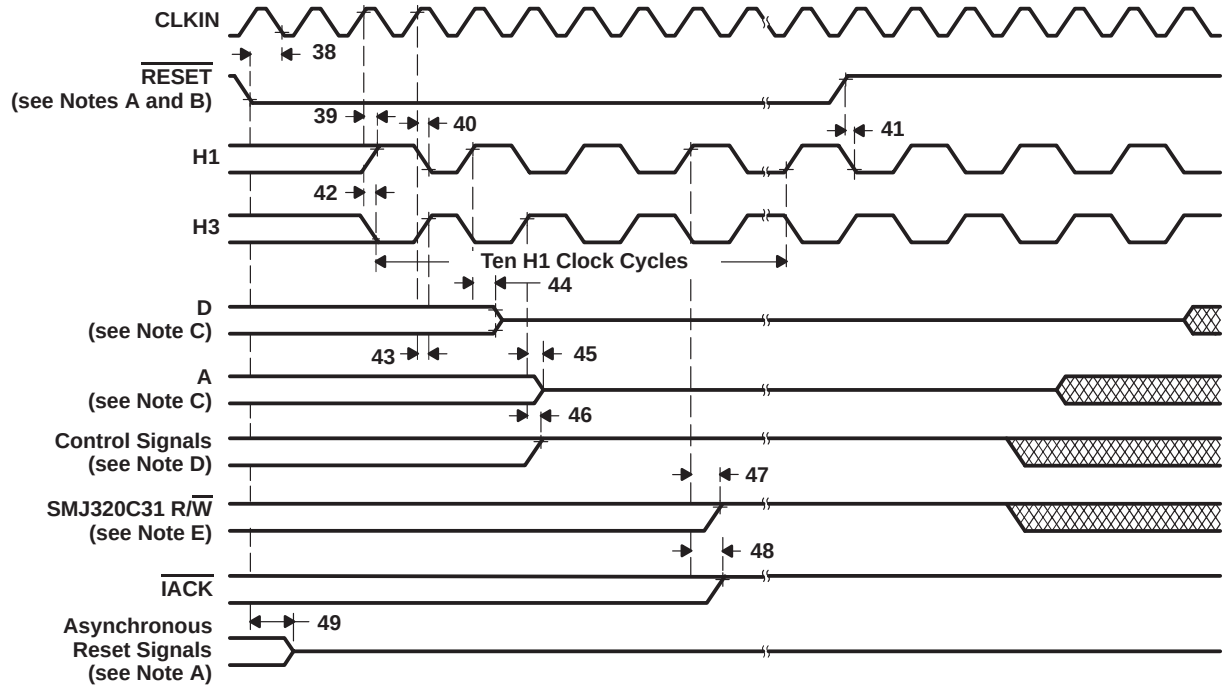
Resetting the device initializes the primary- and expansion-bus control registers to seven software wait states and therefore results in slow external accesses until these registers are initialized.

HOLD is an asynchronous input and can be asserted during reset.

## $\overline{\text{RESET}}$ timing (see Figure 19)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 38 | $t_{su(RESET-CIL)}$ | Setup time, $\overline{\text{RESET}}$ before CLKIN low | 10 | P†* | ns |
| 39 | $t_{d(CLKINH-H1H)}$ | Delay time, CLKIN high to H1 high (see Note 4) | 2 | 14 | ns |
| 40 | $t_{d(CLKINH-H1L)}$ | Delay time, CLKIN high to H1 low (see Note 4) | 2 | 14 | ns |
| 41 | $t_{su(RESETH-H1L)}$ | Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles | 9 | | ns |
| 42 | $t_{d(CLKINH-H3L)}$ | Delay time, CLKIN high to H3 low (see Note 4) | 2 | 14 | ns |
| 43 | $t_{d(CLKINH-H3H)}$ | Delay time, CLKIN high to H3 high (see Note 4) | 2 | 14 | ns |
| 44 | $t_{dis(H1H-DZ)}$ | Disable time, H1 high to D (high impedance) | | 13* | ns |
| 45 | $t_{dis(H3H-AZ)}$ | Disable time, H3 high to A (high impedance) | | 9* | ns |
| 46 | $t_{d(H3H-CONTROLH)}$ | Delay time, H3 high to control signals high | | 9* | ns |
| 47 | $t_{d(H1H-RWH)}$ | Delay time, H1 high to R/$\overline{\text{W}}$ high | | 9* | ns |
| 48 | $t_{d(H1H-IACKH)}$ | Delay time, H1 high to $\overline{\text{IACK}}$ high | | 9* | ns |
| 49 | $t_{dis(RESETL-ASYNCH)}$ | Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals disabled (high impedance) | | 21* | ns |

† P = $t_{c(CI)}$
* This parameter is not production tested.
NOTE 4: See Figure 9 for typical temperature dependence.




NOTES: A. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
B. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
C. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
D. Control signals include $\overline{\text{STRB}}$.
E. The R/$\overline{\text{W}}$ outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18−22 kΩ, if undesirable spurious writes are caused when these outputs go low.

**Figure 19. Timing for $\overline{\text{RESET}}$**

### interrupt response timing

The following table defines the timing parameters for the $\overline{INT}$ signals.

### timing for $\overline{INT3}$−$\overline{INT0}$ response (see Figure 20)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 50 | $t_{su(INT-H1L)}$ | Setup time, $\overline{INT3}$−$\overline{INT0}$ before H1 low | 15 | | ns |
| 51 | $t_{w(INT)}$ | Pulse duration, interrupt to ensure only one interrupt | P | 2P†* | ns |

† $P = t_{c(H)}$
* This parameter is not production tested.

The interrupt ($\overline{INT}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The SM320LC31-EP interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The SM320LC31-EP can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 20 occurs; otherwise, an additional delay of one clock cycle is possible.

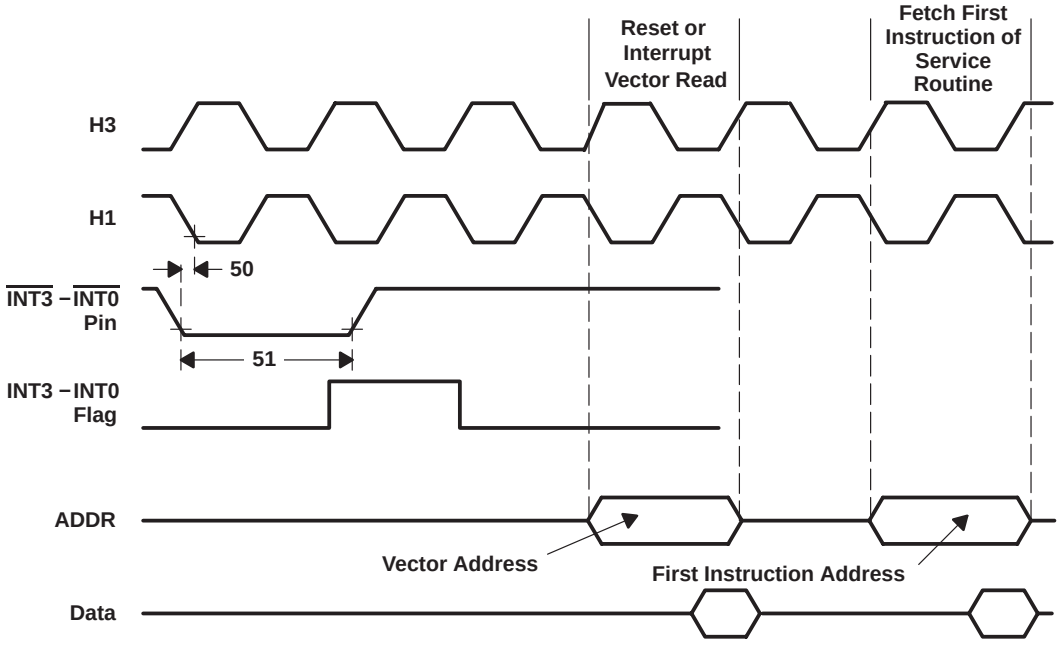



**Figure 20. Timing for $\overline{INT3}$−$\overline{INT0}$ Response**

### interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (HI rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (HI rising) of the read phase of the IACK instruction.

### timing for $\overline{\text{IACK}}$ (see Note 5 and Figure 21)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 52 | $t_{d(H1H-IACKL)}$ | Delay time, H1 high to $\overline{\text{IACK}}$ low | | 9 | ns |
| 53 | $t_{d(H1H-IACKH)}$ | Delay time, H1 high to $\overline{\text{IACK}}$ high | | 9 | ns |

NOTE 5: $\overline{\text{IACK}}$ goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.

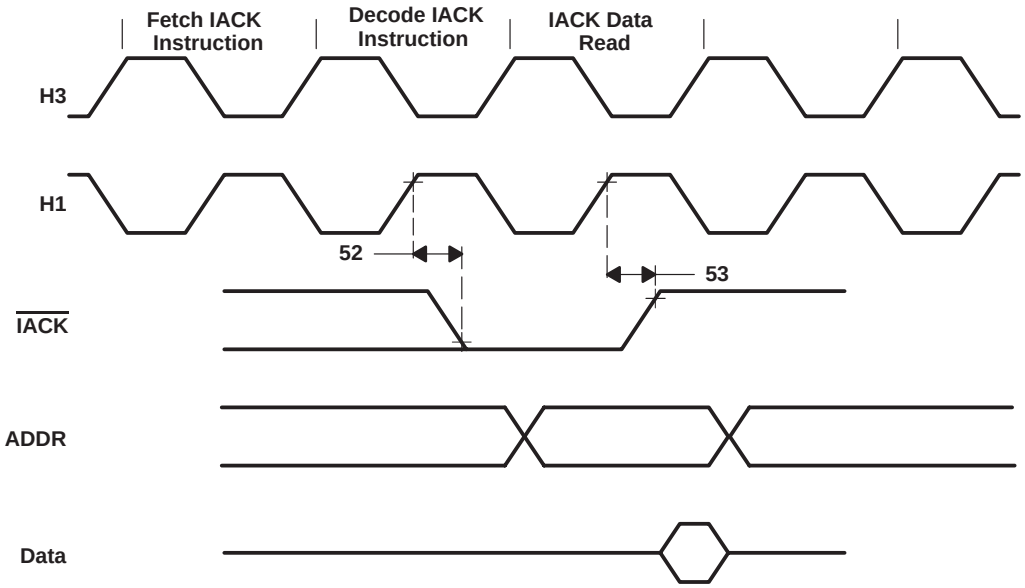



**Figure 21. Timing for $\overline{\text{IACK}}$**

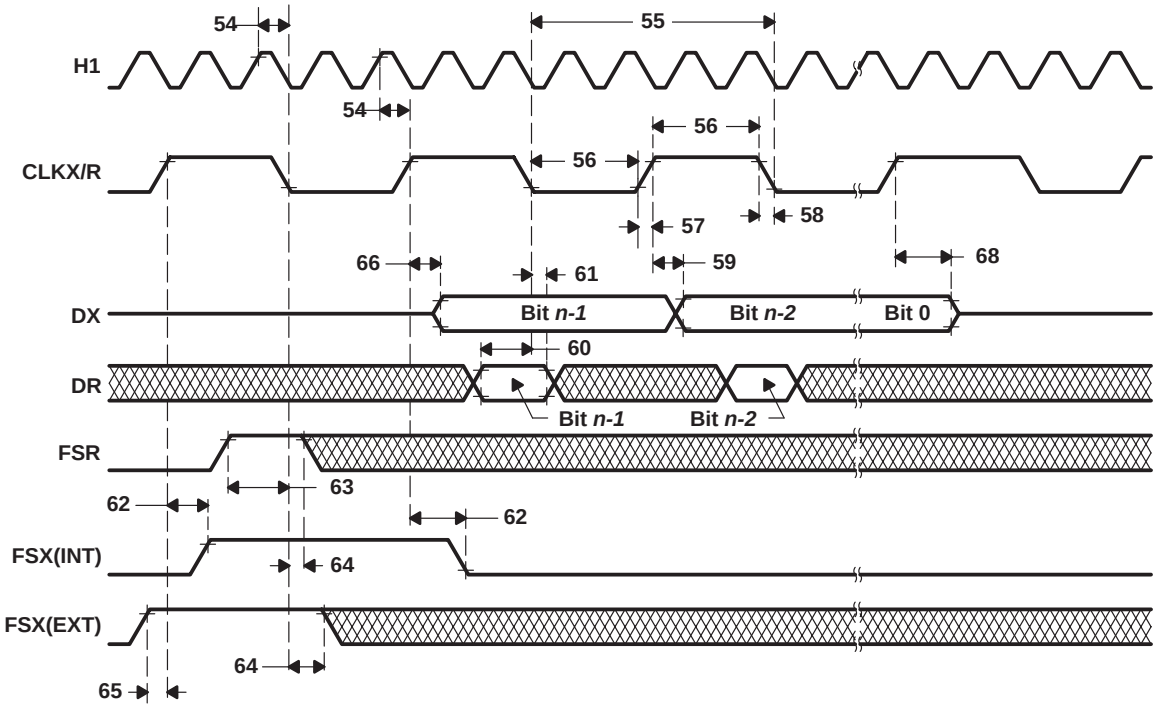
## serial-port timing (see Figure 22 and Figure 23)

| NO. | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 54 | $t_{d(H1H-SCK)}$ | Delay time, H1 high to internal CLKX/R | | | 13 | ns |
| 55 | $t_{c(SCK)}$ | Cycle time, CLKX/R | CLKX/R ext | $t_{c(H)}$x2.6 | | ns |
| | | | CLKX/R int | $t_{c(H)}$x2 | $t_{c(H)}$x2$^{32}$ | |
| 56 | $t_{w(SCK)}$ | Pulse duration, CLKX/R high/low | CLKX/R ext | $t_{c(H)}$+10 | | ns |
| | | | CLKX/R int | [$t_{c(SCK)}$/2]−5 | [$t_{c(SCK)}$/2]+5 | |
| 57 | $t_{r(SCK)}$ | Rise time, CLKX/R | | | 7 | ns |
| 58 | $t_{f(SCK)}$ | Fall time, CLKX/R | | | 7 | ns |
| 59 | $t_{d(C-DX)}$ | Delay time, CLKX to DX valid | CLKX ext | | 30 | ns |
| | | | CLKX int | | 17 | |
| 60 | $t_{su(DR-CLKRL)}$ | Setup time, DR before CLKR low | CLKR ext | 9 | | ns |
| | | | CLKR int | 21 | | |
| 61 | $t_{h(CLKRL-DR)}$ | Hold time, DR from CLKR low | CLKR ext | 9 | | ns |
| | | | CLKR int | 0 | | |
| 62 | $t_{d(C-FSX)}$ | Delay time, CLKX to internal FSX high/low | CLKX ext | | 27 | ns |
| | | | CLKX int | | 15 | |
| 63 | $t_{su(FSR-CLKRL)}$ | Setup time, FSR before CLKR low | CLKR ext | 9 | | ns |
| | | | CLKR int | 9 | | |
| 64 | $t_{h(SCKL-FS)}$ | Hold time, FSX/R input from CLKX/R low | CLKX/R ext | 9 | | ns |
| | | | CLKX/R int | 0 | | |
| 65 | $t_{su(FSX-C)}$ | Setup time, external FSX before CLKX | CLKX ext | −[$t_{c(H)}$−8]* | [$t_{c(SCK)}$/2]−10* | ns |
| | | | CLKX int | [$t_{c(H)}$−21]* | $t_{c(SCK)}$/2* | |
| 66 | $t_{d(CH-DX)V}$ | Delay time, CLKX to first DX bit, FSX precedes CLKX high | CLKX ext | | 30* | ns |
| | | | CLKX int | | 18* | |
| 67 | $t_{d(FSX-DX)V}$ | Delay time, FSX to first DX bit, CLKX precedes FSX | | | 30* | ns |
| 68 | $t_{d(CH-DXZ)}$ | Delay time, CLKX high to DX high impedance following last data bit | | | 17* | ns |

* This parameter is not production tested.

### data-rate timing modes

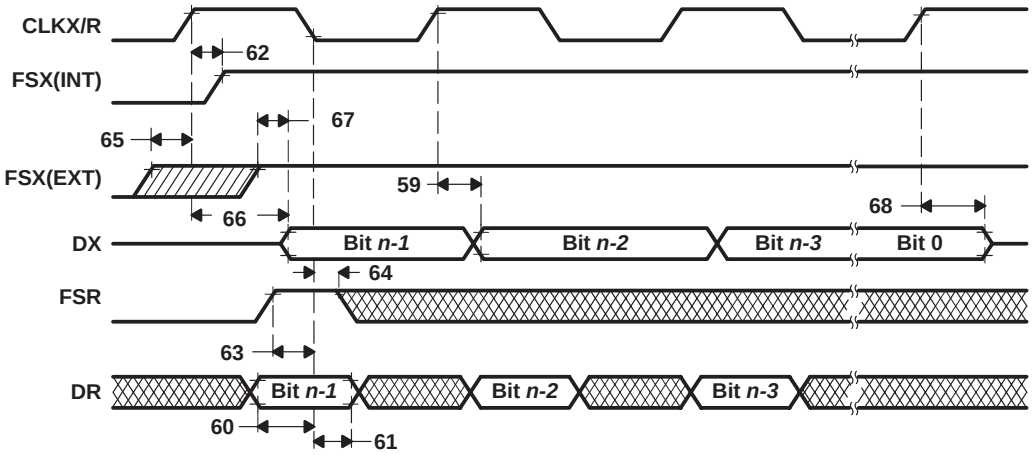
Unless otherwise indicated, the data-rate timings shown in Figure 22 and Figure 23 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation, see the *TMS320C3x User's Guide* (literature number SPRU031).




NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

**Figure 22. Timing for Fixed Data-Rate Mode**

### data-rate timing modes (continued)




NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

**Figure 23. Timing for Variable Data-Rate Mode**

### $\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

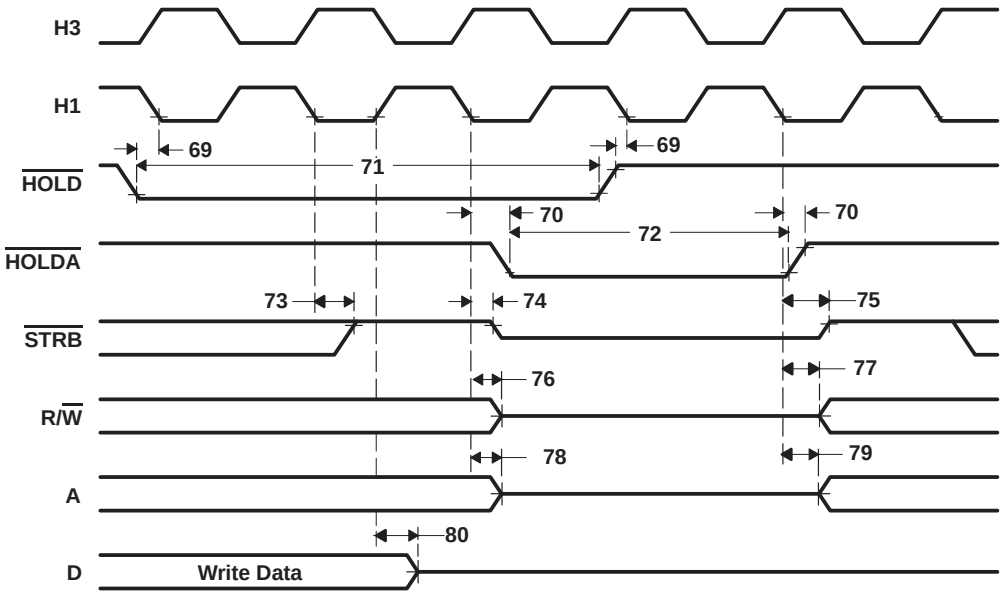
Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue until a second write is encountered.

### timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ (see Figure 24)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 69 | $t_{su(HOLD-H1L)}$ | Setup time, $\overline{\text{HOLD}}$ before H1 low | 13 | | ns |
| 70 | $t_{v(H1L-HOLDA)}$ | Valid time, $\overline{\text{HOLDA}}$ after H1 low | 0* | 9 | ns |
| 71 | $t_{w(HOLD)}$† | Pulse duration, $\overline{\text{HOLD}}$ low | $2t_{c(H)}$ | | ns |
| 72 | $t_{w(HOLDA)}$ | Pulse duration, $\overline{\text{HOLDA}}$ low | $t_{cH}-5$* | | ns |
| 73 | $t_{d(H1L-SH)H}$ | Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$ | 0* | 9 | ns |
| 74 | $t_{dis(H1L-S)}$ | Disable time, H1 low to $\overline{\text{STRB}}$ to the high-impedance state | 0* | 9* | ns |
| 75 | $t_{en(H1L-S)}$ | Enable time, H1 low to $\overline{\text{STRB}}$ enabled (active) | 0* | 9 | ns |
| 76 | $t_{dis(H1L-RW)}$ | Disable time, H1 low to R/$\overline{\text{W}}$ to the high-impedance state | 0* | 9* | ns |
| 77 | $t_{en(H1L-RW)}$ | Enable time, H1 low to R/$\overline{\text{W}}$ enabled (active) | 0* | 9 | ns |
| 78 | $t_{dis(H1L-A)}$ | Disable time, H1 low to address to the high-impedance state | 0* | 10* | ns |
| 79 | $t_{en(H1L-A)}$ | Enable time, H1 low to address enabled (valid) | 0* | 13 | ns |
| 80 | $t_{dis(H1H-D)}$ | Disable time, H1 high to data to the high-impedance state | 0* | 9* | ns |

† $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 24 occurs; otherwise, an additional delay of one clock cycle is possible.

* This parameter is not production tested.




NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

**Figure 24. Timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$**

### general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

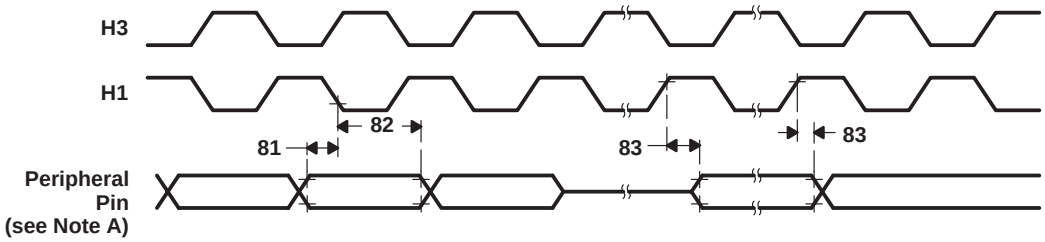
#### *peripheral pin I/O timing*

The table, timing parameters for peripheral pin general-purpose I/O, defines peripheral pin general-purpose I/O timing parameters.

### timing requirements for peripheral pin general-purpose I/O (see Note 6 and Figure 25)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 81 | $t_{su(GPIO-H1L)}$ | Setup time, general-purpose input before H1 low | 10 | | ns |
| 82 | $t_{h(H1L-GPIO)}$ | Hold time, general-purpose input after H1 low | 0 | | ns |
| 83 | $t_{d(H1H-GPIO)}$ | Delay time, general-purpose output after H1 high | | 13 | ns |

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.




NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

**Figure 25. Timing for Peripheral Pin General-Purpose I/O**

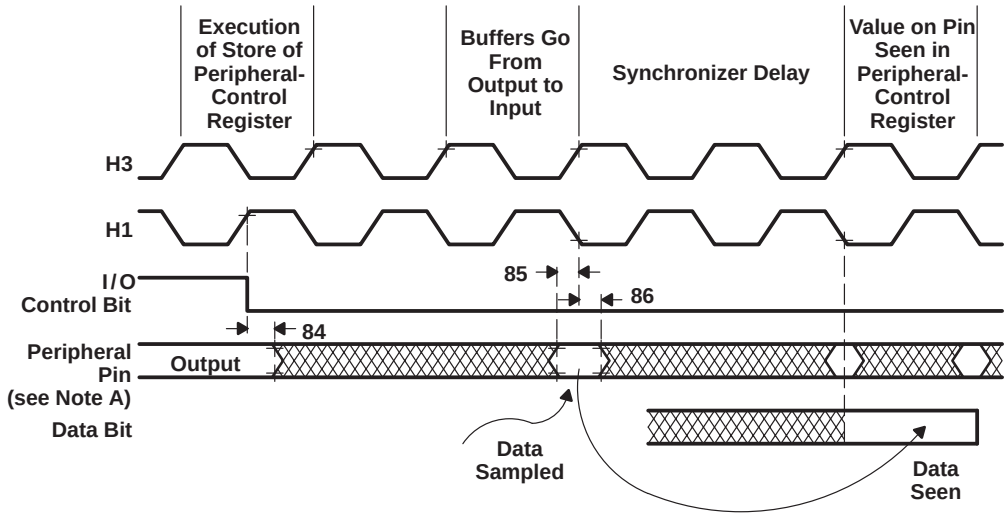
### *changing the peripheral pin I/O modes*

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa.

**timing requirements for peripheral pin changing from general-purpose output to input mode (see Note 6 and Figure 26)**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 84 | $t_{h(H1H)}$ | Hold time, peripheral pin after H1 high | | 13 | ns |
| 85 | $t_{su(GPIO-H1L)}$ | Setup time, peripheral pin before H1 low | 9 | | ns |
| 86 | $t_{h(H1L-GPIO)}$ | Hold time, peripheral pin after H1 low | 0 | | ns |

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



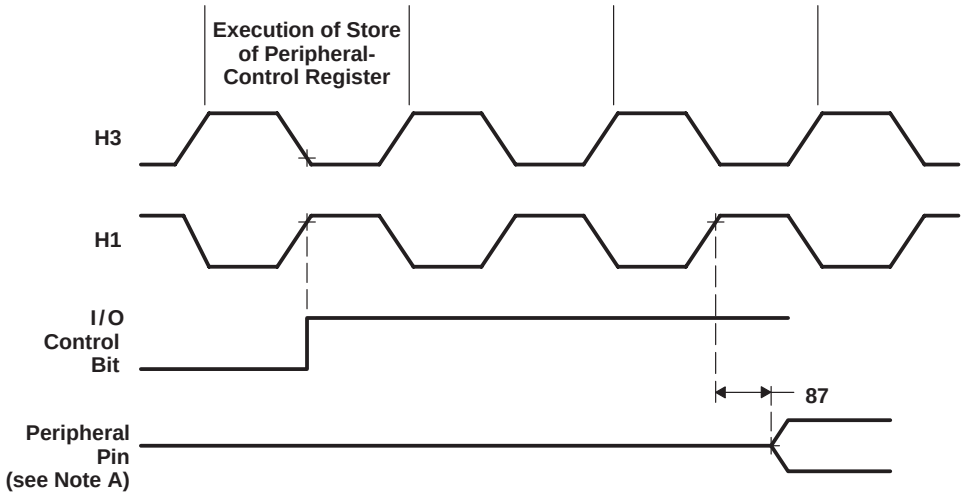

NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

**Figure 26. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode**

### timing for peripheral pin changing from general-purpose input to output mode (see Note 6 and Figure 27)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 87 | $t_{d(H1H-GPIO)}$ | Delay time, H1 high to peripheral pin switching from input to output | | 13 | ns |

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.




NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

**Figure 27. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode**

### timer pin timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers.

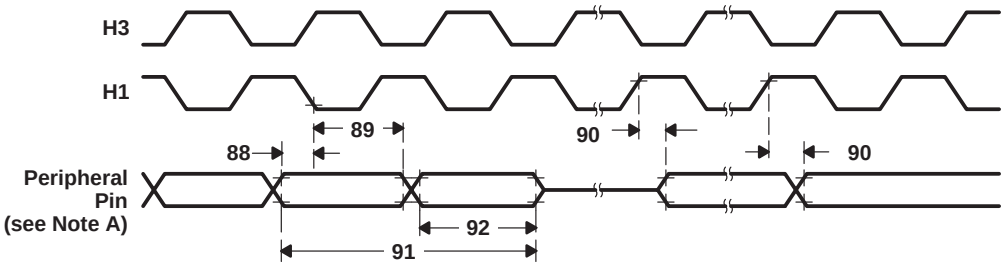
The following tables define the timing requirements for the timer pin.

### timing for timer pin (see Note 7 and Figure 28)

| NO. | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 88 | $t_{su(TCLK-H1L)}$ | Setup time, TCLK external before H1 low | | 10 | | ns |
| 89 | $t_{h(H1L-TCLK)}$ | Hold time, TCLK external after H1 low | | 0 | | ns |
| 90 | $t_{d(H1H-TCLK)}$ | Delay time, H1 high to TCLK internal valid | | | 9 | ns |
| 91 | $t_{c(TCLK)}$ | Cycle time, TCLK | TCLK ext | $t_{C(H)}\times 2.6$ | | ns |
| | | | TCLK int | $t_{C(H)}\times 2$ | $t_{C(H)}\times 2^{32}$* | |
| 92 | $t_{w(TCLK)}$ | Pulse duration, TCLK high/low | TCLK ext | $t_{C(H)}+10$ | | ns |
| | | | TCLK int | $[t_{C(TCLK)}/2]-5$ | $[t_{C(TCLK)}/2]+5$ | |

* This parameter is not production tested.

NOTE 7: Numbers 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.




NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

**Figure 28. Timing for Timer Pin**

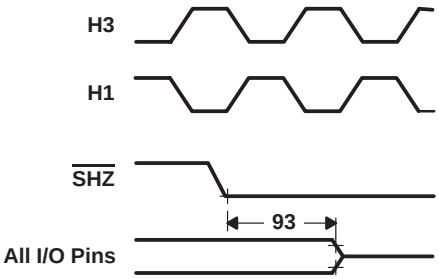
### $\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin.

### timing parameters for $\overline{\text{SHZ}}$ (see Figure 29)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 93 | $t_{dis(SHZ)}$ | Disable time, $\overline{\text{SHZ}}$ low to all O, I/O pins disabled (high impedance) | 0* | 2P†* | ns |

† P = $t_{c(CI)}$
* This parameter is not production tested.

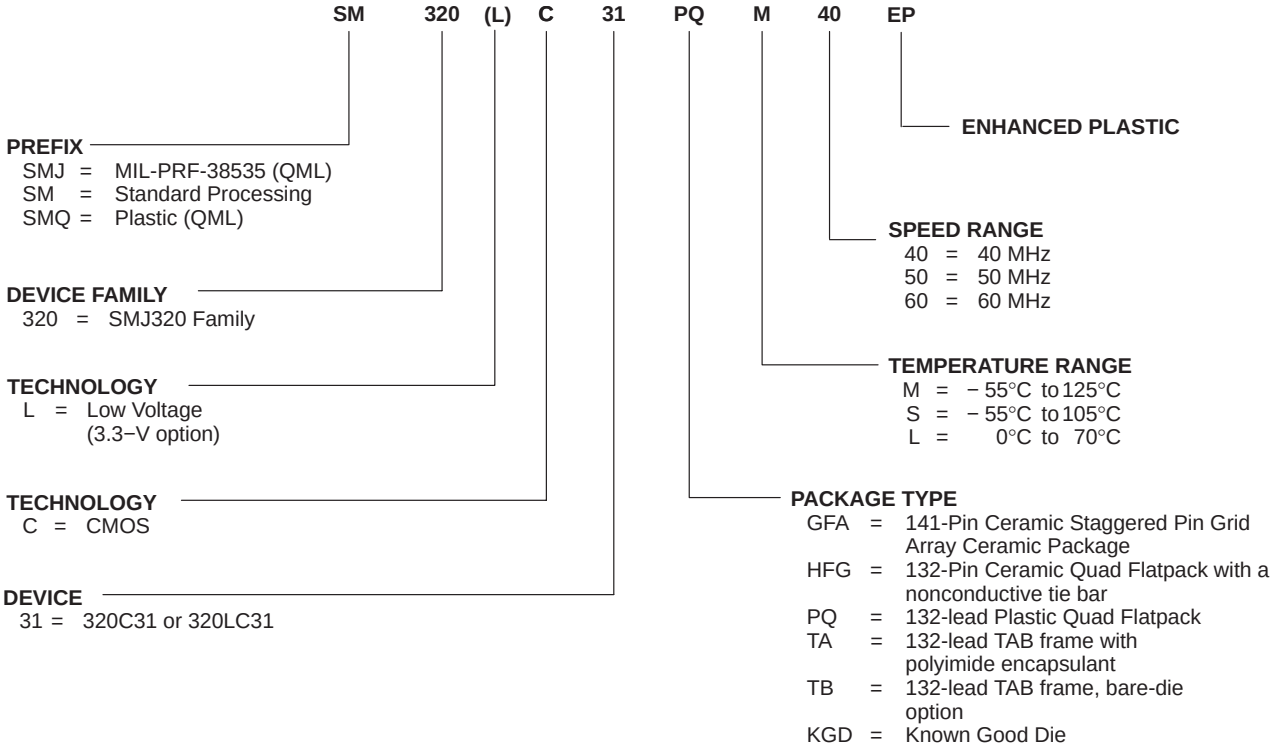



NOTE A: Enabling $\overline{\text{SHZ}}$ destroys SM320LC31-EP register and memory contents. Assert $\overline{\text{SHZ}}$ = 1 and reset the SM320LC31-EP to restore it to a known condition.

**Figure 29. Timing for $\overline{\text{SHZ}}$**

## part order information

| DEVICE | TECHNOLOGY | POWER SUPPLY | OPERATING FREQUENCY | PACKAGE TYPE | PROCESSING LEVEL |
|---|---|---|---|---|---|
| SM320LC31PQM40EP | 0.72-µm CMOS | 3.3 V ± 5% | 40 MHz | Plastic 132-lead good flatpack | EP |



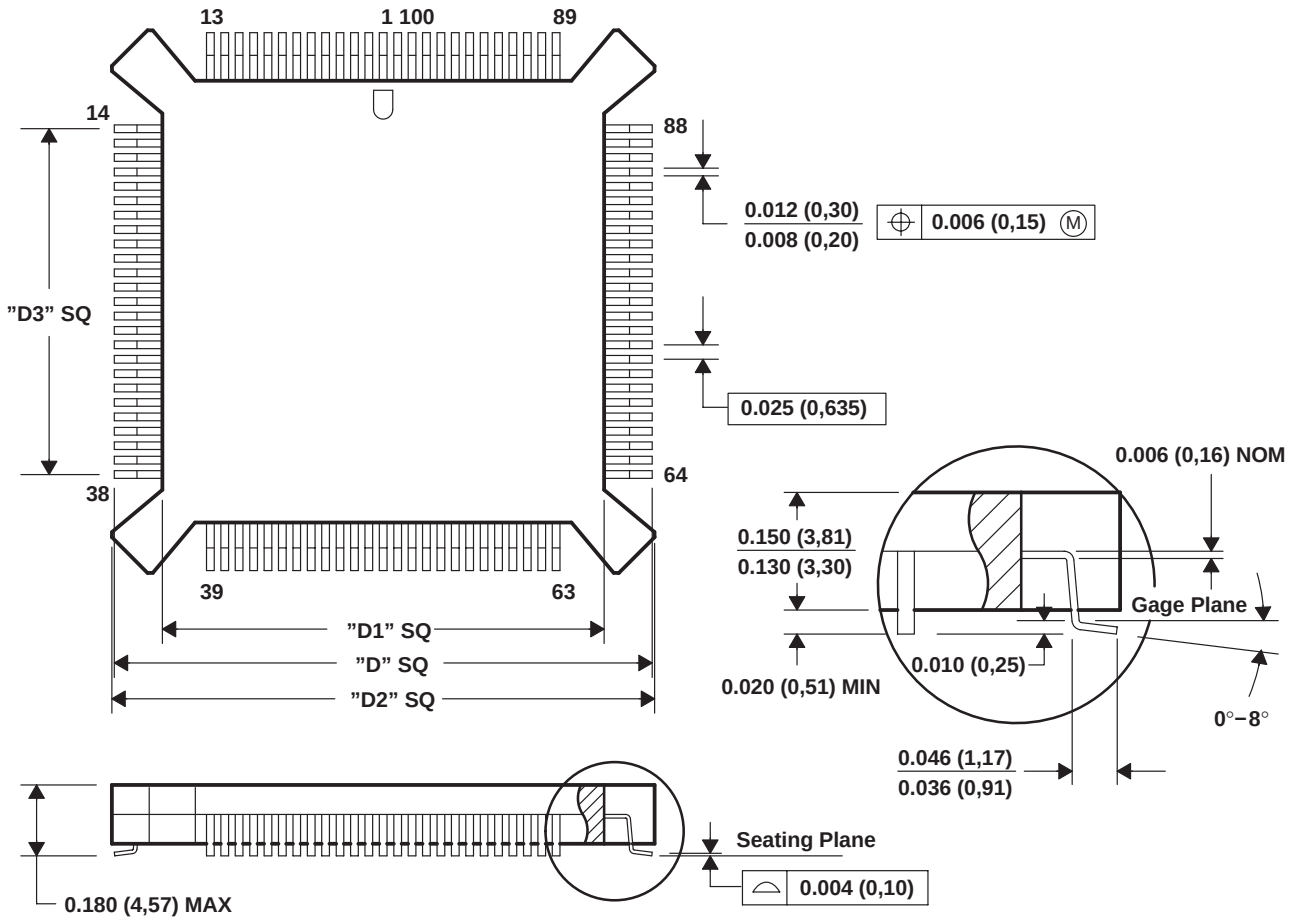

Note: Not all speed, package, process, or temperature combinations are available.

**Figure 30. Device Nomenclature**

## MECHANICAL DATA

**PQ (S-PQFP-G***)** **PLASTIC QUAD FLATPACK**

**100 LEAD SHOWN**




| DIM \ LEADS *** | | 100 | 132 |
|---|---|---|---|
| "D" | MAX | 0.890 (22,61) | 1.090 (27,69) |
| | MIN | 0.870 (22,10) | 1.070 (27,18) |
| "D1" | MAX | 0.766 (19,46) | 0.966 (24,54) |
| | MIN | 0.734 (18,64) | 0.934 (23,72) |
| "D2" | MAX | 0.912 (23,16) | 1.112 (28,25) |
| | MIN | 0.888 (22,56) | 1.088 (27,64) |
| "D3" | NOM | 0.600 (15,24) | 0.800 (20,32) |

**4040045/C 11/95**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SM320LC31PQM40EP | NRND | Production | BQFP (PQ) \| 132 | 55 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-4-260C-72 HR | -55 to 125 | 320LC31PQM40EP |
| V62/03617-01XE | NRND | Production | BQFP (PQ) \| 132 | 55 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-4-260C-72 HR | -55 to 125 | 320LC31PQM40EP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

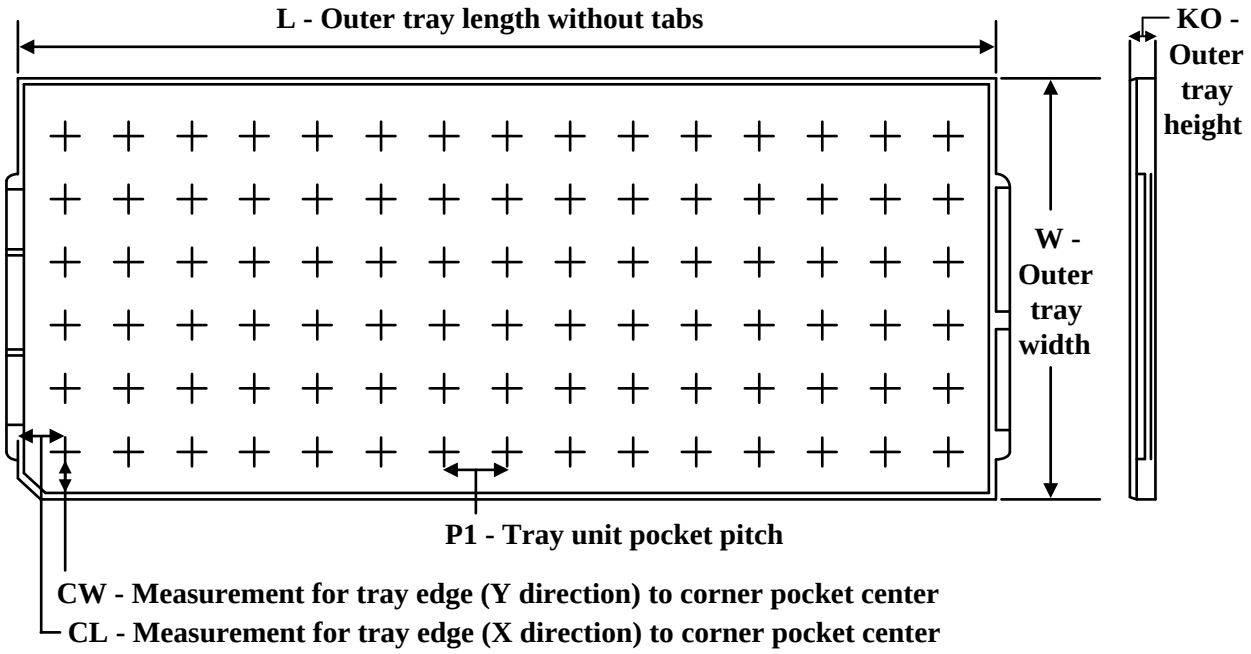
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SM320LC31PQM40EP | PQ | BQFP | 132 | 55 | 4X9 | 180 | 315 | 135.9 | 7620 | 33.37 | 23.98 | 20.93 |
| V62/03617-01XE | PQ | BQFP | 132 | 55 | 4X9 | 180 | 315 | 135.9 | 7620 | 33.37 | 23.98 | 20.93 |

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