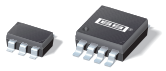


SBVS031D – MARCH 2001 – REVISED SEPTEMBER 2005

# DMOS
# 400mA Low-Dropout Regulator

## FEATURES

- **CAP-FREE DMOS TOPOLOGY:**
  **Ultra Low Dropout Voltage:**
  **250mV typ at 400mA**
  **Output Capacitor *not* Required for Stability**
- **UP TO 500mA PEAK, TYPICAL**
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE: 28μVrms**
- **HIGH ACCURACY: ±1.5% max**
- **HIGH EFFICIENCY:**
  **$I_{GND}$ = 850μA at $I_{OUT}$ = 400mA**
  **Not Enabled: $I_{GND}$ = 0.01μA**
- **2.5V, 2.85V, 3.0V, 3.3V, AND 5.0V OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**
  **SOT23-5 and MSOP-8**

## APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

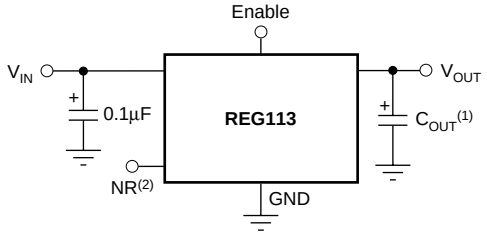
## DESCRIPTION

The REG113 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 250mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1μF.

Typical ground pin current is only 850μA (at $I_{OUT}$ = 400mA) and drops to 10nA when not enabled. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG113 has very low output noise (typically 28μVrms for $V_{OUT}$ = 3.3V with $C_{NR}$ = 0.01μF), making it ideal for use in portable communications equipment. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG113 is well protected—internal circuitry provides a current limit which protects the load from damage, furthermore, thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG113 is available in SOT23-5 and MSOP-8 packages.




NOTES: (1) Optional. (2) NR = Noise Reduction.

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Input Voltage, $V_{IN}$ | –0.3V to 12V |
| Enable Input Voltage, $V_{EN}$ | –0.3V to $V_{IN}$ |
| NR Pin Voltage, $V_{NR}$ | –0.3V to 6.0V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range ($T_J$) | –55°C to +125°C |
| Storage Temperature Range ($T_A$) | –65°C to +150°C |
| Lead Temperature (soldering, 3s) | +240°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | $V_{OUT}$(2) |
|---|---|
| REG113**xx-*yyyy/zzz*** | **XX** is package designator.<br>**YYYY** is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable).<br>**ZZZ** is package quantity. |

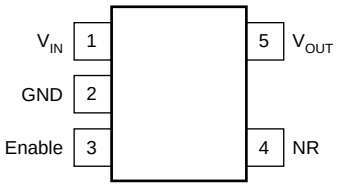
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

## PIN CONFIGURATIONS

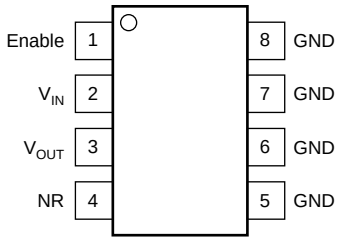
**Top View**

**SOT**




(N Package)

**MSOP**




(E Package)

NOTE: Leads 5 through 8 are fused to the lead frame and can be used for improved thermal dissipation.

# ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range, **$T_J$ = –40°C to +85°C.**

At $T_J$ = +25°C, $V_{IN}$ = $V_{OUT}$ + 1V, $V_{ENABLE}$ = 1.8V, $I_{OUT}$ = 5mA, $C_{NR}$ = 0.01µF, and $C_{OUT}$ = 0.1µF[1], unless otherwise noted.

| PARAMETER | | CONDITION | REG113NA REG113EA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUT VOLTAGE** | | | | | | |
| Output Voltage Range | $V_{OUT}$ | | | | | |
| REG113-2.5 | | | | 2.5 | | V |
| REG113-2.85 | | | | 2.85 | | V |
| REG113-3 | | | | 3.0 | | V |
| REG113-3.3 | | | | 3.3 | | V |
| REG113-5 | | | | 5.0 | | V |
| Accuracy | | | | ±0.5 | ±1.5 | % |
| **Over Temperature** | | | | | **±2.3** | % |
| **vs Temperature** | **$dV_{OUT}/dT$** | | | **50** | **±2.3** | ppm/°C |
| vs Line and Load | | $I_{OUT}$ = 5mA to 400mA, $V_{IN}$ = ($V_{OUT}$ + 0.4V) to 10V | | ±1 | ±2.3 | % |
| **Over Temperature** | | **$I_{OUT}$ = 5mA to 400mA, $V_{IN}$ = ($V_{OUT}$ + 0.6V) to 10V** | | | **±3.0** | **%** |
| **DC DROPOUT VOLTAGE[2]** | $V_{DROP}$ | $I_{OUT}$ = 5mA | | 4 | 10 | mV |
| For all models | | $I_{OUT}$ = 400mA | | 250 | 325 | mV |
| **Over Temperature** | | **$I_{OUT}$ = 400mA** | | | **410** | mV |
| **VOLTAGE NOISE** | | | | | | |
| f = 10Hz to 100kHz | $V_n$ | | | | | |
| Without $C_{NR}$ | | $C_{NR}$ = 0, $C_{OUT}$ = 0 | | 23µVrms/V • $V_{OUT}$ | | µVrms |
| With $C_{NR}$ | | $C_{NR}$ = 0.01µF, $C_{OUT}$ = 10µF | | 7µVrms/V • $V_{OUT}$ | | µVrms |
| **OUTPUT CURRENT** | | | | | | |
| Current Limit[3] | $I_{CL}$ | | 425 | 500 | 575 | mA |
| **Over Temperature** | | | | | **600** | mA |
| Short-Circuit Current Limit | $I_{SC}$ | | | 200 | | mA |
| **RIPPLE REJECTION** | | | | | | |
| f = 120Hz | | | | 65 | | dB |
| **ENABLE CONTROL** | | | | | | |
| $V_{ENABLE}$ HIGH (output enabled) | $V_{ENABLE}$ | | 1.8 | | $V_{IN}$ | V |
| $V_{ENABLE}$ LOW (output disabled) | | | –0.2 | | 0.5 | V |
| $I_{ENABLE}$ HIGH (output enabled) | $I_{ENABLE}$ | $V_{ENABLE}$ = 1.8V to $V_{IN}$, $V_{IN}$ = 1.8V to 6.5[4] | | 1 | 100 | nA |
| $I_{ENABLE}$ LOW (output disabled) | | $V_{ENABLE}$ = 0V to 0.5V | | 2 | 100 | nA |
| Output Disable Time | | $C_{OUT}$ = 1.0µF, $R_{LOAD}$ = 13Ω | | 50 | | µs |
| Output Enable Softstart Time | | $C_{OUT}$ = 1.0µF, $R_{LOAD}$ = 13Ω | | 1.5 | | ms |
| **THERMAL SHUTDOWN** | | | | | | |
| Junction Temperature | | | | | | |
| Shutdown | | | | 160 | | °C |
| Reset from Shutdown | | | | 140 | | °C |
| **GROUND PIN CURRENT** | | | | | | |
| Ground Pin Current | $I_{GND}$ | $I_{OUT}$ = 5mA | | 400 | 500 | µA |
| | | $I_{OUT}$ = 400mA | | 850 | 1000 | µA |
| Enable Pin LOW | | $V_{ENABLE}$ ≤ 0.5V | | 0.01 | 0.2 | µA |
| **INPUT VOLTAGE** | $V_{IN}$ | | | | | |
| Operating Input Voltage Range[5] | | | 1.8 | | 10 | V |
| Specified Input Voltage Range | | $V_{IN}$ > 1.8V | $V_{OUT}$ + 0.4 | | 10 | V |
| **Over Temperature** | | **$V_{IN}$ > 1.8V** | **$V_{OUT}$ + 0.6** | | **10** | V |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | $T_J$ | | –40 | | +85 | °C |
| Operating Range | $T_J$ | | –55 | | +125 | °C |
| Storage Range | $T_A$ | | –65 | | +150 | °C |
| Thermal Resistance | | | | | | |
| SOT23-5 Surface-Mount | $\theta_{JA}$ | Junction-to-Ambient | | 200 | | °C/W |
| MSOP-8 Surface-Mount | $\theta_{JC}$ | Junction-to-Case | | 35[6] | | °C/W |
| | $\theta_{JA}$ | Junction-to-Ambient | | 160[6] | | °C/W |

NOTES: (1) The REG113 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.

(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at $V_{IN}$ = $V_{OUT}$ + 1V at fixed load.

(3) Current limit is the output current that produces a 10% change in output voltage from $V_{IN}$ = $V_{OUT}$ + 1V and $I_{OUT}$ = 5mA.

(4) For $V_{ENABLE}$ > 6.5V, see typical characteristic *$I_{ENABLE}$ vs $V_{ENABLE}$*.

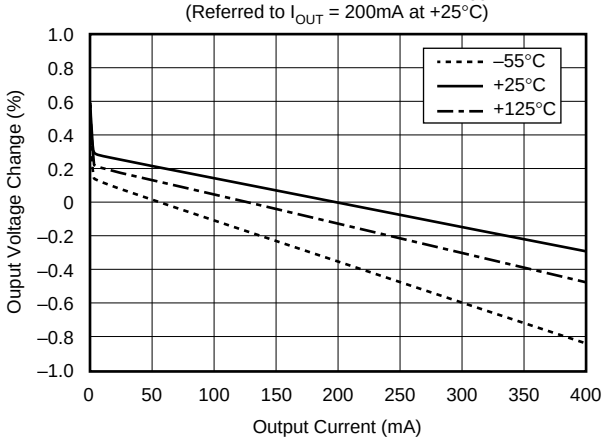
(5) The REG113 no longer regulates when $V_{IN}$ < $V_{OUT}$ + $V_{DROP\ (MAX)}$. In dropout, the impedance from $V_{IN}$ to $V_{OUT}$ is typically less than 1Ω at $T_J$ = +25°C.

(6) See Figure 7.

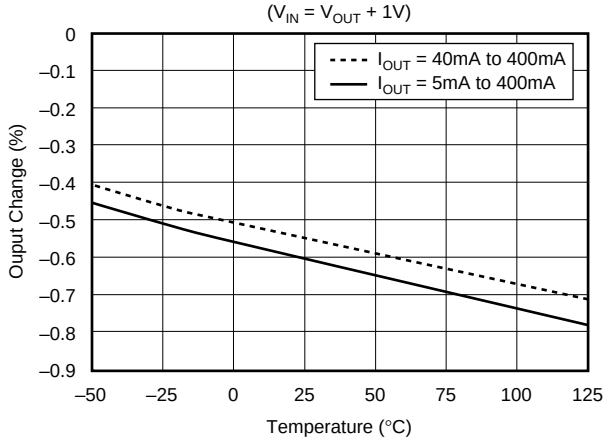
# TYPICAL CHARACTERISTICS

For all models, at $T_J$ = +25°C and $V_{ENABLE}$ = 1.8V, unless otherwise noted.

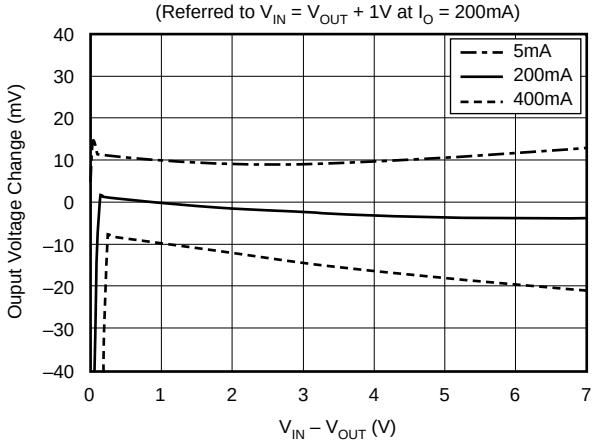
OUTPUT VOLTAGE CHANGE vs $I_{OUT}$
(Referred to $I_{OUT}$ = 200mA at +25°C)



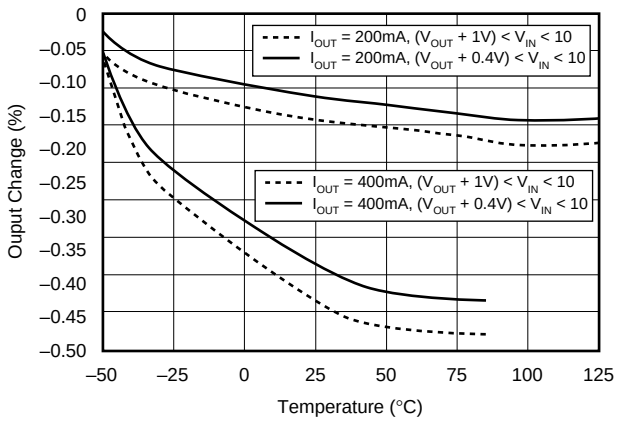

LOAD REGULATION vs TEMPERATURE
($V_{IN}$ = $V_{OUT}$ + 1V)



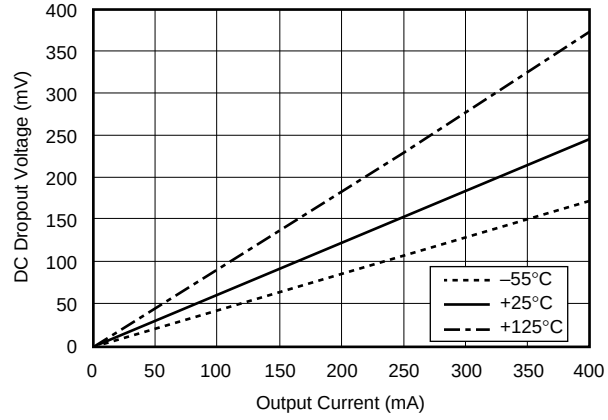

LINE REGULATION
(Referred to $V_{IN}$ = $V_{OUT}$ + 1V at $I_O$ = 200mA)



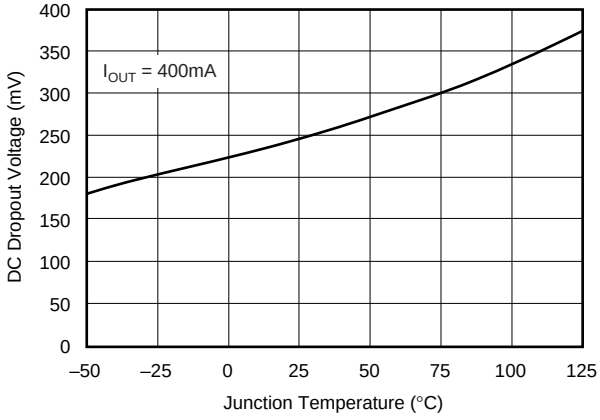

LINE REGULATION vs TEMPERATURE




DC DROPOUT VOLTAGE vs OUTPUT CURRENT



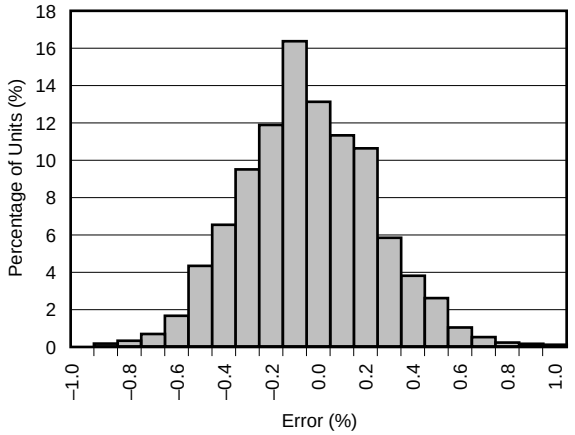

DC DROPOUT VOLTAGE vs TEMPERATURE



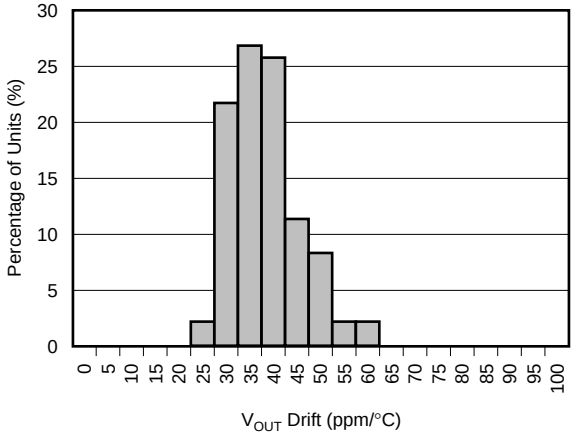
# TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J$ = +25°C and $V_{ENABLE}$ = 1.8V, unless otherwise noted.

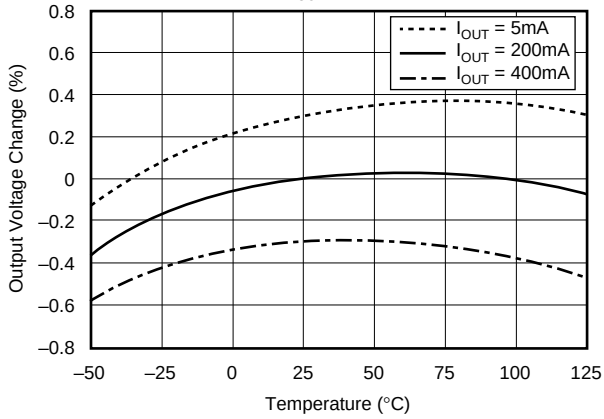
OUTPUT VOLTAGE ACCURACY HISTOGRAM



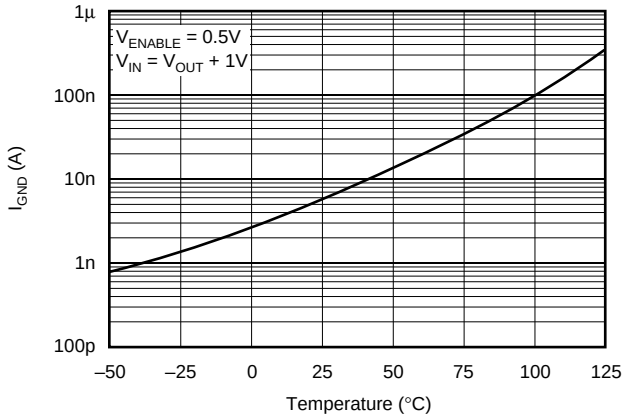

OUTPUT VOLTAGE DRIFT HISTOGRAM



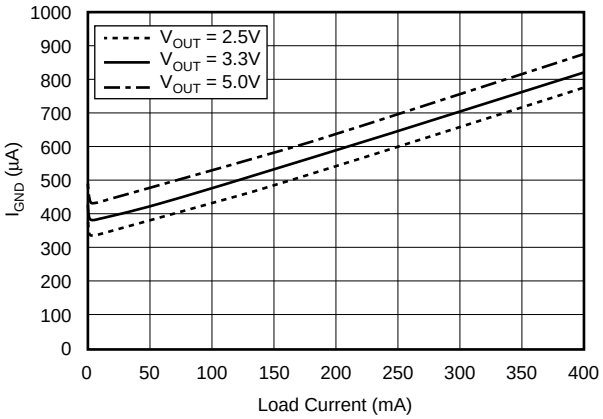

OUTPUT VOLTAGE vs TEMPERATURE
(Referred to $I_{OUT}$ = 200mA at +25°C)



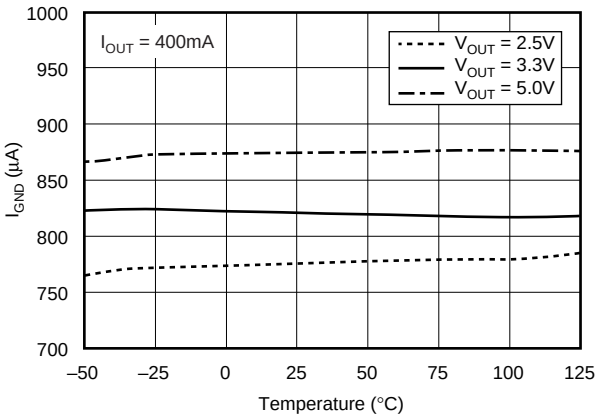

GROUND PIN CURRENT, NOT ENABLED
vs TEMPERATURE




GROUND CURRENT vs LOAD CURRENT



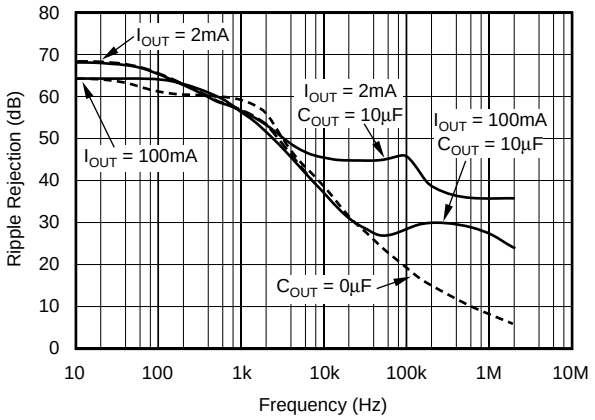

GROUND CURRENT vs TEMPERATURE



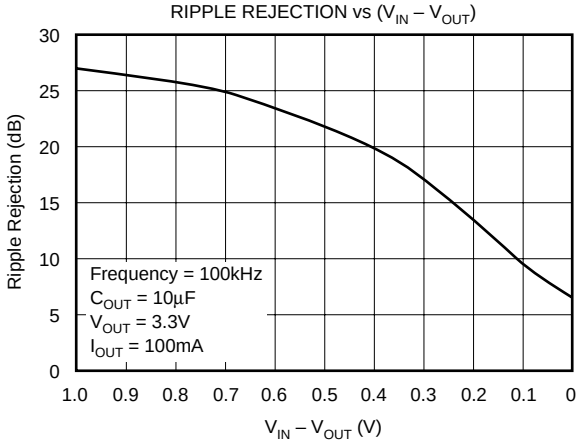
# TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J$ = +25°C and $V_{ENABLE}$ = 1.8V, unless otherwise noted.

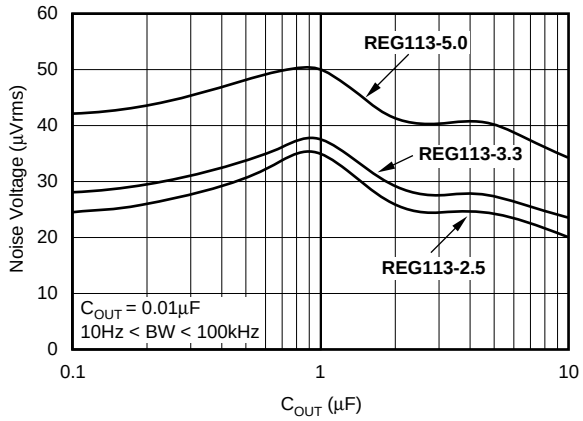
RIPPLE REJECTION vs FREQUENCY



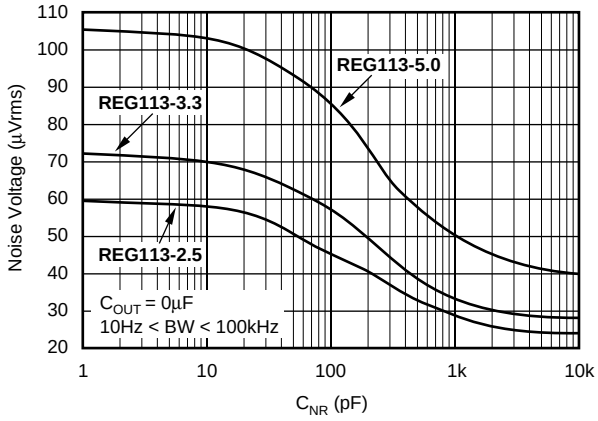

RIPPLE REJECTION vs ($V_{IN}$ – $V_{OUT}$)



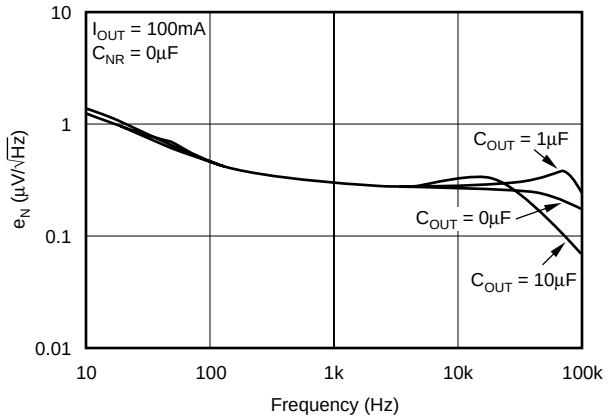

RMS NOISE VOLTAGE vs $C_{OUT}$



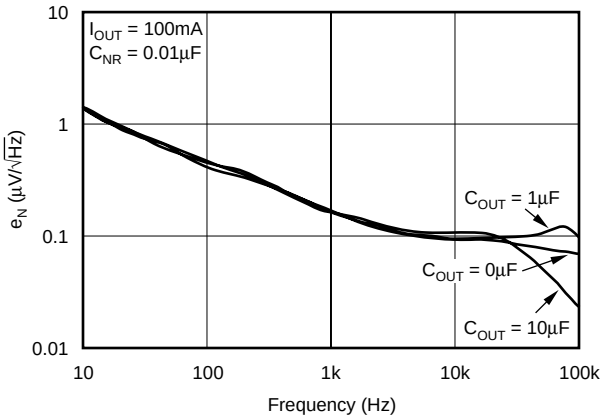

RMS NOISE VOLTAGE vs $C_{NR}$




NOISE SPECTRAL DENSITY



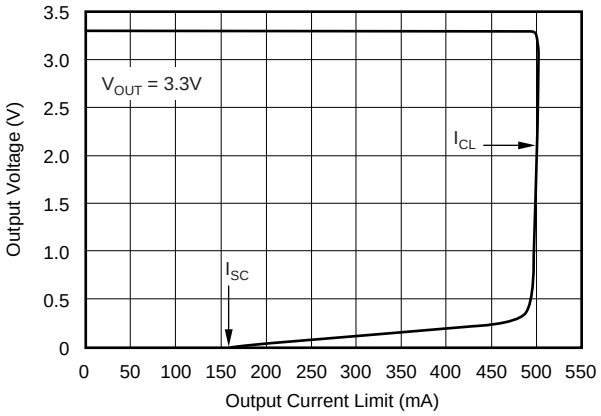

NOISE SPECTRAL DENSITY



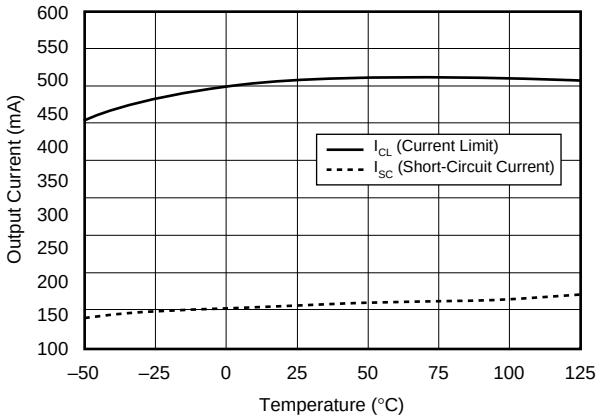
# TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J$ = +25°C and $V_{ENABLE}$ = 1.8V, unless otherwise noted.

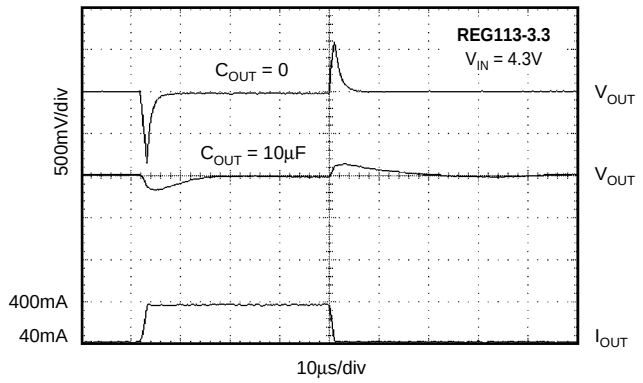
CURRENT LIMIT FOLDBACK



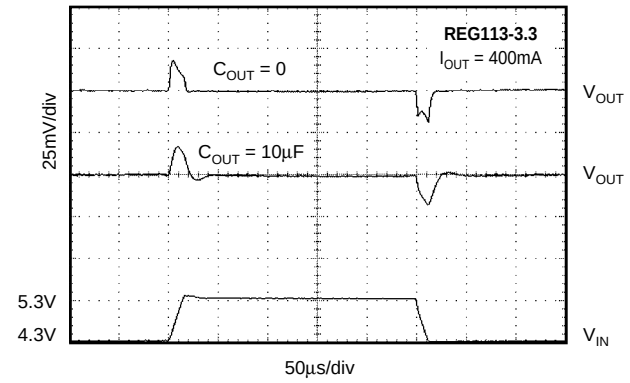

CURRENT LIMIT vs TEMPERATURE



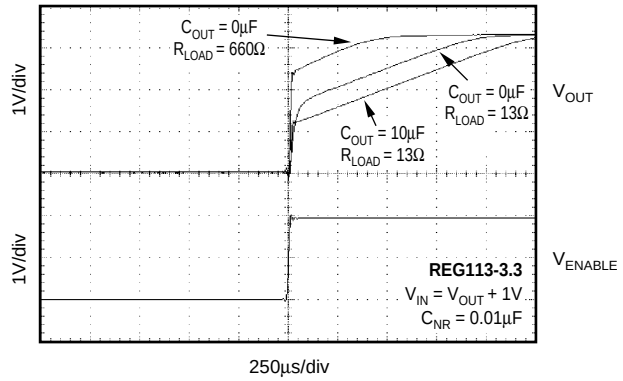

LOAD TRANSIENT RESPONSE



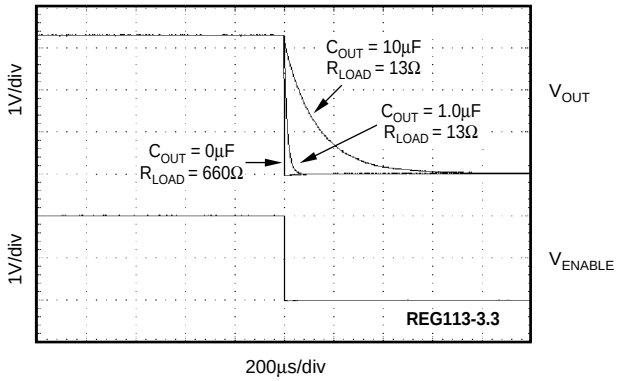

LINE TRANSIENT RESPONSE




TURN-ON

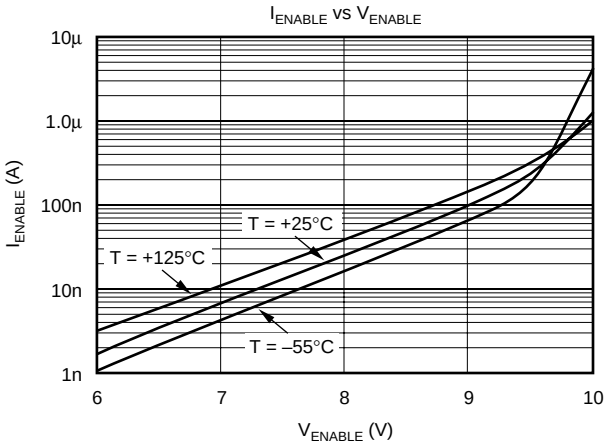


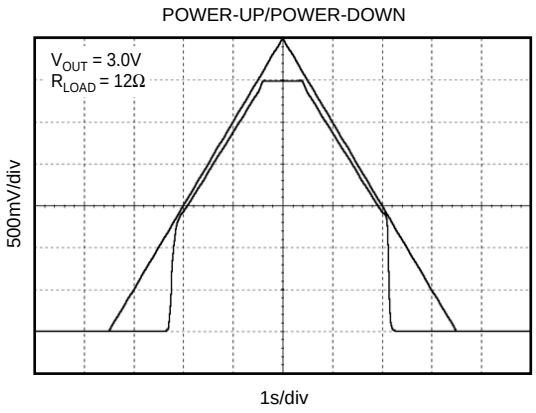

TURN-OFF



# TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J$ = +25°C and $V_{ENABLE}$ = 1.8V, unless otherwise noted.




# BASIC OPERATION

The REG113 series of LDO (low dropout) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version. The REG113 belongs to a family of new generation LDO regulators that use a DMOS pass transistor to achieve ultra low-dropout performance and freedom from output capacitor constraints. Ground pin current remains under 1mA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG113 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10µF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by adding a 1kΩ to 2kΩ load resistor, using capacitance values smaller than 10µF, or keeping the effective series resistance greater than 0.05Ω including the capacitor ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is a good standard analog design practice to connect a 0.1µF low ESR capacitor across the input supply voltage; this is recommended to counteract reactive input sources and improve ripple rejection by reducing input voltage ripple. Figure 1 shows the basic circuit connections for the fixed voltage models.

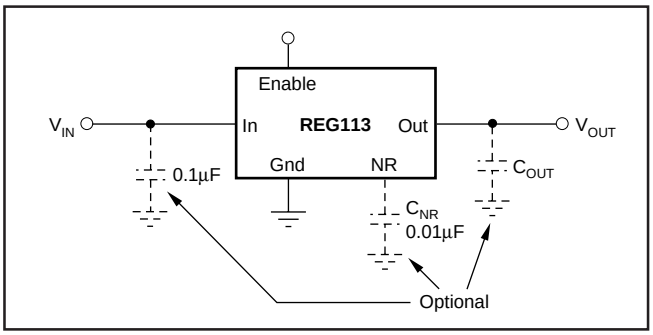



FIGURE 1. Fixed Voltage Nominal Circuit for the REG113.

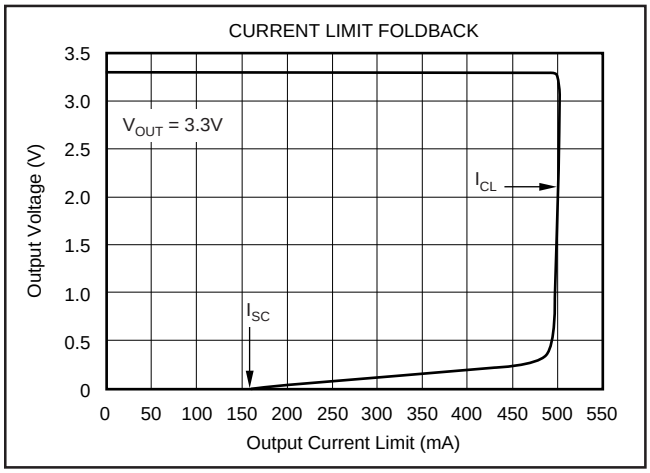



FIGURE 2. Foldback Current Limit of the REG113-3.3 at 25°C.

### INTERNAL CURRENT LIMIT

The REG113 internal current limit has a typical value of 500mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 200mA. A curve of $V_{OUT}$ versus $I_{OUT}$ is given in Figure 2, and in the Typical Characteristics section.

### ENABLE

The Enable pin is active high and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When not used, the Enable pin can be connected to $V_{IN}$.

## OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage, $V_{REF}$. This reference is the dominant noise source within the REG113 and generates approximately 29µVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu Vrms \frac{R_1 + R_2}{R2} = 29\mu Vrms \bullet \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of $V_{REF}$ is 1.26V, this relationship reduces to:

$$V_N = 23 \frac{\mu Vrms}{V} \bullet V_{OUT} \quad (2)$$

Connecting a capacitor, $C_{NR}$, from the Noise Reduction (NR) pin to ground (as shown in Figure 3) forms a low-pass filter for the voltage reference. For $C_{NR}$ = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for $V_{OUT}$ = 3.3V. This noise reduction effect is shown in Figure 4, and as *RMS Noise Voltage vs $C_{NR}$* in the Typical Characteristics section.

Noise can be further reduced by carefully choosing an output capacitor, $C_{OUT}$. Best overall noise performance is achieved with very low (< 0.22µF) or very high (> 2.2µF) values of $C_{OUT}$ (see the *RMS Noise Voltage vs $C_{OUT}$* typical characteristic).

The REG113 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above $V_{IN}$. The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of $I_{OUT}$ and $C_{OUT}$.

## DROPOUT VOLTAGE

The REG113 uses an N-channel DMOS as the pass element. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DROP}$), the DMOS pass device behaves like a resistor; therefore, for low values of ($V_{IN}$ – $V_{OUT}$), the regulator input-to-output resistance is the $Rds_{ON}$ of the DMOS pass element (typically 600mΩ). For static (DC) loads, the REG113 will typically maintain regulation down to a ($V_{IN}$ – $V_{OUT}$) voltage drop of 250mV at full rated output current. In Figure 5, the bottom line (DC dropout) shows the minimum $V_{IN}$ to $V_{OUT}$ voltage drop required to prevent dropout under DC load conditions.

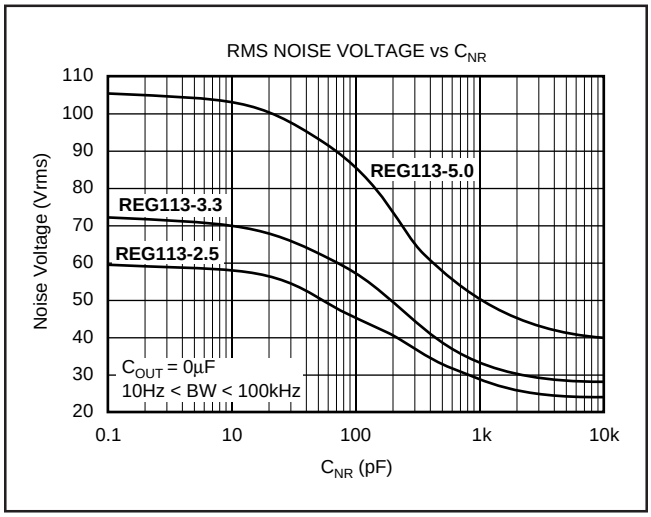



FIGURE 4. Output Noise versus Noise Reduction Capacitor.

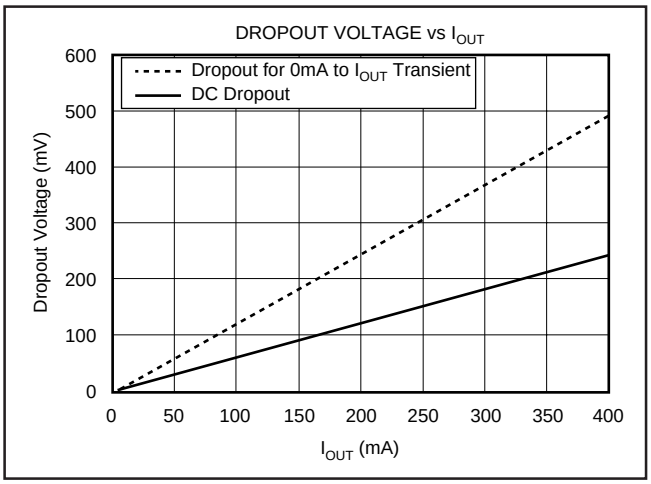



FIGURE 5. Transient and DC Dropout.

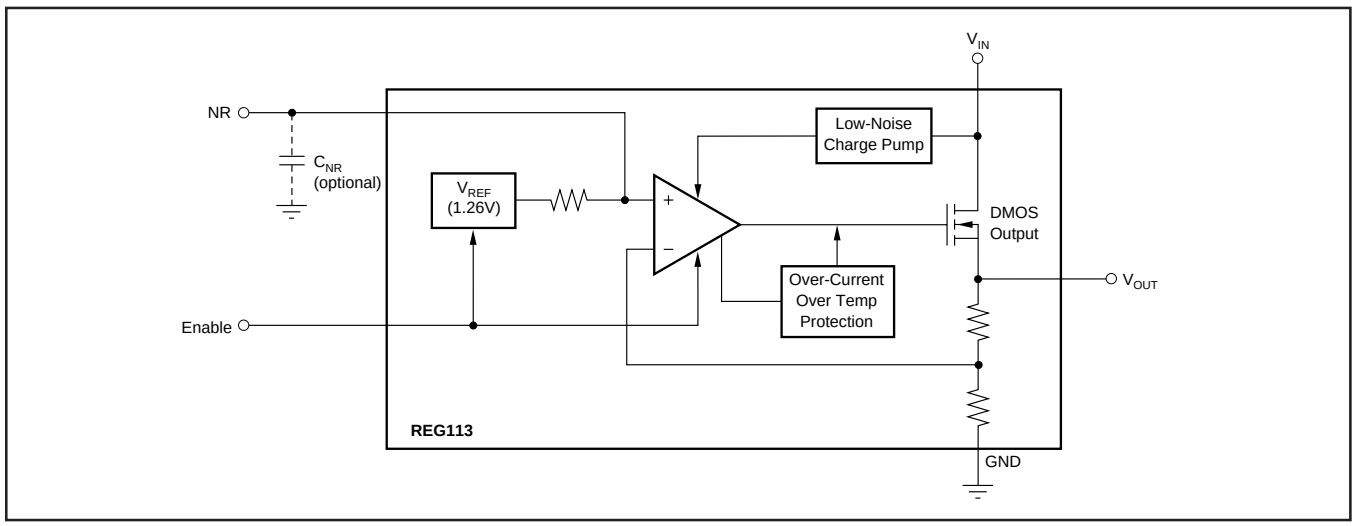



FIGURE 3. Block Diagram.

For large step changes in load current, the REG113 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient dropout region is shown as the top line in Figure 5. Values of $V_{IN}$ to $V_{OUT}$ voltage drop above this line insure normal transient response.

In the transient dropout region between DC and Transient, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available headroom $V_{IN}$ to $V_{OUT}$ voltage drop. Under worst-case conditions (full-scale load change with ($V_{IN} - V_{OUT}$) voltage drop close to DC dropout levels), the REG113 can take several hundred microseconds to re-enter the specified window of regulation.

## TRANSIENT RESPONSE

The REG113 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 0.47µF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, $C_{FB}$ (nominal value 10nF), from the output to the adjust pin also improves the transient response.

## THERMAL PROTECTION

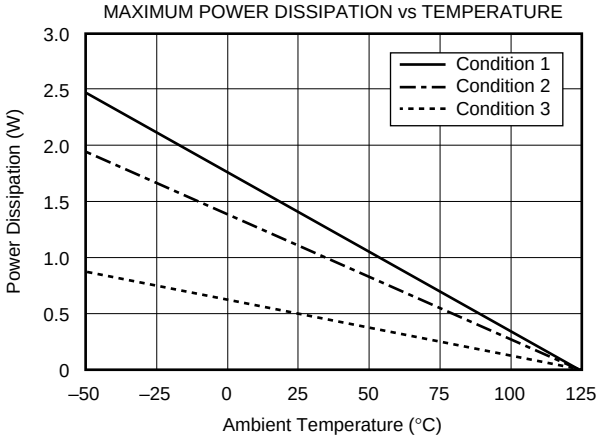
Power dissipated within the REG113 can cause the junction temperature to rise, however, the REG113 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, but can have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG113 is designed to protect against overload conditions and is not intended to replace proper heat sinking. Continuously running the REG113 into thermal shutdown will degrade reliability.

## POWER DISSIPATION

The REG113 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. On the MSOP-8 package, leads 5 through 8 are fused to the lead frame and may be used to improve the thermal performance of the package. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Although it is difficult or impossible to quantify all of the variables in a thermal design of this type, performance data for several simplified configurations are shown in Figure 6. In all cases the PCB copper area is bare copper, free of solder resist mask, and not solder plated. All examples are for 1-ounce copper and in the case of the MSOP-8, the copper area is connected to fused leads 5 to 8. See Figure 7 for thermal resistance for varying areas of copper. Using heavier copper can increase the effectiveness in removing the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.




| CONDITION | PACKAGE | PCB AREA | $\theta_{JA}$ |
|---|---|---|---|
| 1 | MSOP-8 | 1 sq. in. Cu, 1 Side | 71 |
| 2 | MSOP-8 | 0.25 sq. in. Cu, 1 Side | 90 |
| 3 | SOT-23-8 | None | 200 |

FIGURE 6. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

Power dissipation depends on input voltage, load conditions, and duty cycle and is equal to the product of the average output current times the voltage across the output element ($V_{IN}$ to $V_{OUT}$ voltage drop):

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT} \quad (3)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

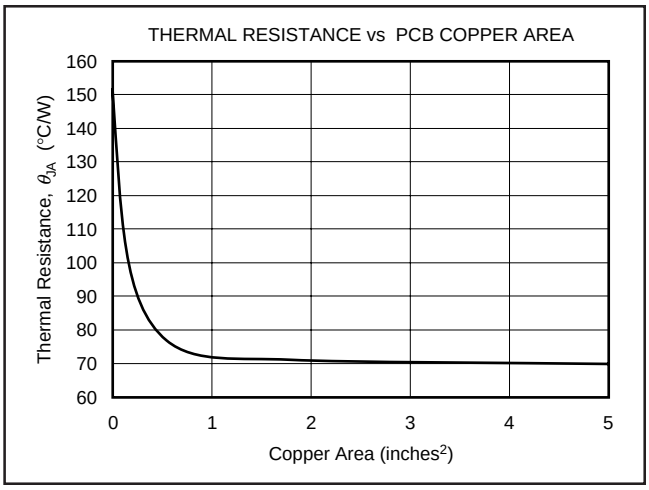



FIGURE 7. Thermal Resistance versus PCB Area for the MSOP-8.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| REG113EA-2.5/250 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13G |
| REG113EA-2.5/250.B | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13G |
| REG113EA-2.5/2K5 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13G |
| REG113EA-2.5/2K5.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13G |
| REG113EA-3.3/250 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13C |
| REG113EA-3.3/250.B | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13C |
| REG113EA-3.3/2K5 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13C |
| REG113EA-3.3/2K5.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13C |
| REG113EA-3/2K5 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13D |
| REG113EA-3/2K5.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13D |
| REG113EA-5/250 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13B |
| REG113EA-5/250.B | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13B |
| REG113EA-5/2K5 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13B |
| REG113EA-5/2K5.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | R13B |
| REG113NA-2.5/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13G |
| REG113NA-2.5/250.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13G |
| REG113NA-2.5/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13G |
| REG113NA-2.5/3K.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13G |
| REG113NA-2.85/250 | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 85 | R13N |
| REG113NA-2.85/3K | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 85 | R13N |
| REG113NA-3.3/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13C |
| REG113NA-3.3/250.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13C |
| REG113NA-3.3/250G4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13C |
| REG113NA-3.3/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13C |
| REG113NA-3.3/3K.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13C |
| REG113NA-3/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13D |
| REG113NA-3/250.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13D |
| REG113NA-3/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13D |
| REG113NA-3/3K.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13D |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| REG113NA-5/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13B |
| REG113NA-5/250.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13B |
| REG113NA-5/250G4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13B |
| REG113NA-5/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13B |
| REG113NA-5/3K.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | R13B |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

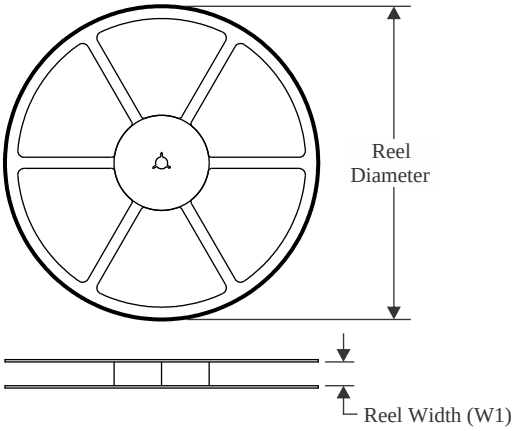
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

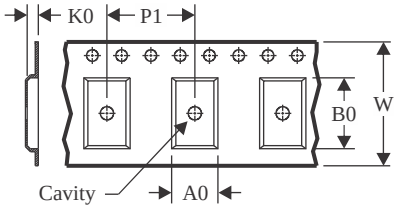
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

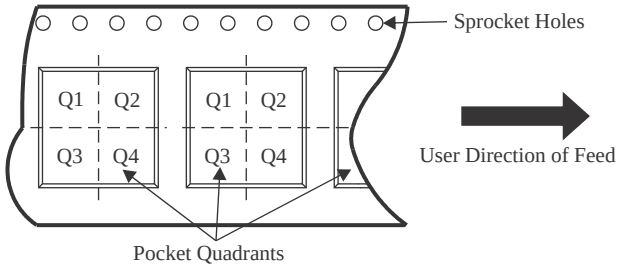



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

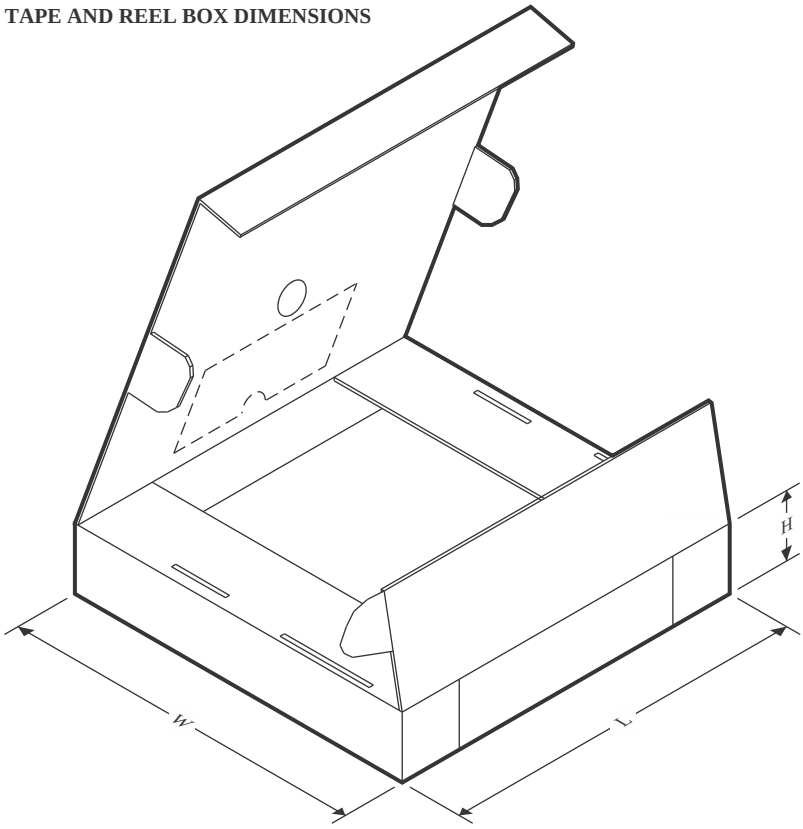
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REG113EA-2.5/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113EA-2.5/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113EA-3.3/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113EA-3.3/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113EA-3/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113EA-5/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113EA-5/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| REG113NA-2.5/250 | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-2.5/3K | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-3.3/250 | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-3.3/3K | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-3/250 | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-3/3K | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-5/250 | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| REG113NA-5/3K | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

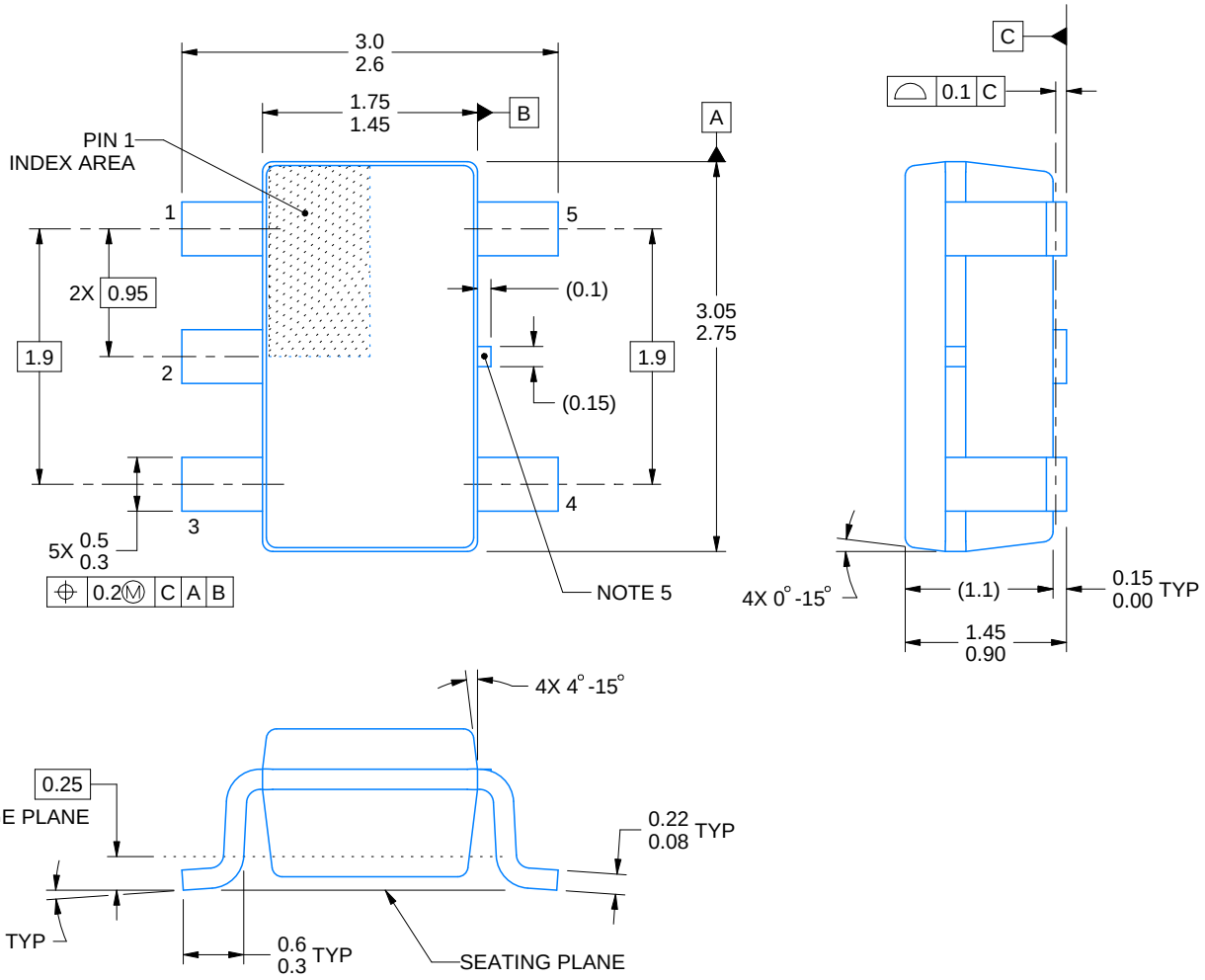
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| REG113EA-2.5/250 | VSSOP | DGK | 8 | 250 | 213.0 | 191.0 | 35.0 |
| REG113EA-2.5/2K5 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REG113EA-3.3/250 | VSSOP | DGK | 8 | 250 | 213.0 | 191.0 | 35.0 |
| REG113EA-3.3/2K5 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REG113EA-3/2K5 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REG113EA-5/250 | VSSOP | DGK | 8 | 250 | 213.0 | 191.0 | 35.0 |
| REG113EA-5/2K5 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| REG113NA-2.5/250 | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |
| REG113NA-2.5/3K | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| REG113NA-3.3/250 | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |
| REG113NA-3.3/3K | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| REG113NA-3/250 | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |
| REG113NA-3/3K | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| REG113NA-5/250 | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |
| REG113NA-5/3K | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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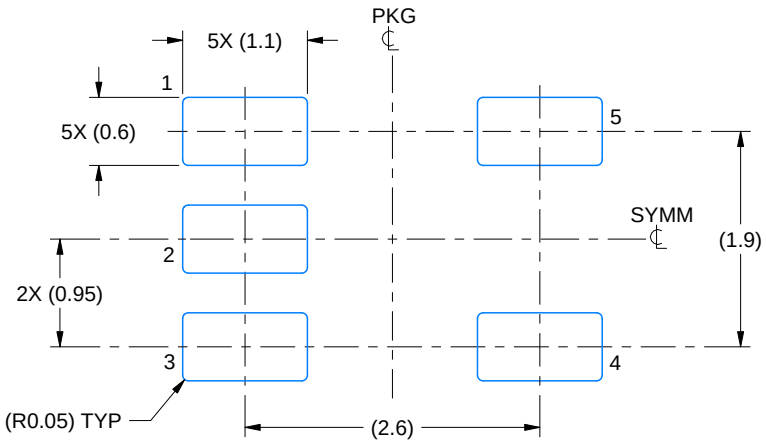
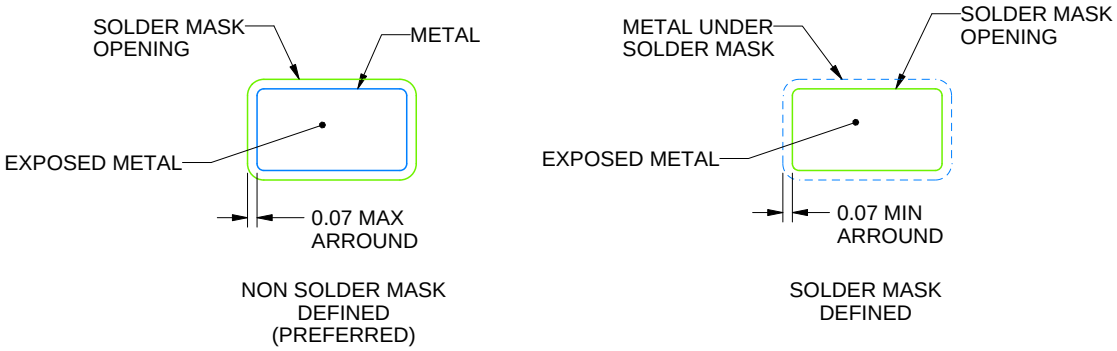
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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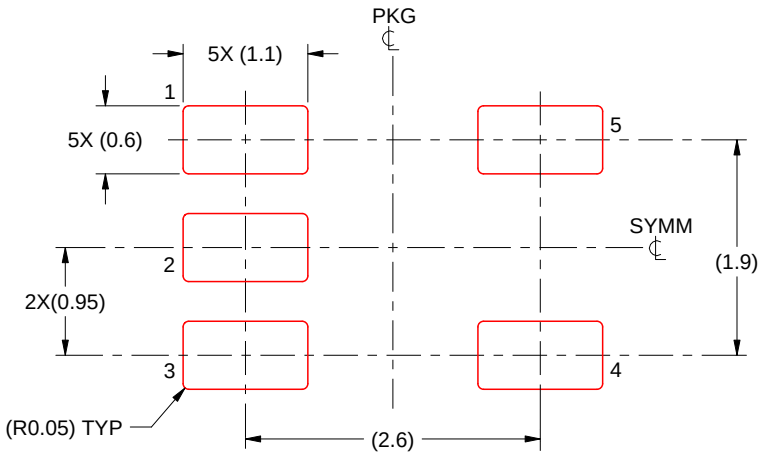
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

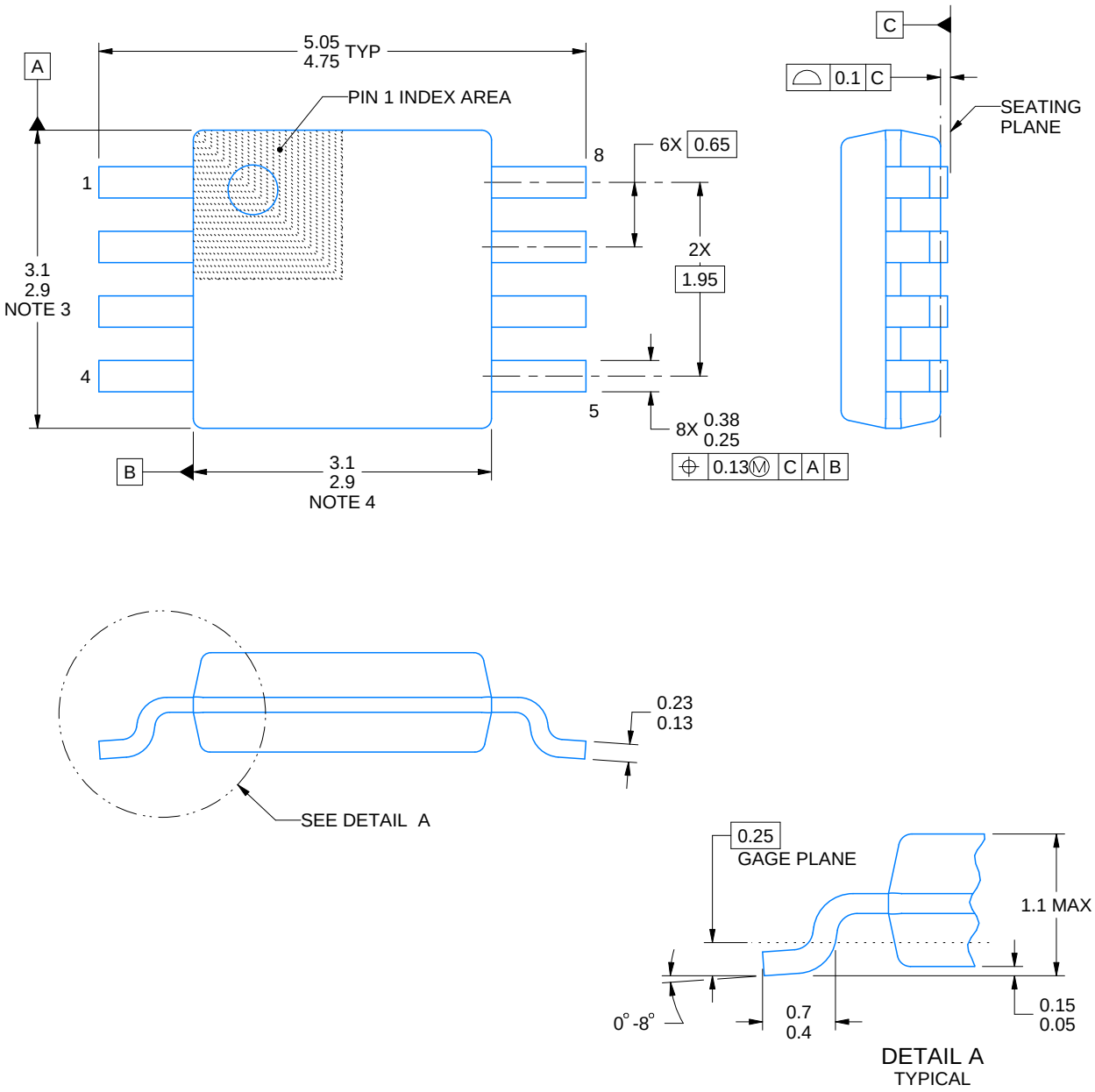
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

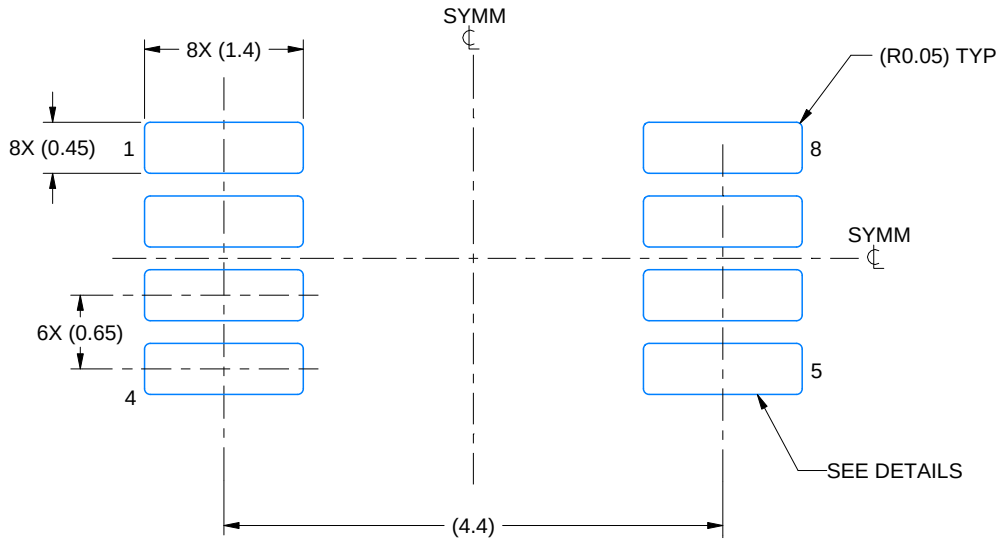
SMALL OUTLINE PACKAGE



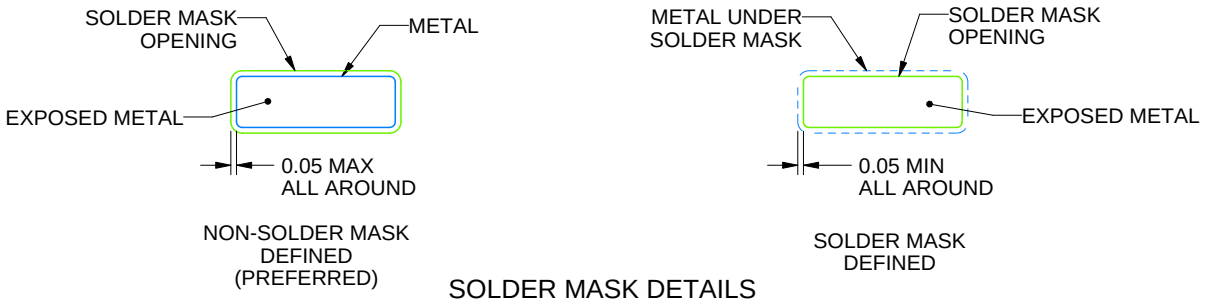

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

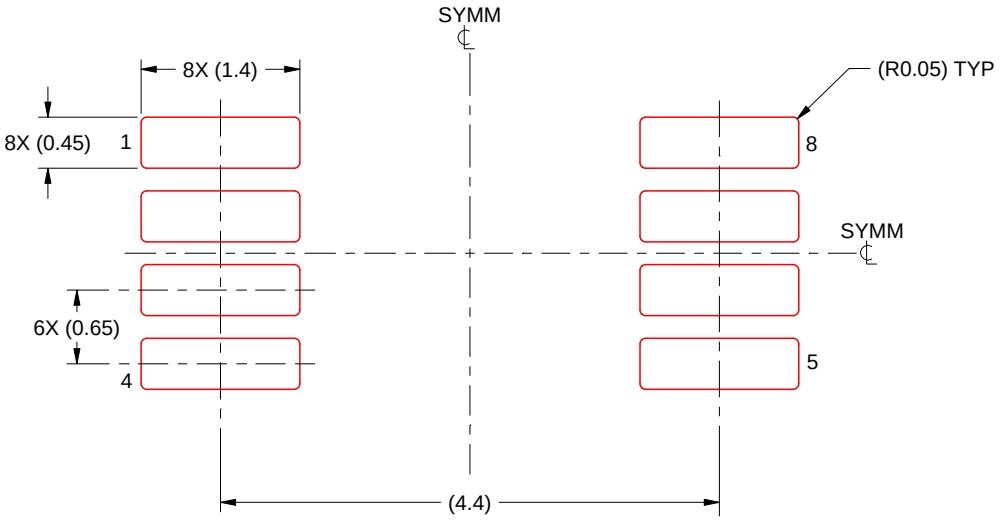



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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