

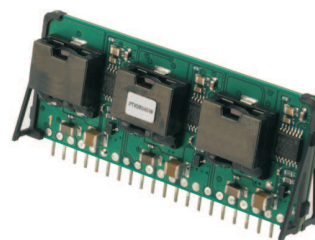
## 50-A, 8-V to 14-V INPUT, NON-ISOLATED, WIDE-OUTPUT ADJUST, VERTICAL POWER MODULE

### FEATURES

- 50-A Output Current
- 8-V to 14-V Input Voltage
- Wide-Output Voltage Adjust (0.8 V to 3.6 V)
- Efficiencies up to 95%
- On/Off Inhibit
- Differential Output Sense
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Overtemperature Protection
- Auto-Track™ Sequencing
- Start Up Into Output Prebias
- Operating Temperature: –40°C to 85°C
- Multi-Phase, Switch-Mode Topology
- Programmable Undervoltage Lockout (UVLO)
- Safety Agency Approvals: (Pending)  
UL/IEC/CSA-22.2 60950-1

### APPLICATIONS

- Advanced Computing and Server Applications



### DESCRIPTION

The PTV08040W is a high-performance 50-A rated, non-isolated, power module, that uses the latest multi-phase switched-mode topology. This provides a small, ready-to-use module, that can power the most densely populated multiprocessor systems. The PTV08040W is produced in a 21-pin, single in-line pin (SIP) package. The SIP footprint minimizes board space, and offers an alternate package option for space conscious applications. The modules use double-sided surface mount construction to provide a low profile and compact footprint.

Operating from an input voltage range of 8 V to 14 V, the PTV08040W requires a single resistor to set the output voltage to any value over the range, 0.8 V to 3.6 V. The wide input voltage range makes the PTV08040W particularly suitable for advanced computing and server applications that utilize a loosely regulated intermediate distribution bus of 8 V to 14 V.

The PTV08040W incorporates Auto-Track™ sequencing. The Auto-Track feature of the PTH and PTV family allows the outputs of multiple modules to track a common voltage during power up and power down transitions. This simplifies power up and power down supply-voltage sequencing in a power supply system.

The module incorporates a comprehensive list of features. They include on/off inhibit, a differential remote output voltage sense which ensures tight load regulation, and an output overcurrent and overtemperature shutdown to protect against load faults. The programmable undervoltage lockout allows the turn-on and turn-off voltage thresholds to be customized.



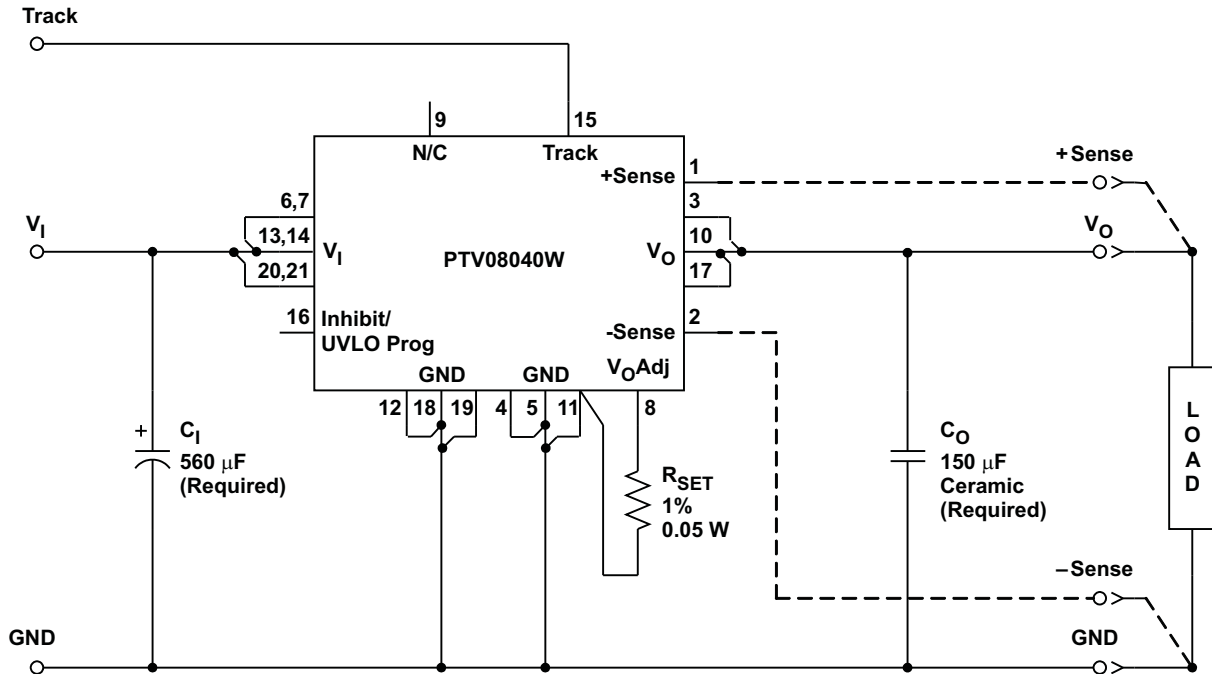
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Auto-Track, TMS320 are trademarks of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## STANDARD APPLICATION



A.  $R_{SET}$  = Required to set the output voltage higher than the minimum value (see the electrical characteristic for values.)

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			UNIT
	Track pin voltage	Track control (pin 15)	–0.3 V to $V_I + 0.3$ V
$T_A$	Operating temperature range	Over $V_I$ range	–40°C to 85°C
$T_{wave}$	Wave solder temperature	Surface temperature of module pins ( <b>5 seconds</b> )	260°C
$T_{stg}$	Storage temperature		–55°C to 125°C
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, Sine, mounted	500 G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20–2000 Hz	15 G
	Weight		16.6 grams
	Flammability	Meets UL94V-O	

## ELECTRICAL CHARACTERISTICS

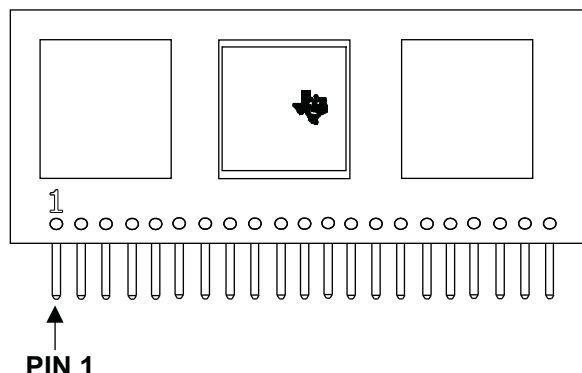
 $T_A = 25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 3.3\text{ V}$ ,  $C_I = 560\text{ }\mu\text{F}$ ,  $C_O = 150\text{ }\mu\text{F}$ , and  $I_O = I_{O\text{max}}$  (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_O$ Output current	$8\text{ V} \leq V_I \leq 14\text{ V}$	$25^\circ\text{C}$ , Natural Convection	0		50 <sup>(1)</sup>	A
		$60^\circ\text{C}$ , 200 LFM airflow	0		48 <sup>(1)</sup>	
$V_I$ Input voltage range	Over $I_O$ range		8		14	V
$V_{O\text{tol}}$ Set-point voltage tolerance					$\pm 2$ <sup>(2)</sup>	% $V_O$
$\Delta\text{Reg}_{\text{temp}}$ Temperature variation	$-40^\circ\text{C} < T_A < 85^\circ\text{C}$			$\pm 0.5$		% $V_O$
$\Delta\text{Reg}_{\text{line}}$ Line regulation	Over $V_I$ range			$\pm 3$		mV
$\Delta\text{Reg}_{\text{load}}$ Load regulation	Over $I_O$ range			$\pm 3$		mV
$\Delta\text{Reg}_{\text{tot}}$ Total output variation	Includes set-point, line, load, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$				$\pm 3$ <sup>(2)</sup>	% $V_O$
$\Delta\text{Reg}_{\text{adj}}$ Output adjust range			0.8		3.6	V
$\eta$ Efficiency	$I_O = 35\text{ A}$	$R_{\text{SET}} = 2.49\text{ k}\Omega$ , $V_O = 3.3\text{ V}$		95		%
		$R_{\text{SET}} = 6.98\text{ k}\Omega$ , $V_O = 2.5\text{ V}$		93		
		$R_{\text{SET}} = 13.0\text{ k}\Omega$ , $V_O = 2\text{ V}$		92		
		$R_{\text{SET}} = 16.9\text{ k}\Omega$ , $V_O = 1.8\text{ V}$		91		
		$R_{\text{SET}} = 27.4\text{ k}\Omega$ , $V_O = 1.5\text{ V}$		90		
		$R_{\text{SET}} = 53.6\text{ k}\Omega$ , $V_O = 1.2\text{ V}$		88		
		$R_{\text{SET}} = 113.0\text{ k}\Omega$ , $V_O = 1\text{ V}$		86		
		$R_{\text{SET}} = \text{open circuit}$ , $V_O = 0.8\text{ V}$		82		
$V_O$ ripple (peak-to-peak)	20-MHz bandwidth	All voltages		15		mV <sub>PP</sub>
$I_{O\text{trip}}$ Overcurrent threshold	Reset, followed by auto-recovery		75	100	115	A
$t_{\text{rr}}$ Transient response	1 A/ $\mu\text{s}$ load step, 50 to 100% $I_{O\text{max}}$ , $C_O = 150\text{ }\mu\text{F}$	Recovery time		50		$\mu\text{s}$
		$V_O$ over/undershoot		140		mV
$I_{\text{Ltrack}}$ Track input current (pin 15)	Pin to GND				$-0.13$ <sup>(3)</sup>	mA
$dV_{\text{track}}/dt$ Track slew rate capability	$C_O \leq C_{O(\text{max})}$				1	V/ms
UVLO Undervoltage lockout threshold	Pin 16 open	$V_I$ Increasing		7.5 <sup>(4)</sup>	7.8	V
		$V_I$ Decreasing	6	6.5 <sup>(4)</sup>		
Inhibit control (pin 16)	Referenced to GND					V
$V_{\text{IH}}$ Input high voltage			2.5		Open <sup>(5)</sup>	
$V_{\text{IL}}$ Input low voltage			$-0.2$		0.5	
$I_{\text{Linh}}$ Input low current	Pin to GND			0.5		mA
$I_{\text{linh}}$ Input standby current	Pin 16 to GND			35		mA
$f_s$ Switching frequency	Over $V_I$ and $I_O$ ranges		900	1050	1200	kHz
$C_I$ External input capacitance			560 <sup>(6)</sup>			$\mu\text{F}$
$C_O$ External output capacitance	Capacitance value	Nonceramic	0		14,000 <sup>(7)</sup>	$\mu\text{F}$
		Ceramic	150 <sup>(8)</sup>		750	
	Equivalent series resistance (nonceramic)		3 <sup>(9)</sup>			m $\Omega$
MTBF Reliability	Per Bellcore TR-332 50% stress, $T_A = 40^\circ\text{C}$ , ground benign		2.7			$10^6$ Hrs

- See SOA curves or consult factory for appropriate derating.
- The set-point voltage tolerance is affected by the tolerance of  $R_{\text{SET}}$ . The stated limit is unconditionally met if  $R_{\text{SET}}$  has a tolerance of 1% with 100 ppm/ $^\circ\text{C}$  or better temperature stability.
- This control pin has an internal pull-up to 5 V. A small, low-leakage (<100 nA) MOSFET or open-drain/collector voltage supervisor IC is recommended to control this pin. For further information, see the related application section.
- These are the default voltages. They may be adjusted using the UVLO Prog control input. See the *Application Information* section for further guidance.
- This control pin has an internal pull-up to 5 V. When left open-circuit the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended to control this pin. For further information, see the related application section.
- A minimum capacitance of 560- $\mu\text{F}$  is required at the input for proper operation. For best results, 1000  $\mu\text{F}$  is recommended. The capacitance must be rated for a minimum of 300 mArms of ripple current.
- This is the calculated maximum. The minimum ESR requirement often results in a lower value. For further information, see the related application section.
- A minimum value of output capacitance is required for proper operation. Adding additional capacitance at the load further improves transient response.
- This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 5 m $\Omega$  as the minimum when using manufacturer's max-ESR values to calculate.

## DEVICE INFORMATION

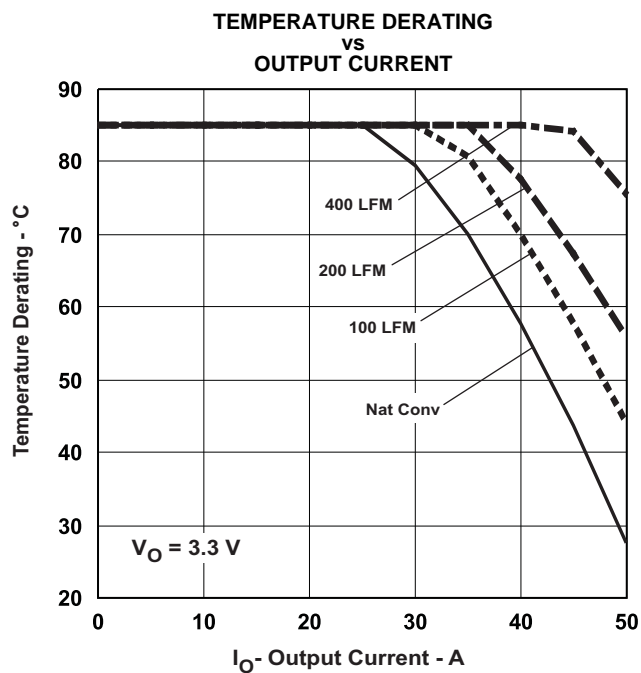
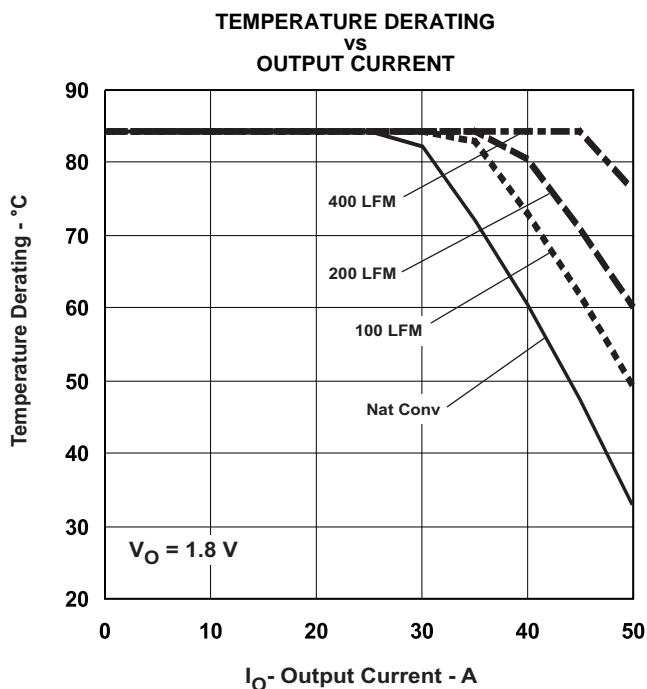
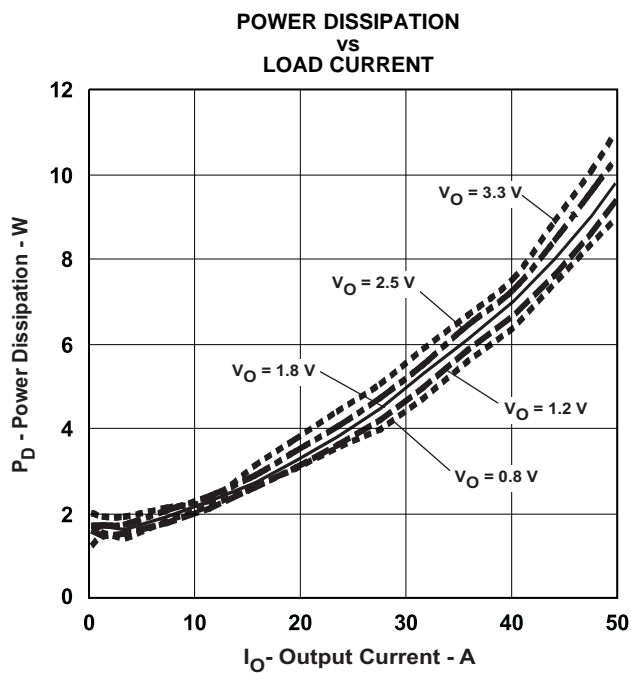
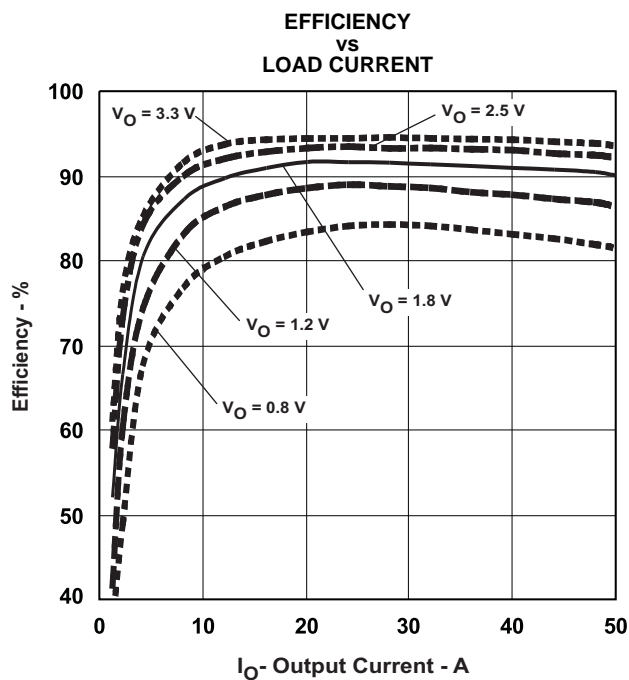
**PTV08040W**  
(Top View)



## TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	4, 5, 11, 12, 18, 19	This is the common ground connection for the $V_I$ and $V_O$ power connections. It is also the 0 $V_{dc}$ reference for the control inputs.
$V_I$	6, 7, 13, 14, 20, 21	The positive input voltage power node to the module, which is referenced to common GND.
$V_O$	3, 10, 17	The regulated positive power output with respect to GND.
Inhibit / UVLO	16	<p>The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever the input voltage is above the UVLO threshold.</p> <p>This pin is also used for input undervoltage lockout (UVLO) programming. Connecting a resistor from this pin to signal ground allows the <i>ON</i> threshold of the UVLO to be adjusted higher than the default value. The hysteresis can also be independently reduced by connecting a second resistor from this pin to <math>V_I</math>. For further information, see the Application Information section.</p>
$V_O$ Adjust	8	<p>A 1%, 0.05-W resistor must be connected between this pin and GND to set the output voltage higher than the minimum value. The set-point range for the output voltage is from 0.8 V to 3.6 V. The resistor required for a given output voltage may be calculated from the following formula. If left open circuit, the module output defaults to its lowest output voltage value. For further information on the adjustment and/or trimming of the output voltage, see the related Application Information section.</p> $R_{SET} = 30.1 \times \frac{0.8}{(V_O - 0.8)} - 7.135 \text{ k}\Omega$ <p>The specification table gives the preferred resistor values for a number of standard output voltages.</p>
+Sense	1	The sense inputs allow the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense should be connected to $V_O$ . If it is left open, a low-value internal resistor ensures that the output remains in regulation.
–Sense	2	For optimal voltage accuracy, –Sense should be connected to the ground return at the load. If it is left open, a low-value internal resistor ensures that the output remains in regulation.
Track	15	This is an analog control input that allows the output voltage to follow another voltage during power up and power down sequences. The pin is active from 0 V, up to the nominal set-point voltage. Within this range, the module output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its nominal output voltage. If unused, this input should be connected to $V_I$ for a faster power up. For further information, see the related Application Information section.
N/C	9	No Connection

# TYPICAL CHARACTERISTICS ( $V_I = 12\text{ V}$ )<sup>(1)(2)</sup>



- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 1](#) and [Figure 2](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4-in. x 4-in., double-sided, 4-layer PCB with 1-oz. copper. See the mechanical specification for more information. Applies to [Figure 3](#) and [Figure 4](#).

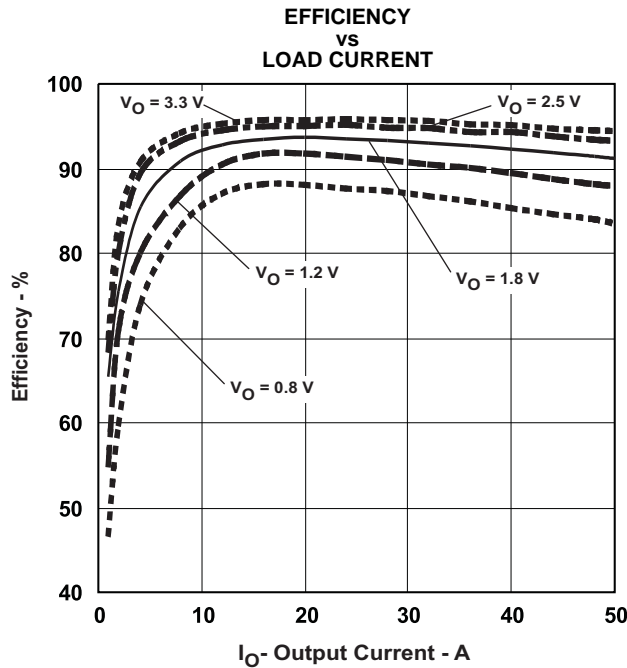
TYPICAL CHARACTERISTICS ( $V_I = 8\text{ V}$ )<sup>(1)(2)</sup>

Figure 5.

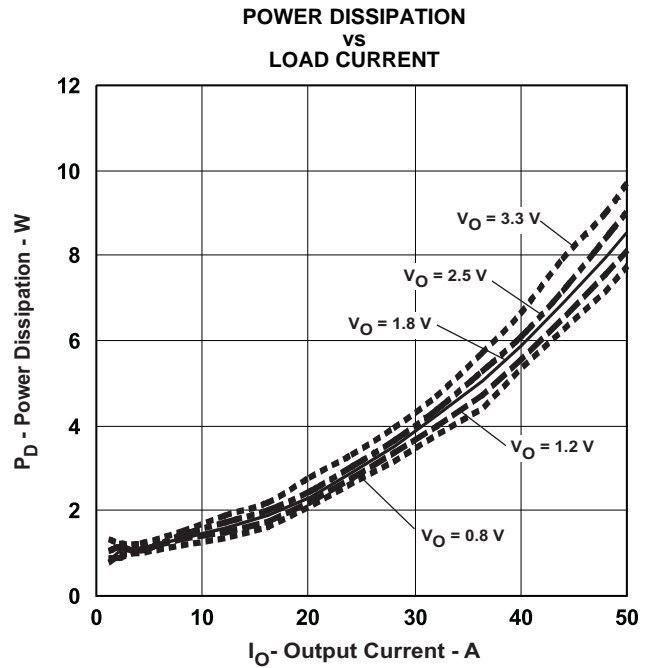


Figure 6.

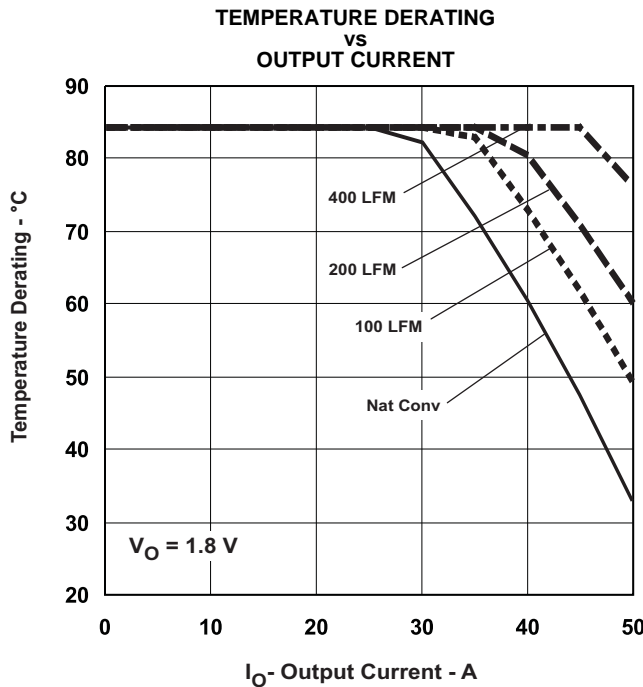


Figure 7.

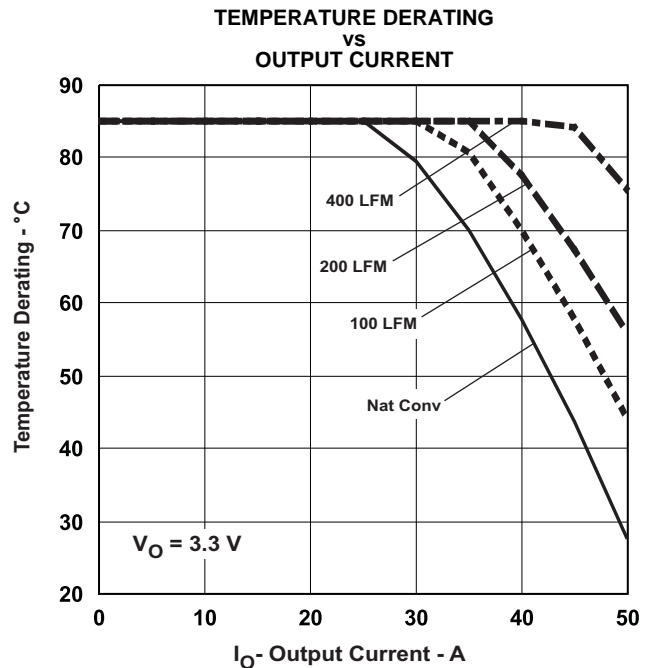


Figure 8.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 5](#) and [Figure 6](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4-in. x 4-in., double-sided, 4-layer PCB with 1-oz. copper. See the mechanical specification for more information. Applies to [Figure 7](#) and [Figure 8](#).

## APPLICATION INFORMATION

### CAPACITOR RECOMMENDATIONS FOR THE PTV08040W POWER MODULE

The PTV08040W is a state-of-the-art multi-phase power converter topology that uses three parallel switching and filter inductor paths between the common input and output filter capacitors. The three paths share the load current, operate at the same frequency, and are evenly displaced in phase.

With multiple switching paths the transient output current capability is significantly increased. This reduces the amount of external output capacitance required to support a load transient. As a further benefit, the ripple current, as seen by the input and output capacitors, is reduced in magnitude and effectively tripled in frequency.

#### Input Capacitor (Required)

The improved transient response of a multi-phase converter places a bigger burden on the transient capability of the input source. The size and value of the input capacitor is therefore determined by this converter's transient performance capability. The minimum amount of input capacitance required is 560  $\mu\text{F}$ , with an RMS ripple current rating of 300 mA. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes. For high-performance applications, or wherever the transient performance of the input source is limited, 1000  $\mu\text{F}$  of input capacitance is recommended.

Ripple current, less than 100 mV of equivalent series resistance (ESR), and temperature are the main considerations when selecting input capacitors. The ripple current reflected from the input of the PTV08040W module is moderate to low. Therefore any good quality, computer-grade electrolytic capacitor, of either value suggested, has an adequate ripple current rating.

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of  $2 \times$  (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement. When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, Os-Con, poly-aluminum, and polymer-tantalum types should be considered. Adding one or two ceramic capacitors to the input reduces high-frequency reflected ripple current.

#### Output Capacitors (Ceramic Required)

The PTV08040W requires a minimum output capacitance of 150  $\mu\text{F}$  of ceramic capacitors. This is necessary for the stable operation of the regulator. Additional capacitance can be added to improve the module's performance to load transients. High quality computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C. For operation below 0°C, tantalum, ceramic, or Os-Con type capacitors are necessary.

When using a combination of one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 3 m $\Omega$  (5 m $\Omega$  when calculating using the manufacturer's maximum ESR values). A list of preferred low-ESR type capacitors are identified in [Table 1](#).

#### Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitors, with values between 10  $\mu\text{F}$  and 100  $\mu\text{F}$ , does not exceed 750  $\mu\text{F}$ . Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10  $\mu\text{F}$  or greater.



## Tantalum Capacitors

Tantalum type capacitors are only used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable due to their reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer-tantalum capacitors for the output, the minimum ESR limit is encountered before the maximum capacitance value is reached.

## Capacitor Table

[Table 1](#) identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

*This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.*

## Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/μs. The typical voltage deviation for this load transient is given in the data sheet specification table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.



**Table 1. Input/Output Capacitors<sup>(1)</sup>**

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity		Vendor Part No.
	Working Voltage	Value (μF)	Max. ESR at 100 kHz	Max Ripple Current at 85°C (Irms)	Physical Size (mm)	Input Bus	Output Bus	
Panasonic FC (Radial)	25 V	1000	0.043 Ω	>1690 mA	16 × 15	1	1	EEUFC1E102S
	25 V	560	0.065 Ω	1205 mA	12,5 × 15	1	1	EEUFC1E561S
FK (SMD)	16 V	680	0.080 Ω	>850 mA	10 × 10,2	1	1	EEVFK1C681P
	35 V	1000	0.060 Ω	1100 mA	12,5 × 13,5	1	1	EEVFK1V102Q
United Chemi-Con MVZ(SMD)	25 V	470	0.090 Ω	670 mA	10 × 10	2	1	MVZ25VC471MJ10TP
LXZ, Aluminum (Radial)	16 V	470	0.090 Ω	760 mA	10 × 12,5	2	1	LXZ16VB471M10X12LL
	16 V	680	0.068 Ω	1050 mA	10 × 16	1	1	LXZ16VB681M10X16LL
PS, Poly-Aluminum(Radial)	16 V	330	0.014 Ω	5060 mA	10 × 12,5	2	≤3	16PS330MJ12
PXA, Poly-Aluminum (SMD)	16 V	330	0.014 Ω	5050 mA	10 × 12,2	2	≤3	PXA16VC331MJ12TP
Nichicon, Aluminum HD (Radial)	25 V	680	0.038 Ω	1430 mA	10 × 16	1	1	UHD1C681MHR
PM (Radial)	25 V	560	0.060 Ω	1060 mA	12,5 × 15	1	1	UPM1E561MHH6
	35 V	560	0.048 Ω	1360 mA	16 × 15	1	1	UPM1V561MHH6
Panasonic, Poly-Aluminum	6.3 V	180	0.005 Ω	4000 mA	7,3 × 4,3 × 4,2	N/R <sup>(2)</sup>	≤4	EEFWA1C331P
Sanyo TPE, Poscap (SMD)	10 V	330	0.025 Ω	3000 mA	7,3 × 5,7	N/R <sup>(2)</sup>	≤5	10TPE330M
SVP, OS-CON (SMD)	16 V	330	0.016 Ω	>4700 mA	10 × 12,6	2	≤3	16SVP330M
SEPC, OS-CON (Radial)	16 V	470	0.010Ω	>6000 mA	11 × 13	2	≤2	16SEPC470M
AVX, Tantalum, Series III TPS (SMD)	10 V	470	0.045 Ω	>1723 mA	7,3 × 5,7 × 4,1	N/R <sup>(2)</sup>	≤7	TPSE477M010R0045
	10 V	330	0.045 Ω	1723 mA	7,3 × 5,7 × 4,1	N/R <sup>(2)</sup>	≤7	TPSE337M010R0045
Kemet, Poly-Tantalum T520 (SMD)	10 V	330	0.040 Ω	1800 mA	4,3 × 7,3 × 4	N/R <sup>(2)</sup>	≤7	T520X337M010AS
T530 (SMD)	10 V	330	0.015 Ω	>3800 mA	4,3 × 7,3 × 4	N/R <sup>(2)</sup>	≤3	T530X337M010AS
	6.3 V	470	0.012 Ω	4200 mA	4,3 × 7,3 × 4	N/R <sup>(2)</sup>	≤2	T530X477M006AS
Vishay-Sprague 595D, Tantalum (SMD)	10 V	470	0.100 Ω	1440 mA	7,2 × 5,7 × 4,1	N/R <sup>(2)</sup>	2	595D477X0010R2T
94SA, Os-con (Radial)	16 V	1000	0.015 Ω	9740 mA	16 × 25	1	≤3	94SA108X0016HBP
Kemet, Ceramic X5R (SMD)	16 V	10	0.002 Ω	–	3225	1	≤10	C1210C106M4PAC
	6.3 V	47	0.002 Ω	–	3225	N/R <sup>(2)</sup>	≤10	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 V	100	–	–	3225	N/R <sup>(2)</sup>	≤5	GRM32ER60J107M
	6.3 V	47	–	–	3225	N/R <sup>(2)</sup>	≤ 10	GRM32ER60J476M
	16 V	47	–	–	3225	1	≤ 10	GRM32ER61C476K
	16 V	22	–	–	3225	1	≤ 10	GRM32ER61C226K
	16 V	10	–	–	3225	1	≤ 10	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V	100	–	–	3225	N/R <sup>(2)</sup>	≤5	C3225X5R0J107MT
	6.3 V	47	–	–	3225	N/R <sup>(2)</sup>	≤ 10	C3225X5R0J476MT
	16 V	22	–	–	3225	1	≤ 10	C3225X5R1C226MT
	16 V	10	–	–	3225	1	≤ 10	C3225X5R1C106MT

**(1) Capacitor Supplier Verification**

1.Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.

**RoHS, Lead-free and Material Details**

2.Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.

(2) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.

## ADJUSTING THE OUTPUT VOLTAGE OF THE PTV08040W WIDE-OUTPUT ADJUST POWER MODULE

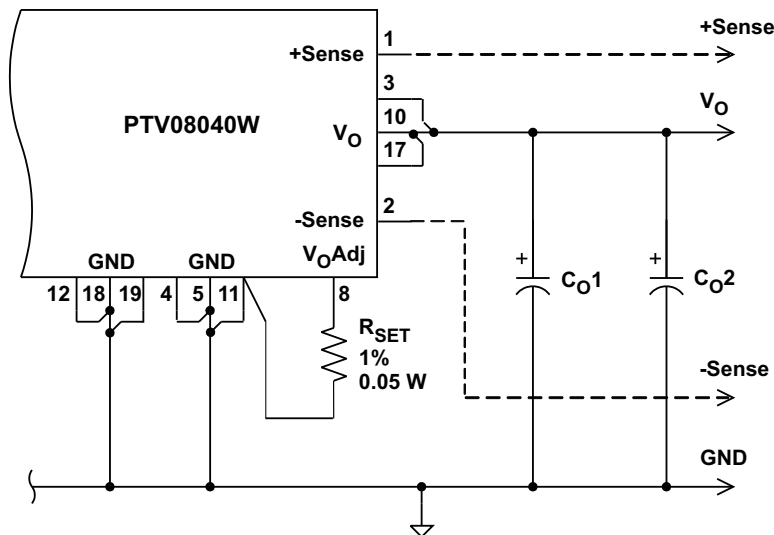
The  $V_O$  Adjust control (pin 8) sets the output voltage of the PTV08040W product. The adjustment range is from 0.8 V to 3.6 V. The adjustment method requires the addition of a single external resistor,  $R_{SET}$ , that must be connected directly between the  $V_O$  Adjust and GND pins. Table 2 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages, the value of the required resistor can either be calculated using Equation 1, or simply selected from the range of values given in Table 3. Figure 9 shows the placement of the required resistor.

$$R_{SET} = 30.1 \times \frac{0.8}{(V_O - 0.8)} - 7.135 \text{ k}\Omega \quad (1)$$

**Table 2. Standard Values of  $R_{SET}$  for Common Output Voltages**

$V_O$ (Required)	PTV08040W	
	$R_{SET}$	$V_O$ (Actual)
3.3 V	2.49 k $\Omega$	3.303 V
2.5 V	6.98 k $\Omega$	2.5 V
2.0 V	13.0 k $\Omega$	1.997 V
1.8 V	16.9 k $\Omega$	1.796 V
1.5 V	27.4 k $\Omega$	1.498 V
1.2 V	53.6 k $\Omega$	1.202 V
1.0 V	113 k $\Omega$	1 V
0.8 V	Open	0.8 V



**Figure 9.  $V_O$  Adjust Resistor Placement**

- A 0.05-W rated resistor may be used. The tolerance should be 1%, and the temperature stability, 100 ppm/ $^{\circ}\text{C}$  (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pin 8 and nearest GND pin (pin 11) using dedicated PCB traces.
- Never connect capacitors from  $V_O$  Adjust to either GND or  $V_O$ . Any capacitance added to the  $V_O$  Adjust pin affects the stability of the regulator.

**Table 3. Output Voltage Set-Point Resistor Values**

$V_O$	$R_{SET}$	$V_O$	$R_{SET}$	$V_O$	$R_{SET}$
0.8	Open	1.375	34.8 k $\Omega$	2.4	7.87 k $\Omega$
0.825	953 k $\Omega$	1.4	33.2 k $\Omega$	2.45	7.50 k $\Omega$
0.85	475 k $\Omega$	1.425	31.6 k $\Omega$	2.5	6.98 k $\Omega$
0.875	316 k $\Omega$	1.45	30.1 k $\Omega$	2.55	6.65 k $\Omega$
0.9	232 k $\Omega$	1.475	28.7 k $\Omega$	2.6	6.19 k $\Omega$
0.925	187 k $\Omega$	1.5	27.4 k $\Omega$	2.65	5.90 k $\Omega$
0.95	154 k $\Omega$	1.55	24.9 k $\Omega$	2.7	5.49 k $\Omega$
0.975	130 k $\Omega$	1.6	22.6 k $\Omega$	2.75	5.23 k $\Omega$
1	113 k $\Omega$	1.65	21.0 k $\Omega$	2.8	4.87 k $\Omega$
1.025	100 k $\Omega$	1.7	19.6 k $\Omega$	2.85	4.64 k $\Omega$
1.05	88.7 k $\Omega$	1.75	18.2 k $\Omega$	2.9	4.32 k $\Omega$
1.075	80.6 k $\Omega$	1.8	16.9 k $\Omega$	2.95	4.02 k $\Omega$
1.1	73.2 k $\Omega$	1.85	15.8 k $\Omega$	3	3.83 k $\Omega$
1.125	66.5 k $\Omega$	1.9	14.7 k $\Omega$	3.05	3.57 k $\Omega$
1.15	61.9 k $\Omega$	1.95	13.7 k $\Omega$	3.1	3.32 k $\Omega$
1.175	57.6 k $\Omega$	2	13.0 k $\Omega$	3.15	3.09 k $\Omega$
1.2	53.6 k $\Omega$	2.05	12.1 k $\Omega$	3.2	2.87 k $\Omega$
1.225	49.9 k $\Omega$	2.1	11.3 k $\Omega$	3.25	2.67 k $\Omega$
1.25	46.4 k $\Omega$	2.15	10.7 k $\Omega$	3.3	2.49 k $\Omega$
1.275	43.2 k $\Omega$	2.2	10.0 k $\Omega$	3.35	2.32 k $\Omega$
1.3	41.2 k $\Omega$	2.25	9.53 k $\Omega$	3.4	2.10 k $\Omega$
1.325	38.3 k $\Omega$	2.3	8.87 k $\Omega$	3.5	1.78 k $\Omega$
1.35	36.5 k $\Omega$	2.35	8.45 k $\Omega$	3.6	1.47 k $\Omega$

## ADJUSTING THE UNDERVOLTAGE LOCKOUT (UVLO) OF THE PTV08040W POWER MODULES

The PTV08040W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the ON threshold ( $V_{THD}$ ) and hysteresis ( $V_{HYS}$ ) voltages. Below the ON threshold, the Inhibit control is overridden, and the module does not produce an output. The hysteresis voltage is the difference between the ON and OFF threshold voltages. It ensures a clean power-up, even when the input voltage is rising slowly. The hysteresis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

### UVLO Adjustment

The UVLO feature of the PTV08040W module allows for limited adjustment of both the on threshold and hysteresis voltages. The adjustment is made via the *UVLO Prog* control pin. When the UVLO Prog pin is left open circuit, the ON threshold and hysteresis voltages are internally set to their default values. The ON threshold has a nominal voltage of 7.5 V, and the hysteresis 1 V. This ensures that the module produces a regulated output when the minimum input voltage is applied (see specifications). The combination correlates to an OFF threshold of approximately 6.5 V. The adjustments are limited. The ON threshold can only be adjusted higher, and the hysteresis voltage can only be reduced in magnitude.

The ON threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. This prevents it from operating if the input bus fails to completely rise to its specified regulation voltage. The hysteresis should not be changed unless absolutely necessary. The hysteresis ensures that the module exhibits a clean startup. Therefore, adjustment of the hysteresis should only be considered if there is a system requirement to specifically set the off threshold voltage (in addition to the on threshold). Depending on the load regulation of the input source, the hysteresis should not be adjusted below 0.5 V without careful consideration.

### Adjustment Method

The resistors,  $R_{THD}$  and  $R_{HYS}$  (see Figure 10), provide the adjustment of the on-threshold and hysteresis voltages.  $R_{THD}$  connects between the UVLO Prog control pin and GND, and  $R_{HYS}$  is connected between the UVLO Prog and  $V_I$ .  $R_{THD}$  alone is used to adjust the on-threshold voltage **higher**. However, to adjust the hysteresis to a **lower** value requires **both** the  $R_{HYS}$  and  $R_{THD}$  resistors to be placed in the circuit.

The recommended adjustment method requires that any change to the hysteresis be determined first. If the hysteresis is changed, then a value for  $R_{THD}$  **must** also be calculated. This is irrespective of whether a change is required to the value of  $V_{THD}$ . If there is no change to  $V_{HYS}$ , then a resistor should not be placed in the  $R_{HYS}$  location.  $R_{HYS}$  should then be assigned an infinite value for calculating the value of  $R_{THD}$ .

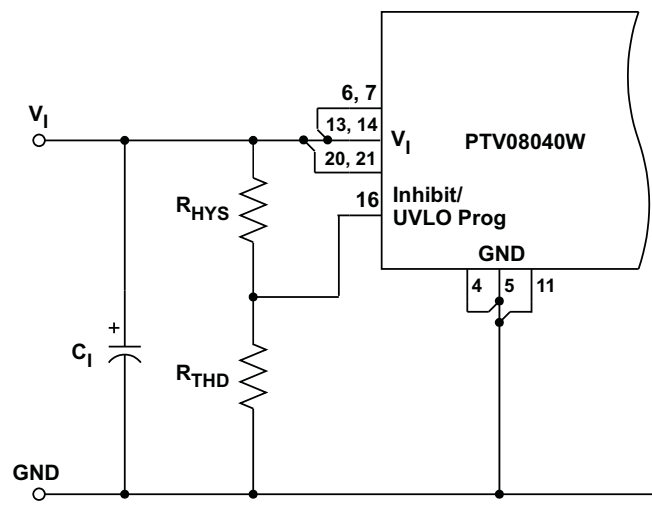


Figure 10. UVLO Program Resistor Placement

## Hysteresis Adjust

The hysteresis voltage,  $V_{HYS}$ , is the difference between the *ON* and *OFF* threshold values. The default value is 1 V and it can only be adjusted to a lower value.

*Caution should be used when changing the hysteresis voltage to a lower value, as it could permit start-up oscillations.*

Any change in the hysteresis voltage requires both  $R_{HYS}$  and  $R_{THD}$  resistors be in place. Adding  $R_{HYS}$  alone does not have the desired effect. The value for  $R_{HYS}$  must first be calculated using Equation 2, and then be used to determine a value for  $R_{THD}$ , using Equation 3.

$$R_{HYS} = \frac{26.1 \times V_{HYS}}{0.365 \times (1 - V_{HYS})} \text{ k}\Omega \quad (2)$$

## Threshold Adjust

Equation 3 determines the value of  $R_{THD}$  required to adjust  $V_{THD}$  to a new value. The default value is 7.5 V, and it may only be adjusted to a higher value. If the hysteresis value has been adjusted, then a value for  $R_{THD}$  must also be calculated. (This is irrespective of whether  $V_{THD}$  is being adjusted.) If there has been no adjustment for the hysteresis voltage, the term  $1/R_{HYS}$  in Equation 3, may be assigned the value, 0.

$$R_{THD} = \frac{39.2}{39.2[(1/R_{HYS} + 0.014)(V_{THD}/2.5 - 1) - 0.0027] - 1} \text{ k}\Omega \quad (3)$$

## Calculated Values

Table 4 shows a matrix of standard resistor values for  $R_{HYS}$  and  $R_{THD}$ , for different options of the on-threshold ( $V_{THD}$ ) and hysteresis ( $V_{HYS}$ ) voltages. For most applications, only the on-threshold voltage should need to be adjusted. In this case select only a value for  $R_{THD}$  from far right-hand column.

The hysteresis should only be adjusted if there is a specific requirement to independently adjust the off-threshold, separately from the on-threshold voltage. In this case, a value for both  $R_{HYS}$  and  $R_{THD}$  must be selected from Table 4. This is irrespective of whether the on-threshold voltage is being adjusted.

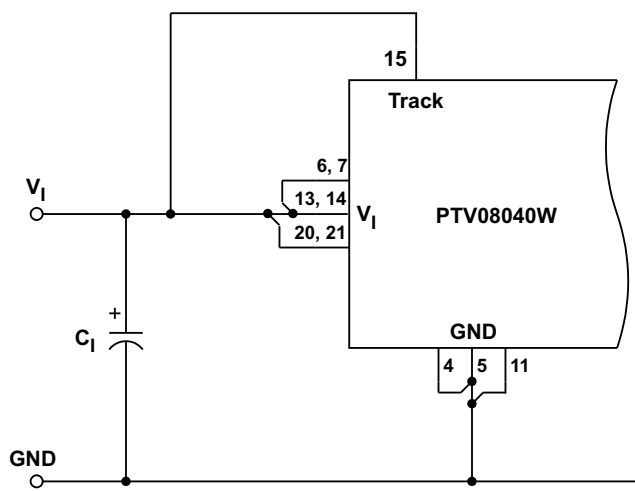
**Table 4. Calculated Values of  $R_{HYS}$  and  $R_{THD}$ , for Various Values of  $V_{HYS}$  and  $V_{THD}$**

	$V_{HYS}$	0.5 V	0.6 V	0.7 V	0.8 V	0.9 V	1 V (default)
$V_{THD}$	$R_{HYS}$	71.5 k $\Omega$	107 k $\Omega$	165 k $\Omega$	287 k $\Omega$	649 k $\Omega$	N/A
8 V	$R_{THD}$	30.1 k $\Omega$	43.2 k $\Omega$	63.4 k $\Omega$	97.6 k $\Omega$	169 k $\Omega$	402 k $\Omega$
8.5 V		25.5 k $\Omega$	36.5 k $\Omega$	51.1 k $\Omega$	73.2 k $\Omega$	110 k $\Omega$	187 k $\Omega$
9 V		23.2 k $\Omega$	30.9 k $\Omega$	42.2 k $\Omega$	57.6 k $\Omega$	82.5 k $\Omega$	124 k $\Omega$
9.5 V		20 k $\Omega$	27.4 k $\Omega$	36.5 k $\Omega$	48.7 k $\Omega$	64.9 k $\Omega$	90.9 k $\Omega$
10 V		18.2 k $\Omega$	24.3 k $\Omega$	31.6 k $\Omega$	41.2 k $\Omega$	54.9 k $\Omega$	73.2 k $\Omega$
10.5 V		16.2 k $\Omega$	21.5 k $\Omega$	28 k $\Omega$	36.5 k $\Omega$	46.4 k $\Omega$	60.4 k $\Omega$
11 V		15 k $\Omega$	19.6 k $\Omega$	25.5 k $\Omega$	32.4 k $\Omega$	41.2 k $\Omega$	52.3 k $\Omega$
11.5 V		14 k $\Omega$	18.2 k $\Omega$	23.2 k $\Omega$	28 k $\Omega$	36.5 k $\Omega$	45.3 k $\Omega$
12 V		12.7 k $\Omega$	16.5 k $\Omega$	21 k $\Omega$	26.1 k $\Omega$	32.4 k $\Omega$	40.2 k $\Omega$

## FEATURES OF THE PTH/PTV FAMILY OF NONISOLATED WIDE OUTPUT ADJUST POWER MODULES

### Soft-Start Power Up

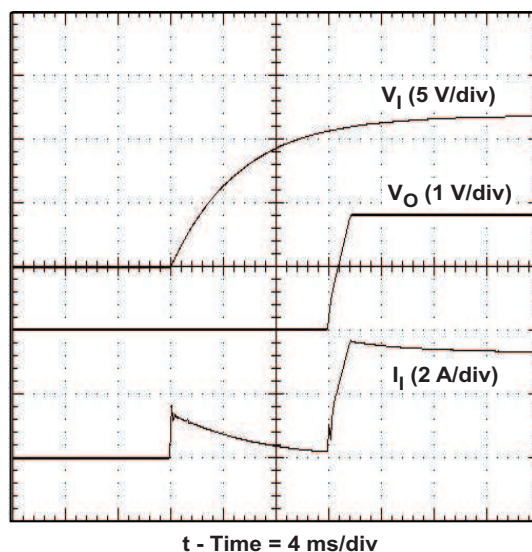
The Auto-Track feature allows the power-up of multiple PTH/PTV modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage,  $V_I$  (see Figure 11).



**Figure 11. Track Pin Connection**

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms–15 ms) before allowing the output voltage to rise.



**Figure 12. Power-Up Waveform**

The output then progressively rises to the module's setpoint voltage. [Figure 12](#) shows the soft-start power-up characteristic of the PTV08040W operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 20-A constant current load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 25 ms.

### Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempt to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

### Overtemperature Protection (OTP)

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

*The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.*

### Remote Sense

Products with this feature incorporate one or two remote sense pins. Remote sensing improves the load regulation performance of the module by allowing it to compensate for any IR voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the Sense pins to the corresponding output voltage node, close to the load circuit. If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the  $V_O$  and GND pins, and that measured at the Sense pins, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

*The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.*



## Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTV08040W incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to  $V_I$  with respect to GND.

Figure 13 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up to a potential of 5 V. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

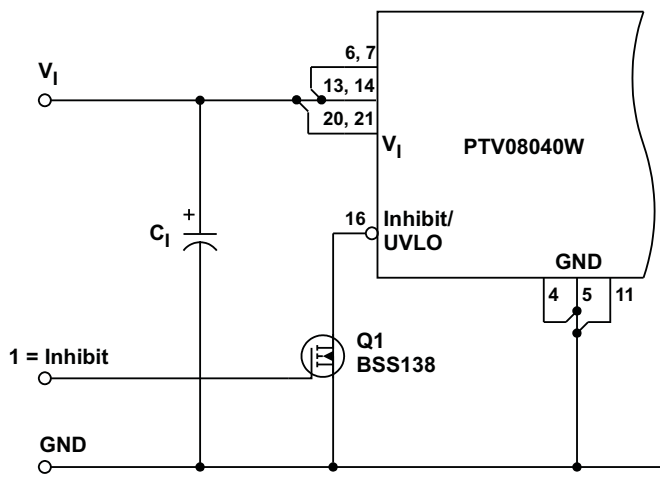


Figure 13. On/Off Inhibit Control Circuit

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 25 ms. Figure 14 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1  $V_{DS}$ . The waveforms were measured with a 20-A constant current load.

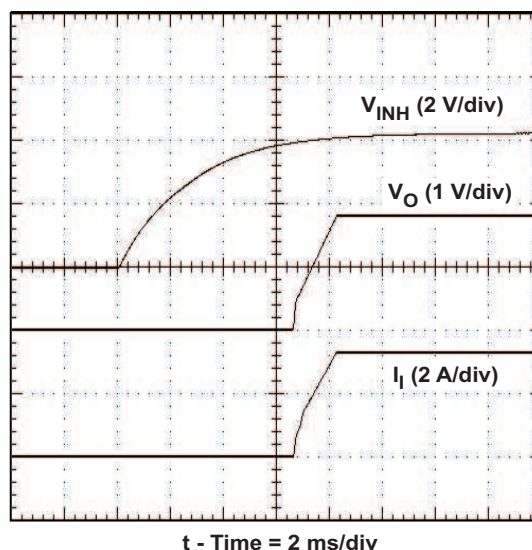


Figure 14. Power-Up Response from Inhibit Control

## Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

### How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin <sup>(1)</sup>. This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point <sup>(2)</sup>. As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit <sup>(3)</sup>. For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

### Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in [Figure 15](#).

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization <sup>(4)</sup>, enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

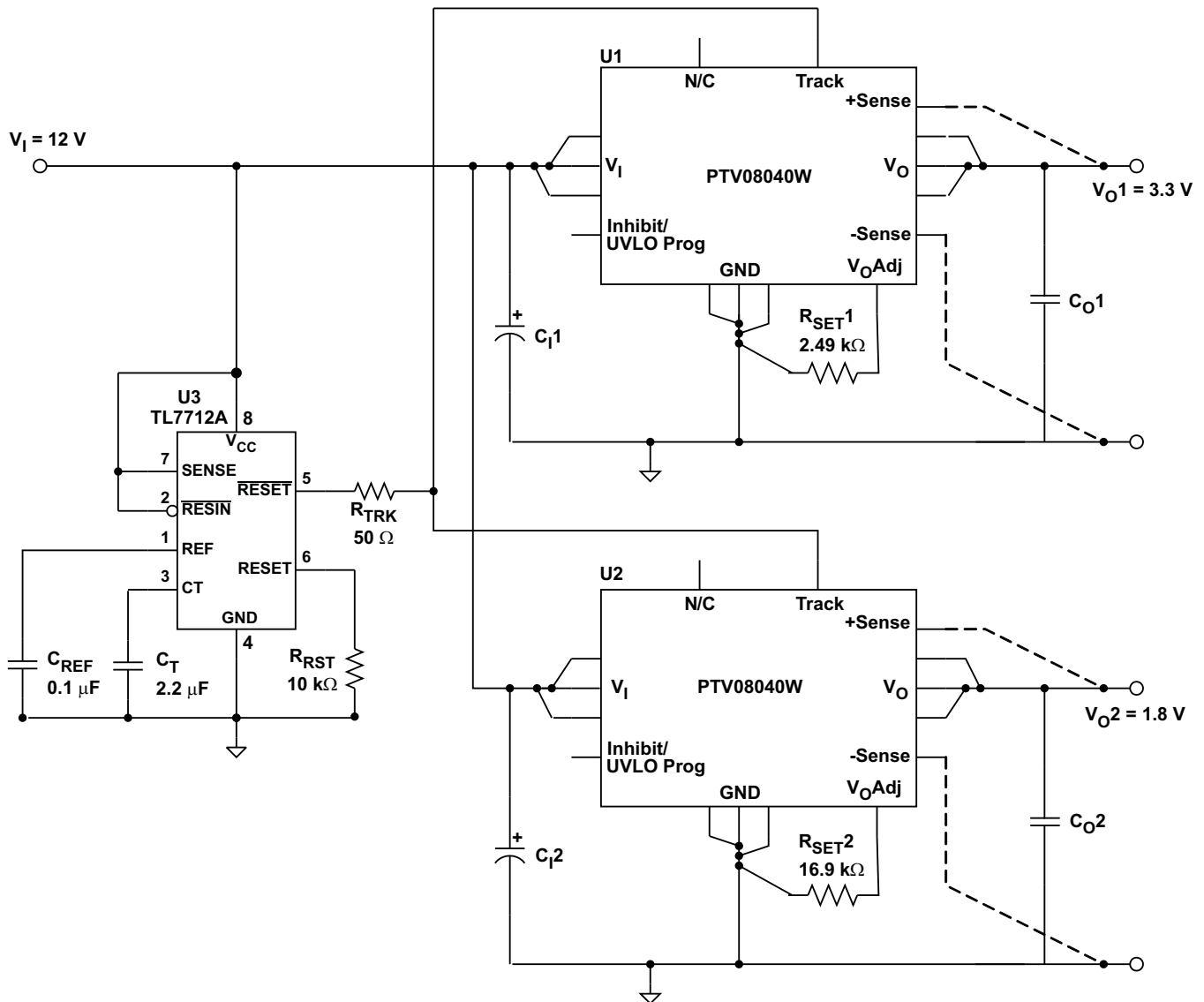
[Figure 15](#) shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of PTV08040W modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 28 ms after the input voltage has risen above U3's voltage threshold, which is 10.95 V. The 28-ms time period is controlled by the capacitor C3. The value of 2.2  $\mu$ F provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

[Figure 16](#) shows the output voltage waveforms after input voltage is applied to the circuit. The waveforms,  $V_{O1}$  and  $V_{O2}$ , represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively.  $V_{TRK}$ ,  $V_{O1}$ , and  $V_{O2}$  are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in [Figure 17](#). Power down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.

## Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage  $V_I$ .
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage ( $V_I$ ). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.



### Figure 15. Sequenced Power Up and Power Down Using Auto-Track

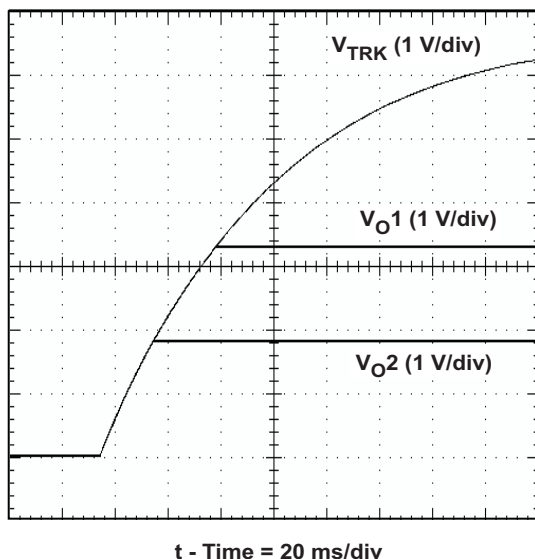


Figure 16. Simultaneous Power Up With Auto-Track Control

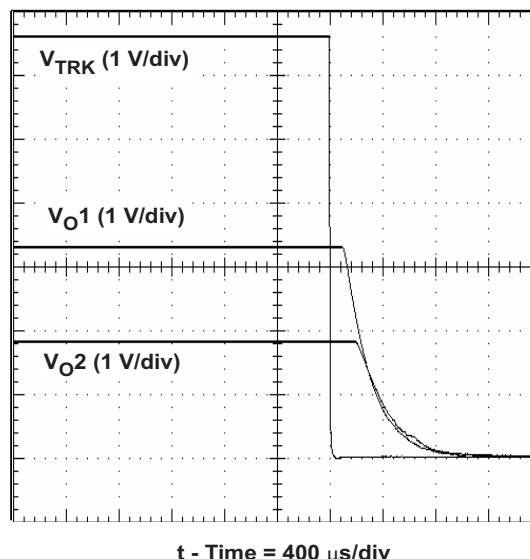


Figure 17. Simultaneous Power Down With Auto-Track Control

### Prebias Startup Capability

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. PTH modules all incorporate synchronous rectifiers. Those that incorporate the prebias feature do not sink current during startup, or whenever the Inhibit pin is held low. Start up includes an initial delay (approximately 8–15 ms), followed by the rise of the output voltage under the control of the module's internal soft-start mechanism; see [Figure 18](#).

### Conditions for PreBias Holdoff

For the module to allow an output prebias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a prebias voltage when the Inhibit pin is held low, and whenever the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled (see [Figure 18](#)). To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its Inhibit), the input voltage must always be greater than the applied prebias source. This condition must exist throughout the power-up sequence.

The soft-start period is complete when the output begins rising above the prebias voltage. Once it is complete the module functions as normal, and sinks current if a voltage higher than the nominal regulation value is applied to its output.

*Note: If a prebias condition is not present, the soft-start period is complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest.*

### Demonstration Circuit

[Figure 19](#) shows the startup waveforms for the demonstration circuit shown in [Figure 20](#). The initial rise in  $V_{O2}$  is the prebias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module ( $I_{O2}$ ) is negligible until its output voltage rises above the applied pre-bias.

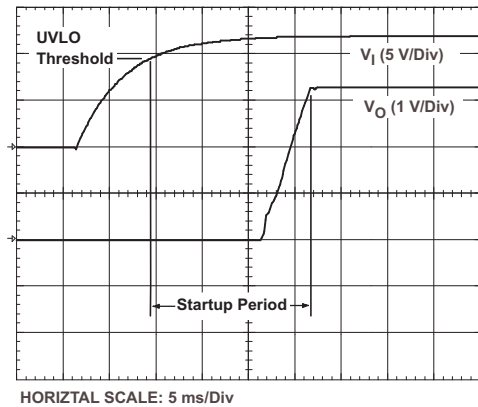


Figure 18. PTH08040W Startup

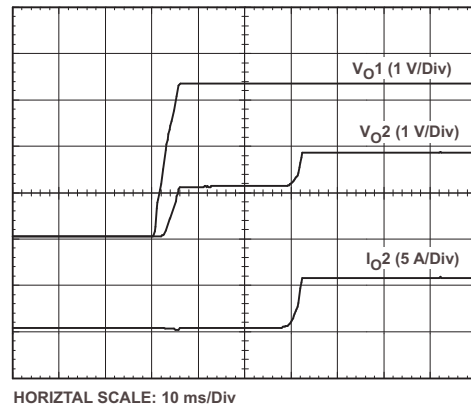


Figure 19. Prebias Startup Waveforms

**Note**

1. The prebias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the Track control pin, the output sinks current during the period that the track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the Track pin to the input voltage,  $V_I$ . This raises the Track pin voltage well above the set-point voltage prior to the module's start up, thereby defeating the Auto-Track feature.

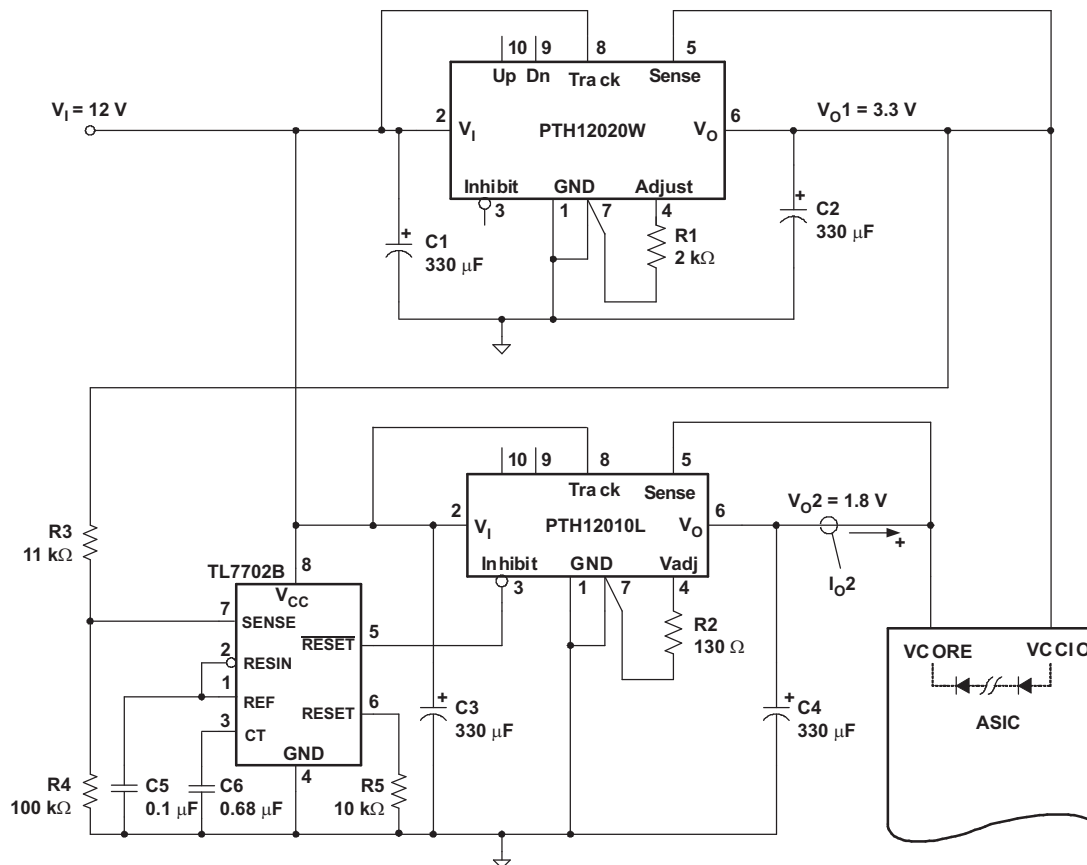


Figure 20. Application Circuit Demonstrating Prebias Startup

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">PTV08040WAD</a>	Active	Production	SIP MODULE (EAN)   21	21   TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTV08040WAD.B	Active	Production	SIP MODULE (EAN)   21	21   TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

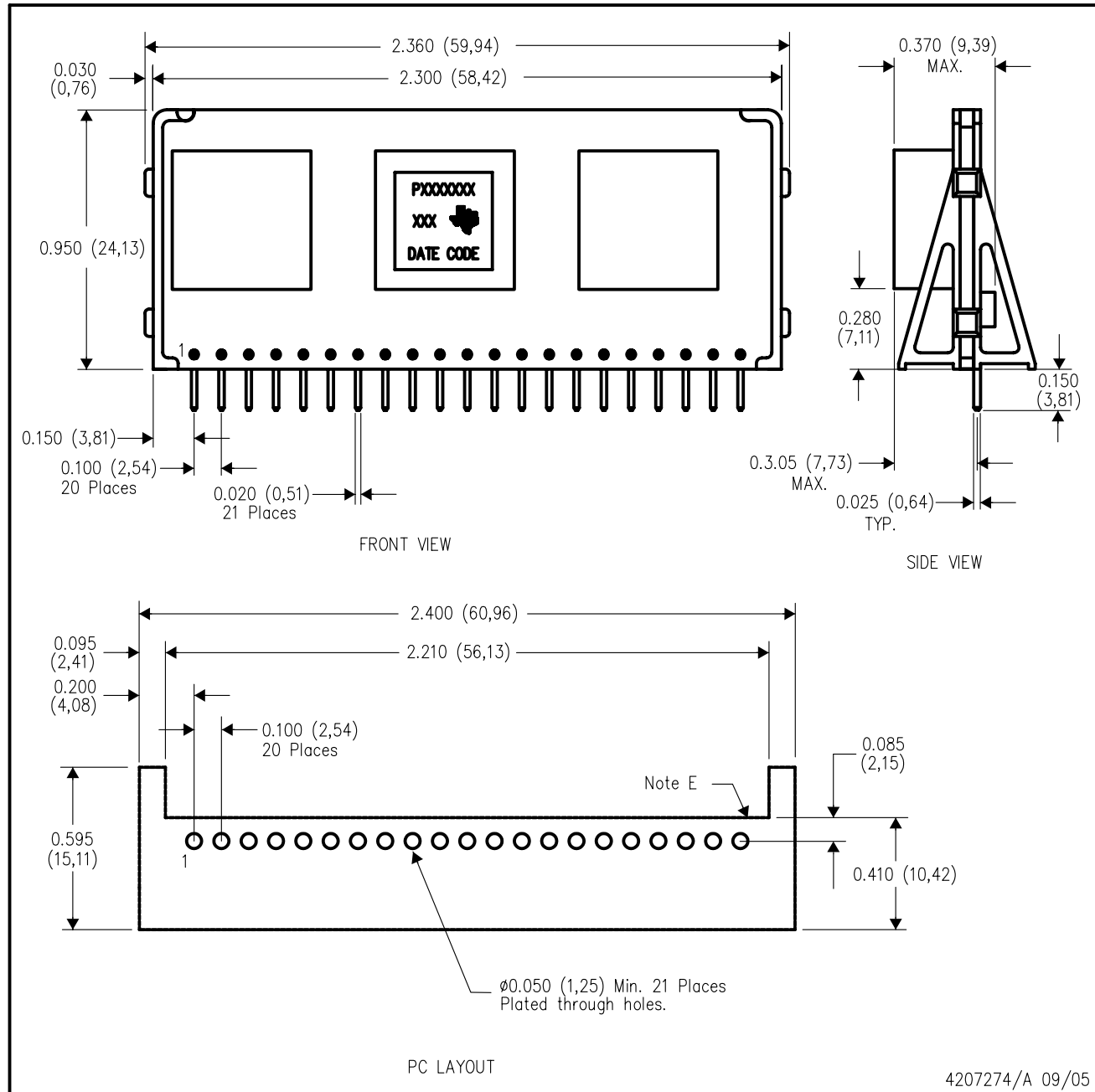
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## EAN (R-PDSS-T21)

## DOUBLE SIDED MODULE



4207274/A 09/05

- NOTES:
- A. All linear dimensions are in inches (mm).
  - B. This drawing is subject to change without notice.
  - C. 2 place decimals are  $\pm 0.030$  ( $\pm 0,76$ mm).
  - D. 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - E. Recommended keep out area for user components.
  - F. Pins are 0.020" (0,51) x 0.025" (0,64).
  - G. All pins: Material – Copper Alloy  
Finish – Tin (100%) over Nickel plate



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