PCM1840 四通道、32 位、192kHz Burr-Brown™ 音频 ADC

Texas Instruments Burr-Brown Audio

1 特性

- 多通道高性能 ADC：
  - 4 通道模拟麦克风输入或线路输入
- ADC 线路和麦克风差分输入性能：
  - 动态范围：
    - 123dB，启用动态范围增强器
    - 113dB，禁用动态范围增强器
  - THD+N：–98dB
- ADC 差分 $2V_{RMS}$ 满量程输入
- ADC 采样率 (f_S) = 8kHz 至 192kHz
- 硬件引脚控制配置
- 线性相位或低延迟滤波器可选
- 灵活的音频串行数据接口：
  - 主或从接口可选
  - 32 位、4 通道 TDM
  - 32 位、2 通道 TDM
  - 32 位、2 通道 I^2S
  - 32 位、2 通道左平衡 (LJ)
- 音频时钟丢失时自动断电
- 集成高性能音频 PLL
- 低噪声麦克风偏置 2.75V 输出
- 单电源运行：3.3V
- I/O 电源运行：3.3V 或 1.8V
- 3.3V AVDD 电源电压下的功耗：
  - 16kHz 采样率下为 17.0mW/通道
  - 48kHz 采样率下为 18.4mW/通道

2 应用

- 智能扬声器
- DVD 录像机和播放器
- AV 接收机
- 视频会议系统
- IP 网络摄像头

3 说明

PCM1840 是一款高性能 Burr-Brown™音频模数转换器 (ADC)，可支持高达四个模拟通道的同步采样。此器件支持差分线路和麦克风输入，具有 $2V_{RMS}$ 满量程信号，集成了麦克风偏置电压、锁相环 (PLL)、直流去除高通滤波器 (HPF) 等特性，并支持高达 192kHz 的采样率。该器件支持时分多路复用 (TDM)、I^2S 或左平衡 (LJ) 音频格式，且硬件引脚电平可选。此外，PCM1840 还支持主从模式选择，从而实现音频总线接口操作。这些集成的高性能 特性，以及采用 3.3V 单电源供电的功能，使该器件非常适用于远场麦克风录音 应用中成本敏感的空间受限型音频系统。

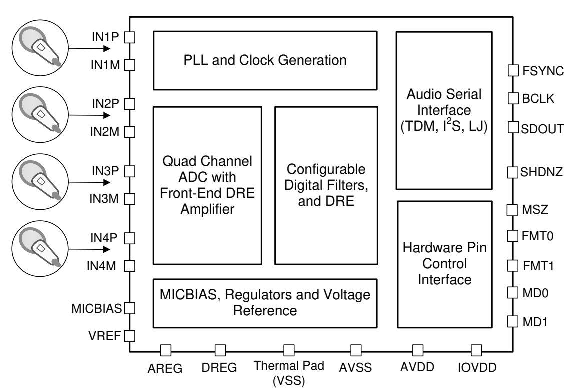
PCM1840 的额定工作温度范围为 –40°C 至 +125°C，并且采用 24 引脚 WQFN 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
PCM1840	WQFN (24)	4.00mm × 4.00mm，间距为 0.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

简化方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

4 修订历史记录

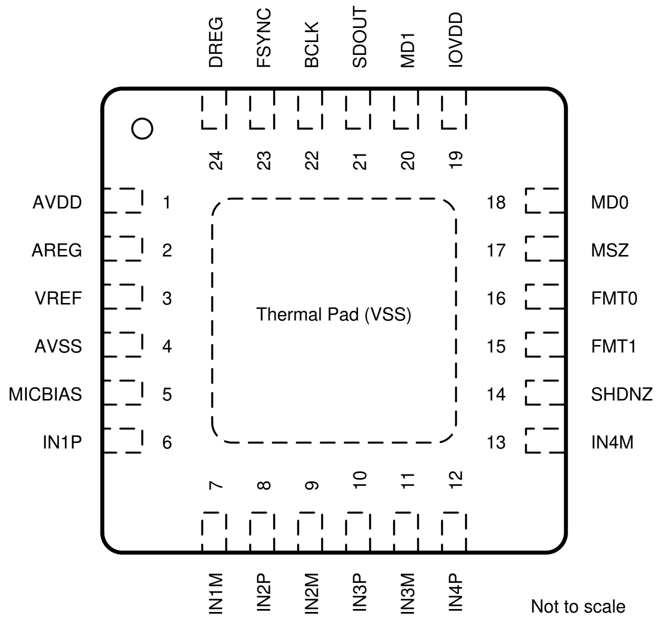
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2020 年 4 月	*	初始发行版。

Copyright © 2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

RTW Package
24-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	Analog supply	Analog power (3.3 V, nominal)
2	AREG	Analog Supply	Analog on-chip regulator output voltage for analog supply (1.8 V, nominal)
3	VREF	Analog	Analog reference voltage filter output
4	AVSS	Analog supply	Analog ground. Short this pin directly to the board ground plane.
5	MICBIAS	Analog	MICBIAS output
6	IN1P	Analog input	Analog input 1P pin
7	IN1M	Analog input	Analog input 1M pin
8	IN2P	Analog input	Analog input 2P pin
9	IN2M	Analog input	Analog input 2M pin
10	IN3P	Analog input	Analog input 3P pin
11	IN3M	Analog input	Analog input 3M pin
12	IN4P	Analog input	Analog input 4P pin
13	IN4M	Analog input	Analog input 4M pin
14	SHDNZ	Digital input	Device hardware shutdown and reset (active low)
15	FMT1	Digital input	Audio interface format select 1 pin
16	FMT0	Digital input	Audio interface format select 0 pin
17	MSZ	Digital input	Audio interface bus master or slave select pin
18	MD0	Digital input	Device configuration mode select 0 pin
19	IOVDD	Digital supply	Digital I/O power supply (1.8 V or 3.3 V, nominal)
20	MD1	Digital input	Device configuration mode select 1 pin
21	SDOUT	Digital output	Audio serial data interface bus output
22	BCLK	Digital I/O	Audio serial data interface bus bit clock
23	FSYNC	Digital I/O	Audio serial data interface bus frame synchronization signal

Copyright © 2019, Texas Instruments Incorporated

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
24	DREG	Digital supply	Digital regulator output voltage for digital core supply (1.5 V, nominal)
Thermal Pad (VSS)		Ground supply	Thermal pad shorted to internal device ground. Short thermal pad directly to board ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
	AREG to AVSS	–0.3	2.0	
	IOVDD to VSS (thermal pad)	–0.3	3.9	
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	AVDD + 0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD, AREG(1)	Analog supply voltage AVDD to AVSS (AREG is generated using onchip regulator) - AVDD 3.3-V operation	3.0	3.3	3.6	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
INPUTS					
	Analog input pins voltage to AVSS	0		AVDD	V
	Digital input pins voltage to VSS (thermal pad)	0		IOVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C
OTHERS					
	Digital input pin used as MCLK input clock frequency			36.864	MHz
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad): all ground pins must be tied together and must not differ in voltage by more than 0.2 V.

Copyright © 2019, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		PCM1840 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CONFIGURATION						
	AC input impedance	Input pins INxP or INxM		2.5		kΩ
ADC PERFORMANCE FOR LINE/MICROPHONE INPUT RECORDING : AVDD 3.3-V OPERATION						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted[1][2]	IN1 differential input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB)	115	122		dB
		IN1 differential input selected and AC signal shorted to ground, DRE disabled	106	112		
DR	Dynamic range, A-weighted[2]	IN1 differential input selected and –60-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB)		123		dB
		IN1 differential input selected and –60-dB full-scale AC signal input, DRE disabled		113		
THD+N	Total harmonic distortion[2][3]	IN1 differential input selected and –1-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB)		–98	–80	dB
		IN1 differential input selected and –1-dB full-scale AC signal input, DRE disabled		–98		
ADC OTHER PARAMETERS						
	Output data sample rate		7.35		192	kHz
	Output data sample word length				32	Bits
	Interchannel isolation	–1-dB full-scale AC-signal input to non measurement channel		–124		dB
	Interchannel gain mismatch	–6-dB full-scale AC-signal input		0.1		dB
	Gain drift	across temperature range 15°C to 35°C		–4.4		ppm/°C
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.02		Degrees
	Phase drift	1-kHz sinusoidal signal, across temperature range 15°C to 35°C		0.0005		Degrees/°C
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		102		dB
CMRR	Common-mode rejection ratio	Differential microphone input selected, 100-mV_{PP}, 1-kHz signal on both pins and measure level at output		60		dB

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) For best distortion performance, use input AC-coupling capacitors with low-voltage-coefficient.

Copyright © 2019, Texas Instruments Incorporated

Electrical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS						
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS		1.6		$µV_{RMS}$
	MICBIAS voltage			VREF		V
	MICBIAS current drive				20	mA
	MICBIAS load regulation	Measured up to max load	0.1	0.6	1.8	%
	MICBIAS over current protection threshold		30			mA
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8-V operation	–0.3		0.30 × IOVDD	V
		All digital pins, IOVDD 3.3-V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8-V operation	0.7 × IOVDD		IOVDD + 0.3	V
		All digital pins, IOVDD 3.3-V operation	2.1		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0 V	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in hardware shutdown mode	SHDNZ = 0, AVDD = 3.3 V, internal AREG		0.5		µA
I_{IOVDD}		SHDNZ = 0, all external clocks stopped, IOVDD = 3.3 V		0.1		
I_{IOVDD}		SHDNZ = 0, all external clocks stopped, IOVDD = 1.8 V		0.1		
I_{AVDD}	Current consumption with ADC 4-channel operating at f_S 16-kHz, BCLK = 256 × f_S and DRE disable	AVDD = 3.3 V, internal AREG		20.6		mA
I_{IOVDD}		IOVDD = 3.3 V		0.05		
I_{IOVDD}		IOVDD = 1.8 V		0.02		
I_{AVDD}	Current consumption with ADC 4-channel operating at f_S 48-kHz, BCLK = 256 × f_S and DRE disable	AVDD = 3.3 V, internal AREG		22.3		mA
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		
I_{AVDD}	Current consumption with ADC 4-channel operating at f_S 48-kHz, BCLK = 256 × f_S and DRE enable	AVDD = 3.3 V, internal AREG		24.4		mA
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		

 Copyright © 2019, Texas Instruments Incorporated

6.6 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 3 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		18			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		18			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time			10	ns

(1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

6.7 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 3 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT			18	ns
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT			18	ns
$f_{(BCLK)}$	BCLK output clock frequency: master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration: master mode		14			ns
$t_{L(BCLK)}$	BCLK low pulse duration: master mode		14			ns
$t_{d(FSYNC)}$	BCLK to FSYNC delay: master mode	50% of BCLK to 50% of FSYNC			18	ns
$t_{r(BCLK)}$	BCLK rise time: master mode	10% - 90% rise time			8	ns
$t_{f(BCLK)}$	BCLK fall time: master mode	90% - 10% fall time			8	ns

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

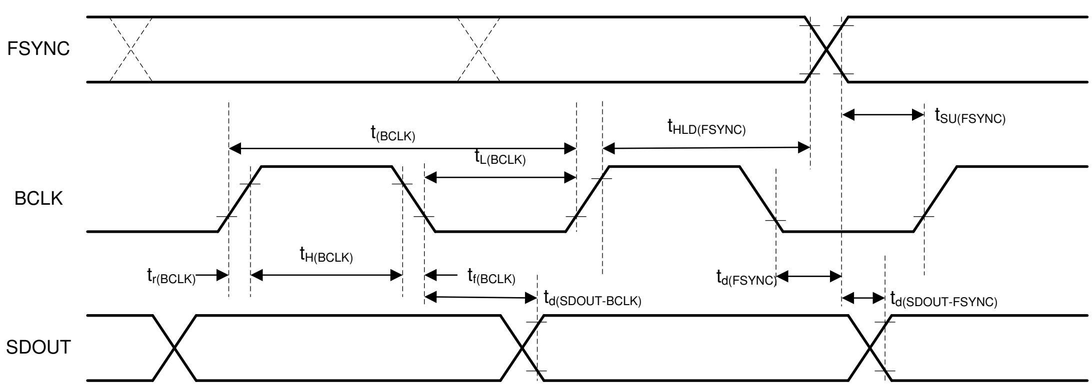
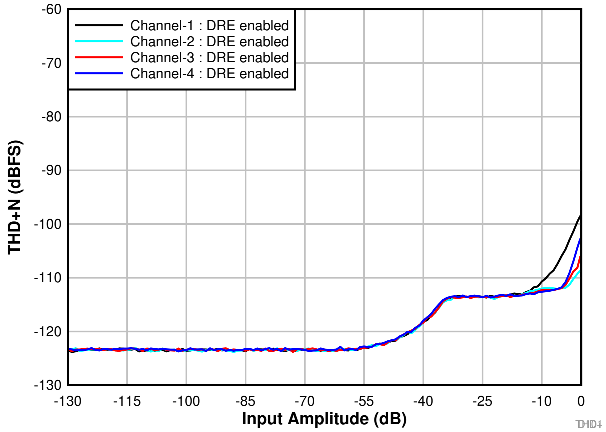


图 1. TDM, I²S, and LJ Interface Timing Diagram

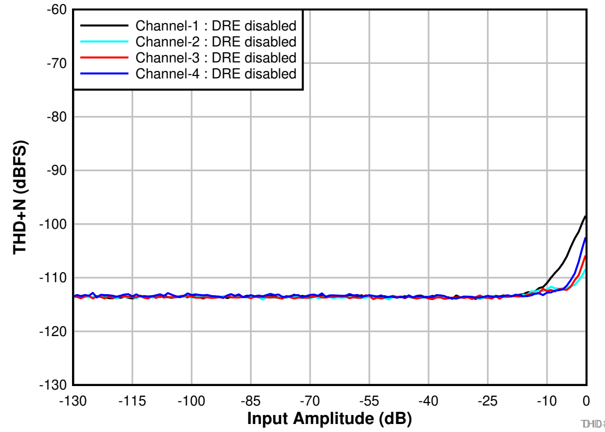
6.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter



Differential input

图 2. THD+N vs Input Amplitude With DRE Enabled



Differential input

图 3. THD+N vs Input Amplitude With DRE Disabled

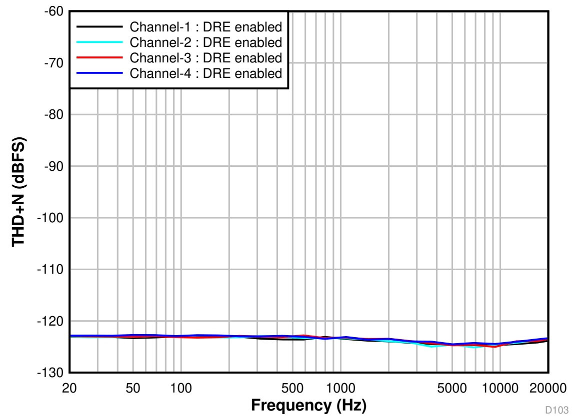


图 4. THD+N vs Input Frequency With a –60-dBr Input

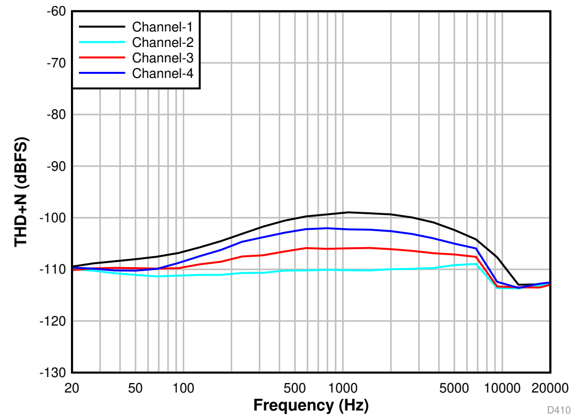


图 5. THD+N vs Input Frequency With a –1-dBr Input

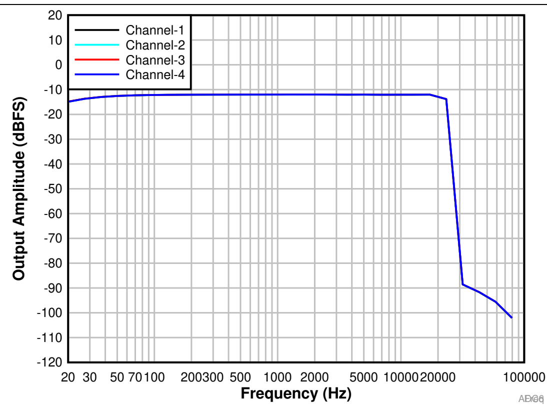


图 6. Frequency Response With a –12-dBr Input

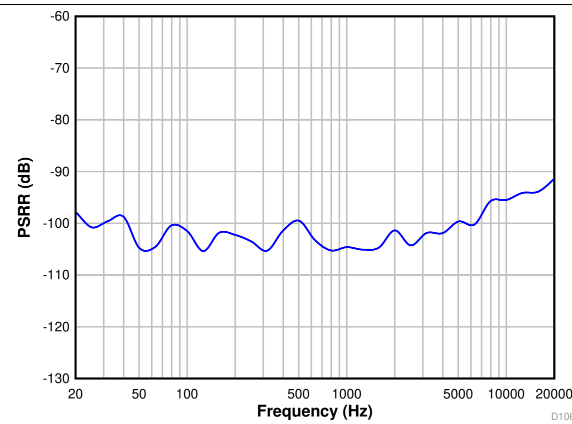


图 7. Power-Supply Rejection Ratio vs Ripple Frequency With 100-mV$_{PP}$ Amplitude

版权 © 2019, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

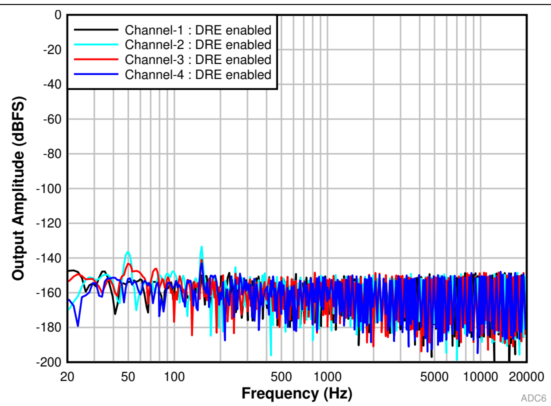


图 8. FFT With Idle Input With DRE Enabled

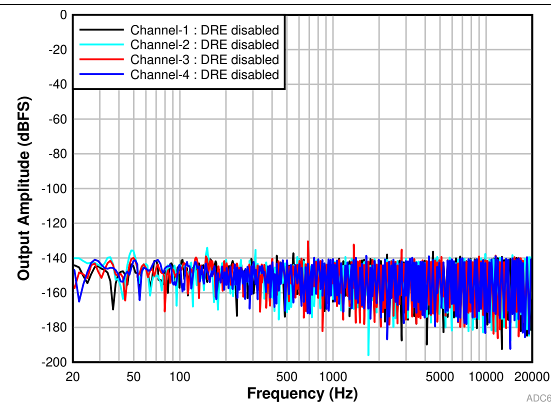


图 9. FFT With Idle Input With DRE Disabled

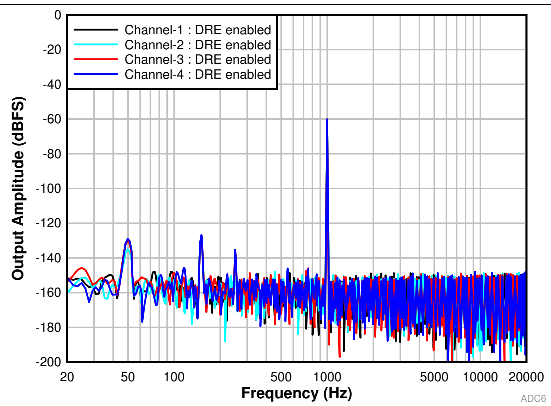


图 10. FFT With a –60-dBr Input With DRE Enabled

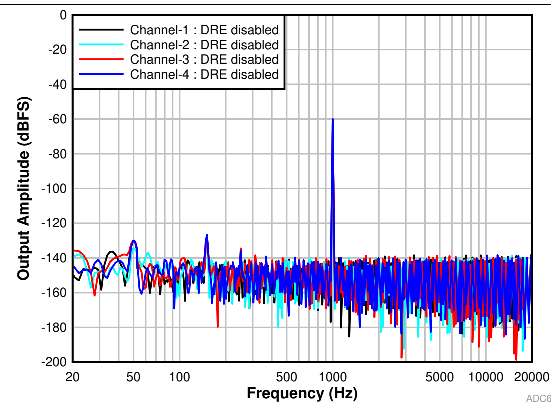


图 11. FFT With a –60-dBr Input With DRE Disabled

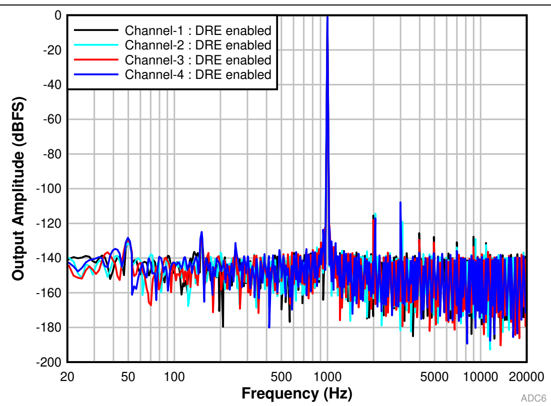


图 12. FFT With a –1-dBr Input With DRE Enabled

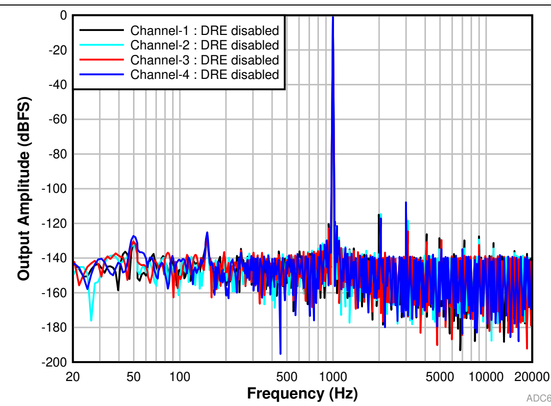


图 13. FFT With a –1-dBr Input With DRE Disabled

7 Detailed Description

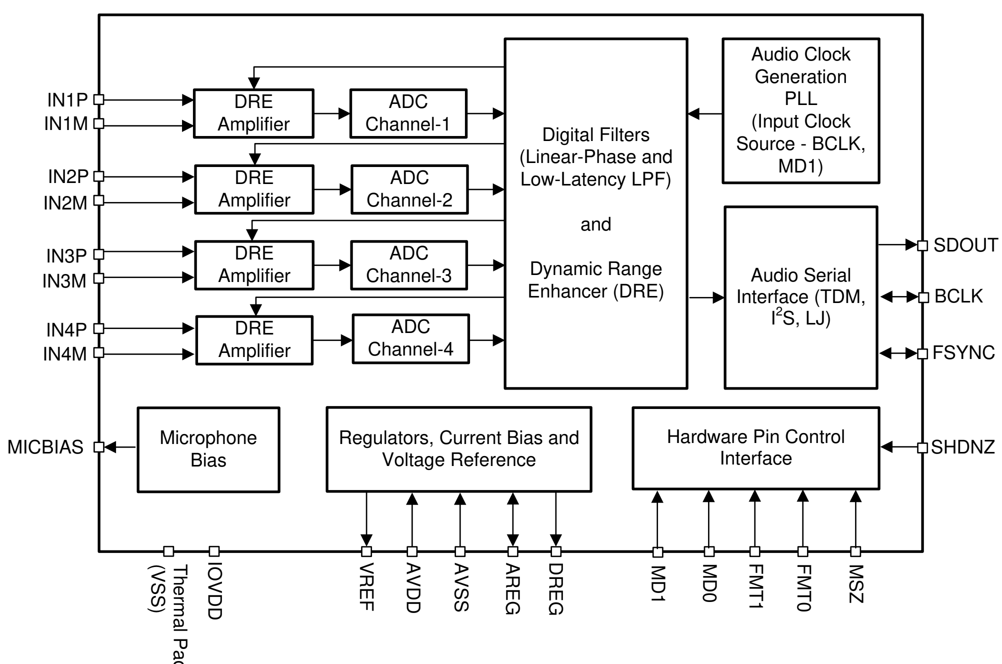
7.1 Overview

The PCM1840 is a high-performance, low-power, quad-channel, audio analog-to-digital converter (ADC) with flexible audio interface control options. This device is intended for applications in voice-activated systems, AV receivers, TV and blu-ray players, professional microphones, audio conferencing, portable computing, communication, and entertainment applications. The high dynamic range of the device enables far-field audio recording with high fidelity. This device integrates a host of features that reduces cost, board space, and power consumption in space-constrained, battery-powered, consumer, home, and industrial applications. The device features are controlled through hardware by pulling pins high or low with resistors or a controller GPIO. The PCM1808 also supports a power-down and reset function by means of halting the system clock.

The PCM1840 consists of the following blocks and features:

- Quad-channel, multibit, high-performance delta-sigma (ΔΣ) ADC
- Differential audio inputs with a 2-V_{RMS} full-scale signal
- Low-noise, 1.6-µV_{RMS}, microphone bias output
- Hardware pin control operation to select the device features
- Audio bus serial interface master or slave select option
- Audio bus serial interface format select option
- Audio bus serial interface supported up to 192 kHz sampling
- Slave mode supports dynamic range enhancer (DRE) with 123-dB dynamic range
- Slave mode supports decimation filters with linear-phase or low-latency filter selection
- Master mode operation supported using system clock of 256 × f_S or 512 × f_S
- Power-down function by means of halting the audio clocks
- Integrated high-pass filter (HPF) that removes the dc component of the input signal
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply 3.3-V operation

7.2 Functional Block Diagram



版权 © 2019, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Hardware Control

The device supports simple hardware pin controlled options to select specific mode of operation and audio interface for a given system. The MSZ, MD0, MD1, FMT0, and FMT1 pins allow the device to be controlled by either pullup or pulldown resistors as well as the GPIO from a digital device.

7.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the PCM1840 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I^2S or left-justified protocols format, and the pin-selectable master-slave configurability for bus clock lines.

The device supports audio bus master or slave mode of operation using the hardware pin MSZ. In slave mode, FSYNC and BCLK work as input pins whereas in master mode, FSYNC and BCLK work as output pins generated by the device.表 1 shows the master and slave mode selection using the MSZ pin.

表 1. Master and Slave Mode Selection

MSZ	MASTER AND SLAVE SELECTION
LOW	Slave mode of operation
HIGH	Master ode of operation

The bus protocol TDM, I^2S, or left-justified (LJ) format can be selected by using the FMT0 and FMT1 pins. As shown in 表 2, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length of 32 bits.

表 2. Audio Serial Interface Format

FMT1	FMT0	AUDIO SERIAL INTERFACE FORMAT
LOW	LOW	4-channel output with time division multiplexing (TDM) mode
LOW	HIGH	2-channel output with time division multiplexing (TDM) mode
HIGH	LOW	2-channel output with left-justified (LJ) mode
HIGH	HIGH	2-channel output with inter IC sound (I^2S) mode

7.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. 图 14 to 图 17 illustrate the protocol timing for TDM operation with various configurations.

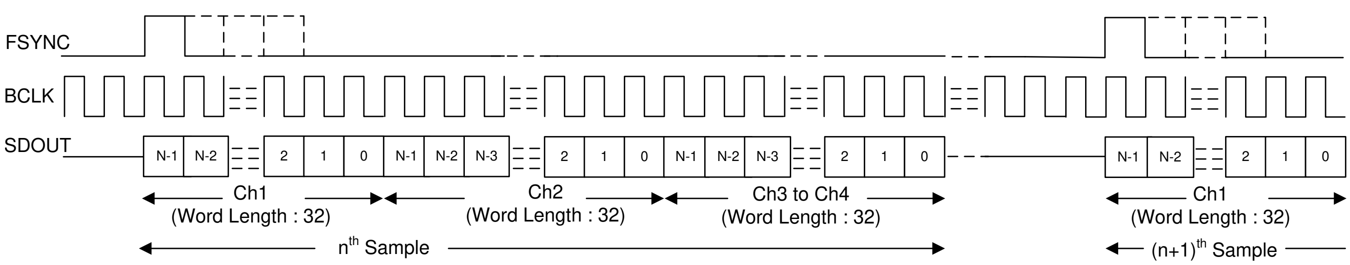


图 14. TDM Mode Protocol Timing (FMT0 = LOW) In Slave Mode

版权 © 2019, Texas Instruments Incorporated

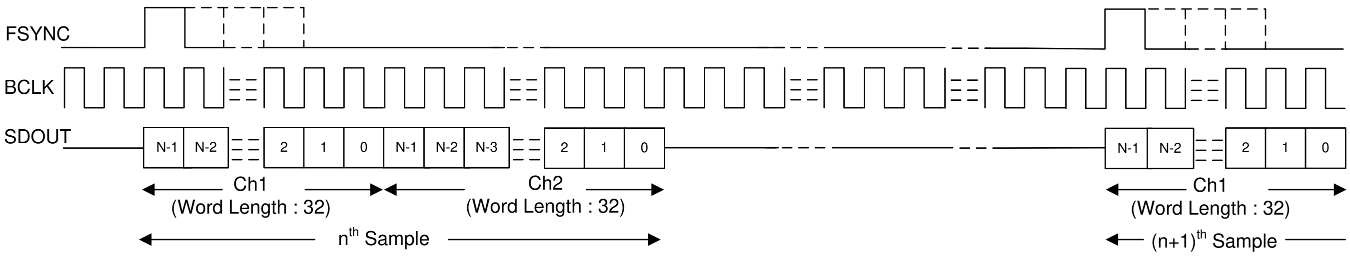


图 15. TDM Mode Protocol Timing (FMT0 = HIGH) In Slave Mode

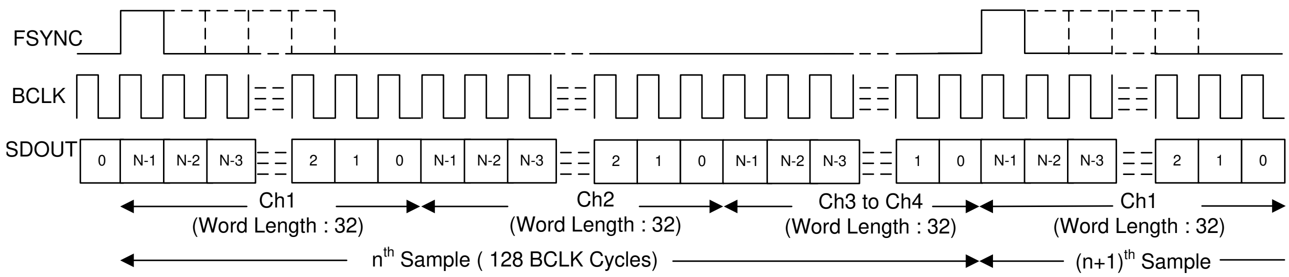


图 16. TDM Mode Protocol Timing (FMT0 = LOW) In Master Mode

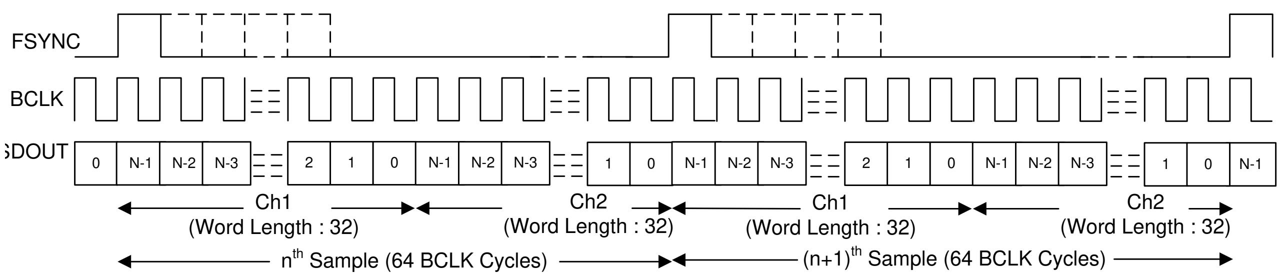


图 17. TDM Mode Protocol Timing (FMT0 = HIGH) In Master Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the 32-bits word length of the output channel data. The device transmits a zero data value on SDOUT for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

7.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In master mode, FSYNC is transmitted on the rising edge of BCLK. 图 18 and 图 19 illustrate the protocol timing for I^2S operation in slave and master mode of operation.

版权 © 2019, Texas Instruments Incorporated

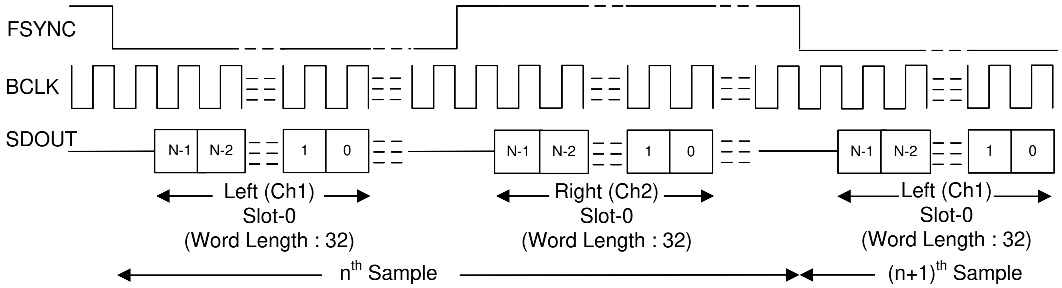


图 18. I²S Mode Protocol Timing in Slave Mode

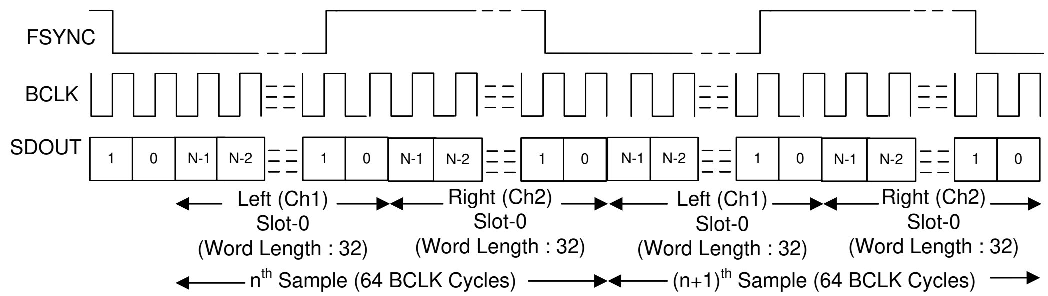


图 19. I²S Protocol Timing In Master Mode

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the 32-bits word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the 32-bits data word length. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the 32-bits data word length. The device transmit zero data value on SDOUT for the extra unused bit clock cycles.

7.3.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In master mode, FSYNC is transmitted on the rising edge of BCLK. 图 20 and 图 21 illustrate the protocol timing for LJ operation in slave and master mode of operation.

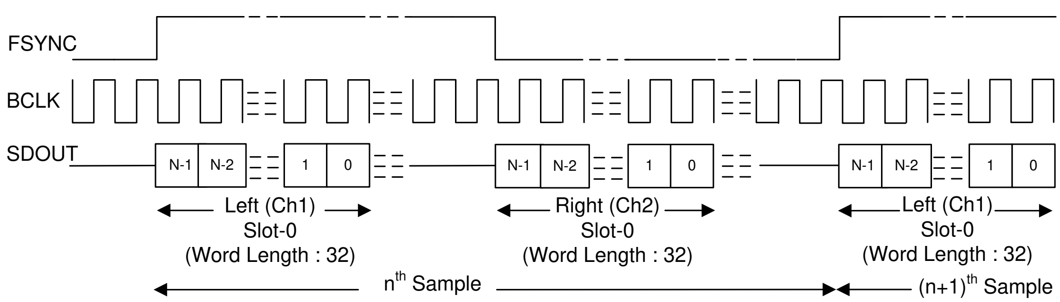


图 20. LJ Mode Protocol Timing In Slave Mode

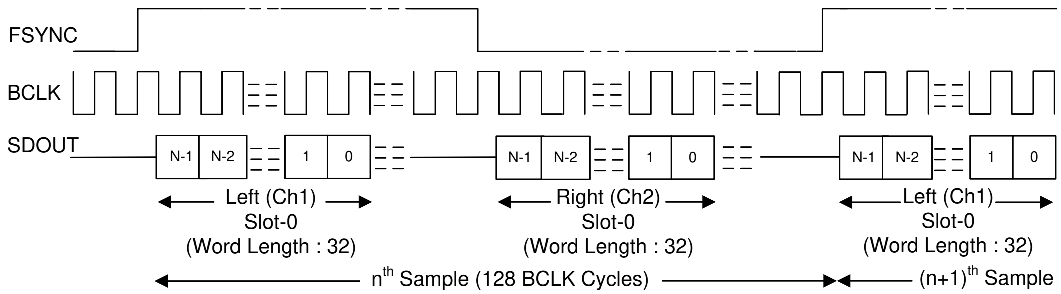


图 21. LJ Mode Protocol Timing In Master Mode

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the 32-bits word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the 32-bits data word length. Similarly, the FSYNC low pulse must be number of BCLK cycles wide that is greater than or equal to the number of active right slots times the 32-bits data word length. The device transmit zero data value on SDOUT for the extra unused bit clock cycles.

版权 © 2019, Texas Instruments Incorporated

7.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulator and digital filter engine, as well as other control blocks.

In slave mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. 表 3 and 表 4 list the supported FSYNC and BCLK frequencies.

表 3. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	Reserved	0.256	0.384	0.512	0.768	1.536	3.072
24	Reserved	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	Reserved
256	2.048	4.096	6.144	8.192	12.288	24.576	Reserved
384	3.072	6.144	9.216	12.288	18.432	Reserved	Reserved
512	4.096	8.192	12.288	16.384	24.576	Reserved	Reserved

表 4. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	Reserved	Reserved	0.3528	0.4704	0.7056	1.4112	2.8224
24	Reserved	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	Reserved	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	Reserved
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	Reserved
384	2.8224	5.6448	8.4672	11.2896	16.9344	Reserved	Reserved
512	3.7632	7.5264	11.2896	15.0528	22.5792	Reserved	Reserved

In the master mode of operation, the device uses the MD1 pin (as system clock, MCLK) as the reference input clock source with supported system clock frequency option of either 256 × f_S or 512 × f_S as configured using the MD0 pin. 表 5 shows the system clock selection for the master mode using the MD0 pin.

表 5. System Clock Selection for the Master Mode

MD0	SYSTEM CLOCK SELECTION (Valid for Master Mode Only)
LOW	System clock with frequency 256 × f_S connected to pin MD1 as MCLK
HIGH	System clock with frequency 512 × f_S connected to pin MD1 as MCLK

版权 © 2019, Texas Instruments Incorporated

See 表 7 and 表 20 for the MD0 and MD1 pin function in the slave mode of operation.

7.3.4 Input Channel Configurations

The device consists of four pairs of analog input pins (INxP and INxM) as differential inputs for the recording channel. The device supports simultaneous recording of up to four channels using the high-performance multichannel ADC. The input source for the analog pins can be from electret condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs must be capacitively coupled (AC-coupled) to the device and for best distortion performance, use the low-voltage coefficient capacitors for AC coupling. The device has the typical input impedance on INxP or INxM as 2.5 kΩ on each pins. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has quick charge scheme to speed up the charging of the coupling capacitor at power-up. The default value of the quick-charge timing is set for a coupling capacitor up to 1 µF.

7.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The PCM1840 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to analog ground (AVSS). The value of this reference voltage, VREF, is set to 2.75 V, which in turn supports a 2-V_{RMS} differential full-scale input to the device. The required minimum AVDD voltage for this VREF voltage is 3 V. Do not connect any external load to a VREF pin.

7.3.6 Microphone Bias

The device integrates a built-in, low-noise, 1.6-µV_{RMS} microphone bias pin with an output voltage of 2.75 V that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The integrated bias amplifier supports up to 20 mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR, and low noise bias voltages to bias microphone for high-end audio applications. When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones.

版权 © 2019, Texas Instruments Incorporated

7.3.7 Signal-Chain Processing

The PCM1840 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the PCM1840 optimized for a variety of end-equipments and applications that require multichannel audio capture. 图 22 shows a conceptual block diagram that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain.

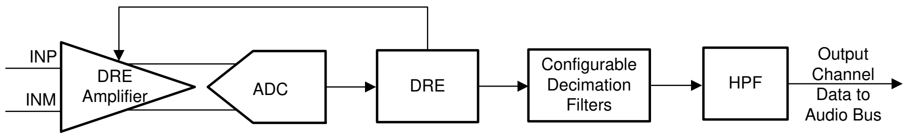


图 22. Signal-Chain Processing Flowchart

The front-end dynamic range enhancer (DRE) gain amplifier is very low noise, with a 123-dB dynamic range performance. Along with a low-noise and low-distortion, multibit, delta-sigma ADC, the front-end DRE gain amplifier enables the PCM1840 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device supports an input signal bandwidth up to 80 kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4-kHz (or higher) sample rate.

7.3.7.1 Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a fixed high-pass filter (HPF) with –3-dB cut-off frequency of 0.00025 × f_S. The HPF is not a channel-independent filter but is globally applicable for all the ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. 表 6 shows the fixed –3-dB cutoff frequency value. 图 23 shows a frequency response plot for the HPF filter.

表 6. HPF Cutoff Frequency Value

-3-dB CUTOFF FREQUENCY VALUE	-3-dB CUTTOFF FREQUENCY AT 16 kHz SAMPLE RATE	-3-dB CUTTOFF FREQUENCY AT 48 kHz SAMPLE RATE
0.00025 × f_S	4 Hz	12 Hz

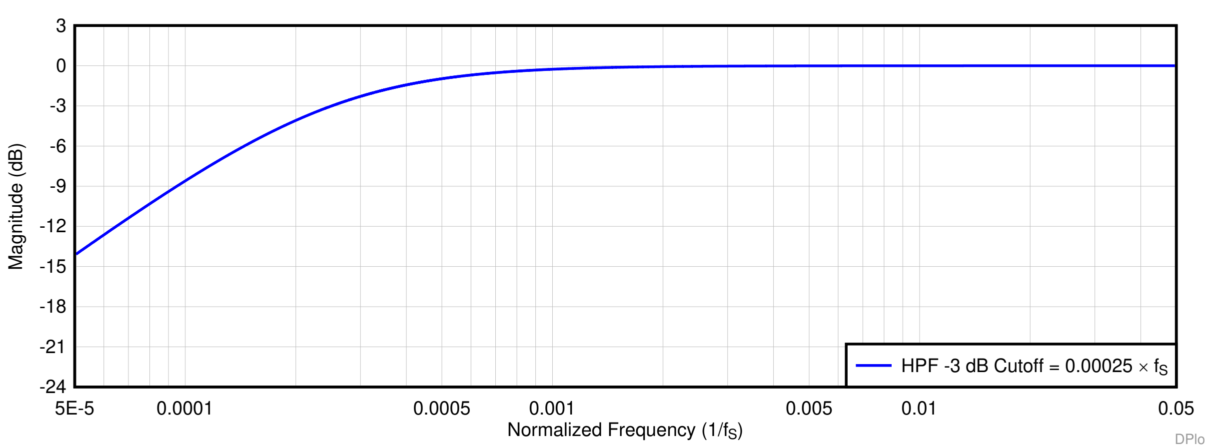


图 23. HPF Filter Frequency Response Plot

7.3.7.2 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filter can be chosen from two different types only in slave mode, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by the MD0 pin. 表 7 shows the decimation filter mode selection for the record channel.

表 7. Decimation Filter Mode Selection for the Record Channel

MD0	DECIMATION FILTER MODE SELECTION (Supported Only in Slave Mode)
LOW	Linear phase filters are used for the decimation in slave mode. For master mode, the device always use linear phase filters for the decimation.
HIGH	Low latency filters are used for the decimation in slave mode. For master mode, the device always use linear phase filters for the decimation.

7.3.7.2.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

7.3.7.2.1.1 Sampling Rate: 8 kHz or 7.35 kHz

图 24 and 图 25 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 8 kHz or 7.35 kHz. 表 8 lists the specifications for a decimation filter with an 8-kHz or 7.35-kHz sampling rate.

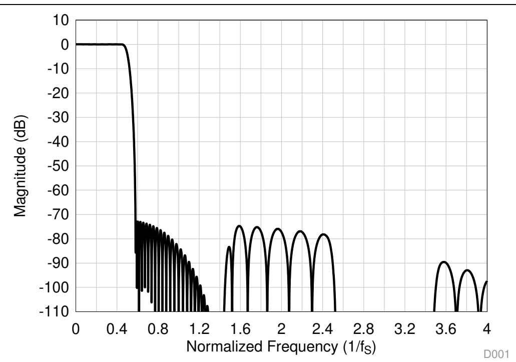


图 24. Linear Phase Decimation Filter Magnitude Response

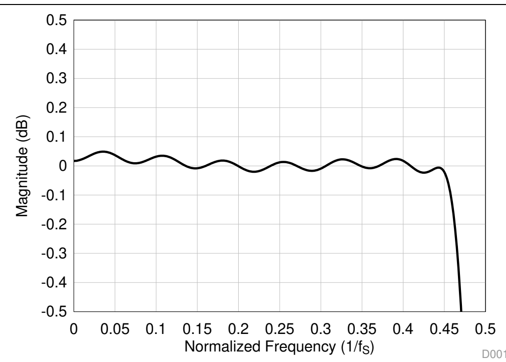


图 25. Linear Phase Decimation Filter Pass-Band Ripple

表 8. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	72.7			dB
	Frequency range is 4 × f_S onwards	81.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

版权 © 2019, Texas Instruments Incorporated

7.3.7.2.1.2 Sampling Rate: 16 kHz or 14.7 kHz

图 26 and 图 27 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. 表 9 lists the specifications for a decimation filter with an 16-kHz or 14.7-kHz sampling rate.

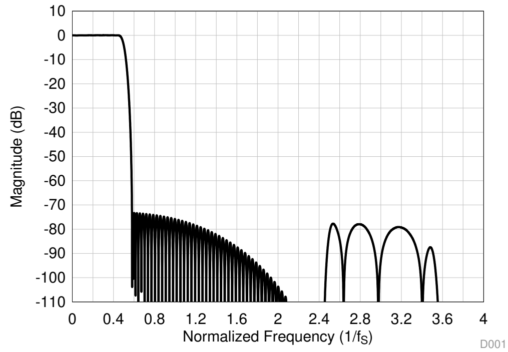


图 26. Linear Phase Decimation Filter Magnitude Response

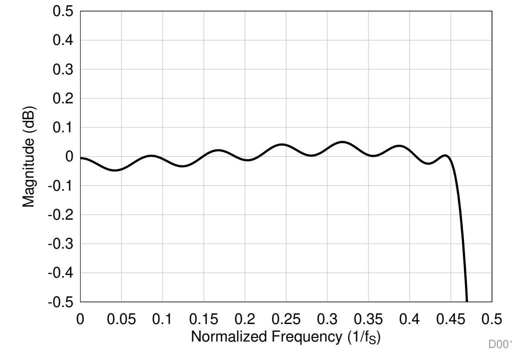


图 27. Linear Phase Decimation Filter Pass-Band Ripple

表 9. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.3			dB
	Frequency range is 4 × f_S onwards	95.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		15.7		$1/f_S$

7.3.7.2.1.3 Sampling Rate: 24 kHz or 22.05 kHz

图 28 and 图 29 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. 表 10 lists the specifications for a decimation filter with an 24-kHz or 22.05-kHz sampling rate.

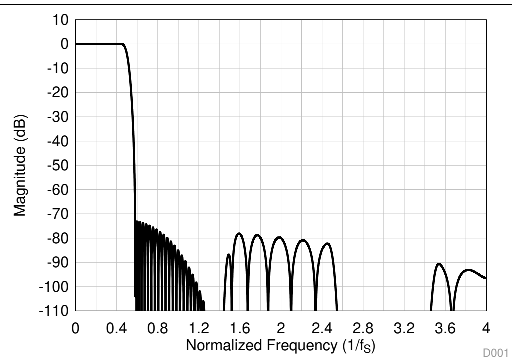


图 28. Linear Phase Decimation Filter Magnitude Response

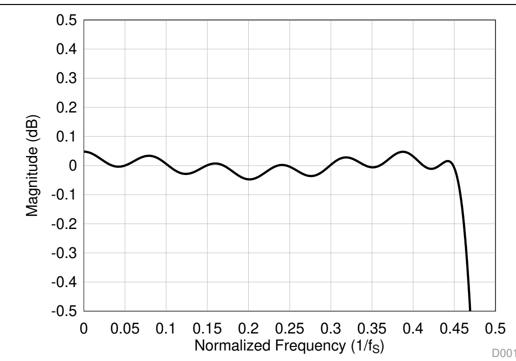


图 29. Linear Phase Decimation Filter Pass-Band Ripple

表 10. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.0			dB
	Frequency range is 4 × f_S onwards	96.4			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.6		$1/f_S$

版权 © 2019, Texas Instruments Incorporated

7.3.7.2.1.4 Sampling Rate: 32 kHz or 29.4 kHz

图 30 and 图 31 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. 表 11 lists the specifications for a decimation filter with an 32-kHz or 29.4-kHz sampling rate.

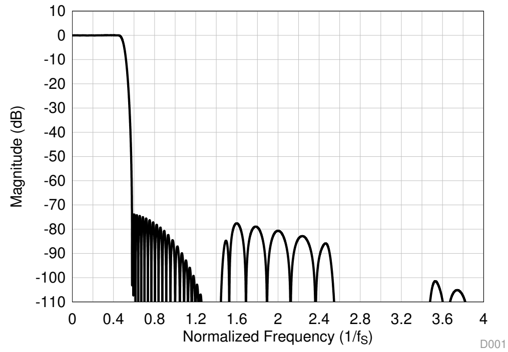


图 30. Linear Phase Decimation Filter Magnitude Response

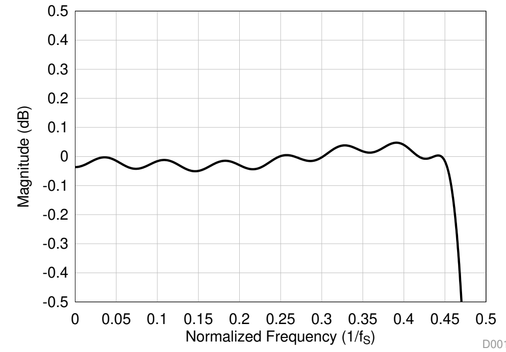


图 31. Linear Phase Decimation Filter Pass-Band Ripple

表 11. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.7			dB
	Frequency range is 4 × f_S onwards	107.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		$1/f_S$

7.3.7.2.1.5 Sampling Rate: 48 kHz or 44.1 kHz

图 32 and 图 33 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. 表 12 lists the specifications for a decimation filter with an 48-kHz or 44.1-kHz sampling rate.

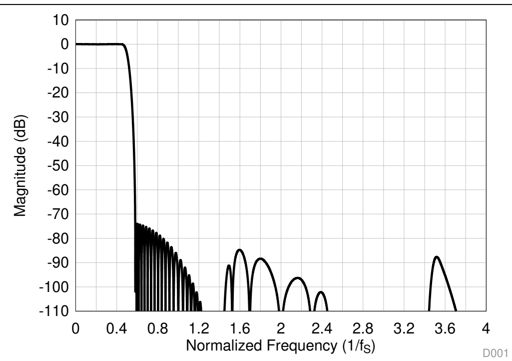


图 32. Linear Phase Decimation Filter Magnitude Response

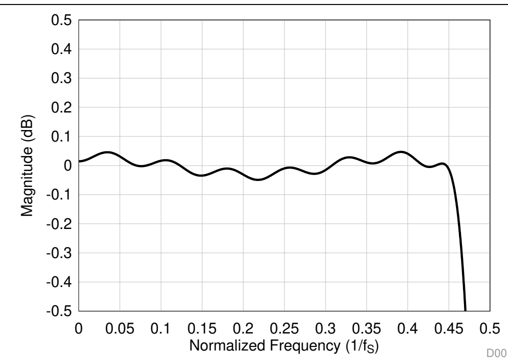


图 33. Linear Phase Decimation Filter Pass-Band Ripple

表 12. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.8			dB
	Frequency range is 4 × f_S onwards	98.1			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

版权 © 2019, Texas Instruments Incorporated

7.3.7.2.1.6 Sampling Rate: 96 kHz or 88.2 kHz

图 34 and 图 35 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. 表 13 lists the specifications for a decimation filter with an 96-kHz or 88.2-kHz sampling rate.

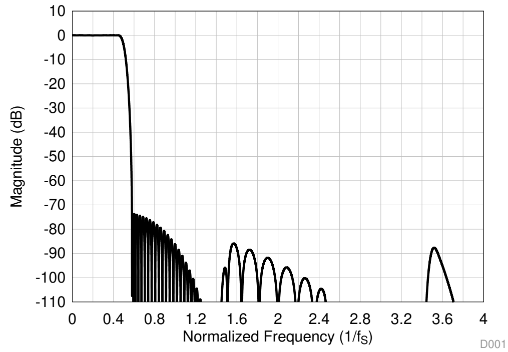


图 34. Linear Phase Decimation Filter Magnitude Response

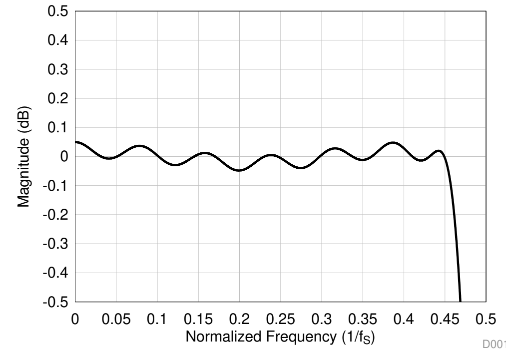


图 35. Linear Phase Decimation Filter Pass-Band Ripple

表 13. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.6			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		$1/f_S$

7.3.7.2.1.7 Sampling Rate: 192 kHz or 176.4 kHz

图 36 and 图 37 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 192 kHz or 176.4 kHz. 表 14 lists the specifications for a decimation filter with an 192-kHz or 176.4-kHz sampling rate.

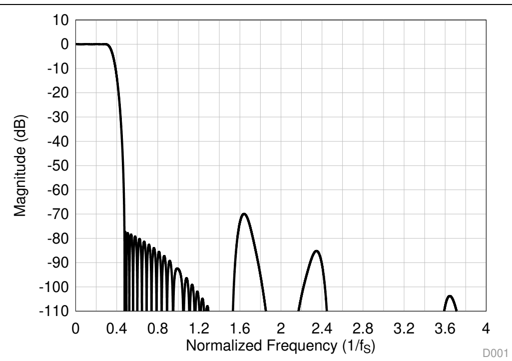


图 36. Linear Phase Decimation Filter Magnitude Response

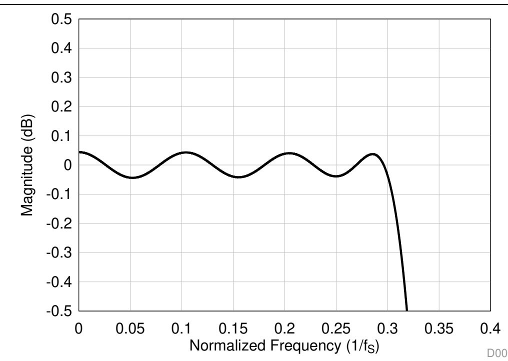


图 37. Linear Phase Decimation Filter Pass-Band Ripple

表 14. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.3 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.473 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	111.0			
Group delay or latency	Frequency range is 0 to 0.3 × f_S		11.9		$1/f_S$

7.3.7.2.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the PCM1840 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.365 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

7.3.7.2.2.1 Sampling Rate: 16 kHz or 14.7 kHz

图 38 shows the magnitude response and 图 39 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. 表 15 lists the specifications for a decimation filter with a 16-kHz or 14.7-kHz sampling rate.

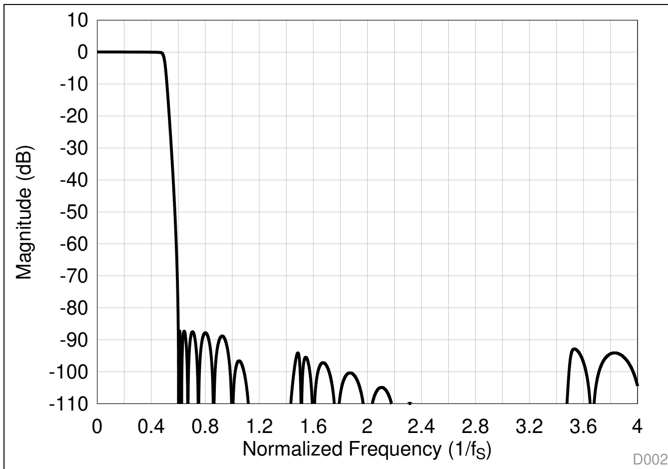


图 38. Low-Latency Decimation Filter Magnitude Response

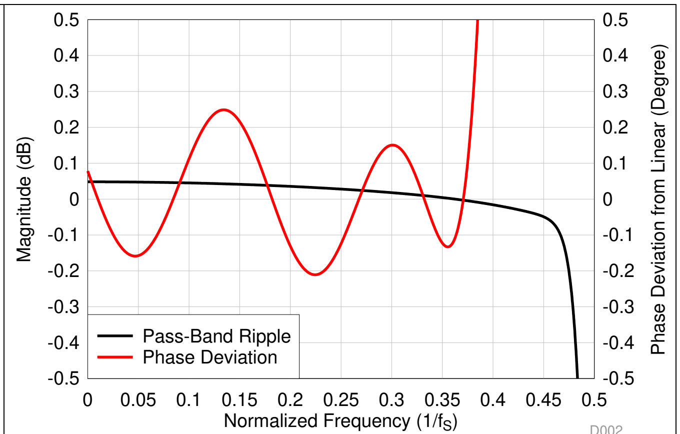


图 39. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 15. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.451 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.61 × f_S onwards	87.3			dB
Group delay or latency	Frequency range is 0 to 0.363 × f_S		7.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.363 × f_S	–0.022		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.363 × f_S	–0.21		0.25	Degrees

版权 © 2019, Texas Instruments Incorporated

7.3.7.2.2.2 Sampling Rate: 24 kHz or 22.05 kHz

图 40 shows the magnitude response and 图 41 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. 表 16 lists the specifications for a decimation filter with a 24-kHz or 22.05-kHz sampling rate.

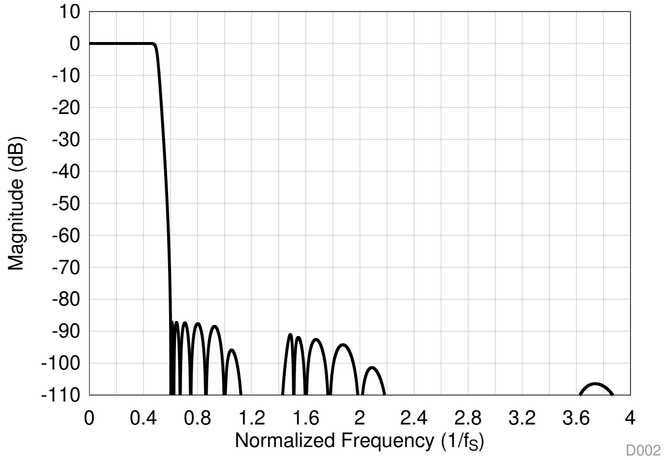


图 40. Low-Latency Decimation Filter Magnitude Response

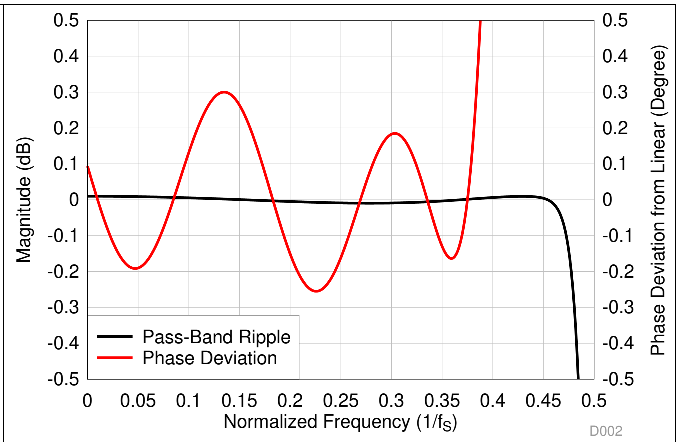


图 41. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 16. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.459 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.5		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

7.3.7.2.2.3 Sampling Rate: 32 kHz or 29.4 kHz

图 42 shows the magnitude response and 图 43 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. 表 17 lists the specifications for a decimation filter with a 32-kHz or 29.4-kHz sampling rate.

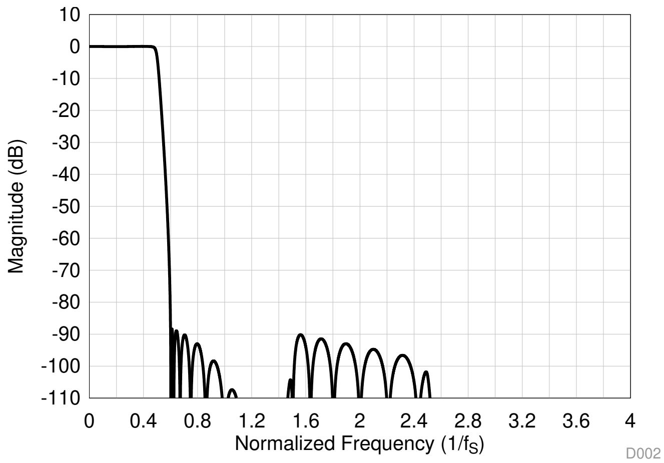


图 42. Low-Latency Decimation Filter Magnitude Response

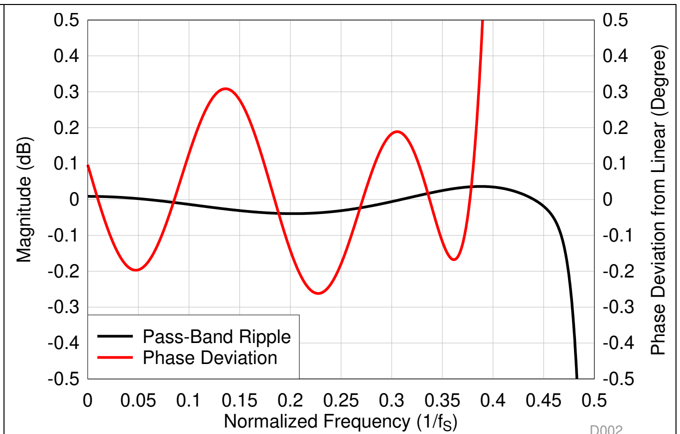


图 43. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

版权 © 2019, Texas Instruments Incorporated

表 17. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.368 × f_S		8.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.368 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.368 × f_S	–0.26		0.31	Degrees

7.3.7.2.2.4 Sampling Rate: 48 kHz or 44.1 kHz

图 44 shows the magnitude response and 图 45 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. 表 18 lists the specifications for a decimation filter with a 48-kHz or 44.1-kHz sampling rate.

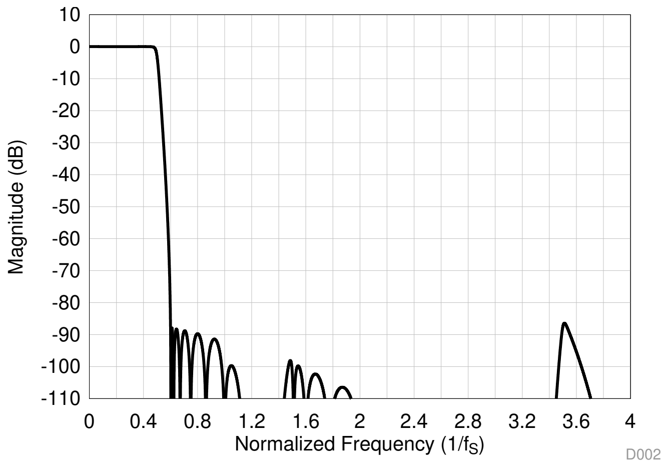


图 44. Low-Latency Decimation Filter Magnitude Response

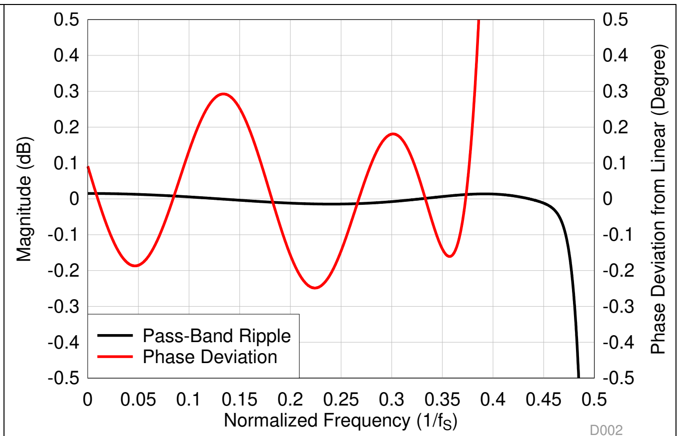


图 45. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 18. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.25		0.30	Degrees

版权 © 2019, Texas Instruments Incorporated

7.3.7.2.2.5 Sampling Rate: 96 kHz or 88.2 kHz

图 46 shows the magnitude response and 图 47 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. 表 19 lists the specifications for a decimation filter with a 96-kHz or 88.2-kHz sampling rate.

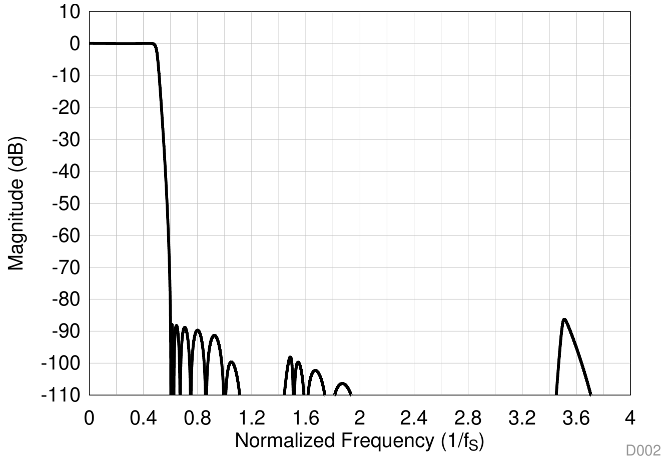


图 46. Low-Latency Decimation Filter Magnitude Response

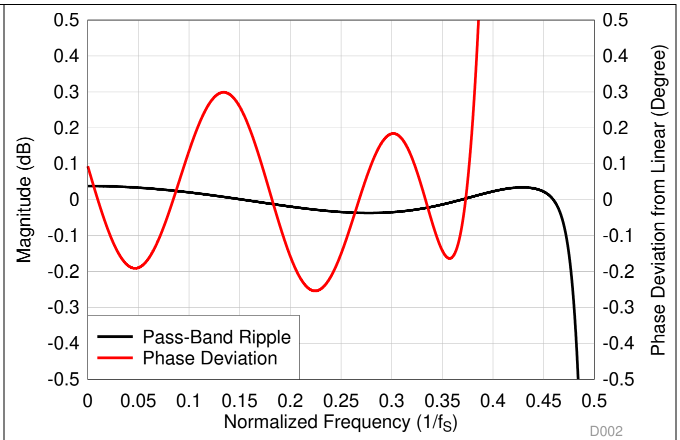


图 47. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 19. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

7.3.8 Dynamic Range Enhancer (DRE)

The device integrates an ultra-low noise front-end DRE gain amplifier with 123-dB dynamic range performance with a low-noise, low-distortion, multibit delta-sigma (ΔΣ) ADC with a 108-dB dynamic range. The dynamic range enhancer (DRE) is a digitally assisted algorithm to boost the overall channel performance. The DRE monitors the incoming signal amplitude and accordingly adjusts the internal DRE amplifier gain automatically. The DRE achieves a complete-channel dynamic range as high as 123 dB. At a system level, the DRE scheme enables far-field, high-fidelity recording of audio signals in very quiet environments and low-distortion recording in loud environments.

The DRE can be enable only in slave mode by driving high to the MD1 pin. 表 20 shows the DRE selection for the record channel.

表 20. DRE Selection for the Record Channel

MD1	DRE SELECTION (Supported Only in Slave Mode)
LOW	DRE is disabled in slave mode. For master mode, DRE is always disabled.
HIGH	DRE is enabled with DRE_LVL = –36 dB and DRE_MAXGAIN = 24 dB in slave mode. For master mode, DRE is always disabled.

This algorithm is implemented with very low latency and all signal chain blocks are designed to minimize any audible artifacts that may occur resulting from dynamic gain modulation. The target signal threshold level, DRE_LVL, at which DRE is triggered is fixed to the –36-dB input signal level. The DRE gain range can be dynamically modulated by using DRE_MAXGAIN, which is fixed to 24 dB to maximize the benefit of the DRE in real-world applications and to minimize any audible artifacts.

Enabling the DRE for processing increases the power consumption of the device because of increased signal processing. Therefore, disable the DRE for low-power critical applications. Furthermore, the DRE is not supported for output sample rates greater than 48 kHz.

7.4 Device Functional Modes

7.4.1 Hardware Shutdown

The device enters hardware shutdown mode when the SHDNZ pin is asserted low or the AVDD supply voltage is not applied to the device. In hardware shutdown mode, the device consumes the minimum quiescent current from the AVDD supply. If the SHDNZ pin is asserted low when the device is in active mode, the device ramps down volume on the record data, powers down the analog and digital blocks, and puts the device into hardware shutdown mode in 25 ms (typical).

7.4.2 Active Mode

In the hardware shutdown state, when the SHDNZ pin goes high, the device starts the internal boot-up sequence and then enters into active mode in less than 20 ms (typical). Assert the SHDNZ pin high only when the IOVDD supply settles to a steady voltage level and all hardware control pins (MSZ, MD0, MD1, FMT0, and FMT1) are driven to the voltage level for the device desired mode of operation.

In active mode, when the audio clocks are available, the device powers up all the ADC channels and starts transmitting the data over the audio serial interface. If the clocks are stopped then the device auto powers down the ADC channels.

版权 © 2019, Texas Instruments Incorporated

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PCM1840 is a multichannel, high-performance audio analog-to-digital converter (ADC) that supports output sample rates of up to 192 kHz. The device supports up to four analog microphones for simultaneous recording applications.

The PCM1840 configuration is supported using various hardware pin control options. The device supports a highly flexible, audio serial interface (TDM, I²S, and LJ) to transmit audio data seamlessly in the system across devices.

8.2 Typical Application

图 48 shows a typical configuration of the PCM1840 for an application using four analog microelectrical-mechanical system (MEMS) microphones for simultaneous recording operation with a time-division multiplexing (TDM) audio data slave interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

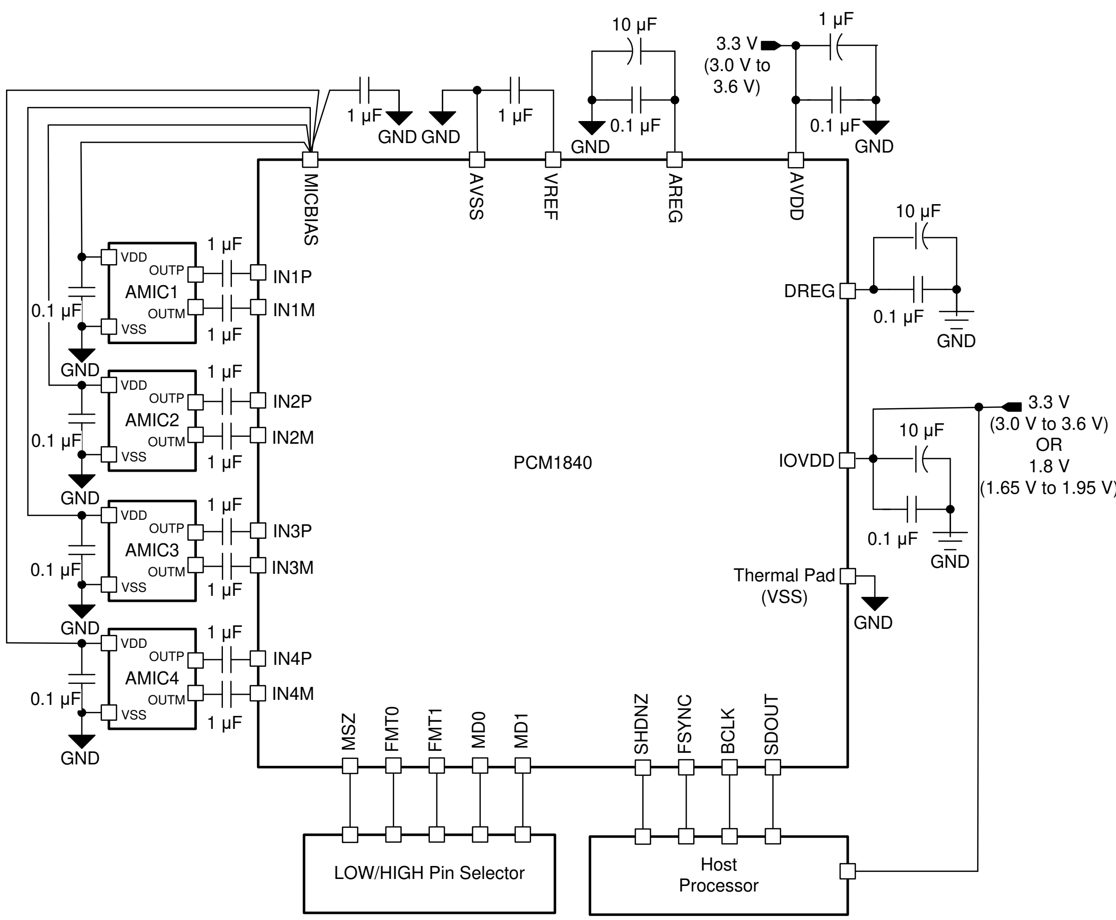


图 48. Four-Channel Analog Microphone Recording Diagram for 3.3-V AVDD Operation

版权 © 2019, Texas Instruments Incorporated

Typical Application (接下页)

8.2.1 Design Requirements

表 21 lists the design parameters for this application.

表 21. Design Parameters

KEY PARAMETER	SPECIFICATION: 3.3-V AVDD OPERATION
AVDD	3.3 V
AVDD supply current consumption	> 23 mA (PLL on, four-channel recording, f_S = 48 kHz)
IOVDD	1.8 V or 3.3 V
Maximum MICBIAS current	10 mA (MICBIAS voltage is the same as VREF)

8.2.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCM1840 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power-up the IOVDD and AVDD power supplies, keeping the SHDNZ pin voltage low
   b. The device now goes into hardware shutdown mode (ultra-low-power mode < 1 µA)
2. Transition from hardware shutdown mode to active mode whenever required for the recording operation:
   a. Connect the MSZ, FMT0, and FMT1 pins voltage low to configure the device in 4-channel TDM slave mode
   b. Release SHDNZ only when the IOVDD and AVDD power supplies settle to the steady-state operating voltage
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a

      See the *Phase-Locked Loop (PLL) and Clock Generation* section for supported sample rates and the BCLK to FSYNC ratio
   d. The device recording data are now sent to the host processor via the TDM audio serial data bus
3. Assert the SHDNZ pin low to enter hardware shutdown mode (again) at any time
4. Follow step 2 onwards to exit hardware shutdown mode (again)

版权 © 2019, Texas Instruments Incorporated

8.2.3 Application Curves

Measurements are done on the EVM by feeding the device analog input signal using audio precision and with a 3.3-V AVDD supply.

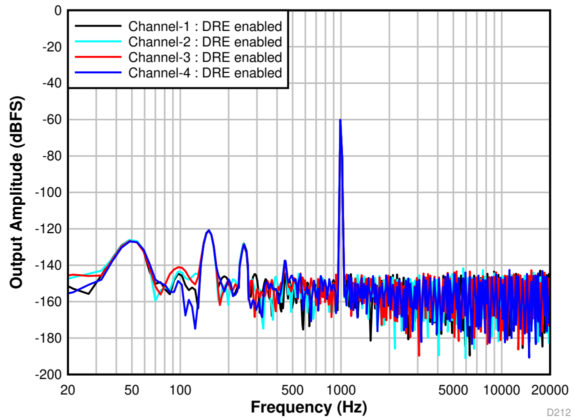


图 49. FFT With a –60-dBr Input With DRE Enabled

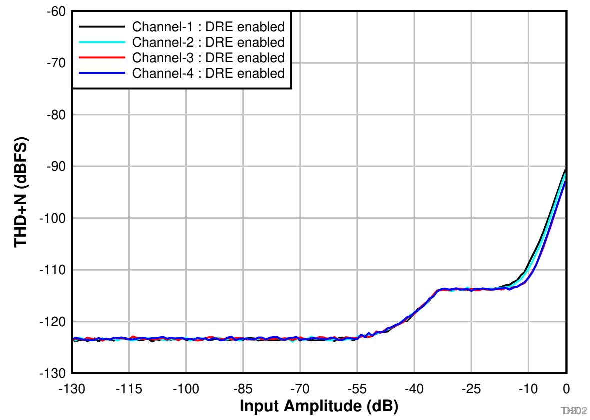


图 50. THD+N vs Input Amplitude With DRE Enabled

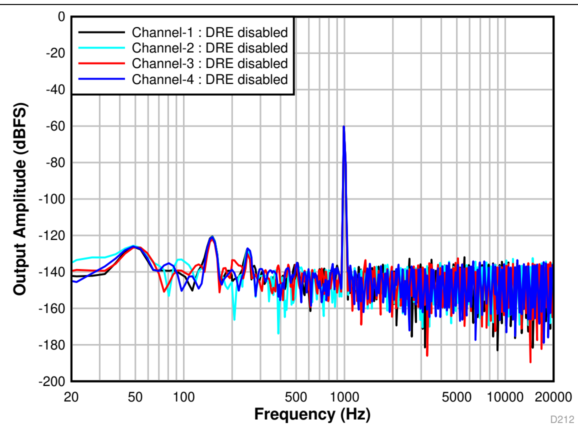


图 51. FFT With a –60-dBr Input With DRE Disabled

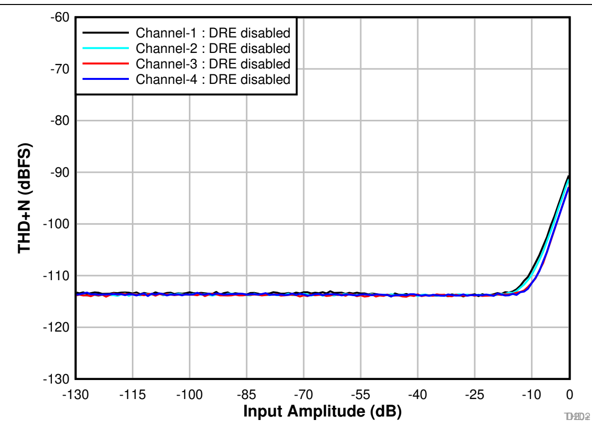


图 52. THD+N vs Input Amplitude With DRE Disabled

9 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, keep the SHDNZ pin low until the IOVDD supply voltage settles to a stable and supported operating voltage range. After all supplies are stable, set the SHDNZ pin high to initialize the device. Assert the SHDNZ pin high only when all hardware control pins (MSZ, MD0, MD1, FMT0, and FMT1) are driven to the voltage level for the device desired mode of operation.

For the supply power-up requirement, t_1 and t_2 must be at least 100 µs. For the supply power-down requirement, t_3 and t_4 must be at least 10 ms. This timing (as shown in 图 53) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into hardware shutdown mode.

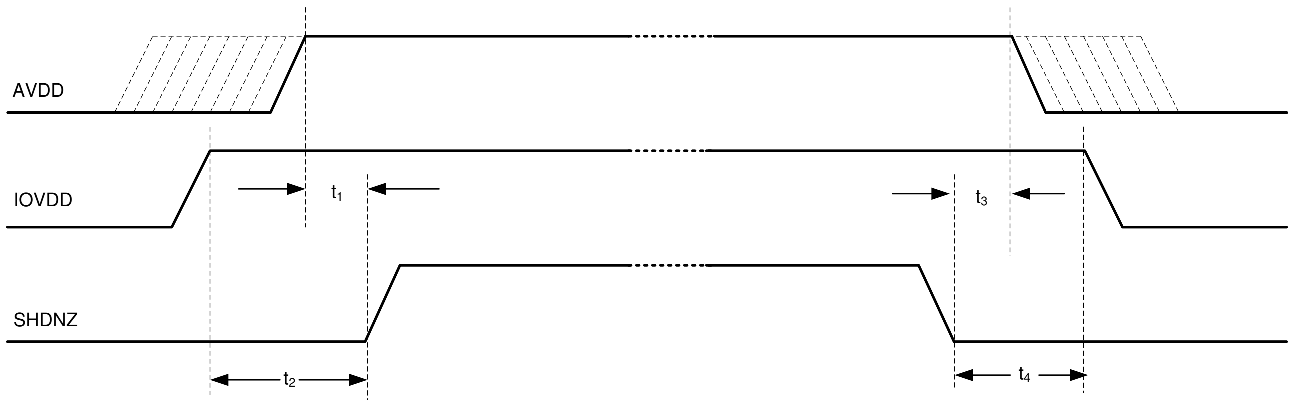


图 53. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 1 V/µs and that the wait time between a power-down and a power-up event is at least 100 ms.

The PCM1840 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG. However, if the AVDD voltage is less than 1.98 V in the system, then short the AREG and AVDD pins onboard.

版权 © 2019, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Directly short the VREF and MICBIAS external capacitors ground terminal to the AVSS pin without using any vias for this connection trace.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

10.2 Layout Example

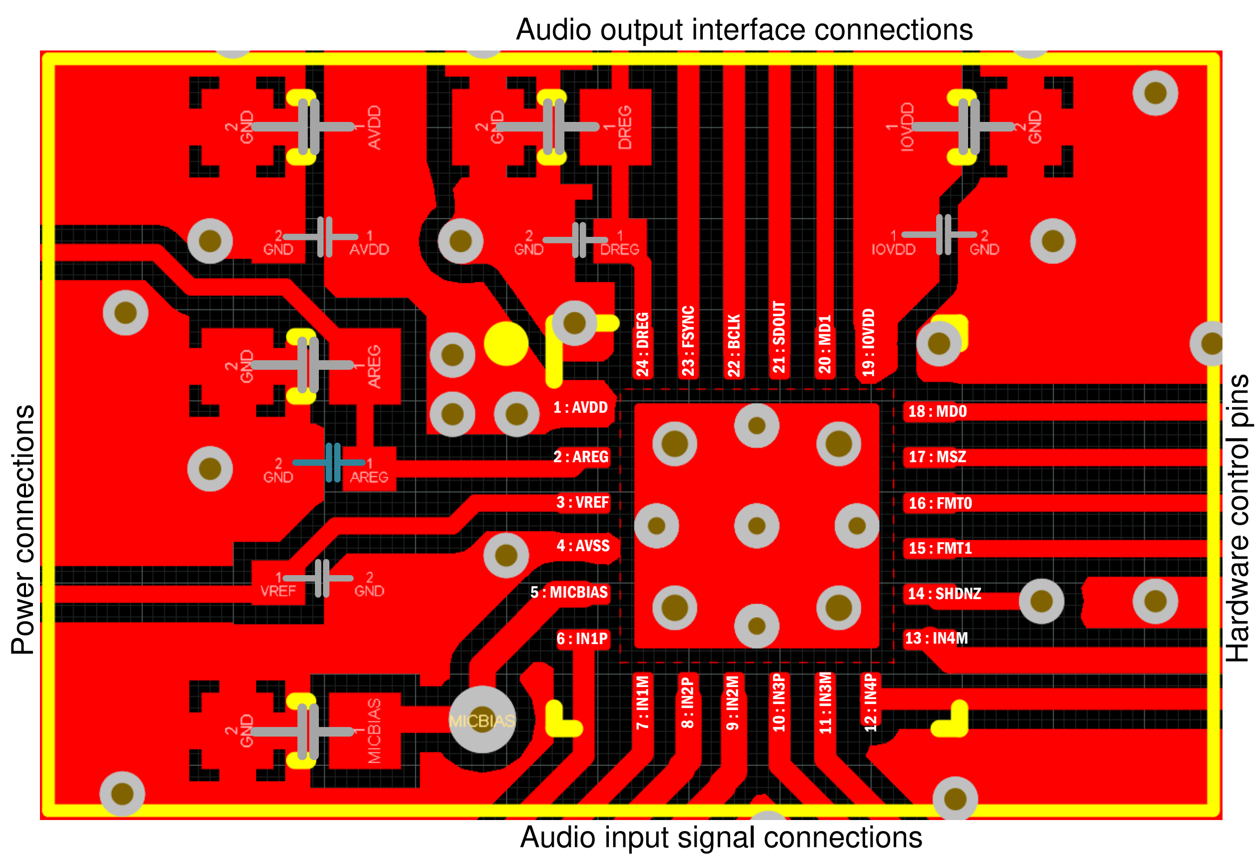


图 54. Example Layout

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 商标

Burr-Brown, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

版权 © 2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1840IRTWR	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PCM1840
PCM1840IRTWR.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PCM1840
PCM1840IRTWRG4	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCM1840
PCM1840IRTWRG4.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCM1840
PCM1840IRTWT	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PCM1840
PCM1840IRTWT.A	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PCM1840

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

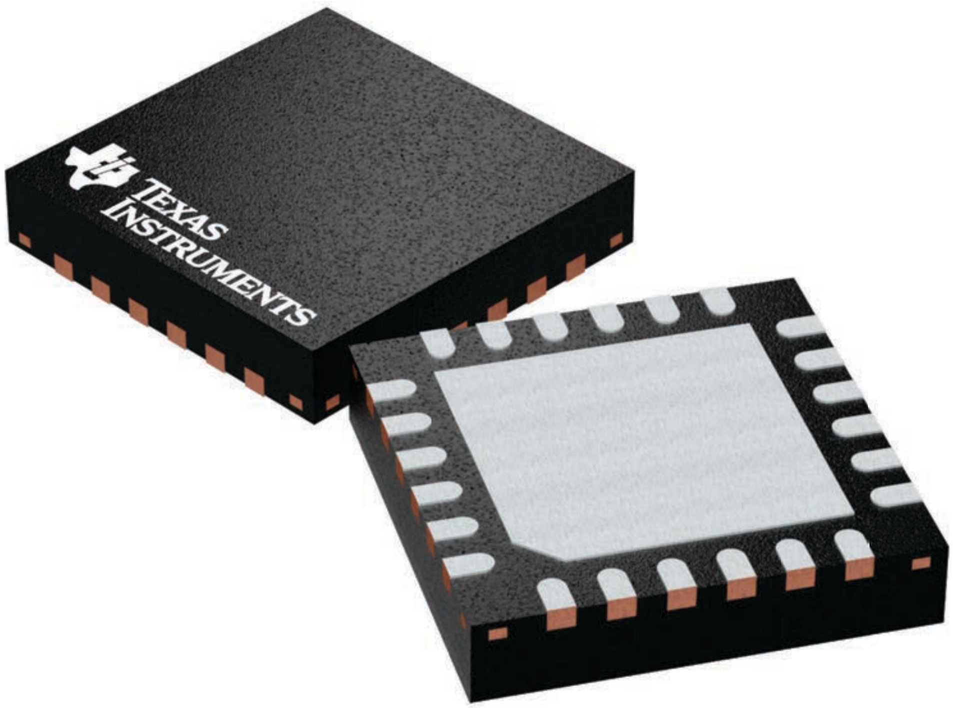
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

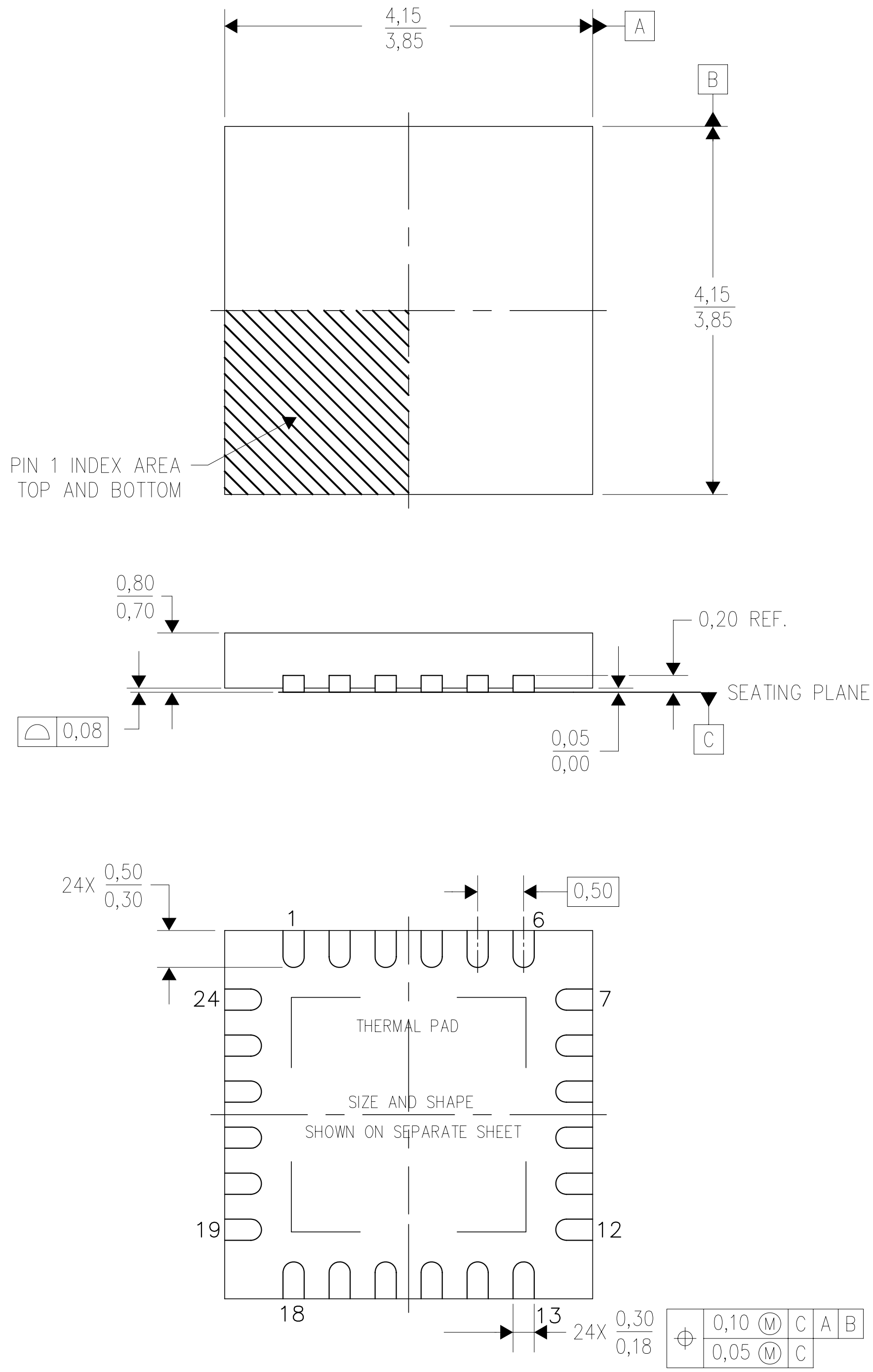
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

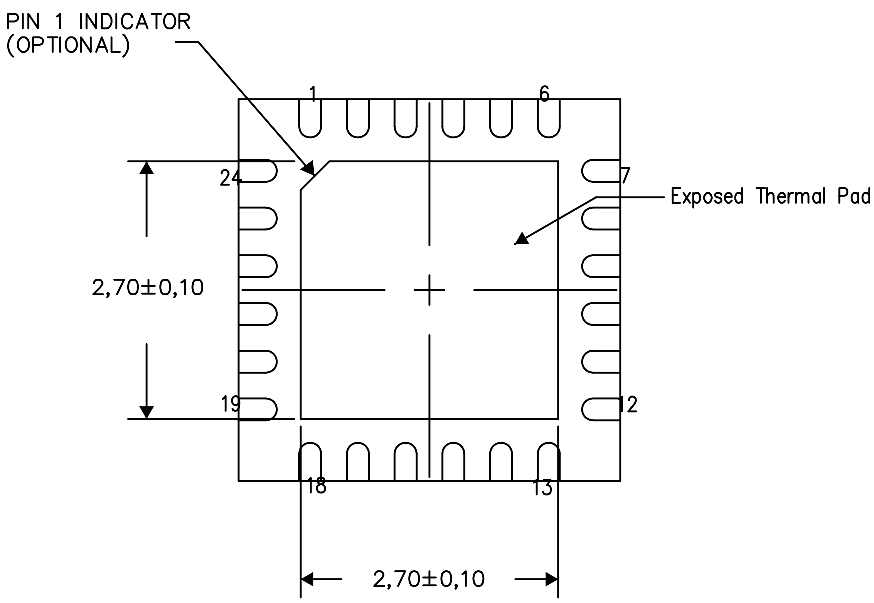
RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



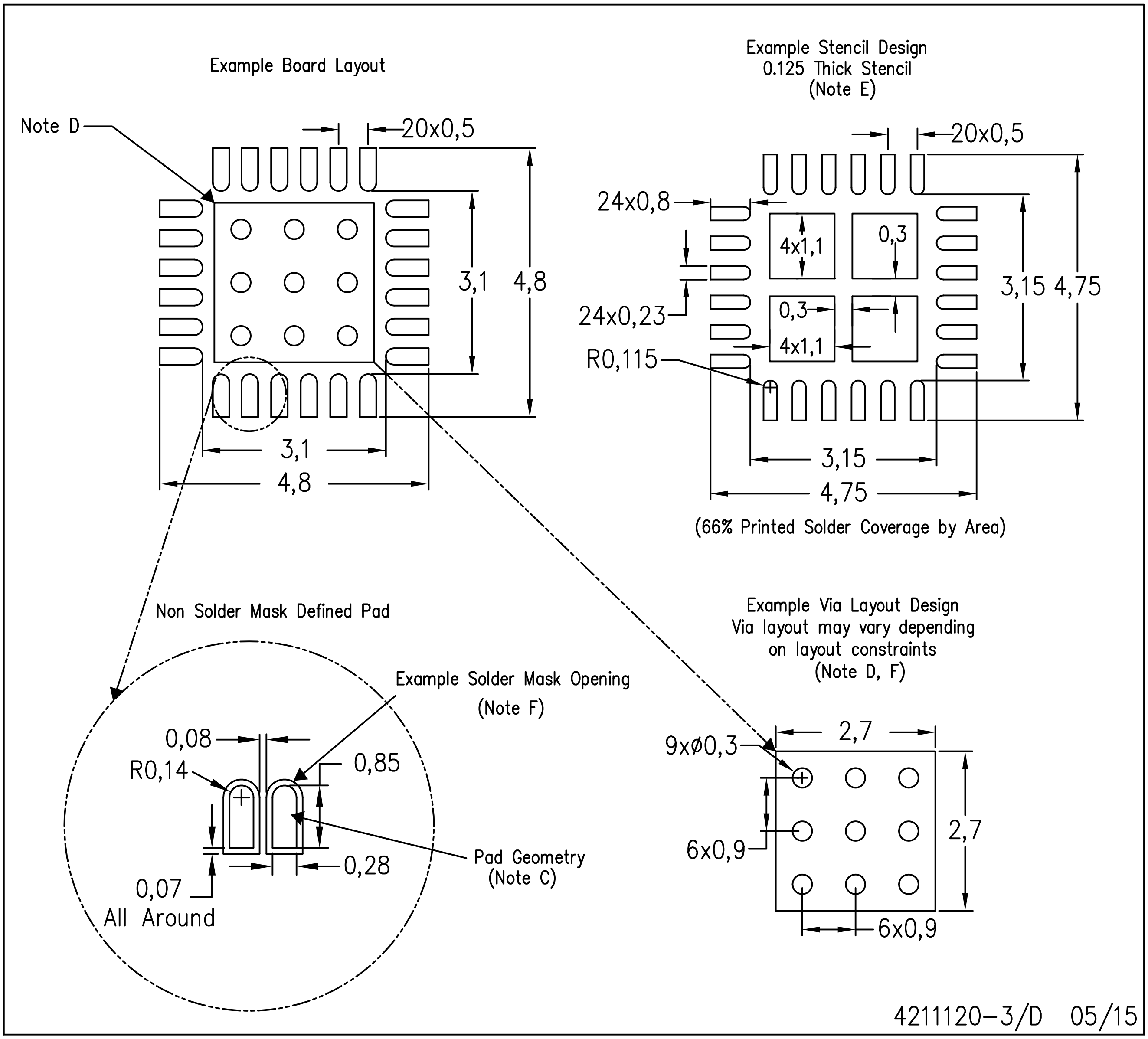
Bottom View

Exposed Thermal Pad Dimensions

4206249-5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月