TEXAS INSTRUMENTS
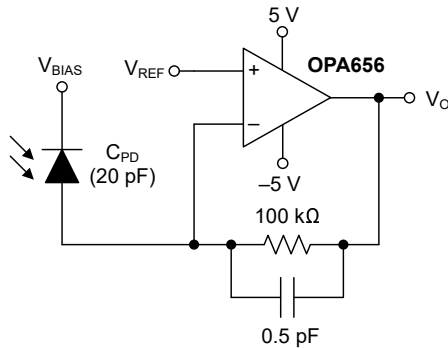
OPA656 550Mhz 单位增益稳定 FET 输入运算放大器

1 特性

- 高带宽：
  - 增益带宽积：230MHz
  - 单位增益带宽：550MHz
  - 大信号带宽 ($2V_{PP}$)：150MHz
- 高精度：
  - 输入失调电压：600μV（最大值）
  - 输入失调电压温漂：6μV/°C（最大值）
- 输入电压噪声：6nV/√Hz
- 输入偏置电流：2pA
- 低失真（R_L = 200Ω，V_O = $2V_{PP}$）：
  - 5MHz 时的 HD2、HD3：﹣80dBc、﹣100dBc
- 电源电压范围：8V 至 12V

2 应用

- 高速数据采集 (DAQ)
- 医学和化学分析器
- 有源探头
- 示波器
- 光学通信模块
- 测试和测量前端
- 光学时域反射法 (OTDR)

3 说明

OPA656 组合了一个宽带单位增益稳定电压反馈运算放大器和一个低噪声结型栅场效应晶体管 (JFET) 输入级，可提供用于跨阻应用和高速数据采集前端的超高动态范围放大器。极低的直流误差在光学应用以及测试和测量中提供了很好的精度。

OPA656 具有超低输入电压噪声 (6nV/√Hz)，可在跨阻应用中实现极低的集成噪声。高输入阻抗和低输入电压噪声的组合使得 OPA656 成为适用于光学测试和通信设备以及医疗和科学仪器的出色宽带跨阻放大器。

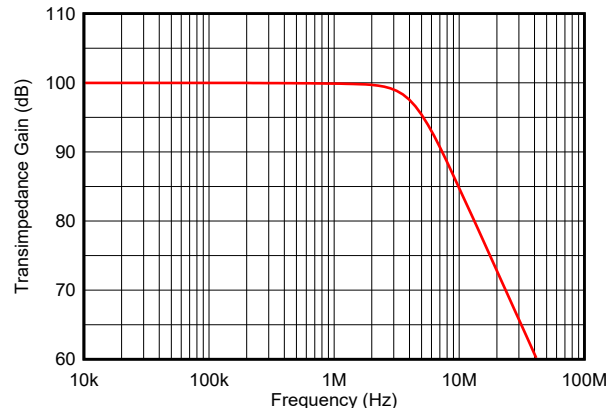OPA656 具有 230MHz 的宽增益带宽。150MHz 的大信号带宽和低失真使得 OPA656 非常适用于高速数字转换器前端、有源探头以及其他测试和测量前端。

OPA656 可在 -40°C 至 +85°C 的工业温度范围内正常运行。

封装信息

器件型号	封装[1]	封装尺寸[2]
OPA656	D（SOIC，8）	4.9mm × 6mm
	DBV（SOT-23，5）	2.9mm × 2.8mm

(1) 如需更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

宽带光电二极管跨阻放大器

100kΩ 跨阻带宽

Table of Contents

4 Device Comparison Table

DEVICE	V_S (V)	GBW (MHz)	SLEW RATE (V/μs)	VOLTAGE NOISE (nV/√Hz)	MINIMUM STABLE GAIN (V/V)
OPA656	±6	230	550	6	1
OPA814	±6.3	250	750	5.3	1
OPA817	±6.3	400	1000	4.5	1
OPA818	±6.5	2700	1400	2.2	7
OPA659	±6.5	350	2550	8.9	1
THS4631	±15	210	1000	7	1

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

5 Pin Configuration and Functions
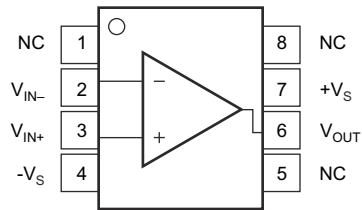
图 5-1. D Package, 8-Pin SOIC Surface-Mount (Top View)
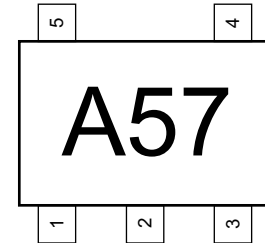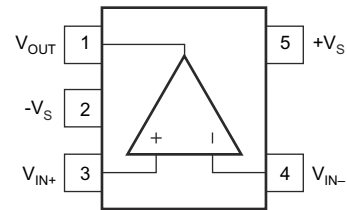
Pin Orientation/Package Marking

图 5-2. DBV Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
| | NO. | | | |
	D (SOIC)	DBV (SOT-23)		
NC	1, 5, 8	—	—	No internal connection
V_{IN-}	2	4	Input	Inverting input
V_{IN+}	3	3	Input	Noninverting input
$-V_S$	4	2	Power	Negative power supply
$+V_S$	7	5	Power	Positive power supply
V_{OUT}	6	1	Output	Output of amplifier

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Supply voltage (total bipolar supplies)		±6.5	V
	Maximum dV_S/dT for supply turn-on and turn-off[2]		1	V/µs
	Internal power dissipation	See *Thermal Information*		
V_I	Input voltage	$-V_S$	$+V_S$	V
V_{ID}	Differential input voltage	$-V_S$	$+V_S$	V
I_I	Continuous input current[3]		±10	mA
I_O	Continuous output current[4]		±30	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying less than this specification keeps the edge-triggered ESD absorption devices across the supply pins off.
(3) Continuous input current limit for the ESD diodes to supply pins.
(4) Long-term continuous current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	8	10	12	V
T_A	Ambient temperature	-40	25	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA656		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123	154	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	88.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.3	55.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.1	33.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	65.5	55.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at $T_A \cong 25°C$, $V_S = \pm5$ V, G = +2 V/V, $R_F = 250$ Ω, $R_L = 100$ Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = +1 V/V, V_O = 200 mV$_{PP}$, R_F = 0 Ω		550		MHz
		G = +2 V/V, V_O = 200 mV$_{PP}$		230		
		G = +5 V/V, V_O = 200 mV$_{PP}$		59		
		G = +10 V/V, V_O = 200 mV$_{PP}$		23		
GBW	Gain-bandwidth product	G ⩾ 10 V/V		230		MHz
	Bandwidth for 0.1-dB flatness	V_O = 200 mV$_{PP}$		50		MHz
	Peaking at G = +1 V/V	V_O = 200 mV$_{PP}$, R_F = 0 Ω		1		dB
LSBW	Large-signal bandwidth	V_O = 2 V$_{PP}$		130		MHz
SR	Slew rate	V_O = 1-V step		400		V/μs
	Rise-and-fall time	V_O = 0.2-V step		1.3		ns
	Settling time to 0.02%	V_O = 2-V step		19		ns
HD2	Second-order harmonic distortion	f = 5 MHz, V_O = 2 V$_{PP}$, R_L = 200 Ω		–75		dBc
		f = 5 MHz, V_O = 2 V$_{PP}$, R_L > 500 Ω		–78		
HD3	Third-order harmonic distortion	f = 5 MHz, V_O = 2 V$_{PP}$, R_L = 200 Ω		–90		dBc
		f = 5 MHz, V_O = 2 V$_{PP}$, R_L > 500 Ω		–100		
e_N	Input voltage noise	f > 100 kHz		6		nV/$\sqrt{Hz}$
	Input current noise	f = 100 kHz		5		fA/$\sqrt{Hz}$
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_O = 0 V	60	75		dB
		V_O = 0 V, T_A = –40°C to +85°C	58			
V_{OS}	Input-referred offset voltage	V_{CM} = 0 V		±0.2	±1.8	mV
		V_{CM} = 0 V, T_A = –40°C to +85°C			±2.6	
	Input offset voltage drift[1]	V_{CM} = 0 V		±2	±12	μV/°C
		V_{CM} = 0 V, T_A = –40°C to +85°C			±12	
I_B	Input bias current	V_{CM} = 0 V		±2	±20	pA
		V_{CM} = 0 V, T_A = –40°C to +85°C			±5000	
I_{OS}	Input offset current	V_{CM} = 0 V		±1	±20	pA
		V_{CM} = 0 V, T_A = –40°C to +85°C			±5000	
INPUT						
CMIR	Most positive input voltage[2]		2.1	2.75		V
		T_A = –40°C to +85°C	2			
CMIR	Most negative input voltage[2]			–4.3	–3.9	V
		T_A = –40°C to +85°C			–3.7	
CMIR	Most positive input voltage[3]		2.6	3.25		V
		T_A = –40°C to +85°C	2.4			
CMIR	Most negative input voltage[3]			–4.5	–4	V
		T_A = –40°C to +85°C			–3.8	
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	80	90		dB
		V_{CM} = ±0.5 V, T_A = –40°C to +85°C	76			
	Input impedance common-mode			10^{12} ‖ 0.4		Ω ‖ pF

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Product Folder Links: *OPA656*

English Data Sheet: SBOS196

6.5 Electrical Characteristics （续）

at $T_A \cong 25°C$, $V_S = \pm5$ V, G = +2 V/V, $R_F = 250$ Ω, $R_L = 100$ Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance differential mode			10^{10} ‖ 2.6		Ω ‖ pF

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

6.5 Electrical Characteristics （续）

at $T_A \cong 25°C$, $V_S = \pm5$ V, $G = +2$ V/V, $R_F = 250\ \Omega$, $R_L = 100\ \Omega$, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing	No Load	±3.7	±3.9		V
		$R_L = 100\ \Omega$	±3.3	±3.5		
		$R_L = 100\ \Omega$, $T_A = -40°C$ to +85°C	±3.1			
	Current output, sourcing		50	70		mA
		$T_A = -40°C$ to +85°C	45			
	Current output, sinking			−70	−50	mA
		$T_A = -40°C$ to +85°C			−45	
	Closed-loop output impedance	G = +1 V/V, f = 0.1 MHz		0.01		Ω
POWER SUPPLY						
	Specified operating voltage			±5		V
	Maximum operating voltage range				±6	V
		$T_A = -40°C$ to +85°C			±6	
I_Q	Quiescent current		11.7	15	16.7	mA
		$T_A = -40°C$ to +85°C	11.1		16.8	
+PSRR	Positive power-supply rejection ratio	$+V_S = 4.5$ to 5.5 V	72	85		dB
		$+V_S = 4.5$ to 5.5 V, $T_A = -40°C$ to +85°C	68			
−PSRR	Negative power-supply rejection ratio	$-V_S = -4.5$ to -5.5 V	56	80		dB
		$-V_S = -4.5$ to -5.5 V, $T_A = -40°C$ to +85°C	52			

(1) Based on electrical characterization of 32 devices. Minimum and maximum values are not specified by final automated test equipment (ATE) nor by QA sample testing. Typical specifications are ±1 sigma.
(2) Tested at 3 dB less than minimum specified CMRR at ±CMIR limits.
(3) Input range to give > 53-dB CMRR.

6.6 Electrical Characteristics: High Grade DC Specifications

at $T_A \cong 25°C$, $V_S = \pm5$ V, $G = +2$ V/V, $R_F = 250\ \Omega$, $R_L = 100\ \Omega$, and input and output referenced to mid-supply (unless otherwise noted)[1]

PARAMETER			MIN	NOM	MAX	UNIT
V_{OS}	Input-referred offset voltage	$V_{CM} = 0$ V		±0.1	±0.6	mV
		$V_{CM} = 0$ V, $T_A = -40°C$ to +85°C			±0.9	
	Input offset voltage drift	$V_{CM} = 0$ V		±2	±6	µV/°C
		$V_{CM} = 0$ V, $T_A = -40°C$ to +85°C			±6	
I_B	Input bias current	$V_{CM} = 0$ V		±2	±20	pA
		$V_{CM} = 0$ V, $T_A = -40°C$ to +85°C			±1250	
I_{OS}	Input offset current	$V_{CM} = 0$ V		±1	±20	pA
		$V_{CM} = 0$ V, $T_A = -40°C$ to +85°C			±1250	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm0.5$ V	84	95		dB
		$V_{CM} = \pm0.5$ V, $T_A = -40°C$ to +85°C	83			
+PSRR	Positive power-supply rejection ratio	$+V_S = 4.5$ to 5.5 V	74	90		dB
		$+V_S = 4.5$ to 5.5 V, $T_A = -40°C$ to +85°C	70			

at $T_A \cong 25°C$, $V_S = \pm 5$ V, G = +2 V/V, $R_F = 250\ \Omega$, $R_L = 100\ \Omega$, and input and output referenced to mid-supply (unless otherwise noted)[1]

PARAMETER			MIN	NOM	MAX	UNIT
–PSRR	Negative power-supply rejection ratio	$-V_S = -4.5$ to -5.5 V	62	85		dB
		$-V_S = -4.5$ to -5.5 V, $T_A = -40°C$ to +85°C	58			

(1)   All other specifications are the same as the standard-grade.

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

6.7 Typical Characteristics: V_S = ±5 V

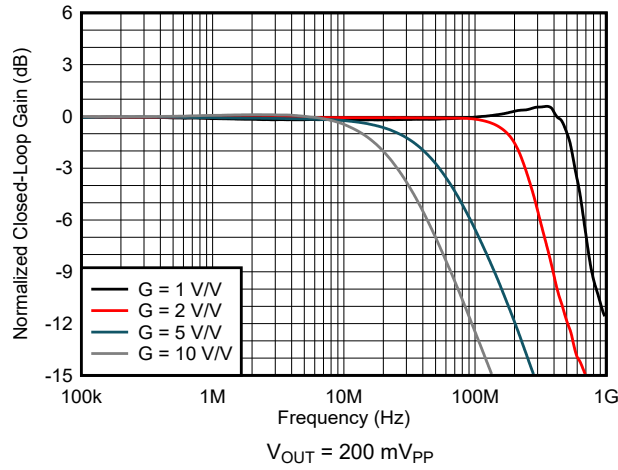at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)

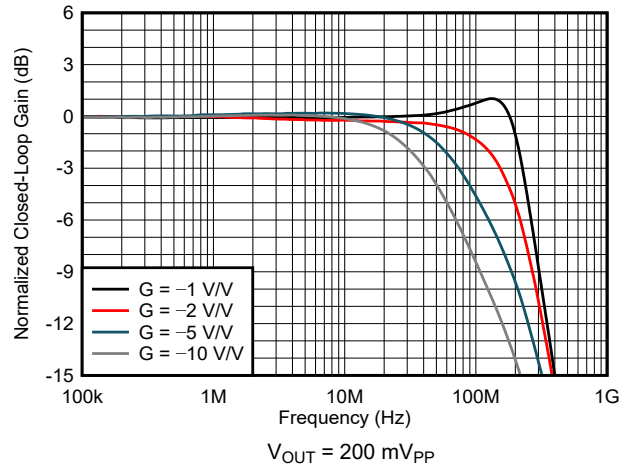图 6-1. Noninverting Small-Signal Frequency Response

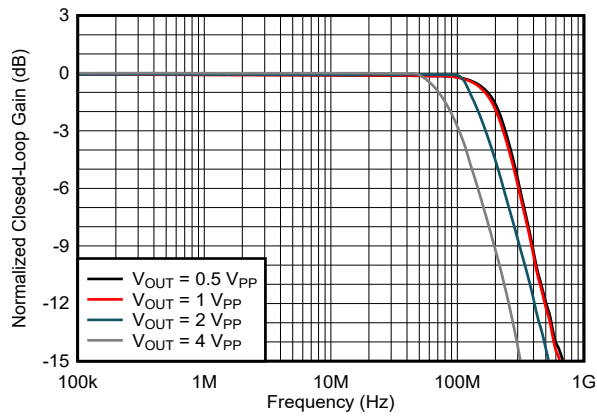图 6-2. Inverting Small-Signal Frequency Response

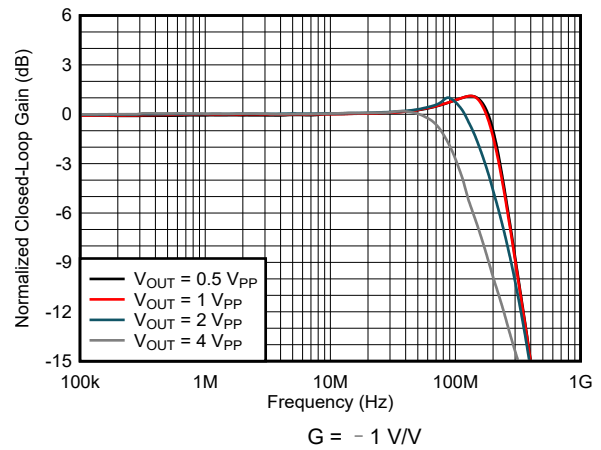图 6-3. Noninverting Large-Signal Frequency Response
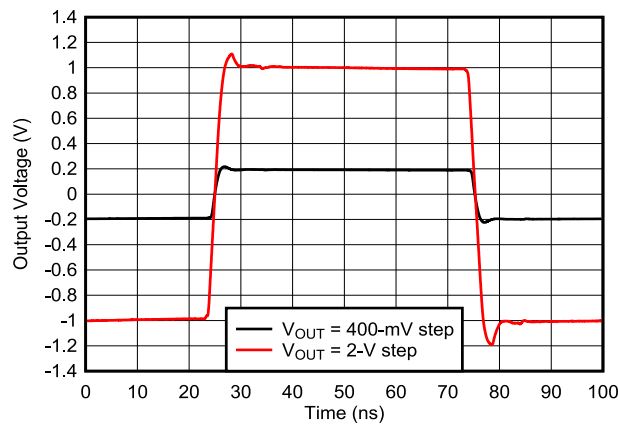

图 6-4. Inverting Large-Signal Frequency Response

图 6-5. Noninverting Pulse Response

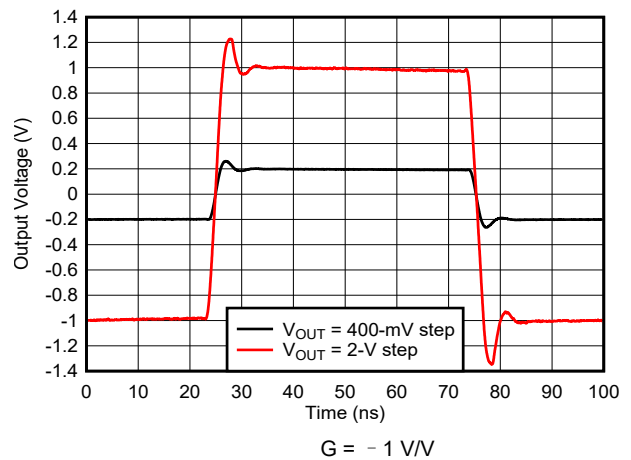图 6-6. Inverting Pulse Response

Product Folder Links: OPA656

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6.7 Typical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)
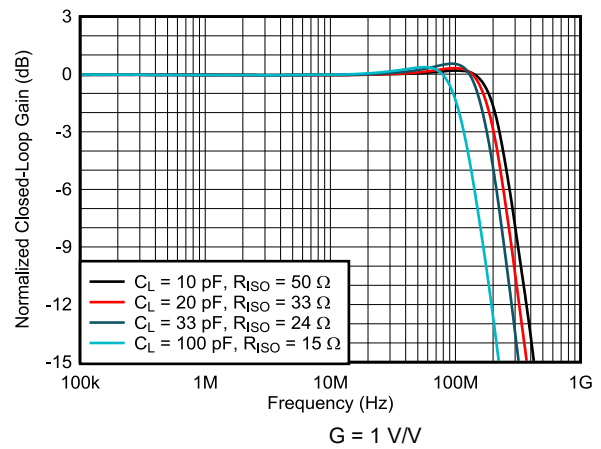

G = 1 V/V
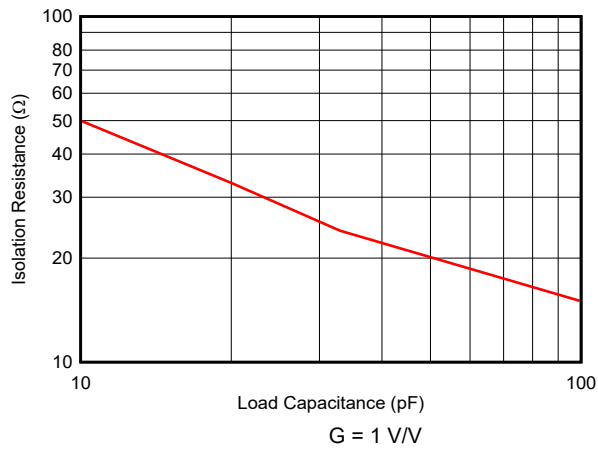
图 6-7. Recommended R_S vs Capacitive Load

- C_L = 10 pF, R_{ISO} = 50 Ω
- C_L = 20 pF, R_{ISO} = 33 Ω
- C_L = 33 pF, R_{ISO} = 24 Ω
- C_L = 100 pF, R_{ISO} = 15 Ω

G = 1 V/V

图 6-8. Frequency Response vs Capacitive Load

f = 5 MHz V_{OUT} = 2 V_{PP}
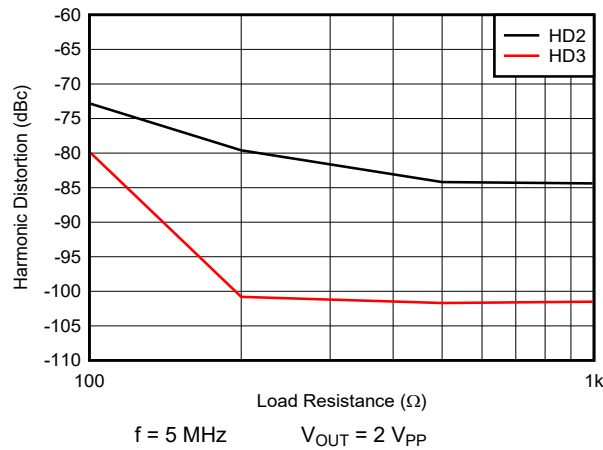
图 6-9. Harmonic Distortion vs Load Resistance

f = 5 MHz R_L = 200 Ω
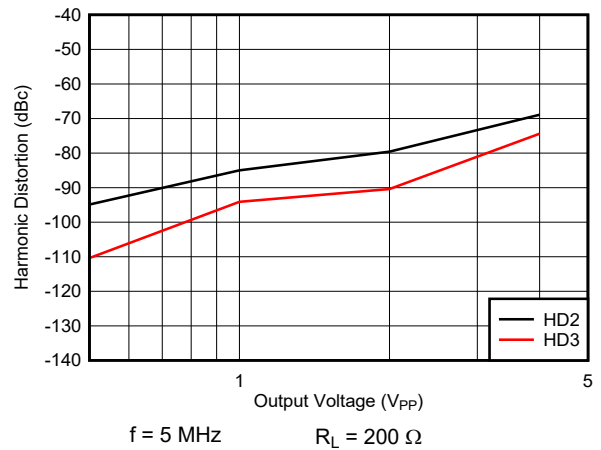
图 6-10. Harmonic Distortion vs Output Voltage

R_L = 200 Ω V_{OUT} = 2 V_{PP}
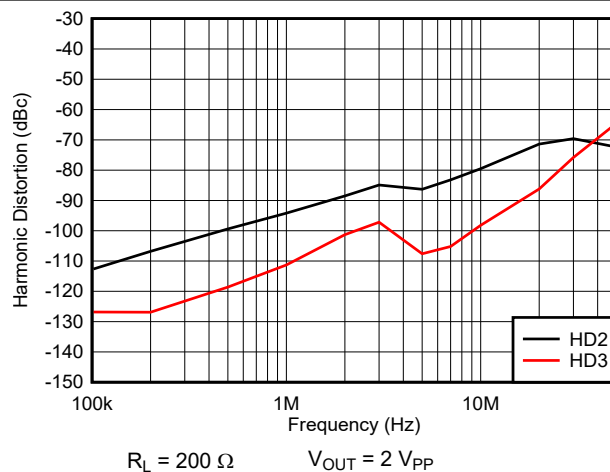
图 6-11. Harmonic Distortion vs Frequency
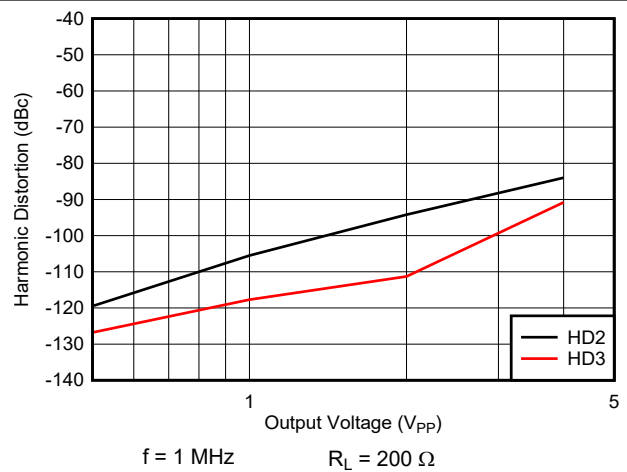
f = 1 MHz R_L = 200 Ω

图 6-12. Harmonic Distortion vs Output Voltage

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6.7 Typical Characteristics: V$_S$ = ±5 V (continued)

at T$_A$ = 25°C, G = +2 V/V, R$_F$ = 250 Ω, and R$_L$ = 100 Ω (unless otherwise noted)

图 6-13. Harmonic Distortion vs Noninverting Gain
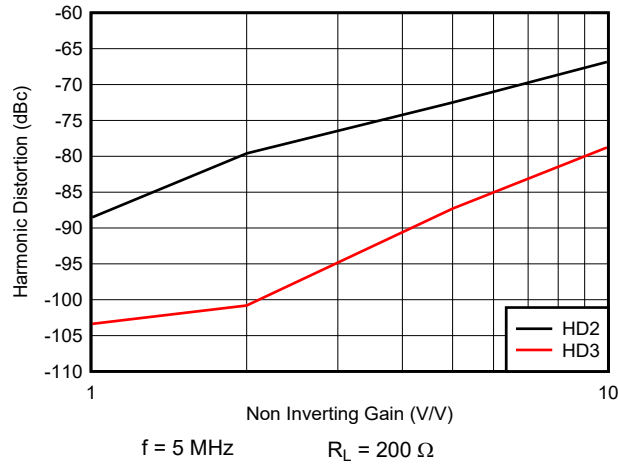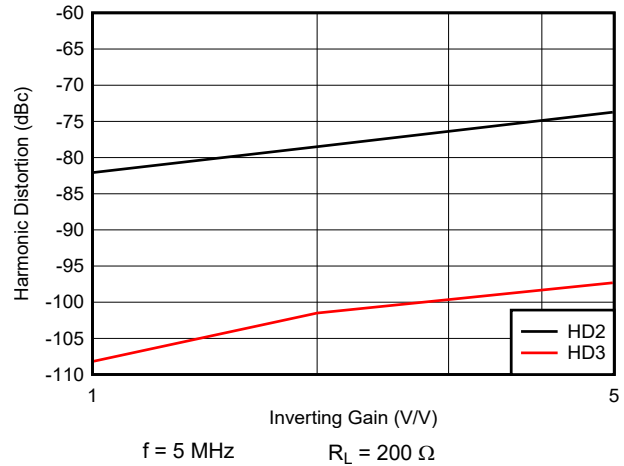
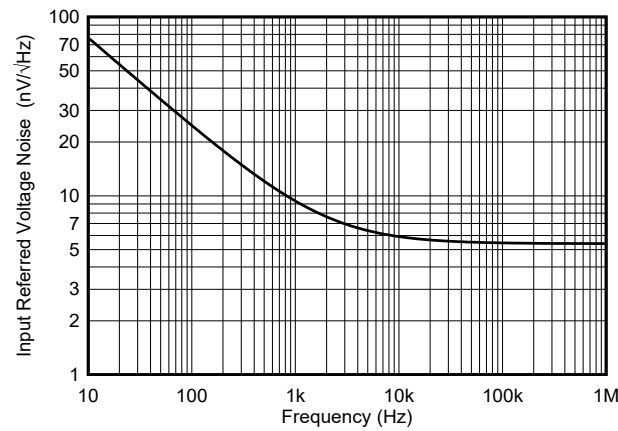图 6-14. Harmonic Distortion vs Inverting Gain

图 6-15. Input Voltage Noise Density
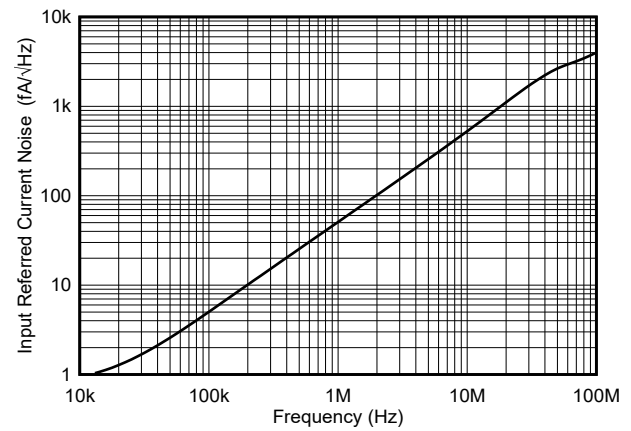
图 6-16. Input Current Noise Density
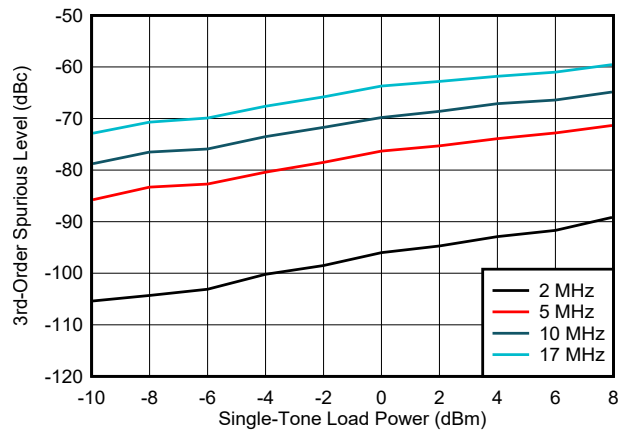
图 6-17. 2-Tone, 3rd-Order Intermodulation Spurious
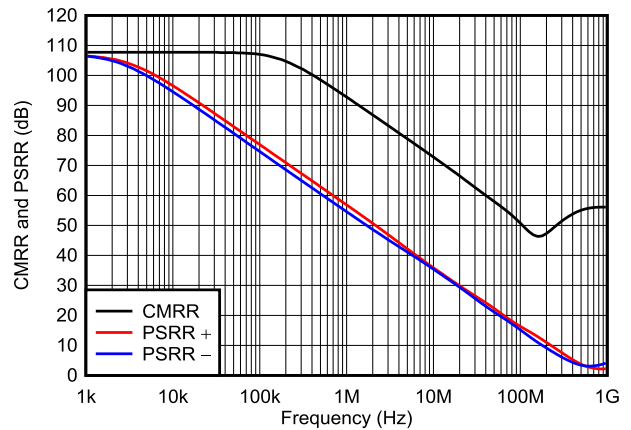
图 6-18. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

6.7 Typical Characteristics: V$_S$ = ±5 V (continued)

at T$_A$ = 25°C, G = +2 V/V, R$_F$ = 250 Ω, and R$_L$ = 100 Ω (unless otherwise noted)
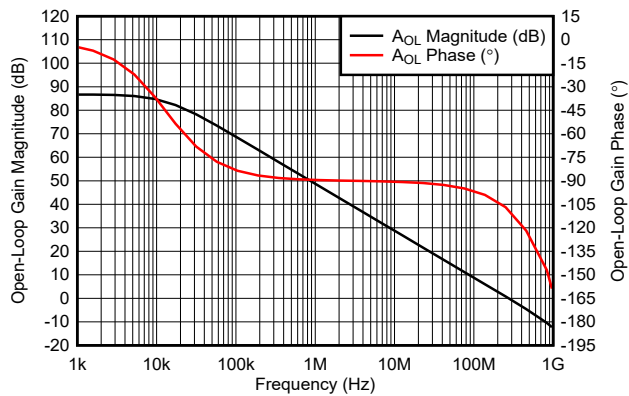
图 6-19. Open-Loop Gain and Phase
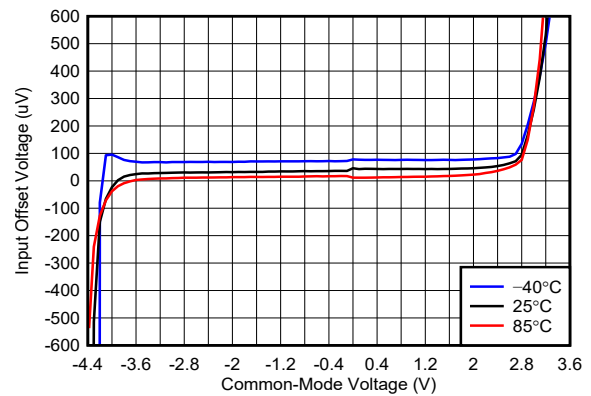
图 6-20. Input offset voltage vs Common-Mode Input Voltage
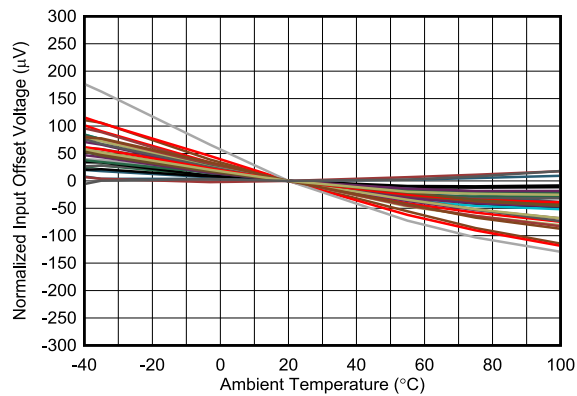
图 6-21. Typical Input Offset Voltage Over Temperature
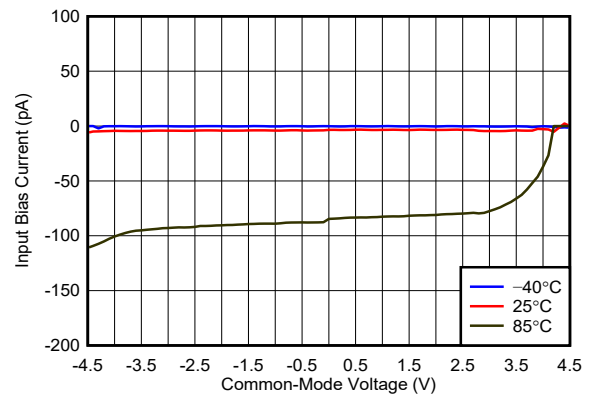
图 6-22. Typical Input Bias Current vs Common-Mode Input Voltage
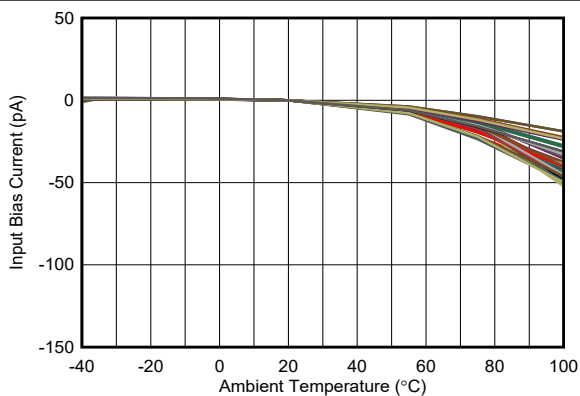
图 6-23. Typical Input Bias Current Over Temperature
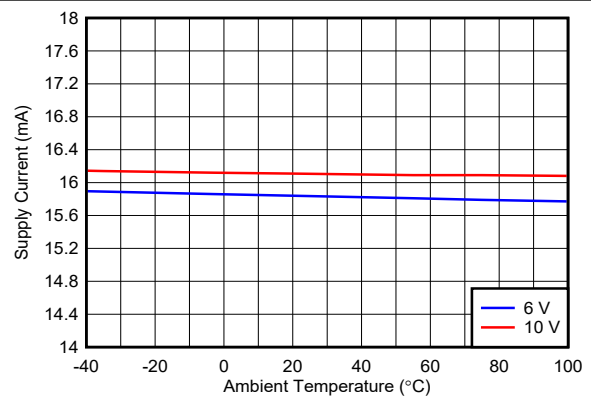
图 6-24. Supply Current vs Temperature

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English Data Sheet: SBOS196

6.7 Typical Characteristics: V$_S$ = ±5 V (continued)

at T$_A$ = 25°C, G = +2 V/V, R$_F$ = 250 Ω, and R$_L$ = 100 Ω (unless otherwise noted)
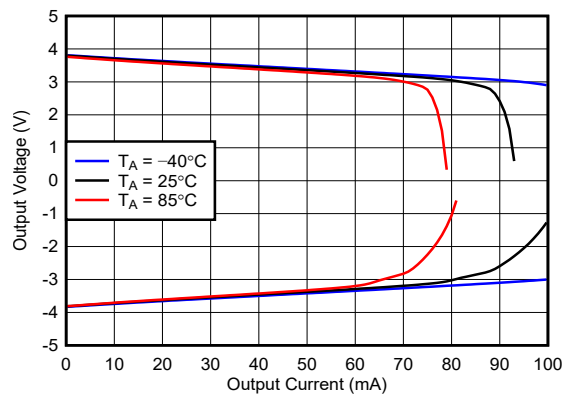
图 **6-25. Output voltage vs Output Current Over Temperature**
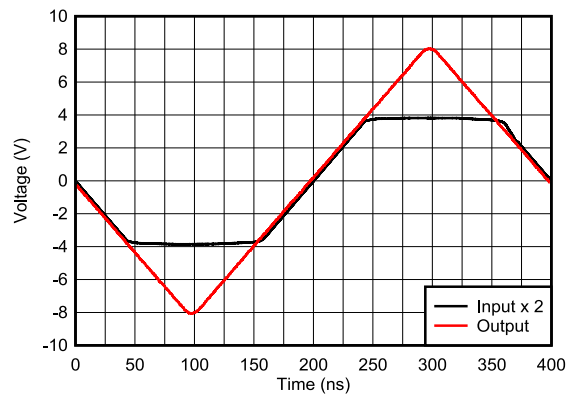
图 **6-26. Noninverting Input Overdrive Recovery**

G = $-$1 V/V
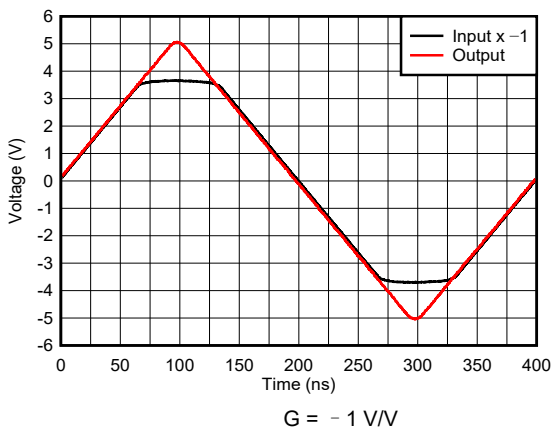
图 **6-27. Inverting Overdrive Recovery**

G = 1 V/V
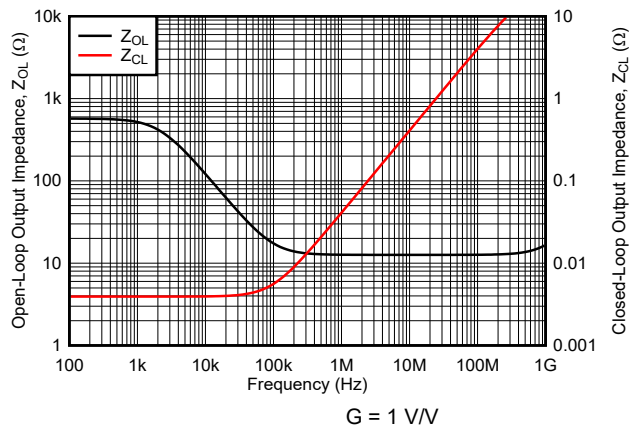
图 **6-28. Closed-Loop and open-loop Output Impedance vs Frequency**

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

7 Detailed Description

7.1 Overview

The OPA656 is a high gain-bandwidth, voltage-feedback operational amplifier featuring a low-noise JFET input stage. The OPA656 is compensated to be unity-gain stable and finds wide use in applications that require high input impedance, such as optical front-end applications and test and measurement systems. For the best dc precision, a high-grade version (OPA656UB or OPA656NB) is available that specifies the key dc parameters to even tighter limits.

7.2 Feature Description

7.2.1 Input and ESD Protection

The OPA656 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the table of *Absolute Maximum Ratings*. 图 7-1 shows how all device pins are protected with internal ESD protection diodes to the power supplies.
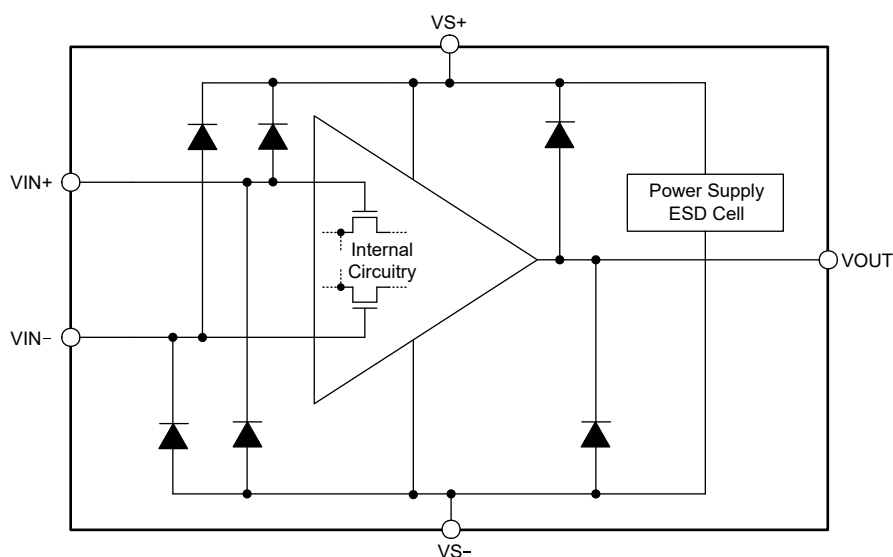
图 **7-1. Internal ESD Protection**

Along with ESD protection, these diodes provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes typically support 10 mA of continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA656), add current limiting series resistors into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

7.3 Device Functional Modes

The OPA656 has a single functional mode and is operational when the power-supply voltage is greater than 8 V. The maximum power supply voltage for the OPA656 is 12 V (±6 V). The OPA656 can be operated on both single and dual supplies.

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Wideband, Noninverting Operation

The OPA656 provides a unique combination of a broadband, unity gain stable, voltage-feedback amplifier with the dc precision of a trimmed JFET-input stage. The very high gain bandwidth product (GBP) of 230 MHz can be used to either deliver high signal bandwidths for low-gain buffers, or to deliver broadband, low-noise transimpedance bandwidth to photodiode-detector applications. To achieve the full performance of the OPA656, careful attention to printed-circuit-board (PCB) layout and component selection is required, as discussed in the remaining sections of this data sheet.

图 8-1 shows the noninverting gain of +2 V/V circuit used as the basis for most of the *Typical Characteristics*. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. In 图 8-1, the 50-Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in 图 8-1) while output power specifications are at the matched 50-Ω load. The total 100-Ω load at the output combined with the 500-Ω total feedback network load, presents the OPA656 with an effective output load of 83 Ω for the circuit of 图 8-1.
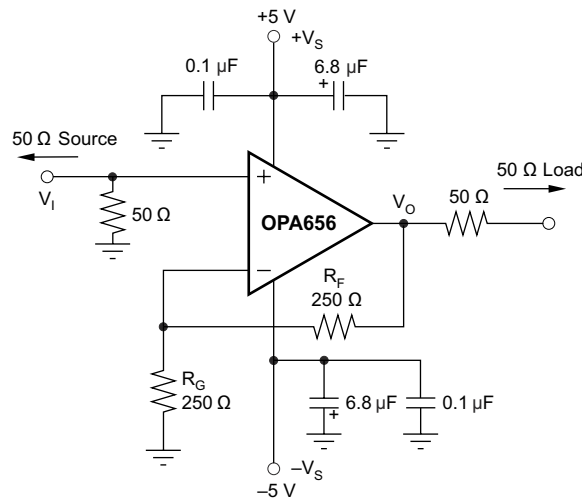
图 8-1. Noninverting G = +2 V/V Specifications and Test Circuit

Voltage-feedback operational amplifiers, unlike current feedback products, can use a wide range of resistor values to set the gain. To retain a controlled frequency response for the noninverting voltage amplifier of 图 8-1, ensure that the parallel combination of $R_F \| R_G$ is always < 200 Ω. In the noninverting configuration, the parallel combination of $R_F \| R_G$ forms a pole with the parasitic input capacitance at the inverting node of the OPA656 (including layout parasitics). For best performance, ensure this pole is at a frequency greater than the closed-loop bandwidth for the OPA656. For this reason, TI recommends a direct short from the output to the inverting input for the unity-gain follower application.

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

8.1.2 Wideband, Inverting Gain Operation

The circuit of 图 8-2 shows the inverting gain of – 1 V/V test circuit used for most of the inverting typical characteristics. In this case, an additional resistor R_M is used to achieve the 50-Ω input impedance required by the test equipment using in characterization. This input impedance matching is optional in a circuit board environment where the OPA656 is used as an inverting amplifier at the output of a prior stage.

In this configuration, the feedback resistor acts as an additional load at output in parallel with the 100-Ω load used for test. Increase the R_F value to decrease the loading on the output (improving harmonic distortion) with the constraint that the parallel combination of $R_F \parallel R_G < 200$ Ω. For higher gains with the dc precision provided by the FET input OPA656, consider the higher gain bandwidth product OPA814 or OPA818.
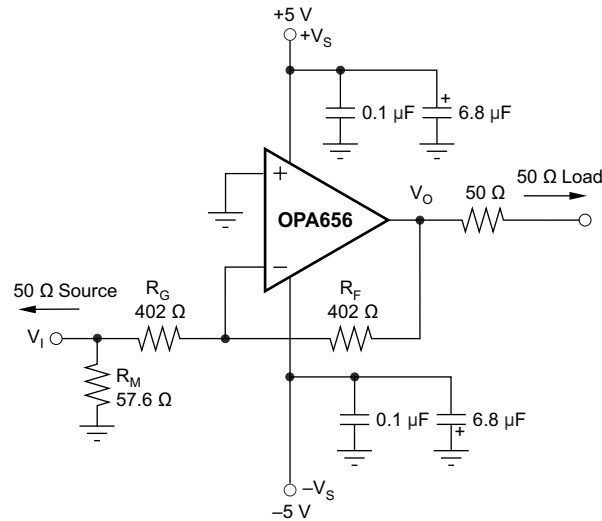
图 8-2. Inverting G = – 1 V/V Specifications and Test Circuit

图 8-2 also shows the noninverting input tied directly to ground. Often, a bias current canceling resistor to ground is included here to null out the dc errors caused by input bias current effects. This resistor is only useful when the input bias currents are matched. For a JFET part such as the OPA656, the input bias currents do not match but are so low to begin with (< 20 pA) that dc errors due to input bias currents are negligible. Thus, no resistor is recommended at the noninverting inputs for the inverting signal path condition.

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

8.2 Typical Application

The high GBP and low input voltage and current noise for the OPA656 make the device an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.
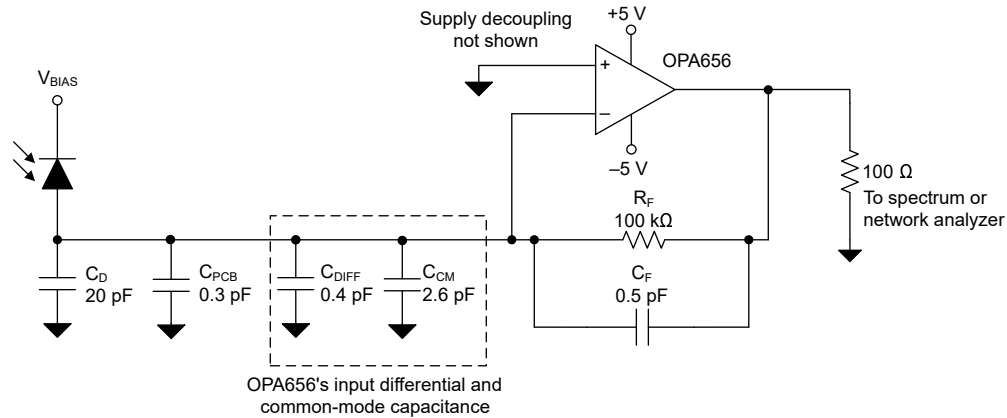
图 8-3. **Wideband, High-Sensitivity, Transimpedance Amplifier**

8.2.1 Design Requirements

Design a high-bandwidth, high-gain transimpedance amplifier with the design requirements shown in 表 8-1.

表 8-1. **Design Requirements**

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (K Ω)	PHOTODIODE CAPACITANCE (pF)
4	100	20

8.2.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA656. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_B) applied the desired transimpedance gain, R_F, and the GBP for the OPA656 (230 MHz). 图 8-3 shows a transimpedance circuit with the parameters as described in 表 8-1. With these three variables set (and including the parasitic input capacitance for the OPA656 and the PCB added to C_D), the feedback capacitor value (C_F) can be set to control the frequency response. To achieve a maximally-flat second-order Butterworth frequency response, set the feedback pole to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}}$$

(1)

The input capacitance of the amplifier is the sum of the common-mode and differential capacitance (0.4 + 2.6) pF. The parasitic capacitance from the photodiode package and the PCB is approximately 0.3 pF. These values result in a total effective input capacitance of C_D = 23.3 pF. From 方程式 1, set the feedback pole at 2.8 MHz. Setting the pole at 2.8 MHz requires a total feedback capacitance of 0.57 pF

The approximate −3-dB bandwidth of the transimpedance amplifier circuit is given by:

$$f_{-3dB} = \sqrt{GBP / (2\pi R_F C_D)} \text{ Hz}$$

(2)

方程式 2 estimates a closed-loop bandwidth of 3.96 MHz. The total feedback capacitance for the circuit used in the design is estimated to be 0.6 pF. The total feedback capacitance includes the physical 0.5 pF feedback capacitor in parallel with 100-fF of parasitic capacitance due to the feedback resistor and PCB trace. The parasitic capacitance from the PCB trace can be minimized by removing the ground and power planes in the feedback path. A TINA SPICE simulation of the circuit in 图 8-3 results in a closed-loop bandwidth of 4.2 MHz.

图 8-4 shows the measured output noise of the system. The low-frequency output noise of 40 nV/√Hz gets input-referred to 0.40 pA/√Hz. The transimpedance gain resistor is the dominant noise source with the operational amplifier contributing a negligible amount, reflecting one of the main benefits in using a JFET input amplifier in a high-gain transimpedance application. If the total output noise of the TIA is band limited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent output noise voltage can be derived by 方程式 3.

$$V_{OUTN} = \sqrt{(I_N R_F)^2 + 4kTR_F + E_N{}^2 + \frac{(E_N 2\pi C_D R_F F)^2}{3}}$$

(3)

where

- V_{OUTN} = Equivalent output noise when band-limited to F < 1 / (2 Ω RfCf)
- I_N = Input current noise for the operational amplifier inverting input
- E_N = Input voltage noise for the operational amplifier
- C_D = Diode capacitance including operational amplifier and PCB parasitic capacitance
- F = Band-limiting frequency in Hz (usually a postfilter before further signal processing)
- 4 kT = 1.6 e – 20 J at T = 290K

图 8-5 shows the frequency response of the design. The 4.2-MHz bandwidth of the circuit approximately matches the theoretical value calculated using 方程式 2.

8.2.3 Application Curves

图 8-4. Total TIA noise over frequency

图 8-5. Closed-Loop bandwidth of TIA
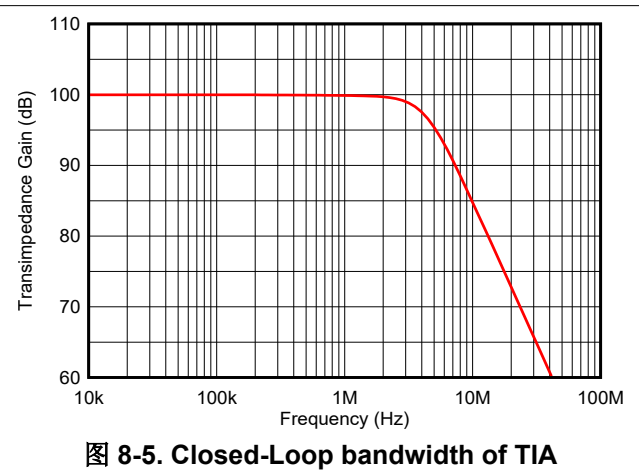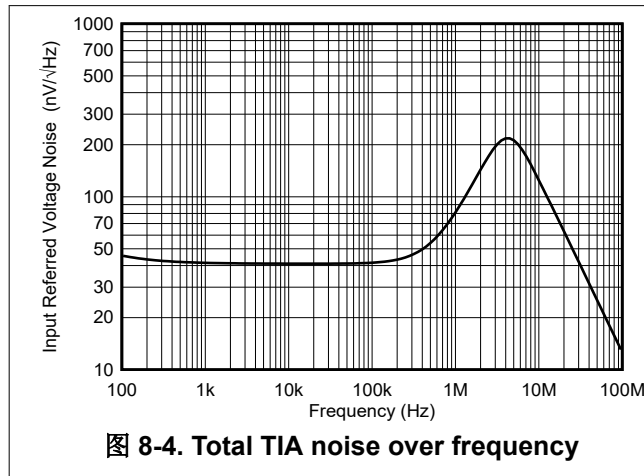
8.3 Power Supply Recommendations

The OPA656 is intended to operate on supplies ranging from 8 V to 12 V. The OPA656 supports single-supply, split, balanced, and unbalanced bipolar supplies. The limit to lower supply-voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply of 12 V can have numerous advantages. With the negative supply at ground, the dc errors due to the – PSRR term can be minimized. Typically, ac performance improves slightly at 12-V operation with a minimal increase in supply current.

Product Folder Links: *OPA656*

English Data Sheet: SBOS196

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA656 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following.

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. Ground and power metal planes act as one of the plates of a capacitor, while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, minimize the routing of the feedback network. A plane cutout around and underneath the inverting input pin on all ground and power planes is recommended. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

2. **Minimize the distance (less than 0.25 inches) from the power-supply pins to high-frequency decoupling capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G- and NPO-type decoupling capacitors. These capacitors must have voltage ratings at least three times greater than the amplifiers maximum power supplies to provide a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequencies, must be used on the supply pins. These larger capacitors can be placed further from the device and shared among several devices in the same area of the PCB.

3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA656.** Use low-reactance resistors. Small form-factor, surface-mount resistors work best and allow a tighter overall layout. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively.

   Place other network components, such as noninverting input termination resistors, close to the package. Even with a low parasitic capacitance at the noninverting input, high external resistor values can create significant time constants that can degrade performance. When the OPA656 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

8.4.1.1 Demonstration Fixtures

Two printed-circuit-boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA656 device in two package options. Both of these are offered as unpopulated PCBs, delivered with a user's guide. 表 8-2 shows the summary information for these fixtures.

表 8-2. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA656U	SO-8	DEM-OPA-SO-1A	SBOU009
OPA656N	SOT23-5	DEM-OPA-SOT-1A	SBOU010

Request the demonstration fixtures at the Texas Instruments website (www.ti.com) through the OPA656 product folder.

8.4.1.2 Thermal Considerations

The OPA656 does not require a heat sink or airflow in most applications. The following section describes how the maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

The operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}), and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the device. The P_{DL} depends on the required output signal and load, but for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced, bipolar supplies). Under this condition, $P_{DL} = V_S^2 / (4 \times R_L)$, where R_L includes feedback network loading.

Be aware that the power in the output stage, and not into the load, determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA656N (SOT23-5 package) in the circuit of 图 8-1 operating at the maximum specified ambient temperature of 85°C and driving a grounded 100-Ω load.

$$P_D = 10 \text{ V} \times 16.8 \text{ mA} + 5^2 / (4 \times (100 \ \Omega \ || \ 800 \ \Omega)) = 238 \text{ mW} \tag{4}$$

$$\text{Maximum } T_J = 85°C + (0.238 \text{ W} \times 154°C/W) = 121.6°C. \tag{5}$$

All actual applications operate at a lower internal power and junction temperature.

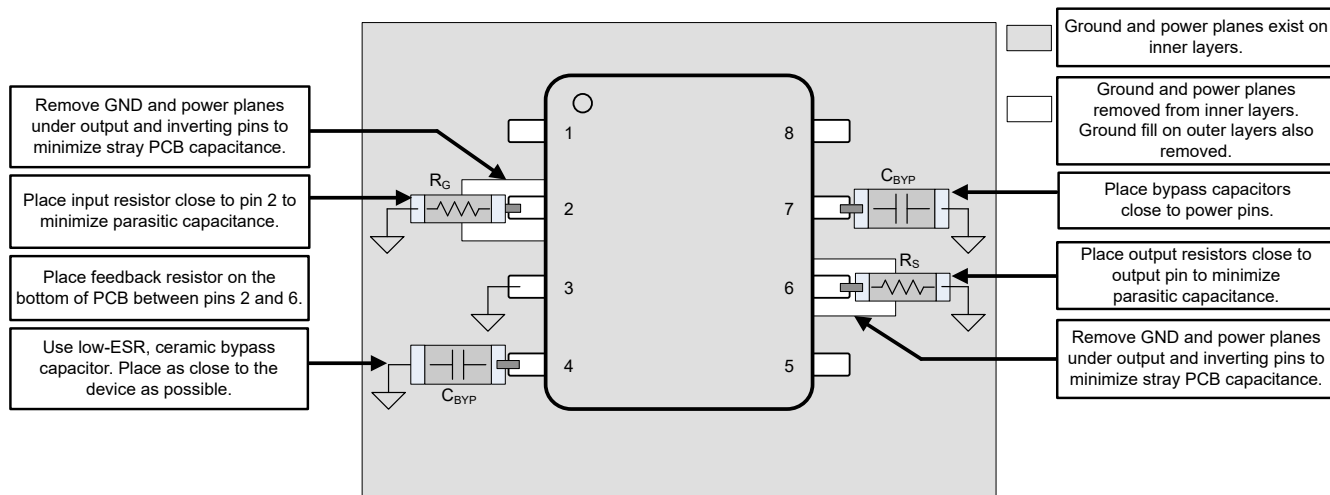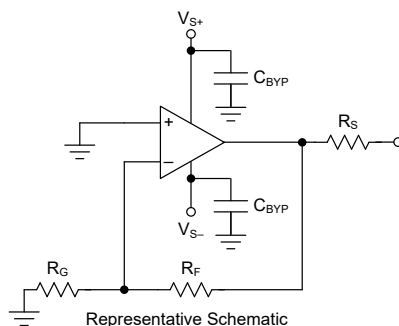### 8.4.2 Layout Example

Representative Schematic

图 **8-6. Layout Recommendation**

9 Device and Documentation Support

9.1 文档支持

9.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*高速放大器跨阻注意事项* 应用报告
- 德州仪器 (TI)，*光学前端系统参考设计*
- 德州仪器 (TI)，*更大限度扩展模拟 TIA 前端的动态范围* 技术简介
- 德州仪器 (TI)，*跨阻放大器须知 – 第 1 部分*
- 德州仪器 (TI)，*跨阻放大器须知 – 第 2 部分*
- 德州仪器 (TI)，*培训视频：如何设计跨阻放大器电路*
- 德州仪器 (TI)，*培训视频：高速跨阻放大器设计流程*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表   本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (November 2008) to Revision H (April 2015)   **Page**

Changes from Revision F (March 2006) to Revision G (November 2008)   **Page**

Changes from Revision E (March 2006) to Revision F (November 2008)   **Page**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA656N/250	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	B56
OPA656NB/250	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	B56
OPA656NB/250.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B56
OPA656U	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 656U
OPA656U/2K5	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 656U
OPA656UB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	OPA 656U B
OPA656UB/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	OPA (656U, B 656U) B
OPA656UB/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA (656U, B 656U) B
OPA656UB/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	OPA (656U, B 656U) B
OPA656UG4	NRND	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA656NB/250	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA656UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA656NB/250	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA656UB/2K5	SOIC	D	8	2500	353.0	353.0	32.0

C

SEATING PLANE

.004 [0.1] C

.228-.244   TYP
[5.80-6.19]

A

PIN 1 ID AREA

6X   .050
[1.27]

1

8

2X

.150
[3.81]

.189-.197
[4.81-5.00]
NOTE 3

4X (0°-15°)

4

5

8X .012-.020
[0.31-0.51]

.069 MAX
[1.75]

B

.150-.157
[3.81-3.98]
NOTE 4

⊕ .010 [0.25]Ⓜ C A B

.005-.010   TYP
[0.13-0.25]

4X (0°-15°)

SEE DETAIL A

.010
[0.25]

0°- 8°

.004-.010
[0.11-0.25]

.016-.050
[0.41-1.27]

(.041)
[1.04]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

4

5

6X (.050)
[1.27]

(R.002) TYP
[0.05]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

SYMM

1

8X (.024)
[0.6]

8

SYMM

6X (.050)
[1.27]

4

(R.002) TYP
[0.05]

5

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
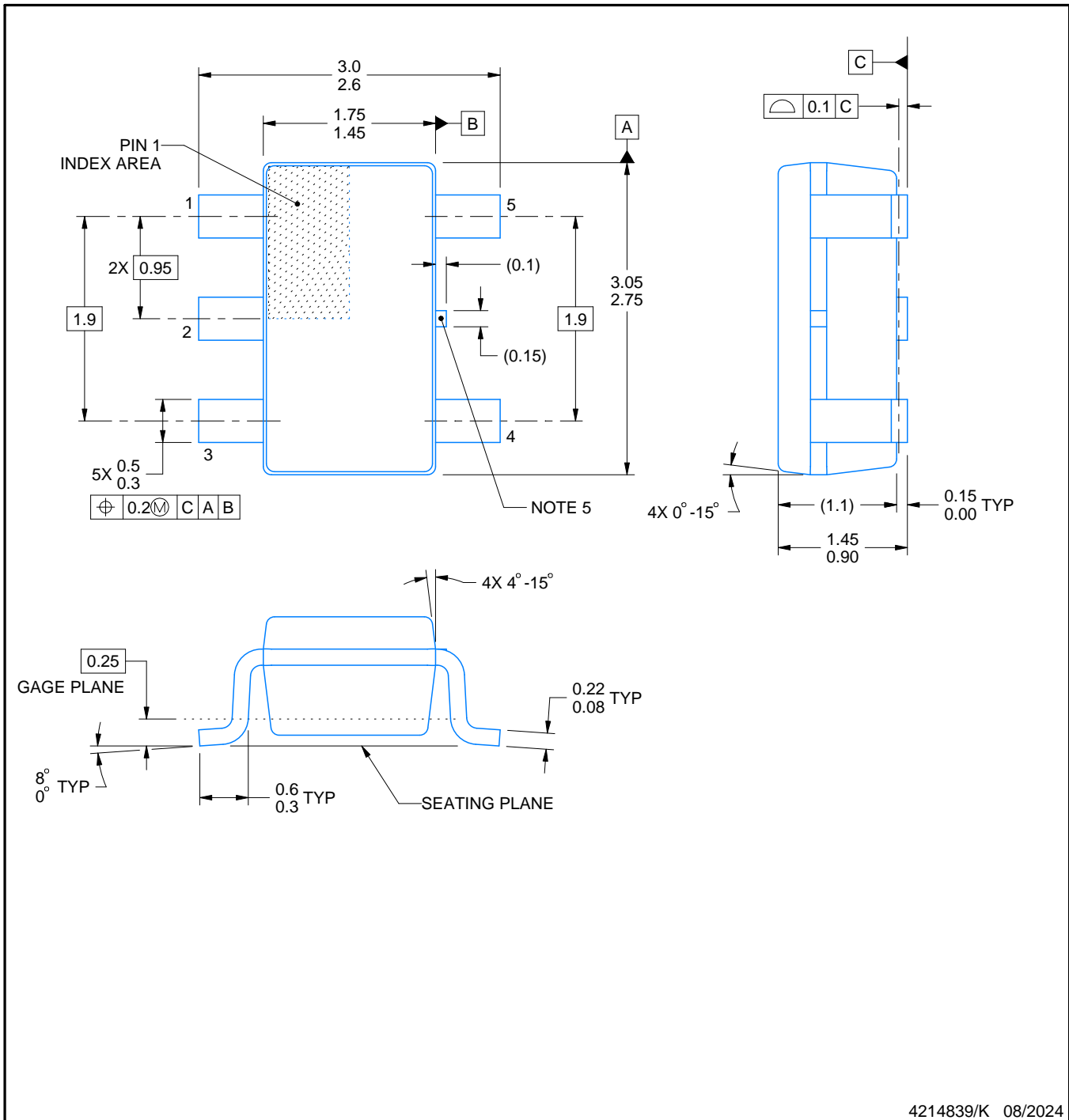SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX
ARROUND

0.07 MIN
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A

SOT-23 - 1.45 mm max height

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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