OPA462 高电压 (180V)、高电流 (30mA) 运算放大器

1 特性

- 宽电源电压范围：
  ±6V (12V) 至 ±90V (180V)
- 高输出负载驱动：I_O ±45mA
- 电流限制保护
- 过热保护
- 状态标志
- 独立输出禁用
- 增益带宽：6.5MHz
- 压摆率：32V/µs
- 宽温度范围：-40°C 至 +85°C
- 8 引脚 HSOIC (SO PowerPAD™) 封装

2 应用

- 半导体测试
- 光学模块
- 实验室和现场仪表
- 半导体制造
- 多参数患者监护仪
- PC 和笔记本电脑显示面板

3 说明

OPA462 是一款高电压 (180V) 和高电流驱动 (45mA) 的运算放大器。该器件的特点是单位增益稳定，且具有 6.5MHz 增益带宽积。

OPA462 在过热条件下以及电流过载时会受到内部保护。该器件完全可以在 ±6V 至 ±90V 的宽电源电压范围内工作或者由 12V 至 180V 的单电源供电工作。状态标志是漏极开路输出，使该器件可以将标准低压逻辑电路作为基准。该高电压运算放大器具有出色的精度与宽输出摆幅，而且不存在相似运算放大器中会出现的反相问题。

可以通过启用/禁用 (E/D) 引脚来禁用输出。E/D 引脚具有公共回路引脚，可轻松与低压逻辑电路连接。此类禁用可在不干扰输入信号路径的情况下实现，不仅省电，还能保护负载。

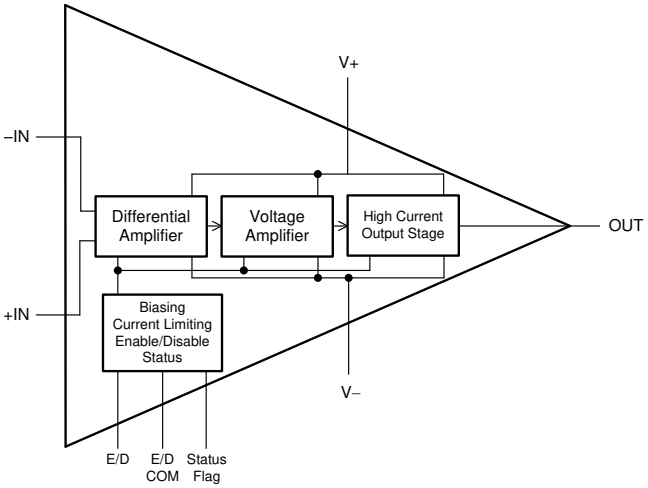
OPA462 采用小型暴露金属焊盘封装，在工业温度范围（–40°C 至 +85°C）内能够散热。

器件信息(1)

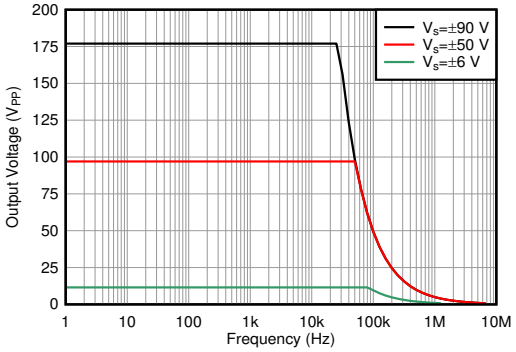
器件型号	封装	封装尺寸（标称值）
OPA462	HSOIC (8)	4.89mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

OPA462 方框图



最大输出电压与频率间的关系



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

4 修订历史记录

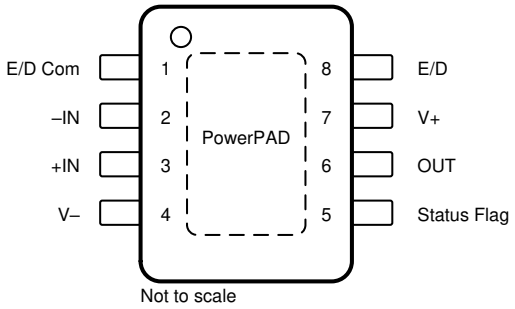
Changes from Original (December 2018) to Revision A **Page**

- 已更改 将 OPA462 从“预告信息（预发布）”更改为“生产数据（正在供货）” ... 1

版权 © 2018–2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

DDA PACKAGE
8-Pin SO PowerPAD™
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
E/D	8	I	Enable or disable
E/D Com	1	I	Enable and disable common
–IN	2	I	Inverting input
+IN	3	I	Noninverting input
OUT	6	O	Output
Status Flag	5	O	Status Flag is an open-drain active-low output referenced to E/D Com. This pin goes active for either an overcurrent or overtemperature condition.
V–	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply
PowerPAD	PowerPAD	—	The PowerPAD is internally connected to V–. The PowerPAD must be soldered to a printed-circuit board (PCB) connected to V–, even with applications that have low power dissipation.

Copyright © 2018–2019, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		190	V
+IN, –IN	Signal input pins(2)	(V–) – 0.3	(V+) + 0.3	V
	E/D to E/D Com		7	V
	All input pins(2)		±10	mA
	Output short circuit(3)	Continuous	Continuous	
T_A	Operating	–55	125	°C
T_J	Junction		150	°C
T_{STG}	Storage	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals, Status Flag, E/D, and E/D Com, and Output are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	±6		±90	V
T_A	Specified temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA462 DDA (HSOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2018–2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±90V R_L = 10 kΩ to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		I_O = 0 mA		±0.2	±3.4	mV
dV_{OS}/dT	Input offset voltage drift		At T_A = –40°C to +85°C		±4	±20	µV/°C
PSRR	Power supply rejection ratio		V_S = ±6 V to ±90 V		0.03	0.3	µV/V
			V_S = ±6 V to ±90 V At T_A = –40°C to +85°C		0.3	1.5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		V_S = ±50V		±30	±100	pA
			At T_A = –40°C to +85°C			±2.2	nA
I_{OS}	Input offset current				±30	±100	pA
			At T_A = –40°C to +85°C			±1.1	nA
NOISE							
e_n	Input voltage noise density		f = 1 kHz		33		nV/√Hz
			f = 10 kHz		23		nV/√Hz
	Input voltage noise		f = 0.1 Hz to 10 Hz		12.5		$µV_{PP}$
i_n	Current noise density		f = 1 kHz		40		fA/√Hz
			f = 10 kHz		450		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage		Linear operation	(V–) + 1		(V+) – 3	V
CMRR	Common-mode rejection	Common-mode rejection	–85 V ≤ V_{CM} ≤ 85 V	120	128		dB
CMRR	Common-mode rejection		–85 V ≤ V_{CM} ≤ 85 V At T_A = –40°C to +85°C	116	120		dB
INPUT IMPEDANCE							
	Differential				10^{13} || 6		Ω || pF
	Common-mode				10^{13} || 3.5		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		(V–) + 3 V < V_O < (V+) – 3 V	126	135		dB
			(V–) + 3 V < V_O < (V+) – 3 V At T_A = –40°C to +85°C	120	134		dB
			(V–) + 5 V < V_O < (V+) – 5 V, R_L = 5kΩ	126	135		dB
			(V–) + 5 V < V_O < (V+) – 5 V, R_L = 5kΩ At T_A = –40°C to +85°C	120	130		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		Small-signal		6.5		MHz
SR	Slew rate		G = ±1 V/V, V_O = 80-V step, R_L = 3.27 kΩ		32		V/µs
	Full-power bandwidth				25		kHz
t_S	Settling time		To ±0.01%, G = ±5 V/V or ±10 V/V, V_O = 120-V step		5.2		µs
THD+N	Total harmonic distortion + noise		G = +10 V/V, f = 1 kHz, V_O = 150 V_{PP}		0.0009		%
			G = +10 V/V, f = 1 kHz, V_O = 150 V_{PP}, R_L = 5 kΩ		0.0012		%
			G = +20 V/V, f = 1 kHz, V_O = 150 V_{PP}		0.0015		%
			G = +20 V/V, f = 1 kHz, V_O = 150 V_{PP}, R_L = 5 kΩ		0.0025		%

Copyright © 2018–2019, Texas Instruments Incorporated

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±90V R_L = 10 kΩ to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
	Overload recovery		G = –10 V/V		150		ns
V_O	Output voltage swing		R_L = 10 kΩ,	(V–) + 3		(V+) – 1.5	V
			R_L = 5 kΩ,	(V–) + 5		(V+) – 3	V
I_{SC}	Short-circuit current		V_S = ±45 V, At T_A = –40°C to +85°C		±45		mA
C_{LOAD}	Capacitive load drive				200		pF
Z_O	Open-loop output impedance		f = 1 MHz		90		Ω
	Output impedance		Output disabled		160		kΩ
	Output capacitance		Output disabled		36		pF
STATUS FLAG PIN (Referenced to E/D Com)							
	Status Flag delay		Enable → Disable, 10 kΩ pull-up to 5 V		3.5		µs
			Disable → Enable, 10 kΩ pull-up to 5V		11		µs
			Overcurrent delay, 10 kΩ pull-up to 5V		1		µs
			Overcurrent recovery delay, 10 kΩ pull-up to 5 V		9		µs
	Device thermal shutdown	Alarm (Status Flag high)			150		°C
		Return to normal operation (Status Flag low)			130		°C
	Status Flag output voltage		Normal operation		See typical curves		V
E/D (ENABLE/DISABLE) PIN							
V_{SD}	High (output enabled)		Pin open or forced high	E/D Com + 0.8		E/D Com + 5.5	V
	Low (output disabled)		Pin forced low	E/D Com		E/D Com + 0.35	V
	Output disable time				4		µs
	Output enable time				2.5		µs
E/D COM PIN							
	Pin voltage		V_S ≥ 106 V	(V–)		(V–) +100	V
			V_S < 106 V	(V–)		(V+) – 6	V
POWER SUPPLY							
I_Q	Quiescent current		I_O = 0 mA		3.2	3.7	mA
	Quiescent current in Shutdown mode		I_O = 0 mA, $V_{E/D}$ = 0.65 V		1.5	2	mA

版权 © 2018–2019, Texas Instruments Incorporated

6.6 Typical Characteristics: Table of Graphs

表 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution at 25°C	图 1
Offset Voltage Distribution at 85°C	图 2
Offset Voltage Distribution at -40°C	图 3
Offset Voltage Drift Distribution from -40°C to 85°C	图 4
Offset Voltage vs Temperature	图 5
Offset Voltage Warmup	图 6
Offset Voltage vs Common-Mode Voltage (Low Vcm)	图 7
Offset Voltage vs Common-Mode Voltage (High Vcm)	图 8
Offset Voltage vs Power Supply (Low Supply)	图 9
Offset Voltage vs Power Supply (High Supply)	图 10
Offset Voltage vs Output Voltage (Low Output)	图 11
Offset Voltage vs Output Voltage (High Output)	图 12
CMRR vs Temperature	图 13
CMRR vs Frequency	图 14
PSRR vs Temperature	图 15
PSRR vs Frequency	图 16
EMIRR vs Frequency	图 17
No Phase Reversal	图 18
Input Bias Current Production Distribution at 25℃	图 19
IB vs Temperature	图 20
IB vs Common-Mode Voltage	图 21
Enable Response	图 22
Current Limit Response	图 23
Open-Loop Gain vs Temperature	图 24
Open-Loop Gain vs Output Voltage	图 25
Open-Loop Gain and Phase vs Frequency	图 26
Open-Loop Output Impedance vs Frequency	图 27
Closed-Loop Gain vs Frequency	图 28
Maximum Output Voltage vs Frequency	图 29
Positive Output Voltage vs Output Current	图 30
Negative Output Voltage vs Output Current	图 31
Short-Circuit Current vs Temperature	图 32
Negative Overload Recovery	图 33
Positive Overload Recovery	图 34
Settling Time	图 35
Phase Margin vs Capacitive Load	图 36
Small-Signal Overshoot vs Capacitive Load (G = –1)	图 37
Small-Signal Overshoot vs Capacitive Load (G = +1)	图 38
Small-Signal Step Response (G = –1)	图 39
Small-Signal Step Response (G = +1)	图 40
Large-Signal Step Response (G = –1)	图 41
Large-Signal Step Response (G = +1)	图 42
Slew Rate vs Output Step Size	图 43
Slew Rate vs Supply Voltage (Inverting)	图 44
Slew Rate vs Supply Voltage (Noninverting)	图 45
THD+N Ratio vs Frequency (G = 10)	图 46

版权 © 2018–2019, Texas Instruments Incorporated

Typical Characteristics: Table of Graphs (接下页)

表 1. Table of Graphs (接下页)

DESCRIPTION	FIGURE
THD+N Ratio vs Frequency (G = 20)	图 47
THD+N Ratio vs Output Amplitude (G = 10)	图 48
THD+N Ratio vs Output Amplitude (G = 20)	图 49
0.1-Hz to 10-Hz Noise	图 50
Input Voltage Noise Spectral Density	图 51
Current Noise Density	图 52
Quiescent Current Production Distribution at 25℃	图 53
Quiescent Current vs Supply Voltage	图 54
Quiescent Current vs Temperature	图 55
Status Flag Voltage vs Temperature	图 56
Quiescent Current vs Enable Voltage	图 57
Enable Current vs Enable Voltage	图 58
Status Flag Current vs Voltage	图 59

版权 © 2018–2019, Texas Instruments Incorporated

6.7 Typical Characteristics

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

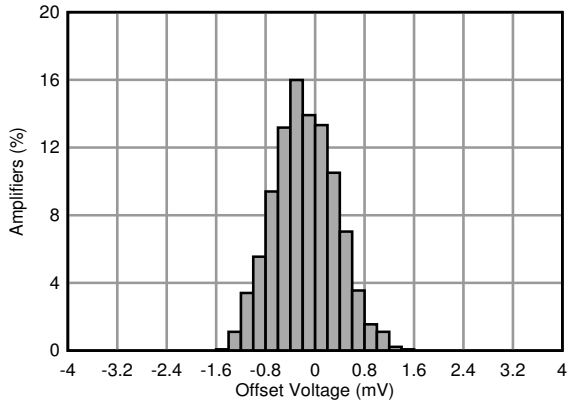


图 1. Offset Voltage Production Distribution at 25°C

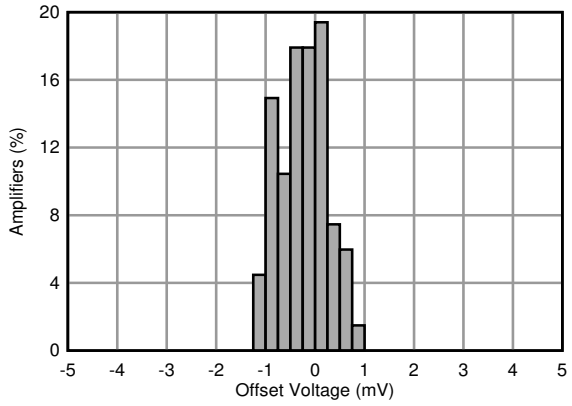


图 2. Offset Voltage Distribution at 85°C

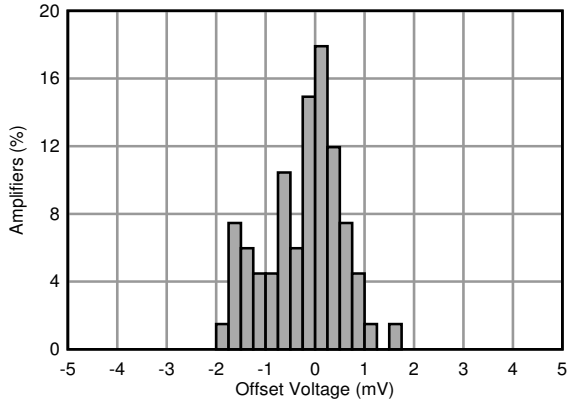


图 3. Offset Voltage Distribution at –40°C

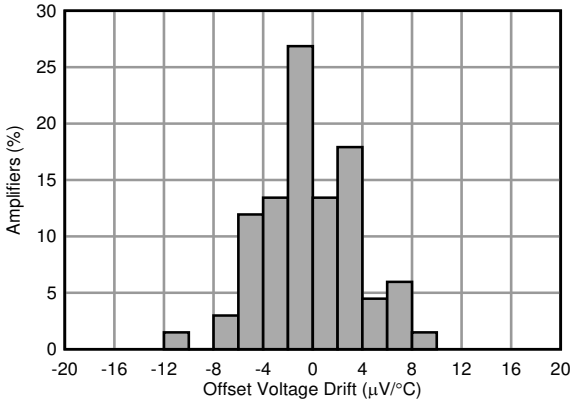


图 4. Offset Voltage Drift Distribution from –40°C to +85°C

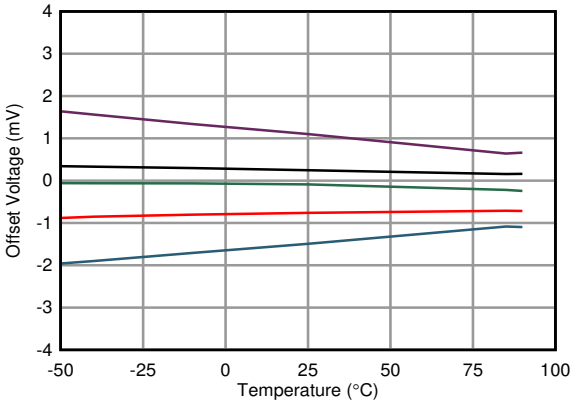


图 5. Offset Voltage vs Temperature

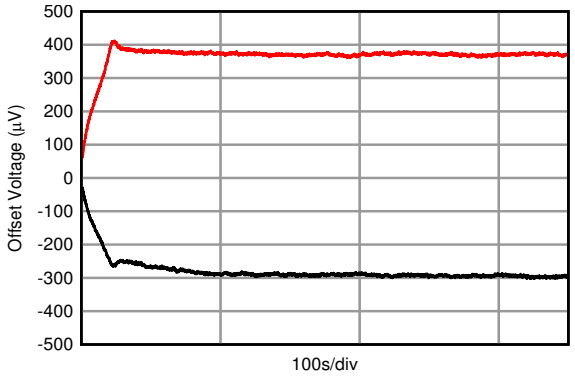


图 6. Offset Voltage Warmup

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

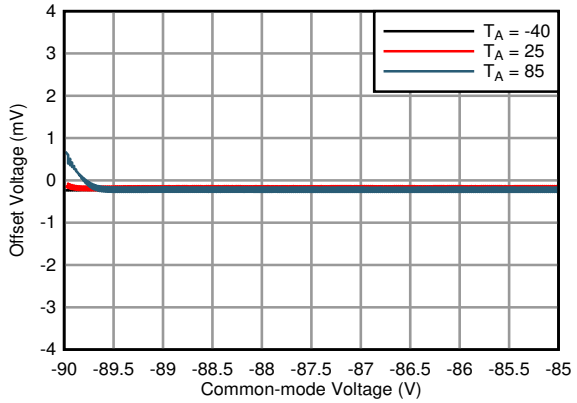


图 7. Offset Voltage vs Common-Mode Voltage (Low V_{CM})

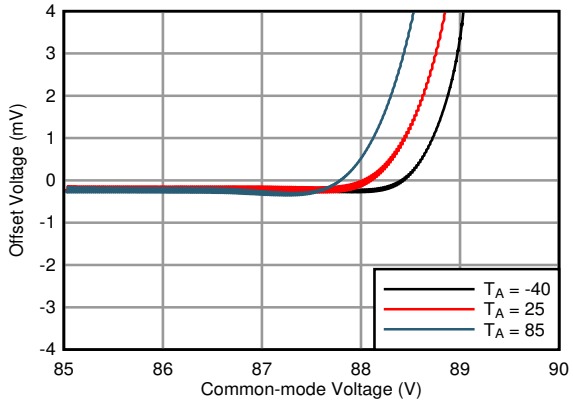


图 8. Offset Voltage vs Common-Mode Voltage (High V_{CM})

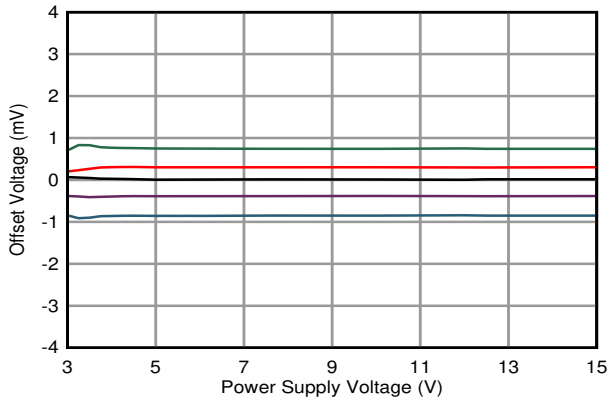


图 9. Offset Voltage vs Power Supply (Low Supply)

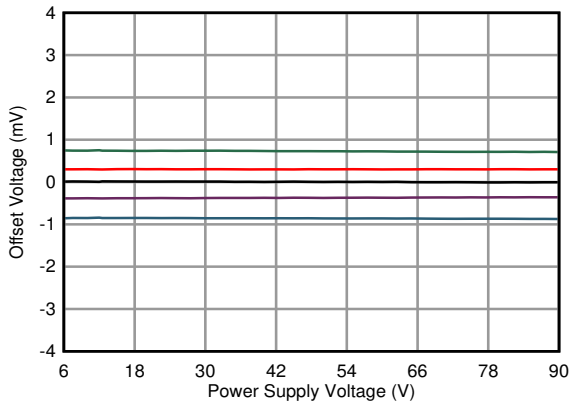


图 10. Offset Voltage vs Power Supply (High Supply)

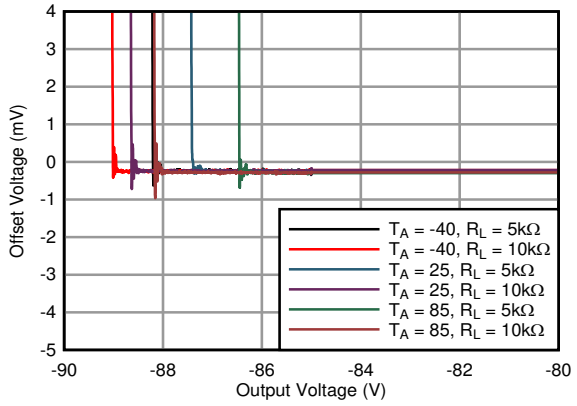


图 11. Offset Voltage vs Output Voltage (Low Output)

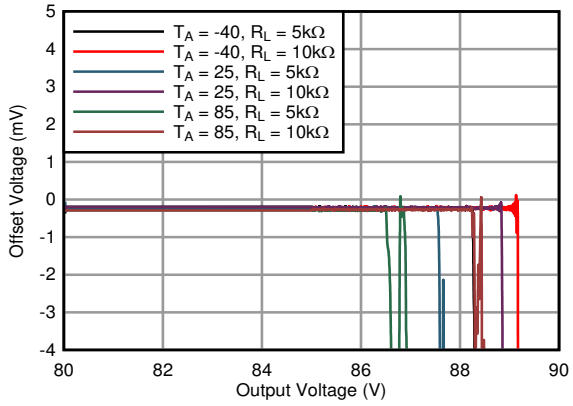


图 12. Offset Voltage vs Output Voltage (High Output)

版权 © 2018–2019, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

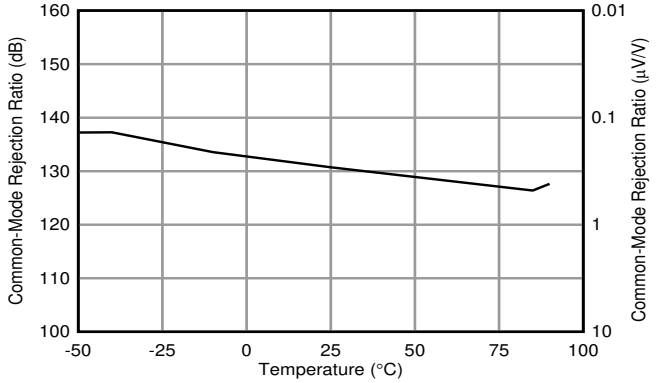


图 13. CMRR vs Temperature

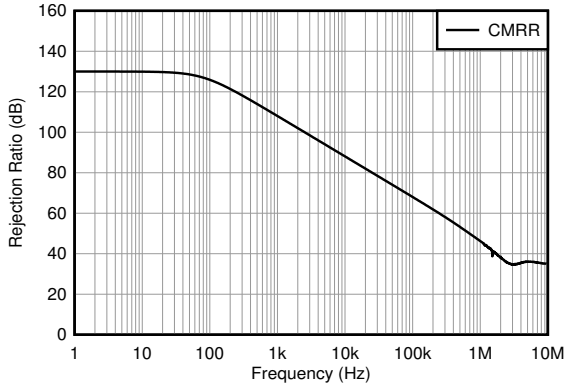


图 14. CMRR vs Frequency

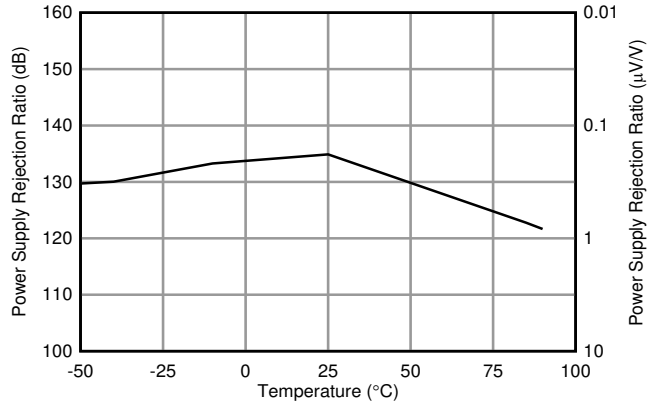


图 15. PSRR vs Temperature

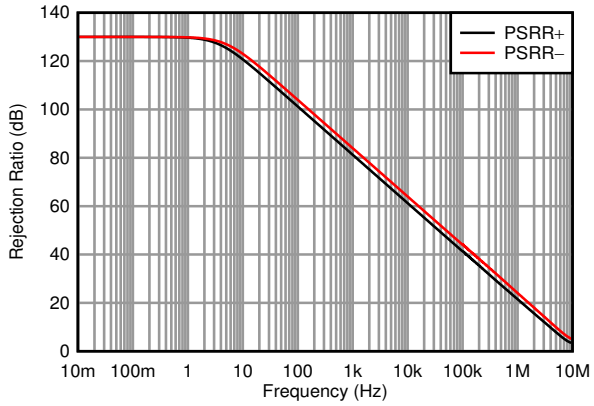


图 16. PSRR vs Frequency

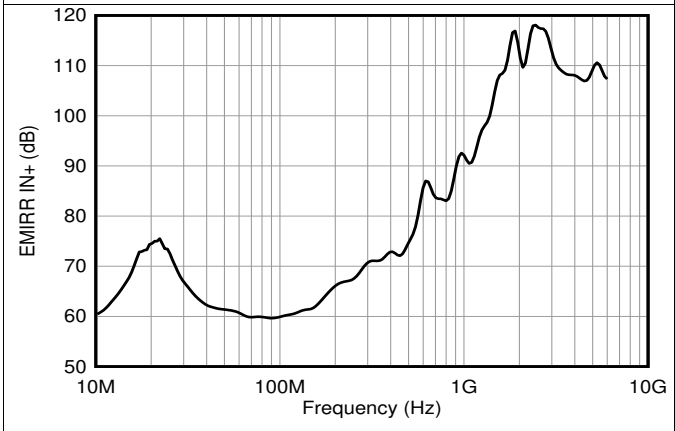


图 17. EMIRR vs Frequency

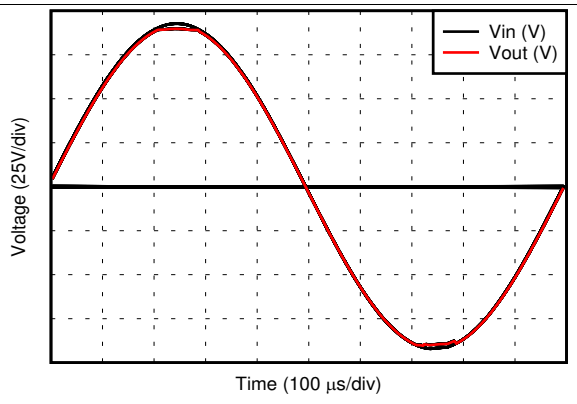


图 18. No Phase Reversal

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

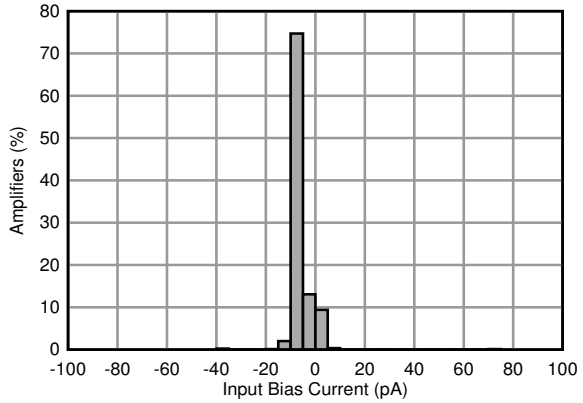


图 19. Input Bias Current Production Distribution at 25℃

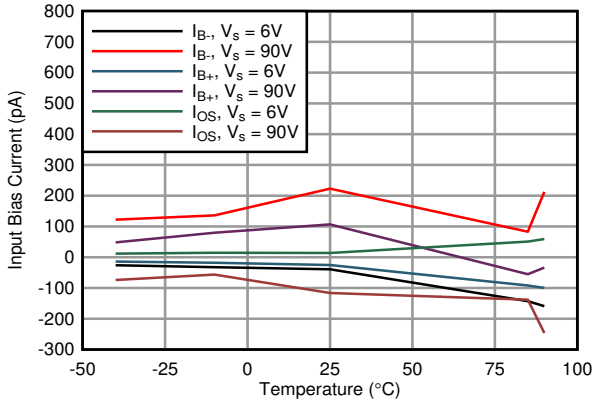


图 20. IB vs Temperature

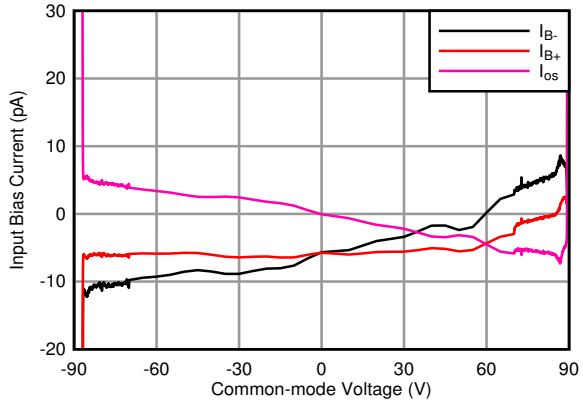


图 21. IB vs Common-Mode Voltage

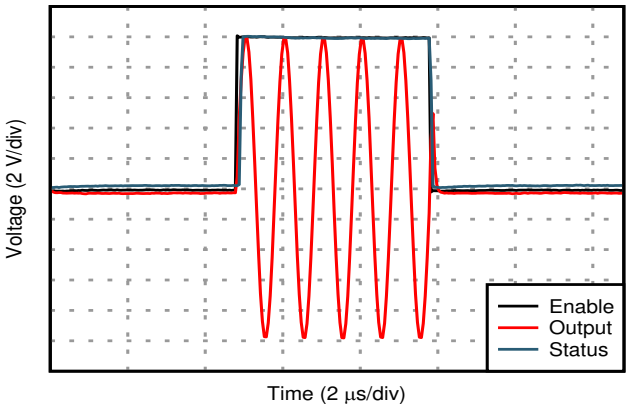


图 22. Enable Response

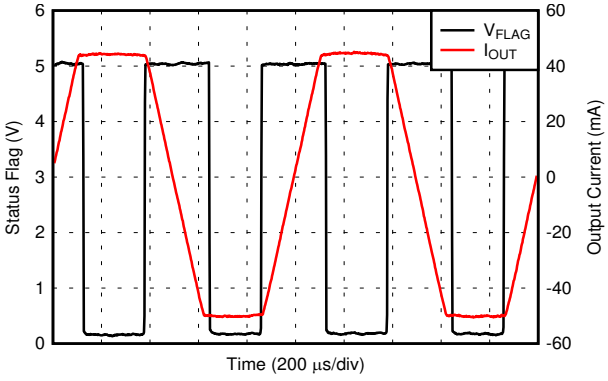


图 23. Current Limit Response

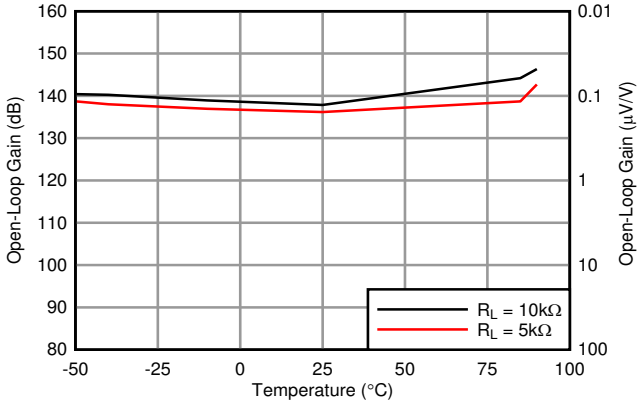


图 24. Open-Loop Gain vs Temperature

版权 © 2018–2019, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

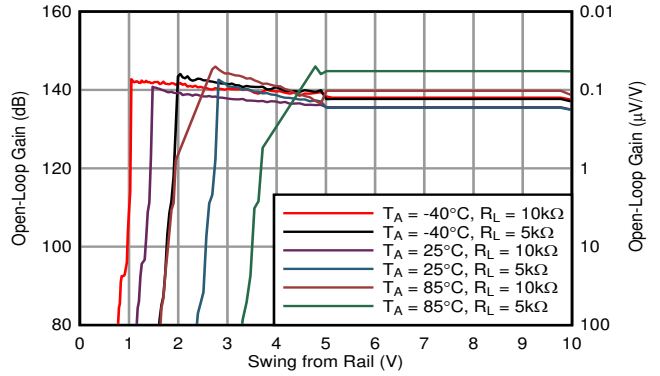


图 25. Open-Loop Gain vs Output Voltage

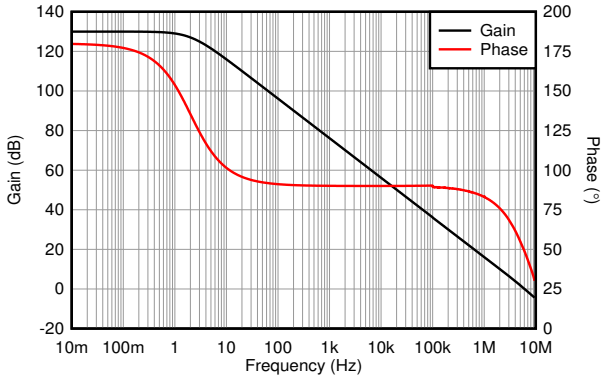


图 26. Open-Loop Gain and Phase vs Frequency

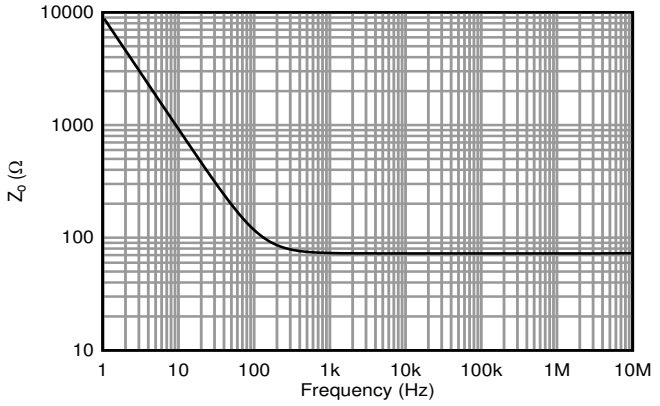


图 27. Open-Loop Output Impedance vs Frequency

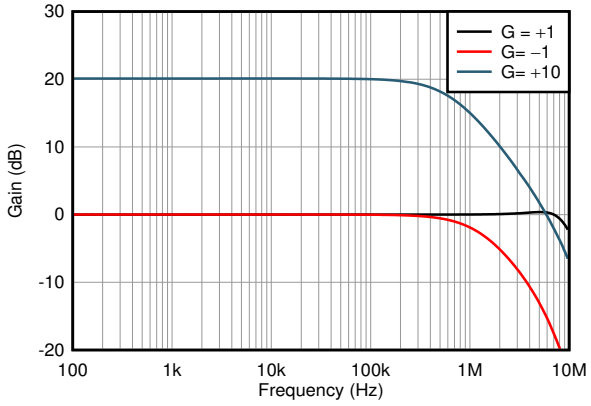


图 28. Closed-Loop Gain vs Frequency

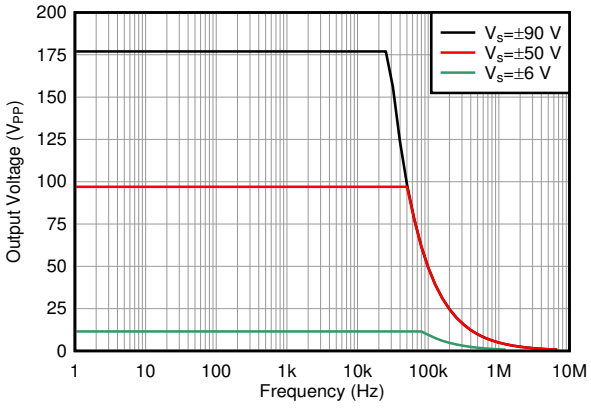


图 29. Maximum Output Voltage vs Frequency

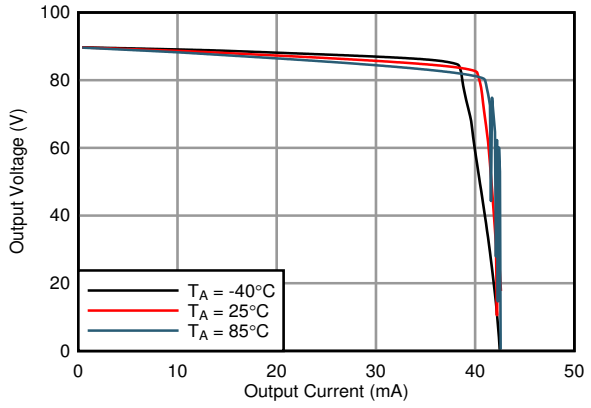


图 30. Positive Output Voltage vs Output Current

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

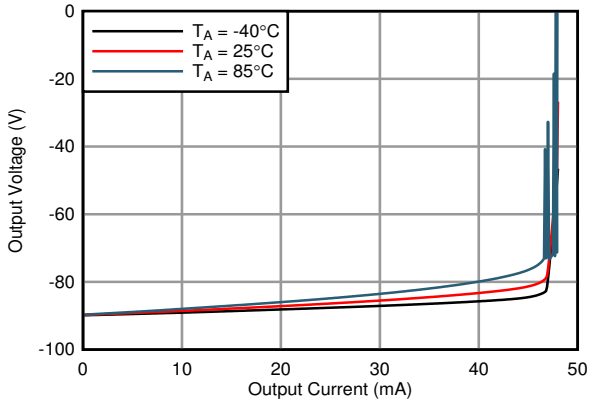


图 31. Negative Output Voltage vs Output Current

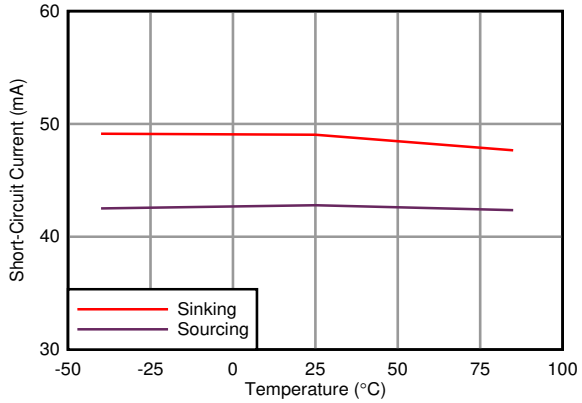


图 32. Short-Circuit Current vs Temperature

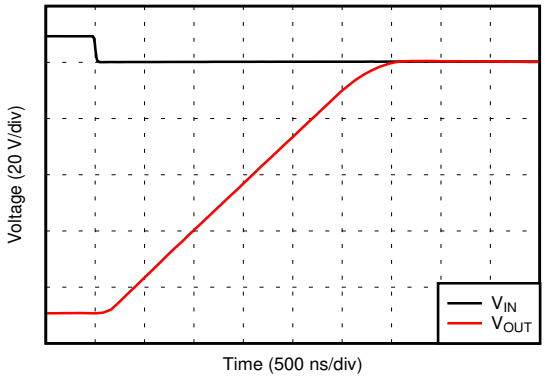


图 33. Negative Overload Recovery

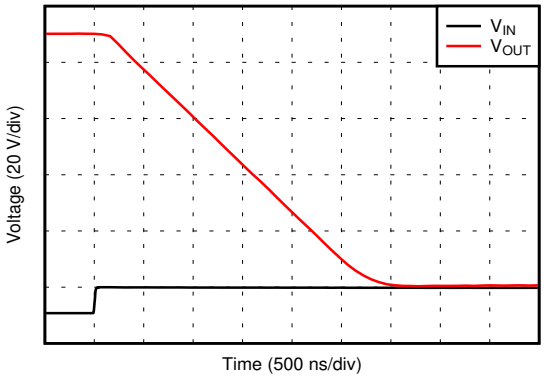


图 34. Positive Overload Recovery

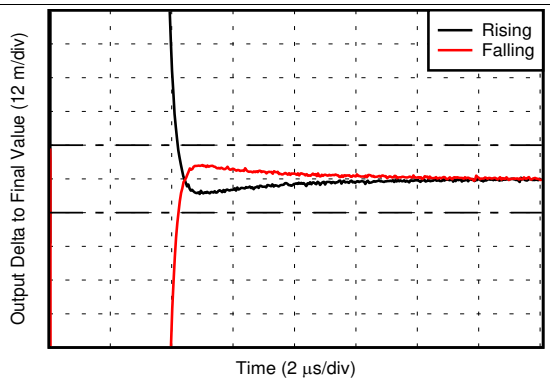


图 35. Settling Time

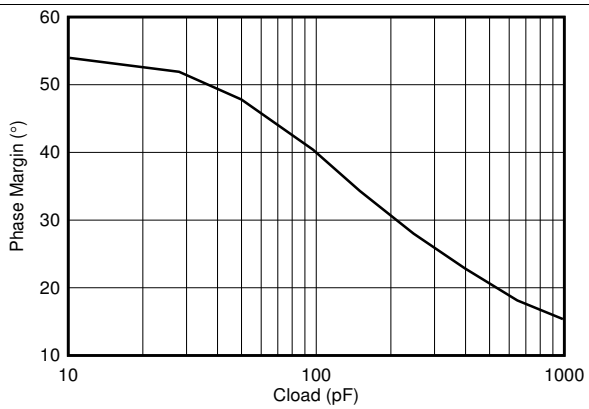
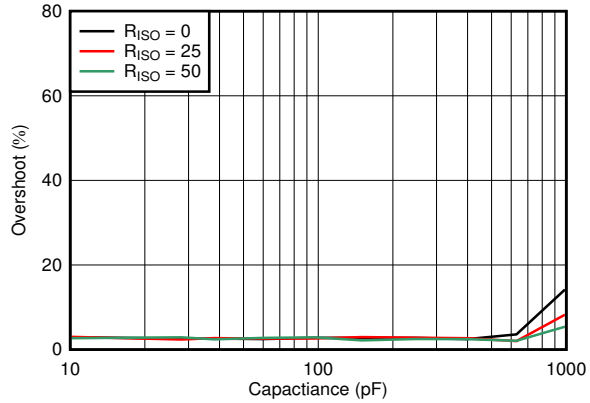


图 36. Phase Margin vs Capacitive Load

版权 © 2018–2019, Texas Instruments Incorporated

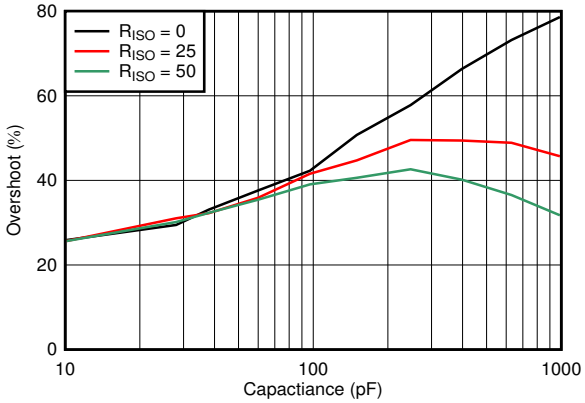
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)



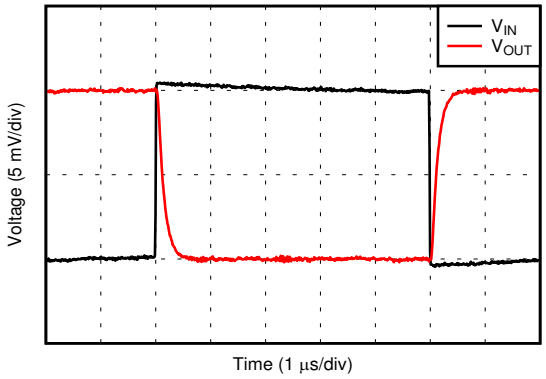
G = –1

图 37. Small-Signal Overshoot vs Capacitive Load



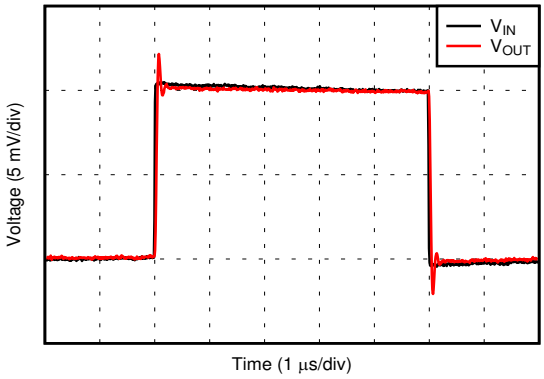
G = +1

图 38. Small-Signal Overshoot vs Capacitive Load



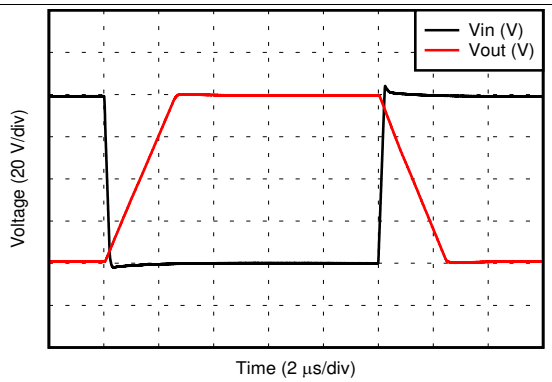
G = –1

图 39. Small-Signal Step Response



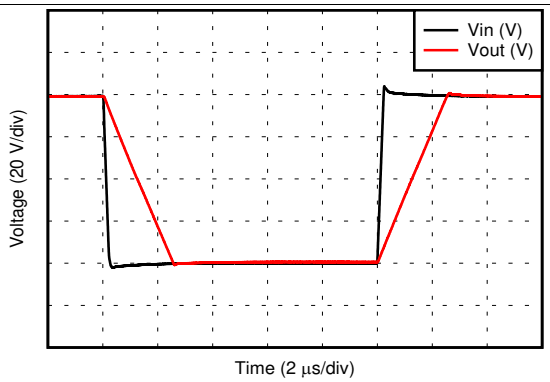
G = +1

图 40. Small-Signal Step Response



G = –1

图 41. Large-Signal Step Response



G = +1

图 42. Large-Signal Step Response

版权 © 2018–2019, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

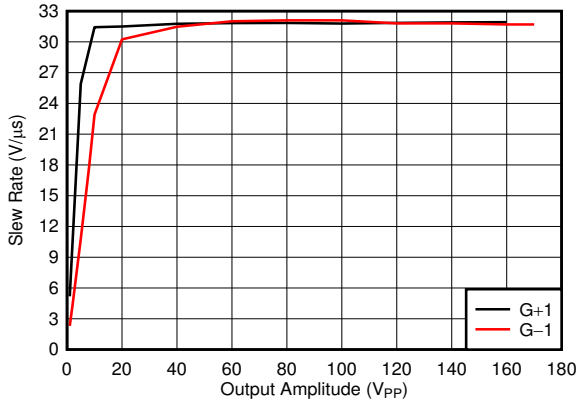


图 43. Slew Rate vs Output Step Size

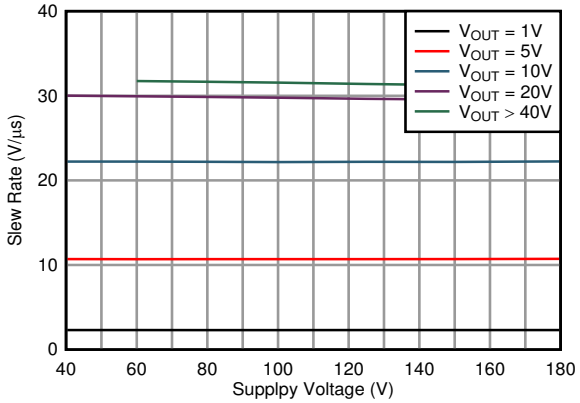


图 44. Slew Rate vs Supply Voltage (Inverting)

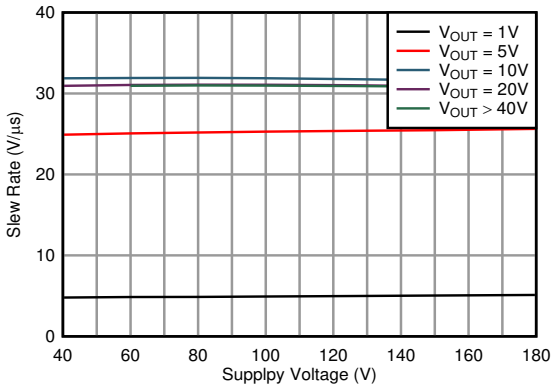


图 45. Slew Rate vs Supply Voltage (Noninverting)

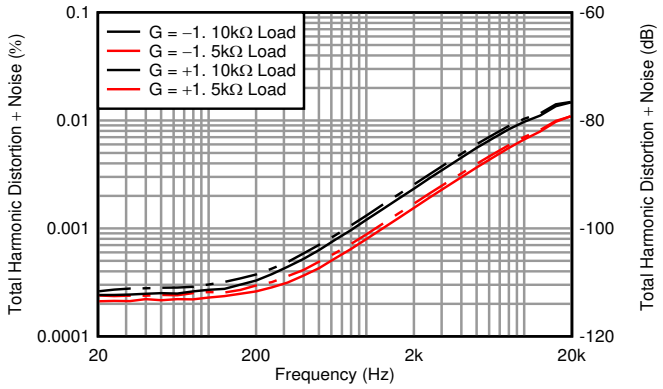


图 46. THD+N Ratio vs Frequency

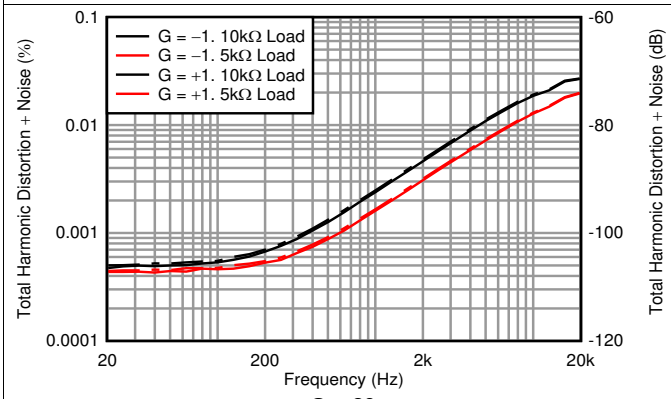


图 47. THD+N Ratio vs Frequency

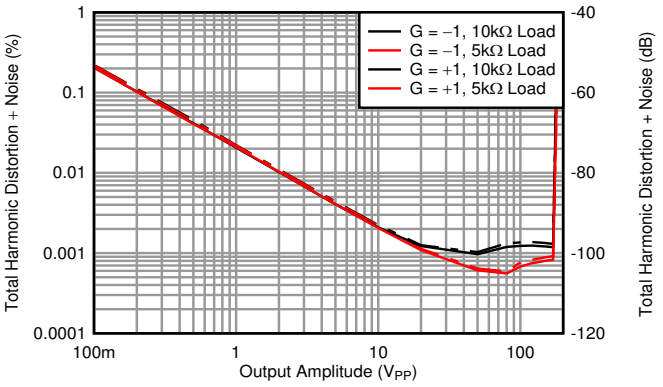


图 48. THD+N Ratio vs Output Amplitude

版权 © 2018–2019, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

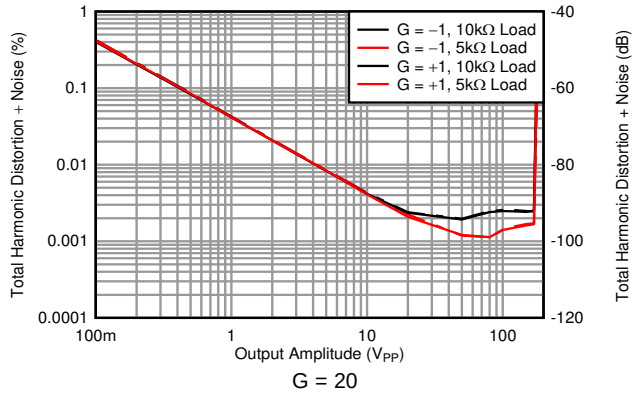


图 49. THD+N Ratio vs Output Amplitude

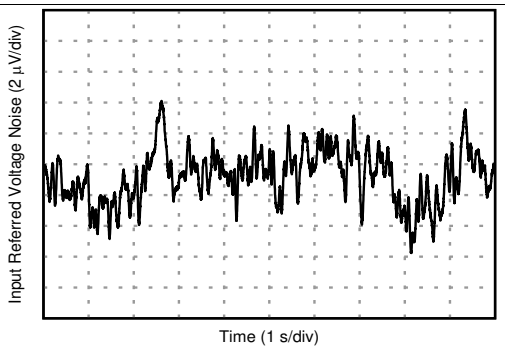


图 50. 0.1-Hz to 10-Hz Noise

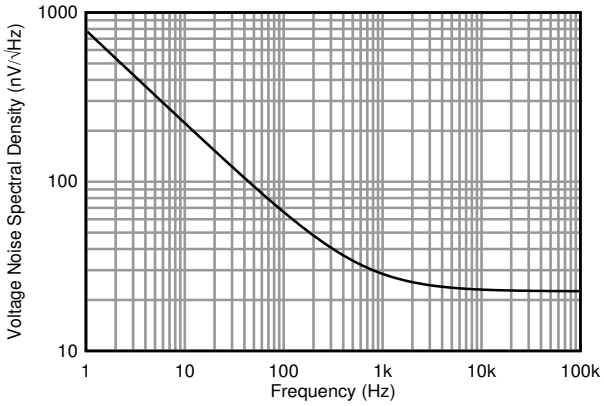


图 51. Input Voltage Noise Spectral Density

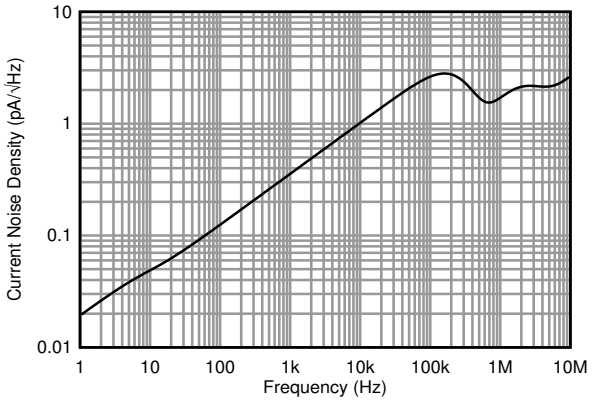


图 52. Current Noise Density

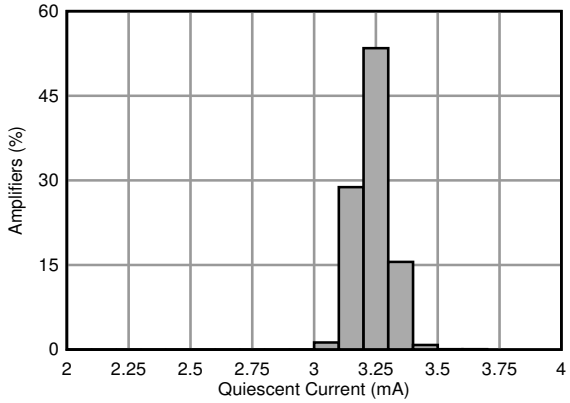


图 53. Quiescent Current Production Distribution at 25℃

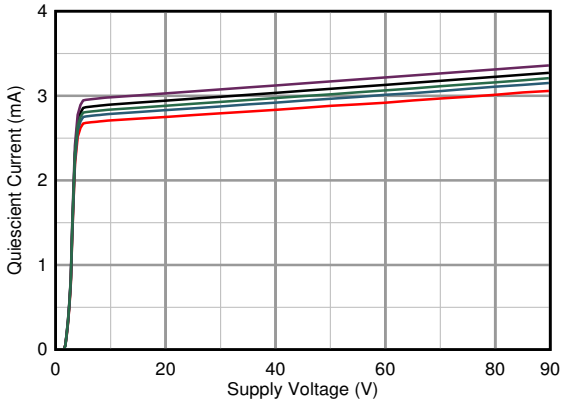


图 54. Quiescent Current vs Supply Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled (unless otherwise noted)

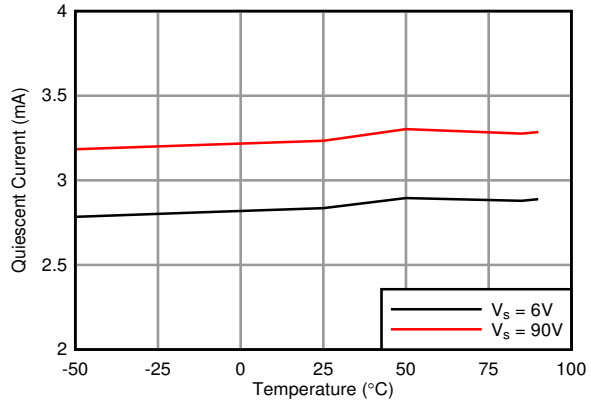


图 55. Quiescent Current vs Temperature

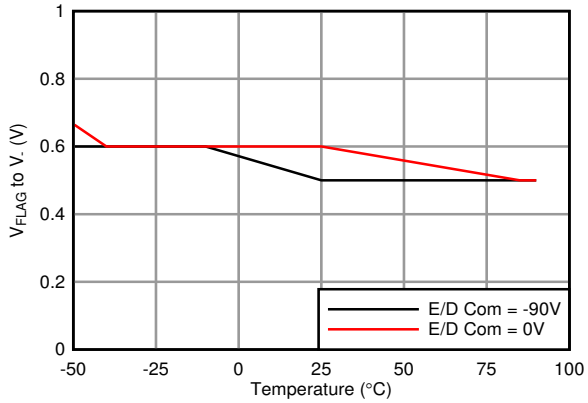


图 56. Status Flag Voltage vs Temperature

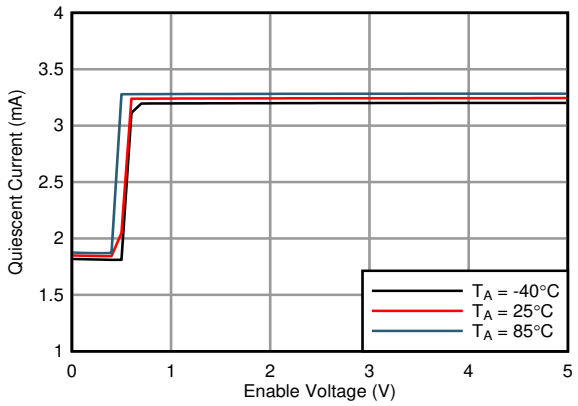


图 57. Quiescent Current vs Enable Voltage

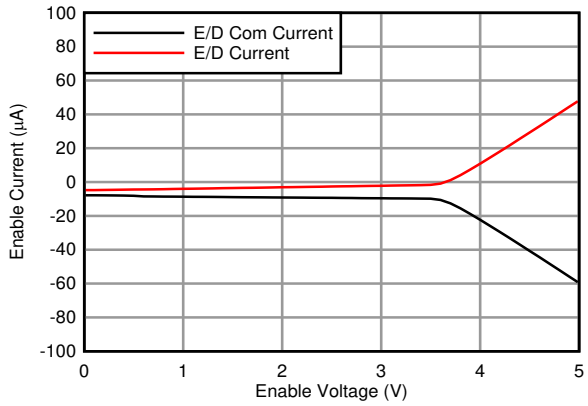


图 58. Enable Current vs Enable Voltage

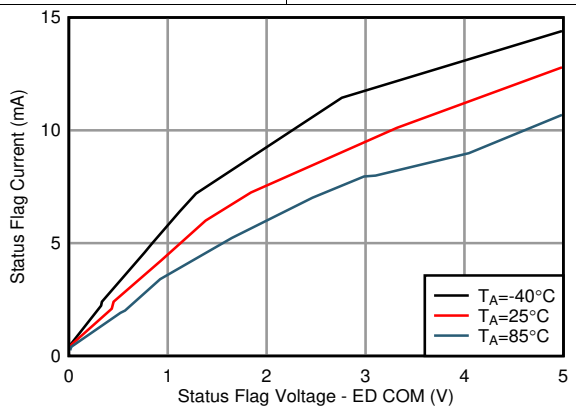


图 59. Status Flag Current vs Voltage

版权 © 2018–2019, Texas Instruments Incorporated

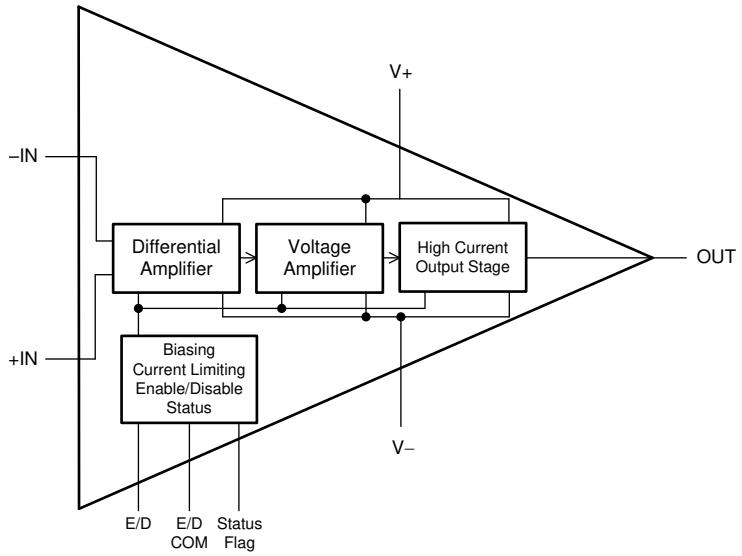
7 Detailed Description

7.1 Overview

The OPA462 is an operational amplifier (op amp) with high voltage of 180 V, and a high current drive of 30 mA. This device is unity-gain stable and features a gain-bandwidth product of 6.5 MHz. The high-voltage OPA462 offers excellent accuracy and wide output swing, and has no phase inversion problems that are typically found in similar op amps. The device can be applied in many common op amp configurations requiring a supply voltage range from ±6-V to ±90-V.

The OPA462 features an enable-disable function that provides the ability to turn off the output stage and reduce power consumption when not being used. The device also features a Status Flag pin that indicates an overtemperature or overcurrent fault conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Status Flag Pin

The Status Flag pin indicates fault conditions and can be used in conjunction with the enable-disable function to implement fault control loops. This pin is triggered when the device enters an overtemperature or overcurrent fault condition.

7.3.2 Thermal Protection

The OPA462 features internal thermal protection that is triggered when the junction temperature is greater than 150°C. When the protection circuit is triggered, thermal shutdown occurs to allow the junction to return a safe operating temperature. Thermal shutdown enables the Status Flag pin, which indicates the device has entered the thermal shutdown state.

7.3.3 Current Limit

Current limiting is accomplished by internally limiting the drive to the output transistors. The output can supply the limited current continuously, unless the die temperature rises to 150°C, which initiates thermal shutdown. With adequate heat dissipation, and use of the lowest possible supply voltage, the OPA462 can remain in current limit continuously without entering thermal shutdown. The best practice is to provide proper heat dissipation (either by a physical plate or by airflow) to remain well below the thermal shutdown threshold. For longest operational life of the device, keep the junction temperature below 125°C.

版权 © 2018–2019, Texas Instruments Incorporated

Feature Description (接下页)

7.3.4 Enable and Disable

If left disconnected, E/D Com is pulled near V– (negative supply) by an internal 10-µA current source. When left floating, E/D is held approximately 2 V above E/D Com by an internal 1-µA source. Even though active operation of the OPA462 results when the E/D and E/D Com pins are not connected, a moderately fast, negative-going signal capacitively coupled to the E/D pin can overpower the 1-µA pullup current and cause device shutdown. This behavior can appear as an oscillation and is encountered first near extreme cold temperatures. If the enable function is not used, a conservative approach is to connect E/D through a 30-pF capacitor to a low impedance source. Another alternative is the connection of an external current source from V+ (positive supply) sufficient to hold the enable level above the shutdown threshold. 图 60 shows a circuit that connects E/D and E/D Com. The E/D Com pin is limited to (V–) + 100 V to enable the use of digital ground in a application where the OPA462 power supply is ±90 V.

When the E/D pin is dropped to a voltage between 0 V and 0.65 V above the E/D Com pin voltage the output of the OPA462 will become disabled. While in this state the impedance of the output increases to approximately 160 kΩ. Because the inputs are still active, an input signal might be passed to the output of the amplifier. The voltage at the amplifier output is reduced because of a drop across this output impedance, and may appear distorted compared to a normal operation output.

After the E/D pin voltage is raised to a voltage between 2.5 V and 5 V greater than the E/D Com, the output impedance returns to a normal state and the amplifier operates normally.

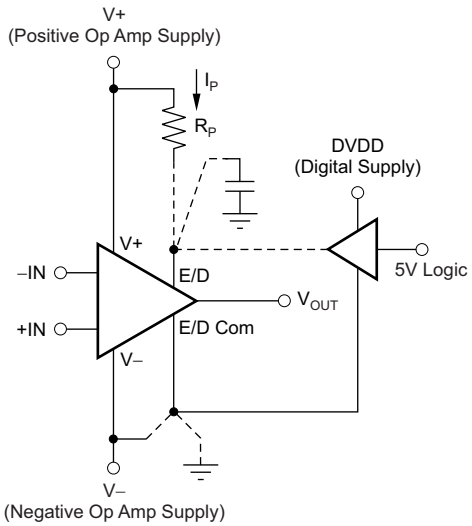


图 60. E/D and E/D Com

7.4 Device Functional Modes

A unique mode of the OPA462 is the output disable capability. This function conserves power during idle periods (quiescent current drops to approximately 1 mA). This disable is accomplished without disturbing the input signal path, not only saving power but also protecting the load. This feature makes disable useful for implementing external fault shutdown loops.

版权 © 2018–2019, Texas Instruments Incorporated

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA462 is a high-voltage, high-current operational amplifier capable of operating with supply voltages as high as ±90 V (180 V), or as low as ±6 V (12 V). The high-voltage process and design of the OPA462 allows the device to be used in applications where most operational amplifiers cannot be applied, such as high-voltage power-supply conditions, or when there is a need for very a high-output voltage swing. The output is capable of delivering up to ±30 mA output current, or swinging within a few volts of the supply rails at moderate current levels. The OPA462 features input overvoltage protection, output current limiting, thermal protection, a status flag, and enable-disable capability.

8.2 Typical Applications

8.2.1 High DAC Gain Stage for Semiconductor Test Equipment

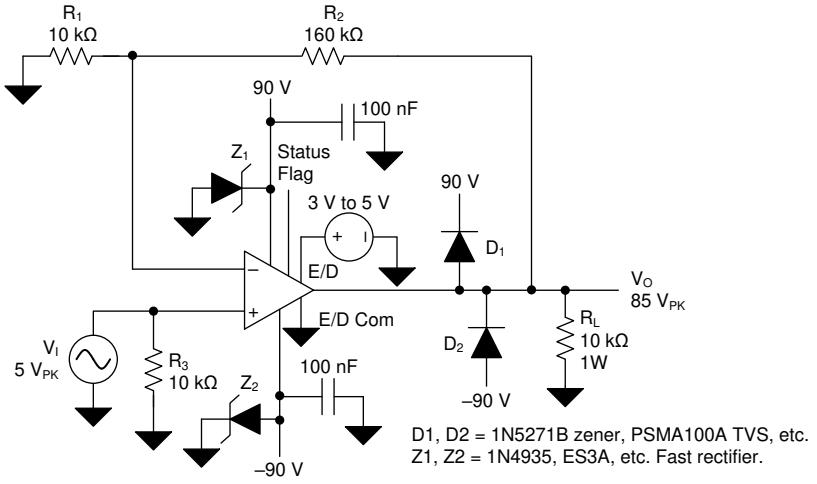


图 61. OPA462, High-Voltage Noninverting Amplifier, A_V = 17 V/V

8.2.1.1 Design Requirements

The OPA462 high-voltage op amp can be used in commonly applied op amp circuits, but with the added capability of allowing for the use of much higher supply voltages. A very common application of an op amp is that of a noninverting amplifier with a gain of 1 V/V or higher. 图 61 shows the OPA462 in a noninverting configuration.

The design goals for this circuit are:

- A noninverting gain of 17 V/V (24.6 dB)
- A peak output voltage of 85 V, while driving a 10 kΩ output load
- Correct biasing of E/D and E/D Com
- Protection against back electromagnetic force (EMF)

Typical Applications (接下页)

8.2.1.2 Detailed Design Procedure

图 61 shows a noninverting circuit with a moderately high closed-loop gain (A_V) of 17 V/V (24.6 dB). In this example, a 5-V_{PK} ac signal is amplified to 85 V_{PK} across a 10-kΩ load resistor connected to the output. The peak current for this application is 8.5 mA, and is well within the OPA462 output current capability. Higher output current, typically up to 30 mA, may be attained at the expense of the output swing to the supply rails. A ±90-V_{DC} power supply is required for this configuration.

The noninverting amplifier circuit shows the OPA462 enable-disable function. When placed in disabled mode the op amp becomes nonfunctional, and the current consumption is reduced to approximately one-third to one-half the enabled level. An enable active state occurs when the E/D pin is left open, or is biased 3 V to 5 V greater than the E/D Com voltage level. If biased between the E/D com level, to E/D Com + 0.65 V, the OPA462 disables. More information about this function is provided in the *Enable and Disable* section.

Op amps designed for high-voltage and high-power applications may encounter output loads that can be quite different than those used in low-voltage, non-power op amp applications. Although every effort is made to make a high-voltage op amp such as the OPA462 robust and tolerant of different supply and different output load conditions, some loads can present potentially harmful circumstances.

Purely resistive output loads operating within the current capability range of the OPA462 do not present an unsafe condition, provided the thermal requirements discussed in the *Layout* section. Complex loads that have inductive or capacitive reactive elements might present an unsafe condition, and must be fully considered and addressed before implementation.

A potentially destructive mechanism is the back EMF transient that can be generated when driving an inductive load. D_1, D_2, Z_1 and Z_2 in 图 61 have been added to the basic OPA462 amplifier circuit to provide protection in the event of back EMF. If the voltage at the OPA462 output attempts to momentarily rise above V+, D_1 becomes forward-biased and clamps the voltage between the output and V+ pins. This clamp must be sufficient to protect the OPA462 output transistor. If the event causes the V+ voltage to increase the power supply bypass capacitor, Z_1, or both, a Zener diode or a transient voltage suppressor (TVS) can provide a path for the transient current to ground. D_2 and Z_2 provide the same protection in the negative supply circuit.

The OPA462 noninverting amplifier circuit with a closed-loop gain of 17 V/V has a small-signal, –3-dB bandwidth of nearly 800 kHz. However, the large-signal bandwidth is likely of greater importance in a high-output-voltage application. For that mode of operation, the slew rate of the op amp and the peak output swing voltage must be considered in order to determine the maximum large-signal bandwidth. The slew rate (SR) of the OPA462 is typically 6.5 V/µs, or 6.5 × 10^6 V/s. Using the 85-V_{PK} output voltage available from the circuit in 图 61, the maximum large-signal bandwidth is calculated from the slew rate formula. 公式 1, 公式 2 and 公式 3 show the calculation process.

$$SR = 2\Pi \times f_{MAX} \times V_{PK} \tag{1}$$

$$f_{MAX} = SR / (2\Pi \times V_{PK}) \tag{2}$$

$$f_{MAX} = 6.5 \times 10^6 \text{ V/s} / (2\Pi / 85 \text{ V}) = 12 \text{ kHz}$$

where

- SR = 6.5 × 10^6 V/s
- V_{PK} = 85 V (3)

The best practice for a typical parameter such as slew rate to allow for variance. In this example, keeping the large signal f_{MAX} to 10 kHz is sufficient to make sure the output avoids slew rate limiting.

版权 © 2018–2019, Texas Instruments Incorporated

Typical Applications (接下页)

8.2.1.3 Application Curve

图 62 shows the OPA462 85-V_{PK} output produced from a 5-V_{PK}, 10-kHz sine input. The results were obtained from a TINA-TI simulation.

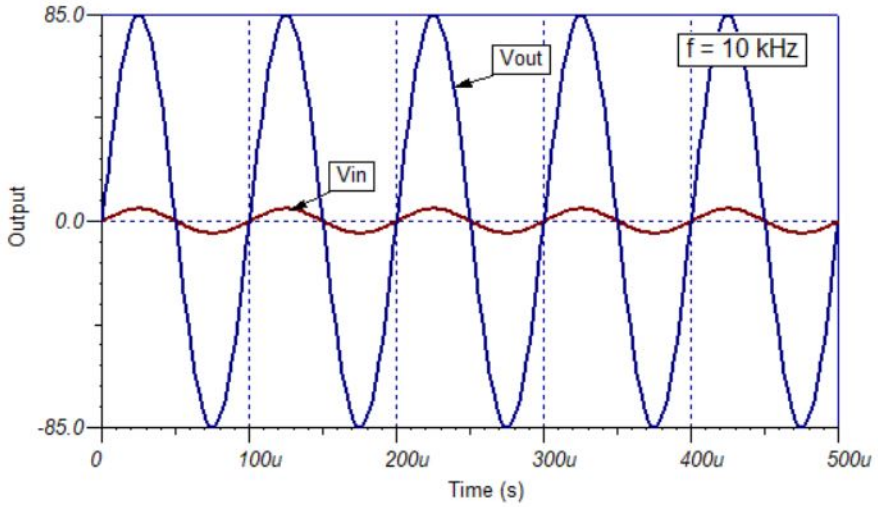


图 62. OPA462 Large-Signal Output With a 10-kHz Sine Input From a TINA-TI Simulation

8.2.2 Improved Howland Current Pump for Bioimpedance Measurements in Multiparameter Patient Monitors

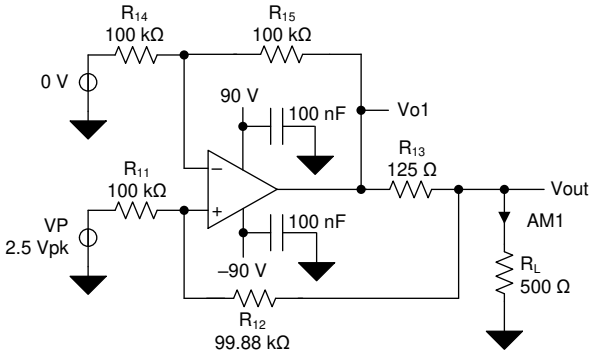


图 63. High-Voltage, 20-mA, Improved Howland Current Pump

8.2.2.1 Design Requirements

The OPA462 can be used to create a high-voltage, improved Howland current pump that provides a constant output current proportional to a single or differential input voltage applied to the pump inputs. The improved Howland current pump is described in section 3 of the *AN-1515 A Comprehensive Study of the Howland Current Pump* application report. Information about how the current pump resistor values are determined for a specific combination of input voltage and corresponding output current are detailed in the report. Here, the OPA462 is used to provide a constant current output over a wide range of output load.

- Input voltage: 2.5 Vpk at 400 Hz
- Output voltage: 20 Vpk
- Output current: ±20 mA in-phase with the output voltage

版权 © 2018–2019, Texas Instruments Incorporated

Typical Applications (接下页)

8.2.2.2 Detailed Design Procedure

The improved Howland current pump circuit is illustrated in 图 63. The OPA462 sources an output current of 20 mA when a low-voltage single-ended, 2.5-V reference voltage is applied to the circuit input. The source could be an actual 2.5-V precision reference. If the current-pump output current requires being set to different levels, a voltage output DAC can be used. If the input voltage polarity is reversed, the output current reverses direction, and 20 mA is sunk from the load through the OPA462 output.

The circuit shown in 图 63 provides the resistance values required to obtain a ±20-mA output current with the 2.5-V input voltage applied. The following can be used to select the resistors, thus setting the voltage gain and output current.

- R_{13} sets the gain, and is adjusted by the ratio of R_{14} / R_{15}
- Selecting a low value for R_{13} enables all other resistors to be high, limiting current through the feedback network
- The ratio of R_{11} / (R_{12} + R_{13}) must equal R_{14} / R_{15}
- If R_{14} = R_{15}, then R_{12} = R_{11} – R_{13}

Applying these relationships the resistors are selected or derived as follows:

- Let R_{14} = R_{15} = 100 kΩ
- R_{13} = [(VP – VN) (R_{15} / R_{14})] / I_L = [(2.5 V – 0 V) (105 Ω / 105 Ω)] = 125 Ω
- R_{12} = (R_{11} – R_{13}) = (100 kΩ – 125 Ω) = 99.875 kΩ

Verifying R_{11} / (R_{12} + R_{13}) must equal R_{14} / R_{15} requirement:

- R_{12} = [R_{11}(R_{15} / R_{14})] – R_{13} = [105 Ω (105 Ω / 105 Ω)] – 125 Ω = 99.875 kΩ

The resistor values for R_{11} through R_{15} are seen in 图 63.

The load is set to be 500 Ω, the sourced output current through the load is 20 mA, and the output voltage is 10 V. The voltage directly at the OPA462 output 2.5 V higher, or 12.5 V, which compensates for the voltage drop across the 125-Ω R_{13} resistor. A feedback capacitor can be added to reduce the ac bandwidth of the improved Howland current pump circuit, if needed. In this example, no capacitor is used.

The improved Howland current pump output is limited to the combined effects of the OPA462 linear output voltage swing range, the voltage drop developed across R_{13}, and the voltage drop developed across load. For a particular output current, a maximum output voltage span can be achieved. This span is referred to as the output voltage compliance range.

The OPA462 current pump sources or sinks a constant current through a load resistance of 0 Ω on the low end, to just beyond 4.25 kΩ on the high end. This current range is portrayed in the dc transfer plot show in 图 64. As shown, the load can be vary from 0 Ω to 4.25 kΩ and the output remains within the span of linear output compliance range.

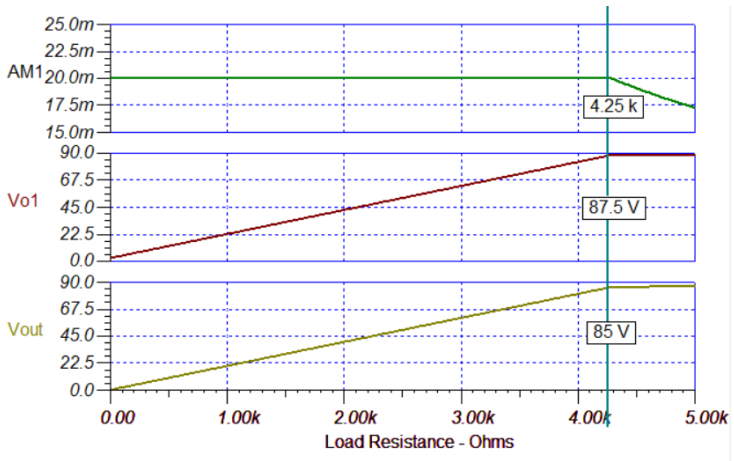


图 64. Output Voltage Compliance for an Improved Howland Current Pump

版权 © 2018–2019, Texas Instruments Incorporated

Typical Applications (接下页)

The 4.25-kΩ limit is determined by the maximum 85-V drop across the load, and the 2.5-V drop across R_{13} when 20 mA flows through both. This voltage drop results in an output voltage of 87.5 V at the output of the OPA462, close to the positive swing limit. Beyond 4.25 kΩ, current-pump operation is forced outside the compliance range, and the output current is longer maintained at the correct level.

The OPA462 provides this wide output compliance range because of the wide, ±90-V power supply rating. If a standard ±15-V amplifier supply had been used with the OPA462, or another amplifier rated for ±15-V supplies, the maximum load resistance is on the order of approximately 500 Ω to 600 Ω, depending on the particular amplifier linear output range when delivering ±20 mA. The wide supply range of the OPA462 enables the device to drive a much wider range of loads.

The improved Howland current pump can also be used to generate an accurate ac current with a peak output that matches a specified dc current level. A ±20-mA dc current source using the OPA462 has already been discussed; therefore, this current source is applied here to demonstrate how a 400-Hz, 20-mA current is produced.

The same circuit used in 图 63 is updated so that the 2.5-V dc voltage source has been replaced by a 400-Hz ac source with a peak voltage of 2.5 V, as shown in 图 65. A sine wave is used in this circuit, but a triangle wave, square wave, and so on, can be used instead. The output current is dependent on the ac input voltage at any particular moment.

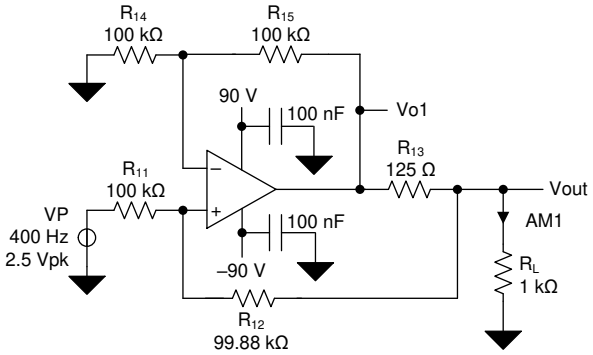


图 65. OPA462 Configured as a 400-Hz AC Current Generator

A 2.5-Vpk sine-wave source applied to the input point at R_{11} results in a 20-mA peak current through the load, as shown in 图 66. The load has been set to 1 kΩ, but any resistance that supports the output compliance range can be used.

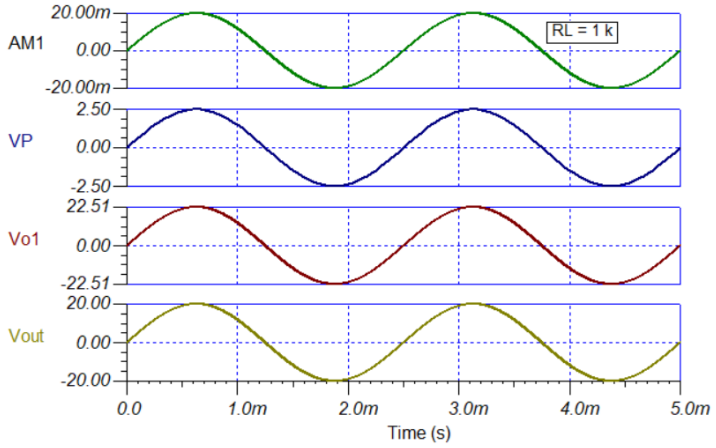


图 66. Improved Howland Current Pump Applied as a Peak AC-Current Generator

Typical Applications (接下页)

Make sure to consider the power handling ratings of the resistors used with a high-power or high-voltage amplifier such as the OPA462. In this design, when the OPA462 is providing 20 mA dc to a 4.25-kΩ load resistance, the dc power for the load and R_{13} is simply:

- Load Power = $I2 \cdot R_L = (20 \cdot 10 – 3\ A)^2\ (4.25 \cdot 103\ \Omega) = 1.7\ W$
- Power $R_{13} = I2 \cdot R_{13} = (20 \cdot 10 – 3\ A)^2\ (125\ \Omega) = 50\ mW$

Clearly, the power dissipation of the load requires attention. However, in this design, R_{13} does not require high power dissipation under these operating conditions. The load must be rated to dissipate the 1.7 W over the expected operating temperature range for this example. Most often, resistor power dissipation is specified at an ambient temperature of 25°C, and reduces as temperature increases. The use of a resistor with a power rating greater than the power that must be dissipated is almost always necessary. For this example, the load may need to be rated for 3 W, or even 5 W, to make sure that the load does not overheat and maintains reliability. in any case, determine the power dissipation for the particular operating conditions. Be especially attentive to the power rating issue regarding surface-mount resistors. The thermal environment in which surface-mount resistors operate may be much different than a resistor exposed in free air.

The improved Howland current pump amplifier circuit relies on both negative and positive feedback for operation. More negative feedback than positive feedback is used, but that does not always provide stability when the output load characteristics are included. When unity-gain stable amplifiers such as the OPA462 are employed, and they drive a resistive load, the amplifier phase margin should be sufficient so that the circuit is stable. However, if the output load is complex, containing both resistive and reactive components (R±jX), certain combinations degrade the phase margin to the point where instability results. Instability is even more evident when this current pump is used to drive certain inductive loads.

When required, compensation is determined based on the particular circuit to which the OPA462 is being applied. Amplifier stability and compensation is a vast subject covered in numerous TI documents, and TI training programs, such as TI Precision Labs – Op Amps.

版权 © 2018–2019, Texas Instruments Incorporated

9 Power Supply Recommendations

The OPA462 operates from power supplies up to ±90 V, or a total of 180 V, with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Make sure that the capacitor voltage rating is suitable for the high voltage across the full operating temperature range. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics* section.

Some applications do not require an equal positive and negative output voltage swing. Power-supply voltages do not have to be equal. The OPA462 operates with as little as 12 V between the supplies, and with up to 180 V between the supplies.

10 Layout

10.1 Layout Guidelines

10.1.1 Thermally-Enhanced PowerPAD™ Package

The OPA462 comes in an 8-pin SO PowerPAD package that provides an extremely low thermal resistance, $R_{\theta JC(bot)}$, path between the die and the exterior of the package. This package features an exposed thermal pad that has direct thermal contact with the die. Thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The OPA462 SO-8 PowerPAD is a standard-size SO-8 package constructed using a downset leadframe upon which the die is mounted, as 图 67 shows. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package. The thermal pad on the bottom of the device can then be soldered directly to the PCB, using the PCB as a heat sink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB. This architecture enhances the OPA462 power dissipation capability significantly, eliminates the use of bulky heat sinks and slugs traditionally used in thermal packages, and allows the OPA462 to be easily mounted using standard PCB assembly techniques.

注

The SO-8 PowerPAD is pin-compatible with standard SO-8 packages, and as such, the OPA462 is a drop-in replacement for operational amplifiers in existing sockets. Always solder the PowerPAD to the PCB V– plane, even with applications that have low power dissipation. Solder the device to the PCB to provide the necessary thermal, mechanical, and electrical connections between the leadframe die pad and the PCB.

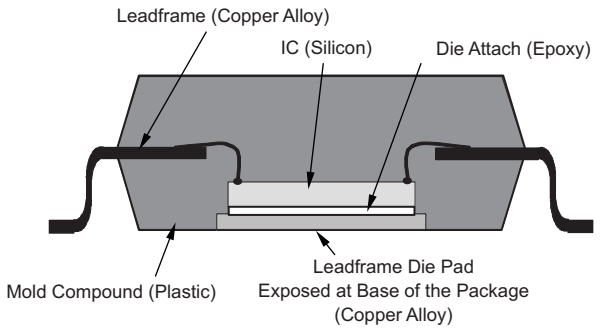


图 67. Cross Section View of a PowerPAD™ Package

Layout Guidelines (接下页)

10.1.2 PowerPAD™ Integrated Circuit Package Layout Guidelines

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into either a ground plane or other heat-dissipating device. Always solder the PowerPAD to the PCB, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. Connect the PowerPAD to the most negative supply voltage on the device, V–.
2. Prepare the PCB with a top-side etch pattern. There must be etching for the leads, as well as etching for the thermal pad.
3. Thermal vias improve heat dissipation, but are not required. The thermal pad can connect to the PCB using an area equal to the pad size with no vias, but externally connected to V–.
4. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package are shown in the thermal land pattern mechanical drawing appended at the end of this document. These holes must be 13 mils (0.013 in, or 0.3302 mm) in diameter. Keep the holes small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
5. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA462 device. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all holes to the internal power plane of the correct voltage potential, V–.
7. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA462 PowerPAD package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask must leave the pins of the package and the thermal pad area exposed. The bottom-side solder mask must cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the device pins.
10. With these preparatory steps in place, simply place the device in position, and run through the solder reflow operation as with any standard surface-mount component.

This preparation results in a properly installed device. For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see the *PowerPAD™ Thermally Enhanced Package* application report.

10.1.3 Pin Leakage

When operating the OPA462 with high supply voltages, parasitic leakages may occur between the inputs and the supplies. This effect is most noticeable at the noninverting input, +IN, when the input common-mode voltage is high compared to the negative supply voltage, V–. To minimize this leakage, place guard tracing, driven at the same voltage as the input signal, alongside the input signal traces and pins.

版权 © 2018–2019, Texas Instruments Incorporated

Layout Guidelines (接下页)

10.1.4 Thermal Protection

图 68 shows the thermal shutdown behavior of a socketed OPA462 that internally dissipates 1 W. Unsoldered and in a socket, the $R_{\theta JA}$ of the DDA package is typically 128°C/W. With the socket at 25°C, the output stage temperature rises to the shutdown temperature of 150°C, which triggers automatic thermal shutdown of the device. The device remains in thermal shutdown (output is in a high-impedance state) until it cools to 130°C where the device is again powered. This thermal protection hysteresis feature typically prevents the amplifier from leaving the safe operating area, even with a direct short from the output to ground or either supply. The absolute maximum specification is 180 V, and the OPA462 must not be allowed to exceed 180 V under any condition. Failure as a result of breakdown, caused by spiking currents into inductive loads (particularly with elevated supply voltage), is not prevented by the thermal protection architecture.

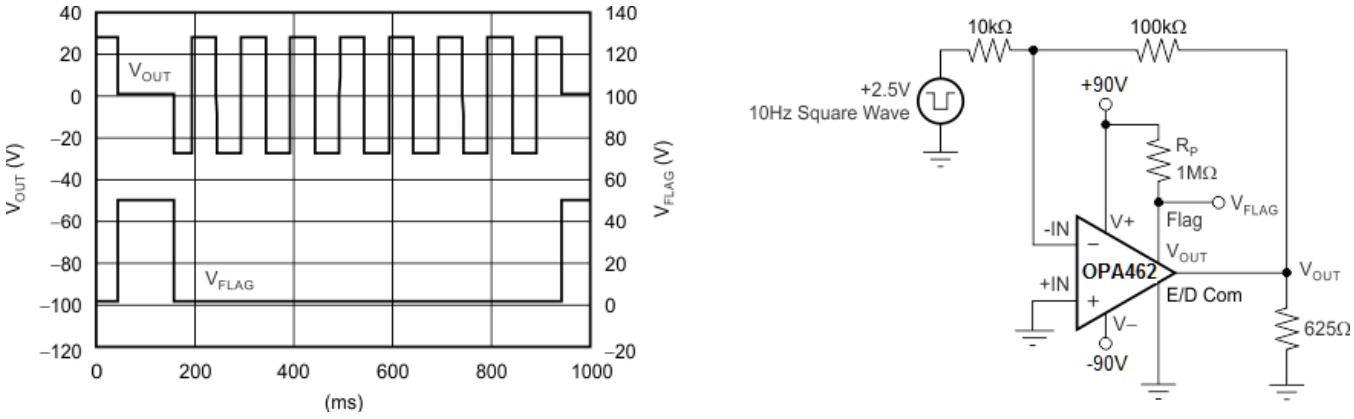


图 68. Thermal Shutdown

10.1.5 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S – V_O)$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower because the root-mean square (RMS) value determines heating. The *Instruments, Power Amplifier Stress and Power Handling Limitations* application bulletin explains how to calculate or measure dissipation with unusual loads or signals.

The OPA462 can supply output currents of up to 45 mA. Supplying this level of current is common for op amps operating from ±15-V supplies. However, with high supply voltages, internal power dissipation of the op amp can be quite high. Relative to the package size, operation from a single power supply (or unbalanced power supplies) can produce even greater power dissipation because a large voltage is impressed across the conducting output transistor. Applications with high power dissipation may require a heat sink or a heat spreader.

10.1.6 Heat Dissipation

Power dissipated in the OPA462 causes the junction temperature to rise. For reliable operation, junction temperature must be limited to 125°C, maximum. Maintaining a lower junction temperature always results in higher reliability. Some applications require a heat sink to make sure that the maximum operating junction temperature is not exceeded. Junction temperature can be determined according to 公式 4:

$$T_J = T_A + P_D R_{\theta JA} \quad (4)$$

Package thermal resistance, $R_{\theta JA}$, is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance to the ambient environment. Many op amps placed closely together also increase the surrounding temperature. Best thermal performance is achieved by soldering the op amp onto a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Increasing circuit board copper area to approximately 0.5 in^2 decreases thermal resistance; however, minimal improvement occurs beyond 0.5 in^2, as shown in 图 69.

版权 © 2018–2019, Texas Instruments Incorporated

Layout Guidelines (接下页)

For additional information on determining heat sink requirements, consult the *Heat Sinking—TO-3 Thermal Model* application bulletin, available for download at www.ti.com.

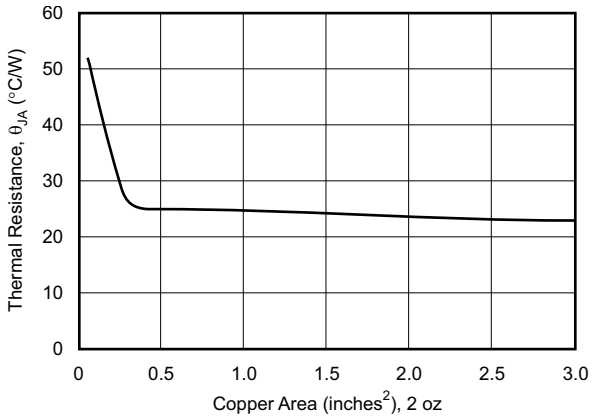


图 69. Thermal Resistance vs Circuit Board Copper Area

10.2 Layout Example

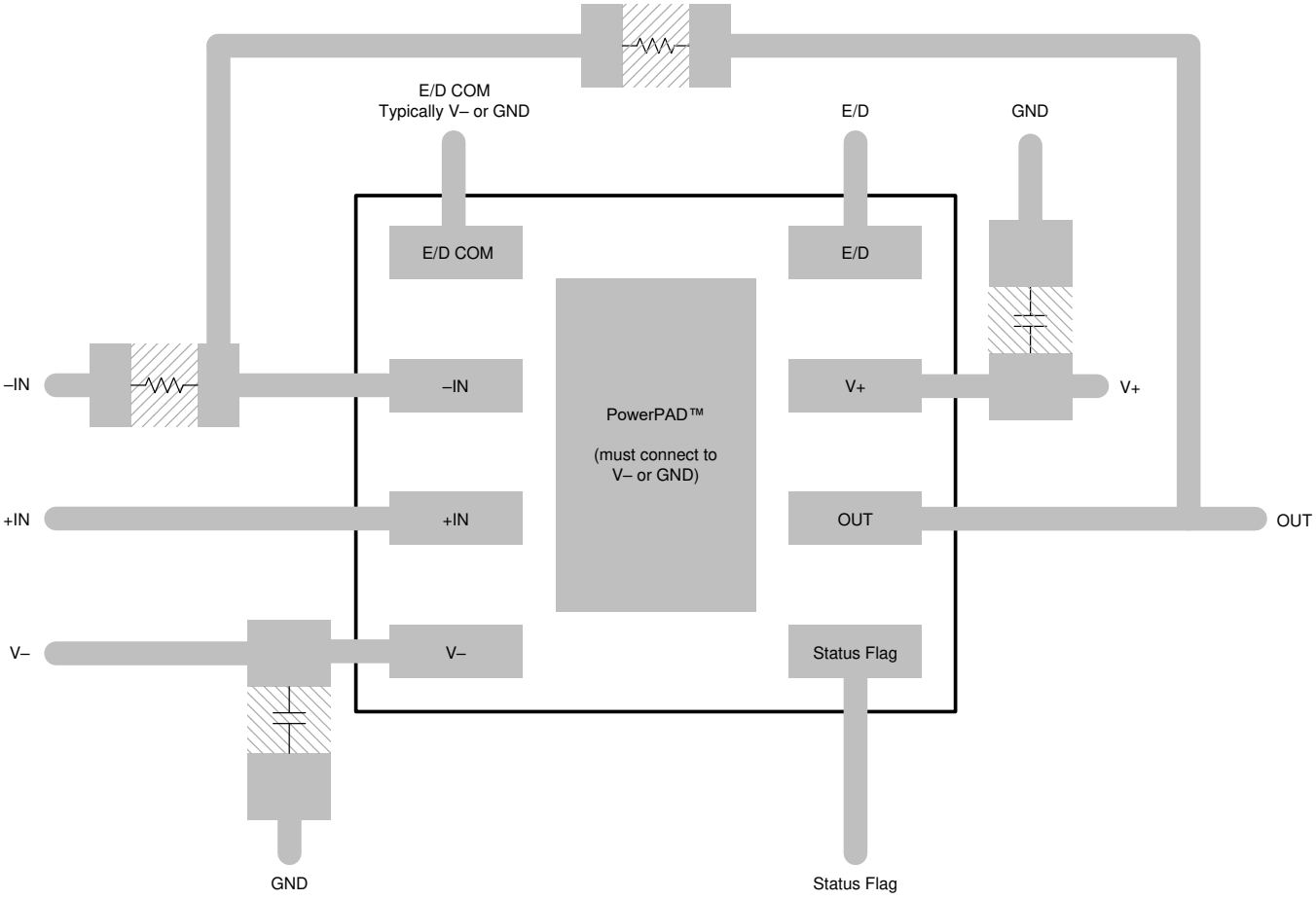


图 70. OPA462 Layout Example

版权 © 2018–2019, Texas Instruments Incorporated

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

11.1.1.3 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波器设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来构建最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在数分钟内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

下列文档与使用 OPA462 相关，建议参考。所有这些文档都可从 www.ti.com.cn 上下载（除非另有说明）。

- 德州仪器 (TI)，*《散热片 - TO-3 热模型》* 应用简报
- 德州仪器 (TI)，*《功率放大器应力和功率处理限制》* 应用简报
- 德州仪器 (TI)，*《运算放大器性能分析》* 应用简报
- 德州仪器 (TI)，*《运算放大器的单电源运行》* 应用简报
- 德州仪器 (TI)，*《放大器调优》* 应用简报
- 德州仪器 (TI)，*《PowerPAD™ 热增强型封装》* 应用报告

11.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 商标

PowerPAD, TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

版权 © 2018–2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA462IDDA	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462
OPA462IDDA.A	Active	Production	SO PowerPAD (DDA) | 8	75 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462
OPA462IDDAR	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462
OPA462IDDAR.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OPA462

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

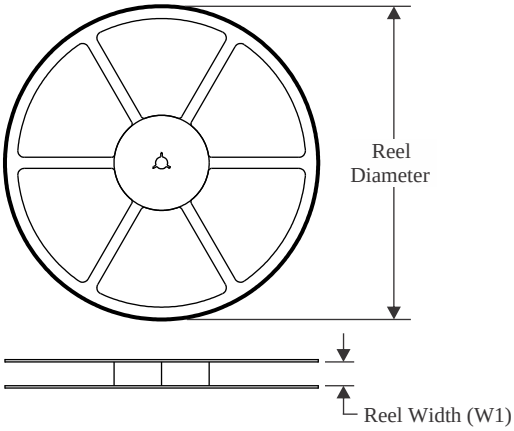
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

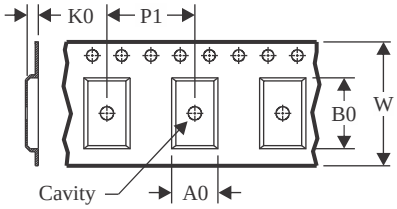
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

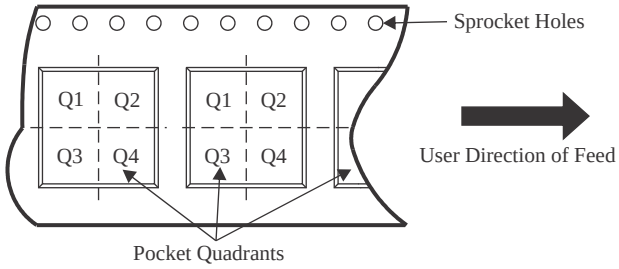


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

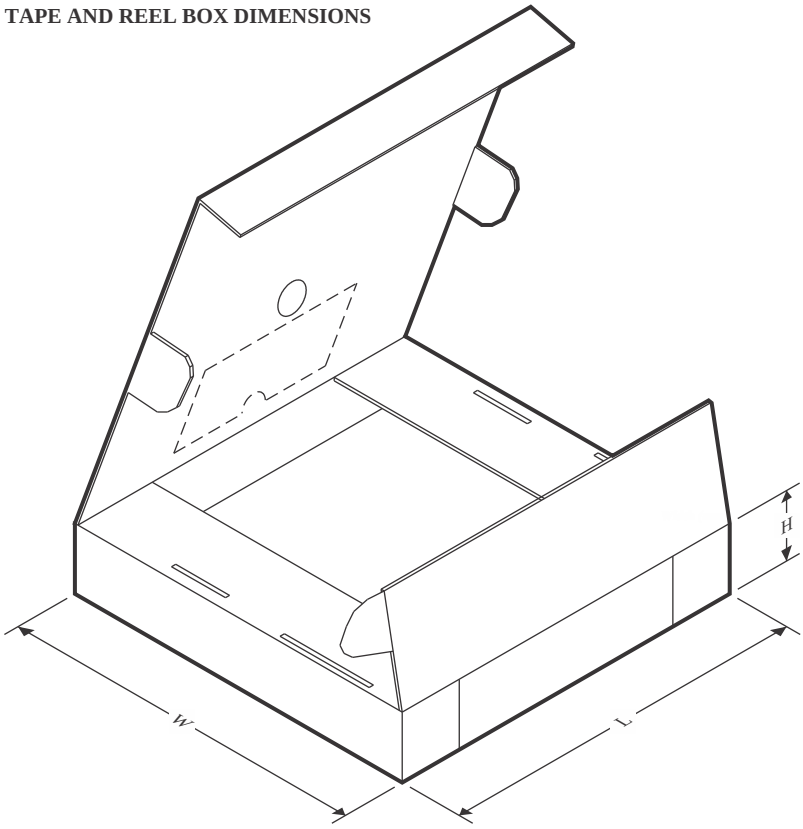
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA462IDDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

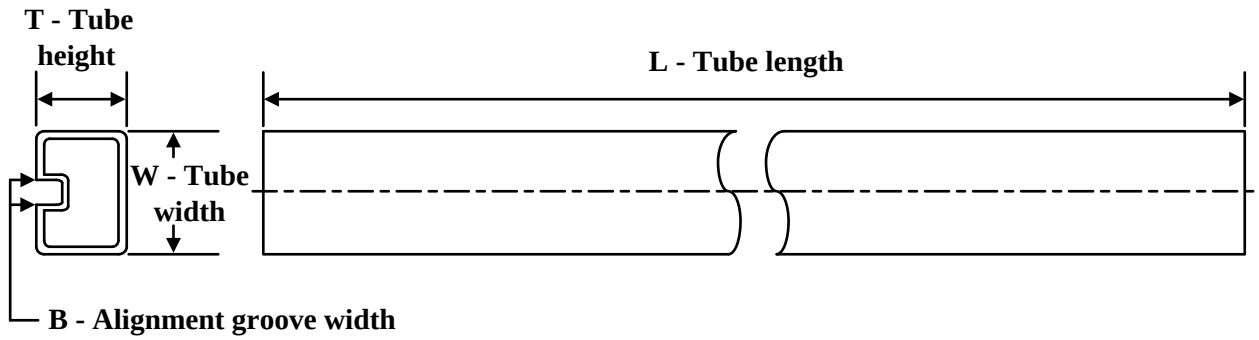
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA462IDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE

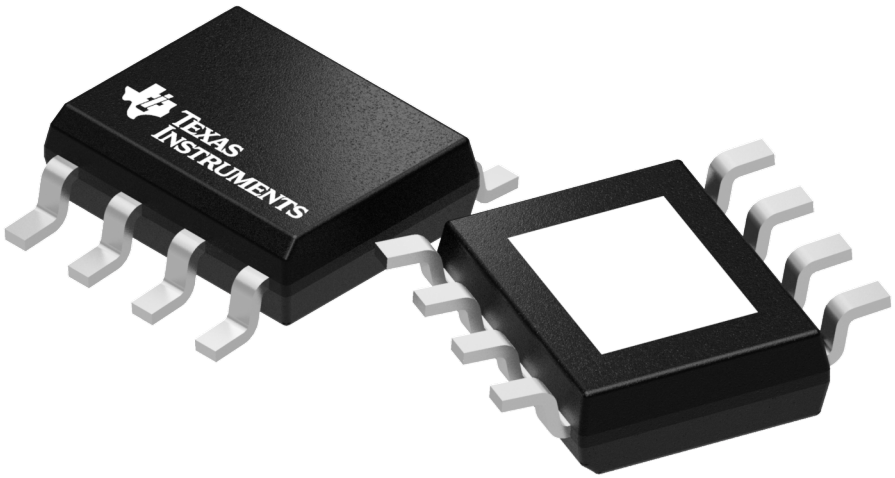


*All dimensions are nominal

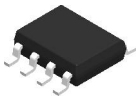
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA462IDDA	DDA	HSOIC	8	75	517	7.87	635	4.25
OPA462IDDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

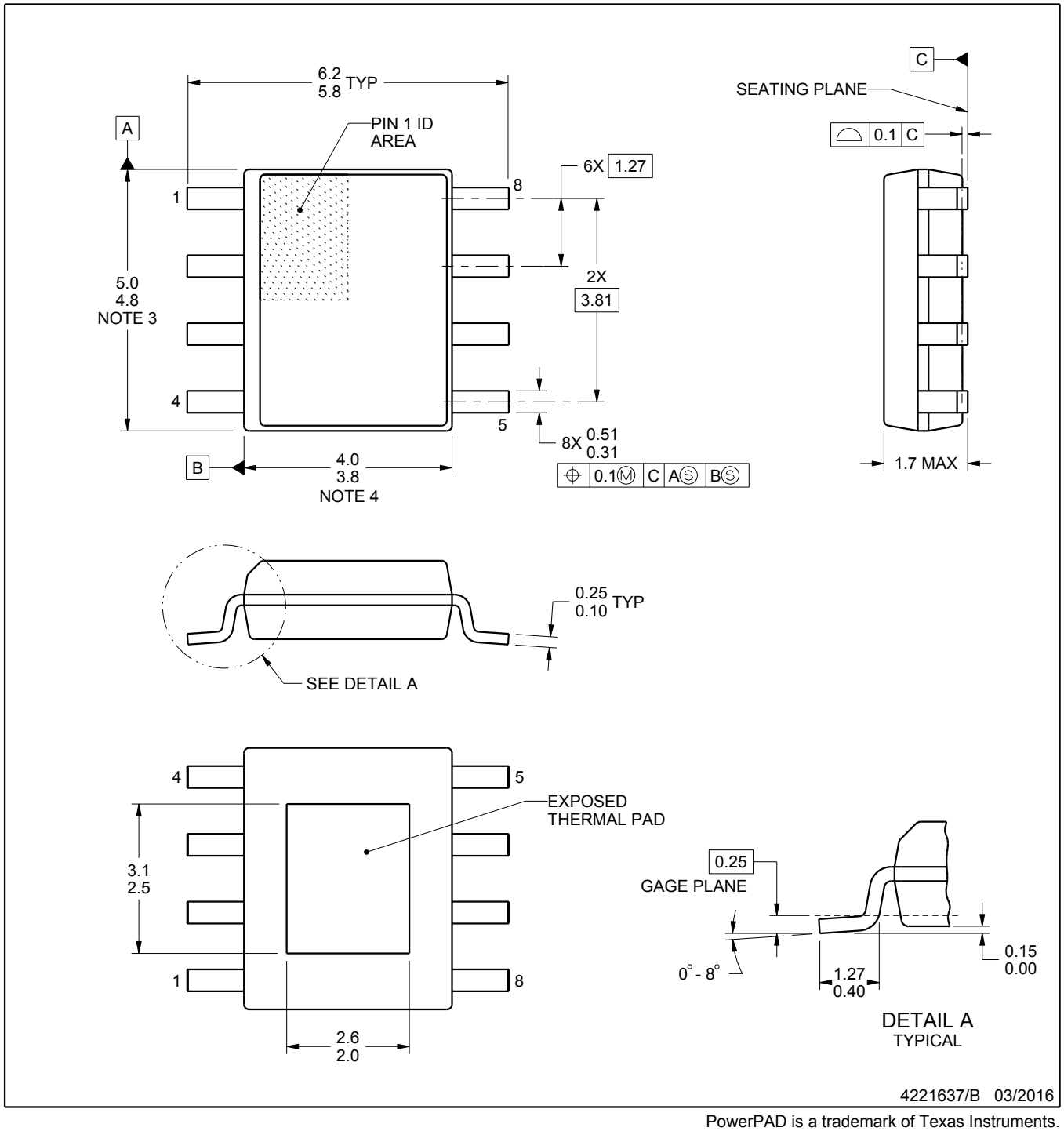


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

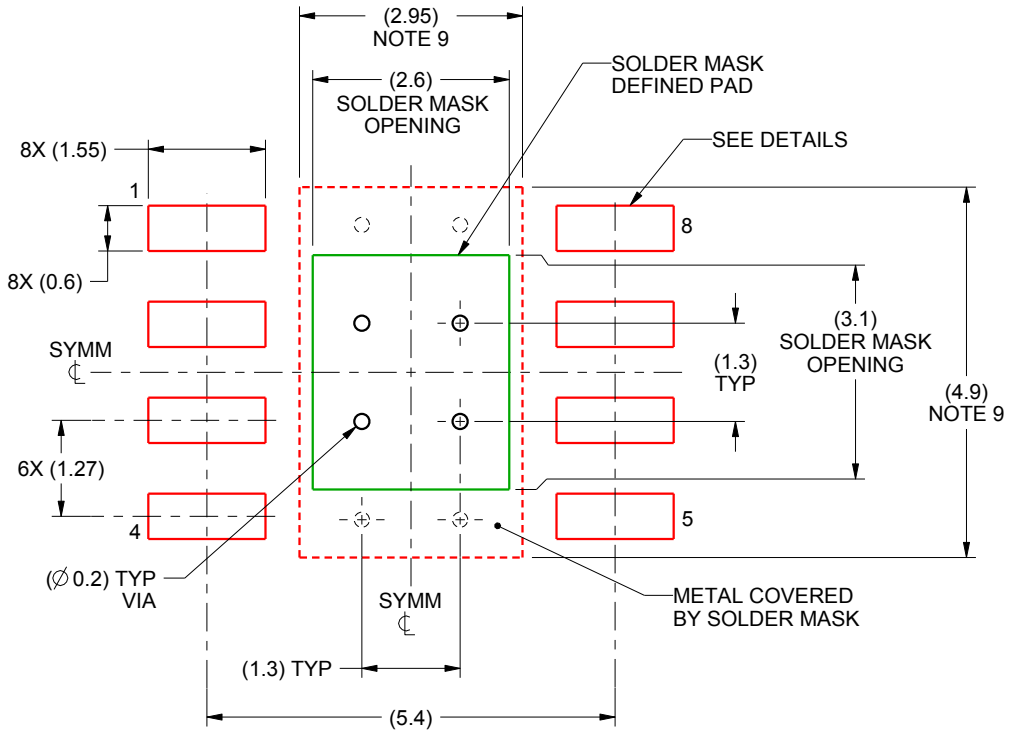
PLASTIC SMALL OUTLINE



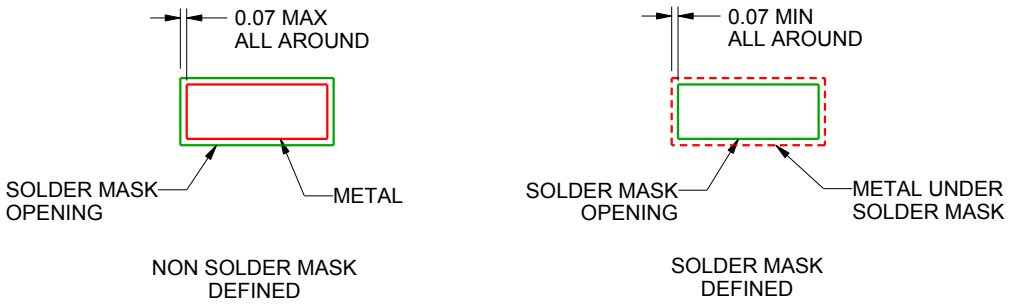
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

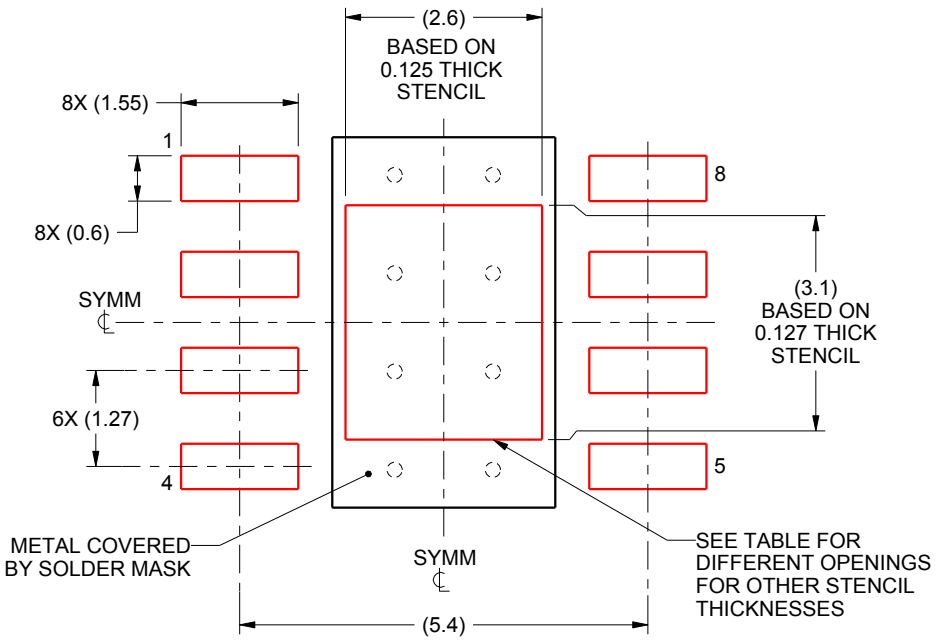


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月