OPA177 0.1µV/°C 温漂、10µV 失调电压、低噪声、双极运算放大器

1 特性

- 低失调电压：25µV（最大值）
- 低失调电压漂移：0.3µV/°C（最大值）
- 高开环增益：134dB（最小值）
- 低静态电流：1.3mA（典型值）
- 低输入偏置电流：±2nA（最大值）
- 宽电源电压范围：6V 至 36V
- 取代了业界通用运算放大器：OP-07、OP-77、OP-177、AD707 等
- 如需通过 ±40V 过压保护来提高性能，请参阅 OPA206

2 应用

- 模拟输入模块
- 数据采集 (DAQ)
- 电池测试
- 实验室和现场仪表
- 温度变送器

3 说明

OPA177 精密双极运算放大器具有超低的失调电压和温漂。激光修整失调电压、温漂和输入偏置电流基本上消除了成本高昂的外部修整。得益于高性能和低成本，此类器件成为各种精密仪表的理想选择。

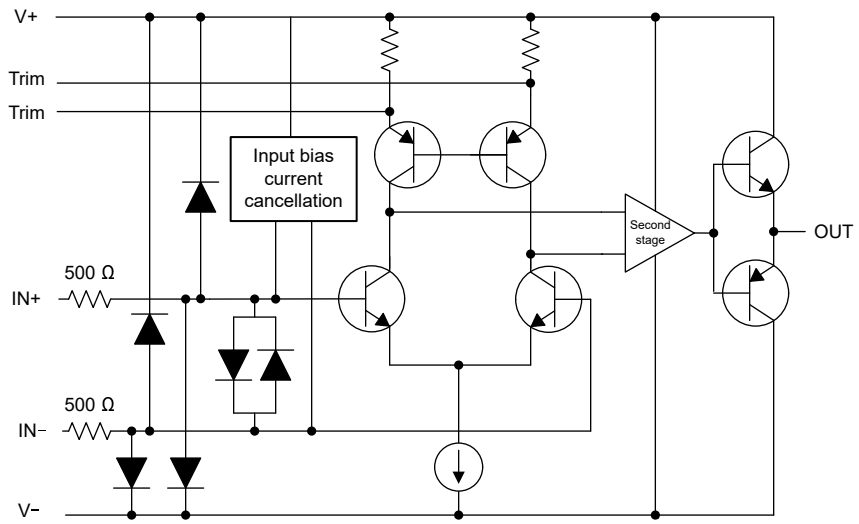
OPA177 的低静态电流显著降低了由于输入互连中的热电效应而导致的预热温漂和误差。OPA177 为斩波稳定型放大器提供了有效的替代方案。OPA177 的低噪声有助于尽可能保持信号完整性。

OPA177 提供多种性能级别的输出。封装选项包括 8 引脚塑料 DIP 和 SO-8 表面贴装型封装。

封装信息

器件型号	封装(1)	封装尺寸(2)
OPA177	D（SOIC，8）	4.9mm × 6mm
	P（PDIP，8）	9.81mm × 9.43mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2000) to Revision A (September 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 为了清晰起见，更改了数据表标题	1
• 添加了*封装信息* 表、*典型应用*、*器件和文档支持* 以及 *机械、封装和可订购信息* 部分	1
• 添加了额外的特性要点并更新了若干项规格，以便与 *电气特性* 保持一致	1
• 更改了应用列表项以显示链接的应用	1
• 为了清晰起见，更改了 *说明*	1
• 更新了首页图	1
• Added pin functions table	3
• Changed supply voltage from ±22 V (44 V) to 40 V in *Absolute Maximum Ratings*	4
• Moved operating temperature from *Absolute Maximum Ratings* to *Recommended Operating Conditions*	4
• Deleted lead temperature from *Absolute Maximum Ratings*	4
• Moved junction to ambient thermal information from *Absolute Maximum Ratings* to *Thermal Information*	4
• Added *ESD Ratings* and *Thermal Information*	4
• Changed several parameter names for consistency with modern data sheets in *Electrical Characteristics*	5
• Updated the format of *Electircal Characteristics*	5
• Added test conditions to the header of *Electrical Characteristics*	5
• Moved test conditions from condition column to the header of *Electrical Characteristics*	5
• Changed open-loop voltage gain unit from V/mV to dB in *Electrical Characteristics*	5
• Changed large signal voltage gain to open-loop voltage gain in *Electrical Characteristics*	5
• Changed Power Supply parameters no load test condition to I_O = 0 A in *Electrical Characteristics*	5
• Updated quiescent current maximum over temperature specification value from 25 mA (typo) to ±2.5 mA	5
• Changed supply current to quiescent current in *Electrical Characteristics*	5
• Added information about integrated overvoltage protection including OPAx206 to Input Protection	10
• Updated Noise Performance with new products such as the OPAx828, OPAx140, and OPAx210	10
• Changed operational amplifier recommendations to reflect new product developments	10

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5 Pin Configuration and Functions

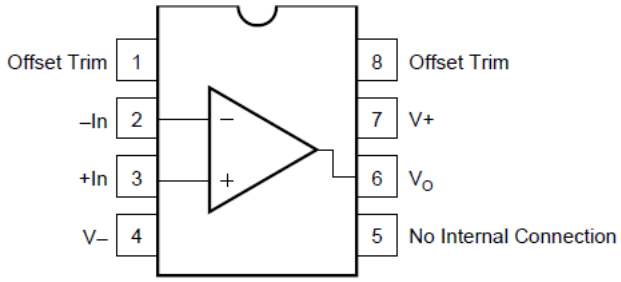

图 5-1. D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
+In	3	Input	Noninverting input
−In	2	Input	Inverting input
No Internal Connection	5	—	No internal connection (can be left floating)
Offset Trim	1, 8	—	Input offset voltage trim (leave floating if not used)
V+	7	Power	Positive (highest) power supply
V−	4	Power	Negative (lowest) power supply
V_O	6	Output	Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		40	V
	Input voltage	(V–)	(V+)	V
	Differential input voltage	–30	30	V
I_{SC}	Output short circuit(2)	Continuous		
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	6	30	36	V
		Dual supply	±3	±15	±18	
T_A	Ambient temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA177		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160.0	100.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

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6.5 Electrical Characteristics

at T_A = 25°C, V_S = 30 V (±15 V), V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
VOS	Input offset voltage	F grade			±10	±25	µV
		G grade			±20	±60	
		T_A = –40°C to +85°C	F grade		±15	±40	
			G grade		±20	±100	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	F grade		±0.1	±0.3	µV/°C
			G grade		±0.7	±1.2	
	Offset adjustment range	R_P = 20 kΩ			±3		mV
	Long-term drift(1)	F grade			0.3		µV/mo
		G grade			0.4		
PSRR	Power-supply rejection ratio	V_S = ±3 V to ±18 V	F grade	115	125		dB
			G grade	110	120		
		V_S = ±3 V to ±18 V T_A = –40°C to +85°C	F grade	110	120		
			G grade	106	115		
INPUT BIAS CURRENT							
I_B	Input bias current	F grade			±0.5	±2	nA
		G grade			±0.5	±2.8	
		T_A = –40°C to +85°C	F grade		±0.5	±4	
			G grade		±0.5	±6	
	Input bias current drift(2)	T_A = –40°C to +85°C	F grade		±8	±40	pA/°C
			G grade		±15	±60	
I_{OS}	Input offset current	F grade			±0.3	±1.5	nA
		G grade			±0.3	±2.8	
		T_A = –40°C to +85°C	F grade		±0.5	±2.2	
			G grade		±0.5	±4.5	
NOISE							
	Input bias current drift(2)	F grade			±1.5	±40	pA/°C
		G grade			±1.5	±85	
	Input voltage noise	f =1 Hz to 100 Hz(3)			85	150	nV_{rms}
	Input current noise	f =1 Hz to 100 Hz			45		pA_{rms}
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range(4)			±13	±14		V
		T_A = –40°C to +85°C		±13	±13.5		
CMRR	Common-mode rejection ratio	V_{CM} = ±13 V	F grade	130	140		dB
			G grade	115	140		
		V_{CM} = ±13 V T_A = –40°C to +85°C	F grade	120	140		
			G grade	110	140		
INPUT IMPEDANCE							
R_{in}	Input resistance	Differential mode(5)	F grade	26	45		MΩ
			G grade	18.5	45		
		Common-mode			200		GΩ

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6.5 Electrical Characteristics（续）

at T_A = 25°C, V_S = 30 V (±15 V), V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain(6)	–10 V ≤ V_O ≤ 10 V	F grade	134	141		dB
			G grade	126	135		
		–10 V ≤ V_O ≤ 10 V, T_A = –40°C to +85°C	F grade	126	135		
			G grade	120	132		
FREQUENCY RESPONSE							
BW_{CL}	Closed-loop bandwidth	G = 1		0.4	0.6		MHz
SR	Slew rate			0.1	0.3		V/µs
OUTPUT							
V_O	Voltage output swing	R_L ≥ 2 kΩ		±13.5	±14		V
			T_A = –40°C to +85°C	±12	±13		
		R_L ≥ 10 kΩ		±12.5	±13		
		R_L ≥ 1 kΩ		±12	±12.5		
I_{SC}	Short-circuit current				±35		mA
R_O	Open-loop output resistance				60		Ω
POWER SUPPLY							
	Power consumption	I_O = 0 A			40	60	mW
			T_A = –40°C to +85°C		60	75	
I_Q	Quiescent current	I_O = 0 A			1.3	2	mA
			T_A = –40°C to +85°C		2	2.5	

(1) Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2 µV.
(2) Specified by characterization.
(3) Sample tested.
(4) Specified CMRR test condition.
(5) Specified by design.
(6) To maintain high open-loop gain throughout the ±10-V output range, A_{OL} is tested at –10 V ≤ V_O ≤ 0 V, 0 V ≤ V_O ≤ +10 V, and –10 V ≤ V_O ≤ +10 V.

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6.6 Typical Characteristics

at T_A = +25°C, V_S = ±15 V (unless otherwise noted)

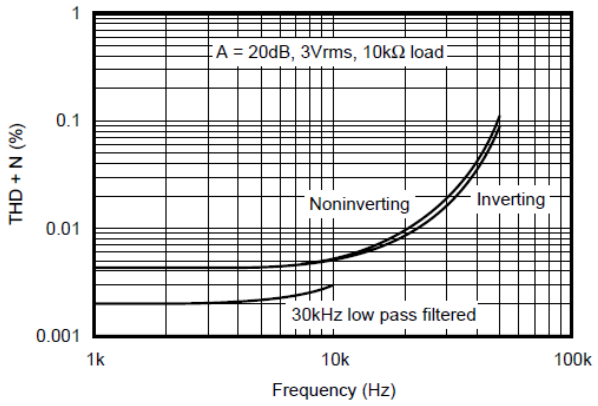

图 6-1. Total Harmonic Distortion and Noise vs Frequency

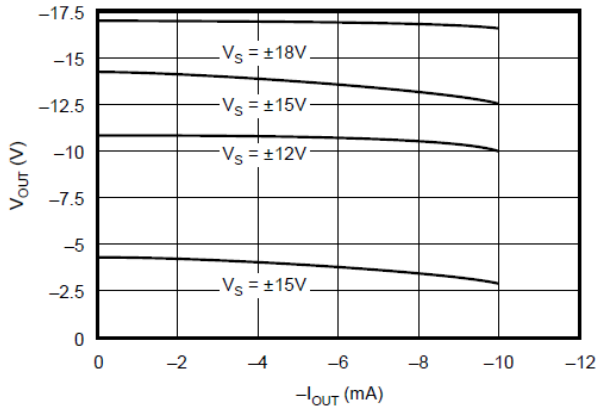

图 6-2. Maximum V_{OUT} vs I_{OUT} (Negative Swing)

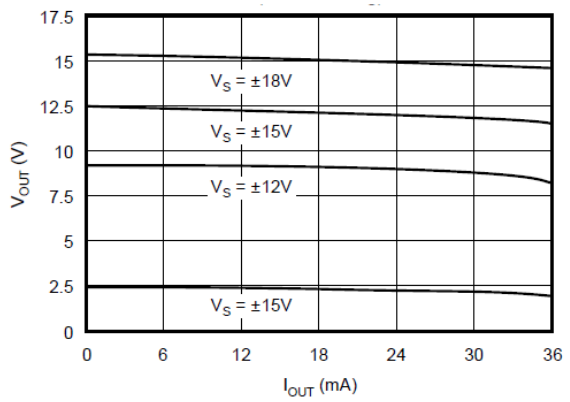

图 6-3. Maximum V_{OUT} vs I_{OUT} (Positive Swing)

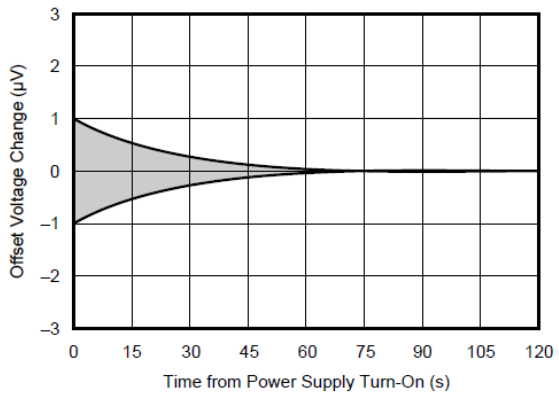

图 6-4. Warm-Up Offset Voltage Drift

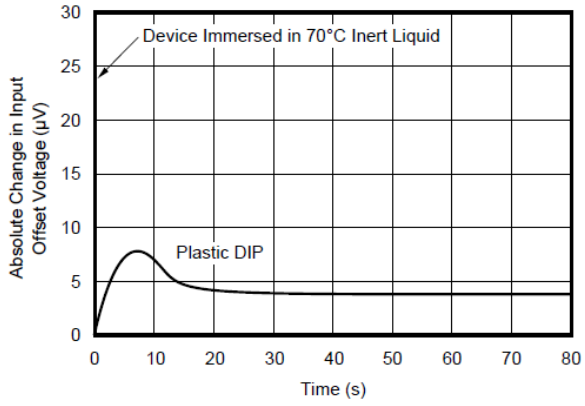

图 6-5. Offset Voltage Change Due To Thermal Shock

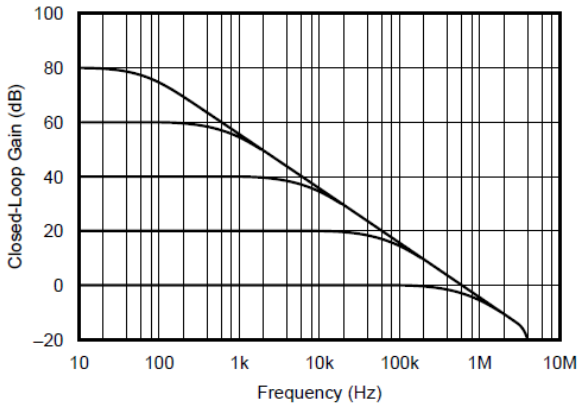

图 6-6. Closed-Loop Response vs Frequency

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6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V (unless otherwise noted)

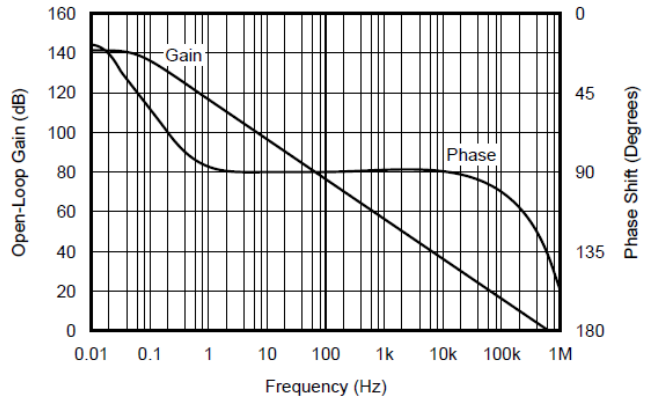

图 6-7. Open-Loop Gain/Phase vs Frequency

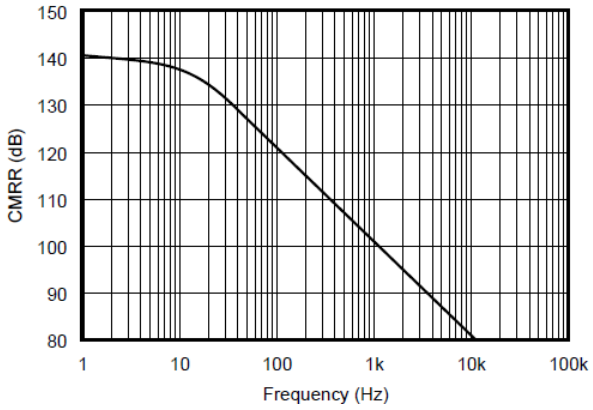

图 6-8. CMRR vs Frequency

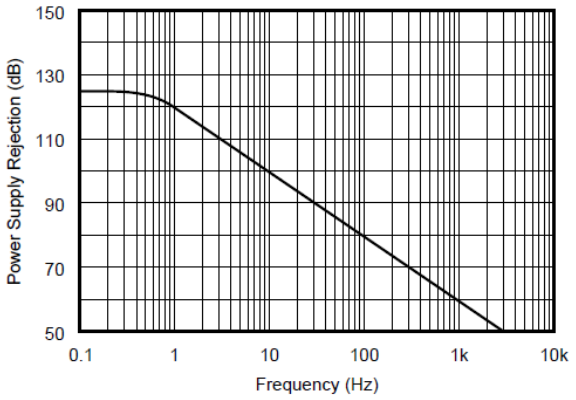

图 6-9. Power Supply Rejection vs Frequency

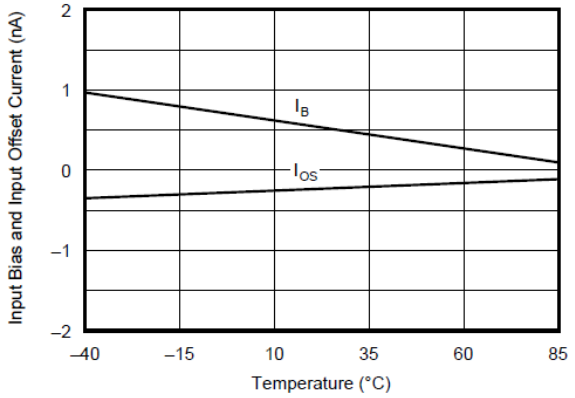

图 6-10. Input Bias and Input Offset Current vs Temperature

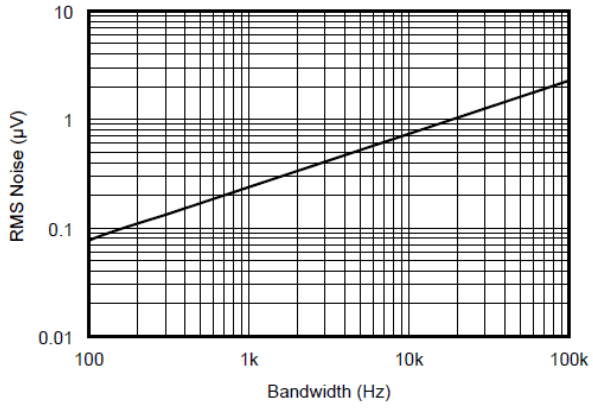

图 6-11. Total Noise vs Bandwidth (0.1Hz to Frequency Indicated)

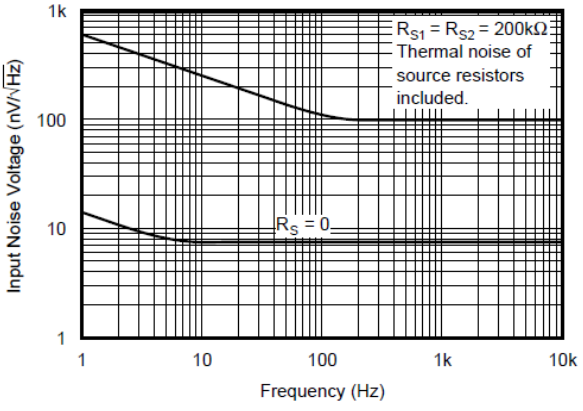

图 6-12. Input Noise Voltage Density vs frequency

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6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V (unless otherwise noted)

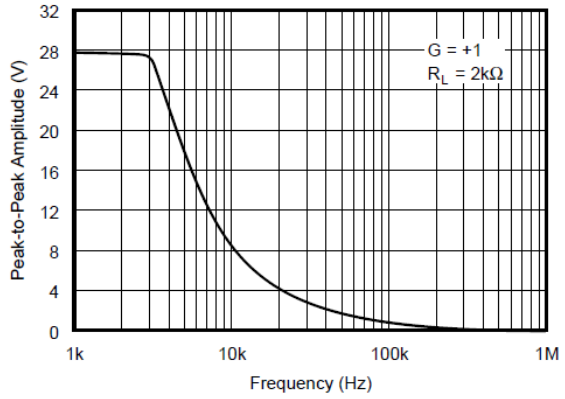

图 6-13. Maximum Output Swing vs Frequency

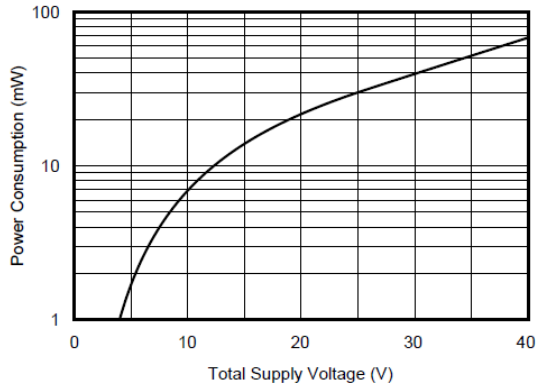

图 6-14. Power Consumption vs Power Supply

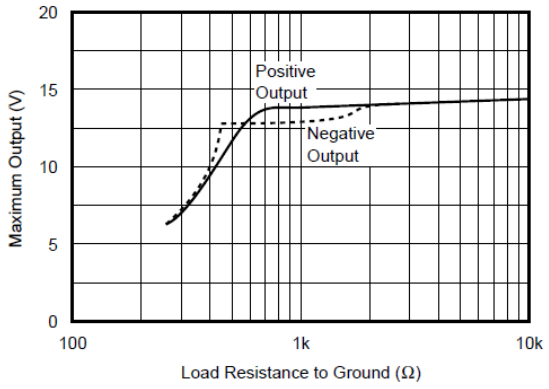

图 6-15. Maximum Output Voltage vs Load Resistance

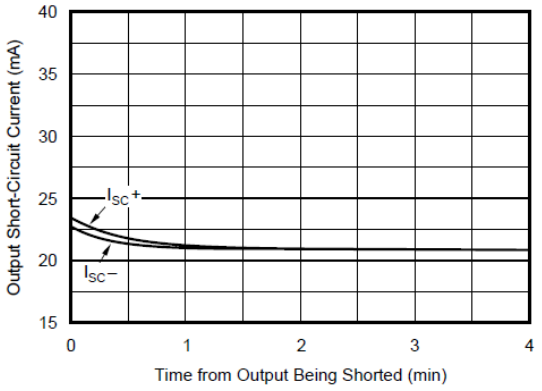

图 6-16. Output Short-Circuit Current vs Time

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7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPA177 is unity-gain stable, making this device easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high-impedance power-supply lines can require decoupling capacitors close to the device pins. In most cases, 0.1-µF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift degrades because of small thermoelectric potentials at the op-amp inputs. Connections of dissimilar metals generate thermal potential that can degrade the ultimate performance of the OPA177. To cancel these thermal potentials, make sure the thermal potentials are equal in both input pins.

1. Keep connections made to the two input pins close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents, such as cooling fans.

7.1.1 Offset Voltage Adjustment

The OPA177 has been laser-trimmed for low offset voltage and drift; therefore, most circuits do not require external adjustment. 图 7-1 shows the optional connection of an external potentiometer to adjust offset voltage. Do not use this adjustment to compensate for offsets created elsewhere in a system because this adjustment can introduce excessive temperature drift.

7.1.2 Input Protection

The inputs of the OPA177 are protected with 500-Ω series input resistors and diode clamps as shown in the simplified circuit diagram on the front page. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This conducted current can disturb the slewing behavior of unity-gain follower applications, but does not damage the op amp. Some applications, such as programmable logic controllers (PLCs) require a robust input-protection design. An input-protection circuit can be implemented using four Schottky diodes; however, the temperature and voltage dependent leakage of the diodes can present undesirable nonlinear errors at the input. For applications requiring high precision and robust input protection, the OPAx206 family of op amps are an excellent choice, offering integrated input overvoltage protection that eliminates the need for external clamping circuits.

7.1.3 Noise Performance

The OPA177 noise performance is optimized for a circuit impedance range of 2 kΩ to 50 kΩ. Total noise in an application is a combination of the op-amp input voltage noise and input bias current noise reacting with circuit impedance. For applications with higher source impedance, the OPAx828 and OPAx140 FET-input op amps generally provide lower noise due to the inherently low input current noise. For low-impedance, low-noise applications, the OPAx210 is an excellent choice because of the exceptionally low op-amp input-voltage noise.

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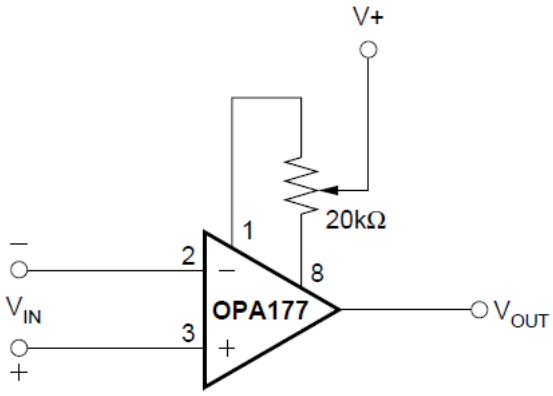
7.1.4 Input Bias Current Cancellation

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

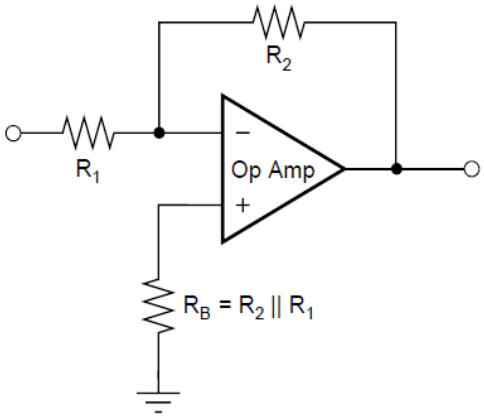
When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, there is no need to balance the dc resistance seen at the two input pins (图 7-2 and 图 7-3). A resistor added to balance the input resistances can actually increase offset and noise.

7.2 Typical Application



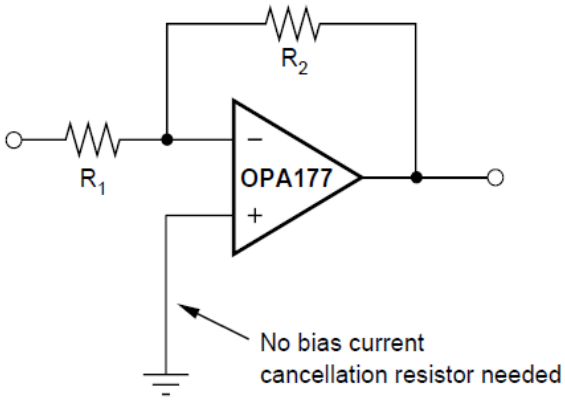
Trim range is approximately ±3.0 mV.

图 7-1. Optional Offset Nulling Circuit



Conventional op amp with external bias current cancellation resistor.

图 7-2. Input Bias Current Cancellation With Conventional Op Amp



OPA177 with no external bias current cancellation resistor.

图 7-3. Input Bias Current Cancellation With OPA177

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 器件支持

8.1.1 开发支持

8.1.1.1 PSpice® for TI

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

8.1.1.2 TINA-TI™ 仿真软件（免费下载）

TINA-TI™ 仿真软件是一款简单易用、功能强大且基于 SPICE 引擎的电路仿真程序。TINA-TI 仿真软件是 TINA™ 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 仿真软件提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 仿真软件提供全面的后处理能力，便于用户以多种方式获得结果，用户可从设计工具和仿真网页免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的能力，从而构建一个动态的快速启动工具。

备注

必须安装 TINA 软件或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI™ 软件文件夹中下载免费的 TINA-TI 仿真软件。

8.1.1.3 DIP-Adapter-EVM

借助 DIP-Adapter-EVM 加快运算放大器的原型设计和测试，该 EVM 有助于快速轻松地连接小型表面贴装器件并且价格低廉。使用随附的 Samtec 端子板连接任何受支持的运算放大器，或者将这些端子板直接连接至现有电路。DIP-Adapter-EVM 套件支持以下业界通用封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV（SOT-23-6、SOT-23-5 和 SOT-23-3）、DCK（SC70-6 和 SC70-5）和 DRL (SOT563-6)。

8.1.1.4 DIYAMP-EVM

DIYAMP-EVM 是一款独特的评估模块 (EVM)，可提供真实的放大器电路，使用户能够快速评估设计概念并验证仿真。此 EVM 采用 3 种业界通用封装选项（SC70、SOT23 和 SOIC）并提供 12 种流行的放大器配置，包括放大器、滤波器、稳定性补偿以及同时适用于单电源和双电源的比较器配置。

8.1.1.5 TI 参考设计

TI 参考设计是由 TI 的精密模拟应用专家创建的模拟解决方案。TI 参考设计提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 参考设计可在线获取，网址为 https://www.ti.com/reference-designs。

8.1.1.6 滤波器设计工具

滤波器设计工具是一款简单、功能强大且便于使用的有源滤波器设计程序。利用滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源器件来打造理想滤波器设计方案。

设计工具和仿真网页以基于网络的工具形式提供滤波设计工具。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA177FP	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-	OPA177FP
OPA177GP	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	OPA177GP
OPA177GS	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-	OPA 177GS
OPA177GS.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 177GS
OPA177GS/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	OPA 177GS
OPA177GS/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 177GS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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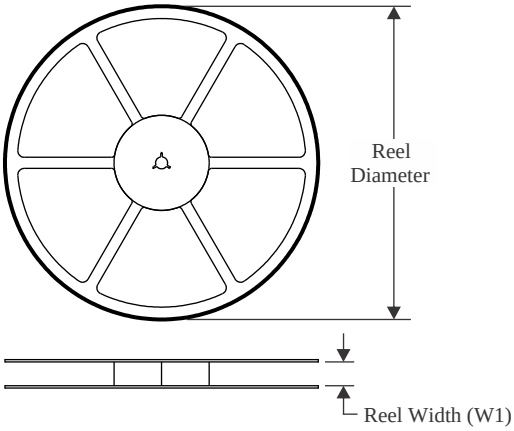
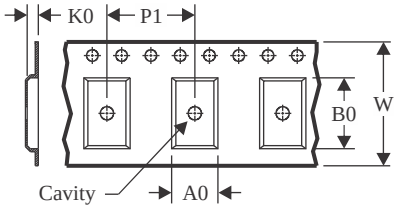
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

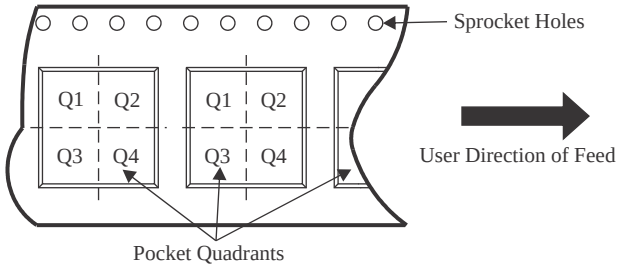


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

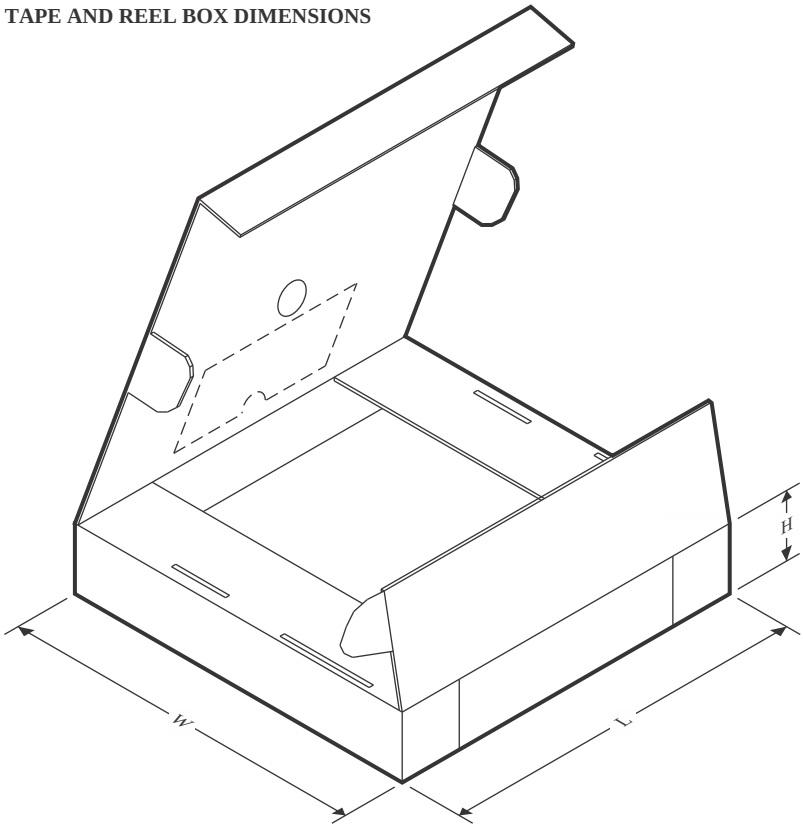
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA177GS/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

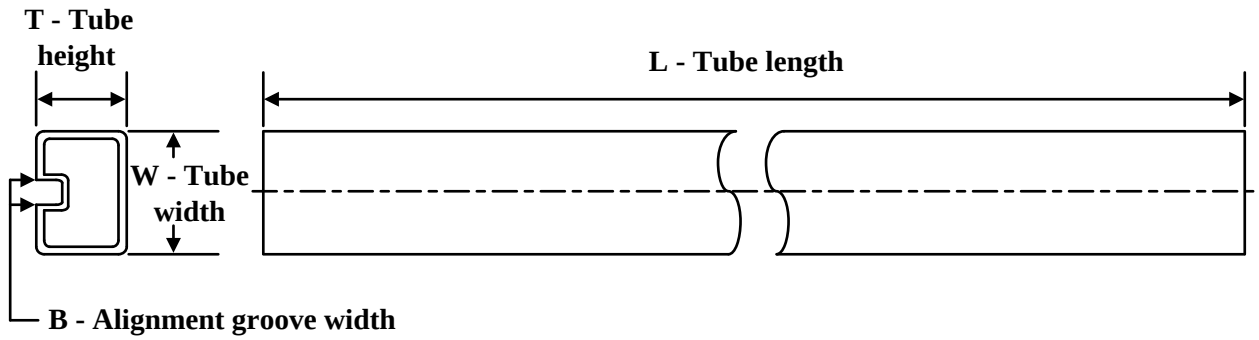
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA177GS/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA177GS	D	SOIC	8	75	506.6	8	3940	4.32
OPA177GS.B	D	SOIC	8	75	506.6	8	3940	4.32

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