OPA1662-Q1 双路 3.3 nV/√Hz 噪声、0.00006% THD+N、RRO、双极输入音频运算放大器

1 特性

- 符合汽车应用 标准
- 具有符合 AEC-Q100 标准的下列结果
  - 器件温度等级 3 级：环境工作温度范围为 –40°C 至 85°C
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C3B
- 低噪声： 1kHz 下为 3.3nV/√Hz
- 低失真：1kHz下为 0.00006%
- 低静态电流：每通道 1.5mA
- 转换率：17V/μs
- 宽增益带宽：22MHz (G = 1)
- 单位增益稳定
- 轨至轨输出
- 宽电源电压范围：±1.5V 至 ±18V，或 3V 至 36V
- 小型封装尺寸：两种封装类型：8 引脚 SOIC 和 VSSOP

2 应用

- 汽车
- 车载音频
- 高级音频设备
- 外部音频放大器
- 车身控制模块

3 说明

OPA1662-Q1 是一个双路双极输入运算放大器，非常适合作为信息娱乐和组合仪表系统中 高级音频设备的外部放大器。音频系统所面临的首要任务是要确保清晰、高质量的输出信号，这意味着要最大程度地减少进入到信号中的任何噪声。OPA1662-Q1 可提供低噪声密度和 0.00006% 的超低失真 (1kHz)，能够最大限度地增大信号输出。此外，该运算放大器在 2kΩ 负载下还可提供 600mV 范围内的轨至轨输出摆幅。宽余量可确保输出信号不发生削波，并由此保护音频质量。

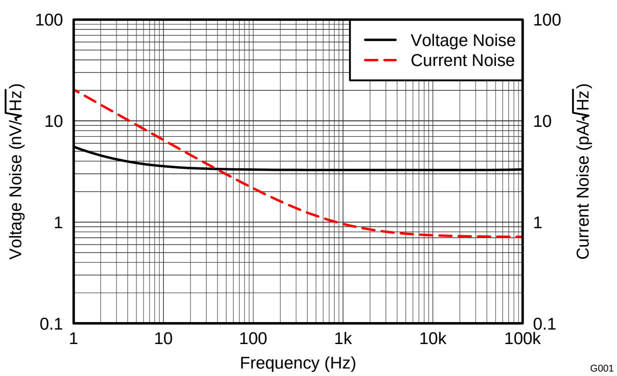
OPA1662-Q1 可在 ±1.5V 至 ±18V，或者 3V 至 36V 这一非常宽的电源电压范围内运行，每通道电源电流仅为 1.5mA。宽电源范围使得器件获得了设计灵活性，因为它既可以从由电池驱动的功率放大器进行集成，也可以从由 ADC 到 DAC 驱动的功率放大器进行集成，以实现低功耗 应用。此外，该器件还具有 ±30mA 的高输出驱动能力，可作为低功耗应用的唯一 音频放大器，例如用于仪表组提示音。

器件信息(1)

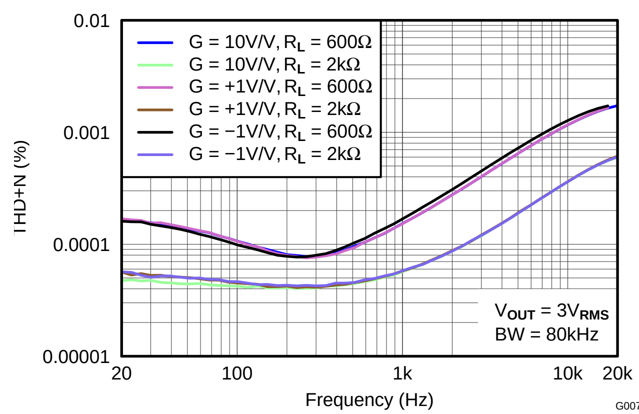
器件型号	封装	封装尺寸（标称值）
OPA1662-Q1	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

输入电压噪声密度和输入电流噪声密度与频率间的关系



THD+N 比与频率间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (October 2012) to Revision C	Page
• 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。	1
• 删除了*订购信息* 表，请参见数据表末尾的 POA	1
• 已更改 （*说明*部分中的第二句）	1

Changes from Revision A (September 2012) to Revision B	Page
• 在*订购信息* 表中，将预览中 OPA1662AIDRQ1 的顶端标记更改为了 O1662Q	1
• 1 级更改为了 3 级（*“特性”部分*）	1

Changes from Original (July 2012) to Revision A	Page
• 将器件从预览（2 页）改为生产状态，本修订版包含了标准长度文档。	1

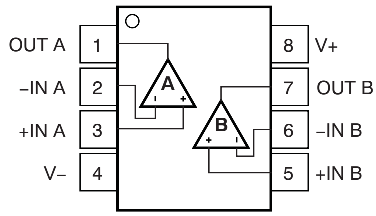
5 说明 （续）

此外，该器件还 具备 两个通道均使用完全独立的电路，可实现低串扰，即便在过驱动或过载时也不受每个通道间相互作用的影响。借助此功能，客户可轻松驱动两个不同的音频信号，因为信号之间不会相互影响。

OPA1662-Q1 提供 22MHz 的宽带宽和 17V/µs 的高转换率，可用于 SMPS 器件或电机驱动器中纹波电流的高侧和低侧感应。作为一个电流传感器，OPA1662-Q1 可作为峰值电流模式控制使用，借助该运算放大器，可为系统提供稳定性并可实现更高带宽。OPA1662-Q1 可应用于车身控制模块和通常使用电机的 HEV 或 EV 转换器。

6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input channel A
–IN A	2	I	Inverting input channel A
+IN B	5	I	Noninverting input channel B
–IN B	6	I	Inverting input channel B
OUT_A	1	O	Output, channel A
OUT_B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, (V+) – (V–)		40	V
Input voltage	(V–) – 0.5	(V+) + 0.5	V
Input current (all pins except power-supply pins)		±10	mA
Output short-circuit(2)	Continuous		
Operating ambient temperature	–40	125	°C
Junction temperature, T_J		200	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	3 (±1.5)	36 (±18)	V
T_A	Operating ambient temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		OPA1662-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	156.3	225.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.5	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	110.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.8	14.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.3	108.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: V_S = ±15 V

T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}			0.00006%		
					–124		dB
IMD	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}	SMPTE two-tone, 4:1 (60 Hz and 7 kHz)		0.00004%		
					–128		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.00004%		
					–128		dB
			CCIF twin-tone (19 kHz and 20 kHz)		0.00004%		
					–128		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 1			22		MHz
SR	Slew rate	G = –1			17		V/µs
	Full power bandwidth (1)	V_O = 1 V_P			2.7		MHz
	Overload recovery time	G = –10			1		µs
	Channel separation (dual and quad)	f = 1 kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20 Hz to 20 kHz			2.8		μV_{PP}
	Input voltage noise density	f = 1 kHz			3.3		$nV/\sqrt{Hz}$
		f = 100 Hz			5		$nV/\sqrt{Hz}$
I_n	Input current noise density	f = 1 kHz			1		$pA/\sqrt{Hz}$
		f = 100 Hz			2		$pA/\sqrt{Hz}$

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.

Electrical Characteristics: V_S = ±15 V (continued)

T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±1.5 V to ±18 V		±0.5	±1.5	mV
		V_S = ±1.5 V to ±18 V, T_A = –40°C to 85°(2)		2	8	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.5 V to ±18 V		1	3	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		600	1200	nA
I_{OS}	Input offset current	V_{CM} = 0 V		±25	±100	nA
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) + 0.5		(V+) – 1	V
CMRR	Common-mode rejection ratio		106	114		dB
INPUT IMPEDANCE						
	Differential resistance			170		kΩ
	Differential capacitance			2		pF
	Common-mode resistance			600		kΩ
	Common-mode capacitance			2.5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 2 kΩ	106	114		dB
OUTPUT						
V_{OUT}	Output voltage	R_L = 2 kΩ	(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current			See *Typical Characteristics*		mA
Z_O	Open-loop output impedance			See *Typical Characteristics*		Ω
I_{SC}	Short-circuit current(3)			±50		mA
C_{LOAD}	Capacitive load drive			200		pF
POWER SUPPLY						
V_S	Specified voltage		±1.5		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		1.5	1.8	mA
		I_{OUT} = 0 A, T_A = –40°C to 85°(2)			2	mA
TEMPERATURE						
	Specified temperature		–40		85	°C

(2) Specified by design and characterization.
(3) One channel at a time.

7.6 Electrical Characteristics: V_S = 5 V

T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

PARAMETERTEST		CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}			0.0001%		
					–120		dB
IMD	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}	SMPTE two-tone, 4:1 (60 Hz and 7 kHz)		0.00004%		
					–128		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.00004%		
					–128		dB
			CCIF twin-tone (19 kHz and 20 kHz)		0.00004%		
					–128		dB

Electrical Characteristics: V_S = 5 V (continued)

T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 2 kΩ (unless otherwise noted)

PARAMETERTEST		CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		20		MHz
SR	Slew rate	G = –1		13		V/µs
	Full power bandwidth(1)	V_O = 1 V_P		2		MHz
	Overload recovery time	G = –10		1		µs
	Channel separation (dual and quad)	f = 1 kHz		–120		dB
NOISE						
e_n	Input voltage noise	f = 20 Hz to 20 kHz		3.3		$µV_{PP}$
	Input voltage noise density	f = 1 kHz		3.3		nV/√Hz
		f = 100 Hz		5		nV/√Hz
I_n	Input current noise density	f = 1 kHz		1		pA/√Hz
		f = 100 Hz		2		pA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±1.5 V to ±18 V		±0.5	±1.5	mV
		V_S = ±1.5 V to ±18 V, T_A = –40°C to 85°(2)		2	8	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.5 V to ±18 V		1	3	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		600	1200	nA
I_{OS}	Input offset current	V_{CM} = 0 V		±25	±100	nA
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) + 0.5		(V+) – 1	V
CMRR	Common-mode rejection ratio		86	100		dB
INPUT IMPEDANCE						
	Differential resistance			170		kΩ
	Differential capacitance			2		pF
	Common-mode resistance			600		kΩ
	Common-mode capacitance			2.5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 2 kΩ	90	100		dB
OUTPUT						
V_{OUT}	Output voltage	R_L = 2 kΩ	(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current			See \		mA
Z_O	Open-loop output impedance			See *Typical Characteristics*		Ω
I_{SC}	Short-circuit current(3)			±40		mA
C_{LOAD}	Capacitive load drive			200		pF
POWER SUPPLY						
V_S	Specified voltage		±1.5		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		1.4	1.7	mA
		I_{OUT} = 0 A, T_A = –40°C to 85°(2)			2	mA
TEMPERATURE						
	Specified temperature		–40		85	°C

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

7.7 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

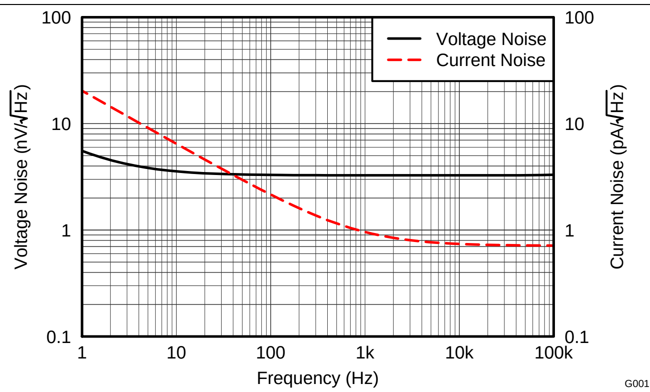


Figure 1. Input Voltage Noise Density and Input Current Noise Density vs Frequency

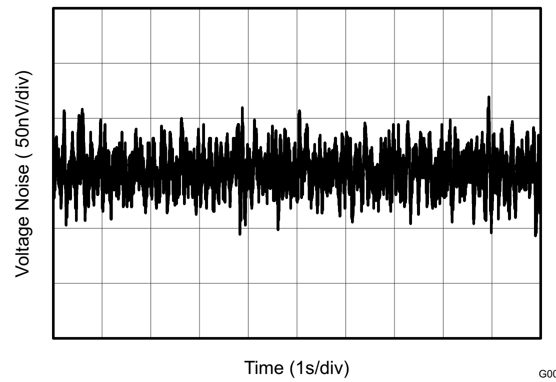


Figure 2. 0.1-Hz to 10-Hz Noise

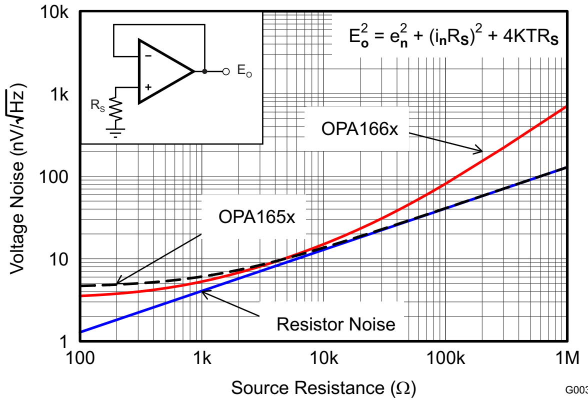


Figure 3. Voltage Noise vs Source Resistance

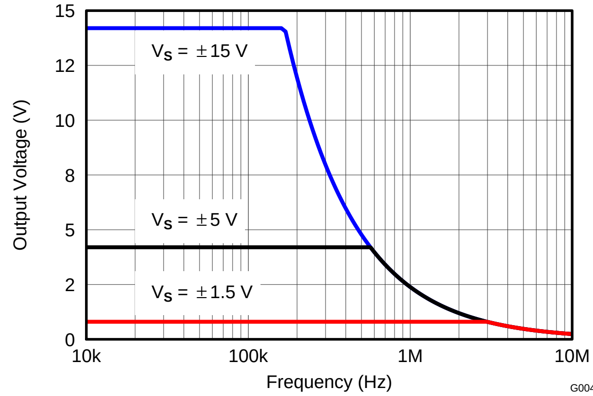


Figure 4. Maximum Output Voltage vs Frequency

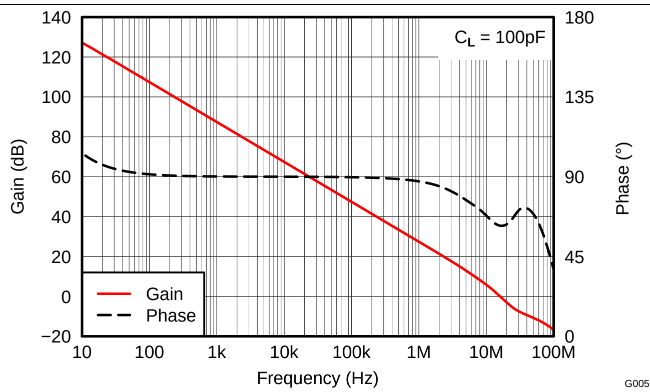


Figure 5. Gain and Phase vs Frequency

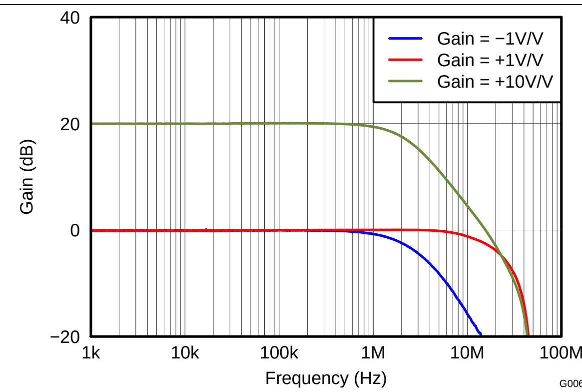


Figure 6. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

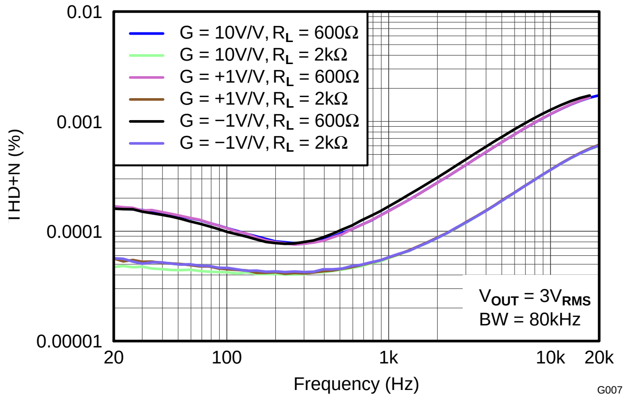


Figure 7. THD+N Ratio vs Frequency

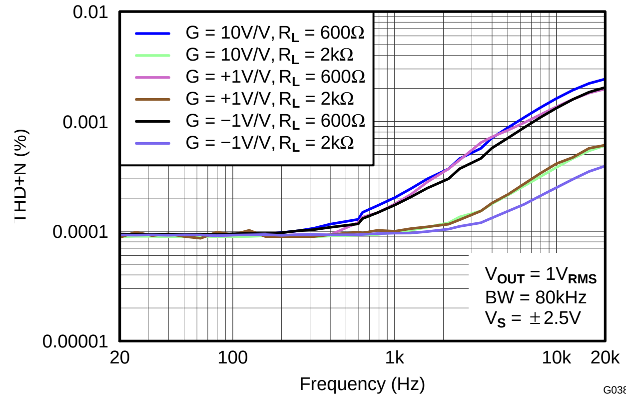


Figure 8. THD+N Ratio vs Frequency

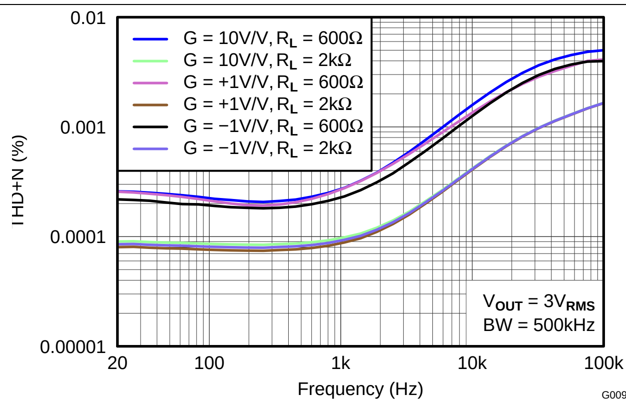


Figure 9. THD+N Ratio vs Frequency

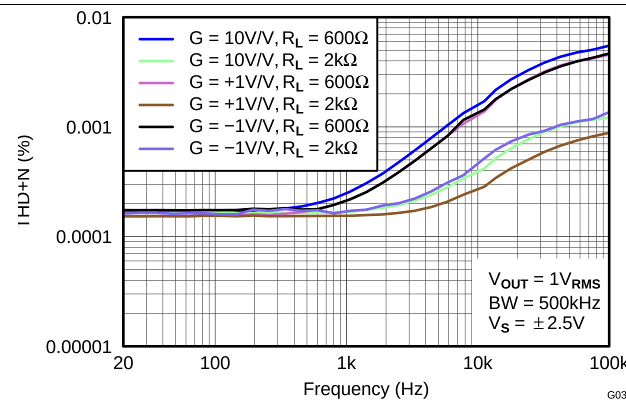


Figure 10. THD+N Ratio vs Frequency

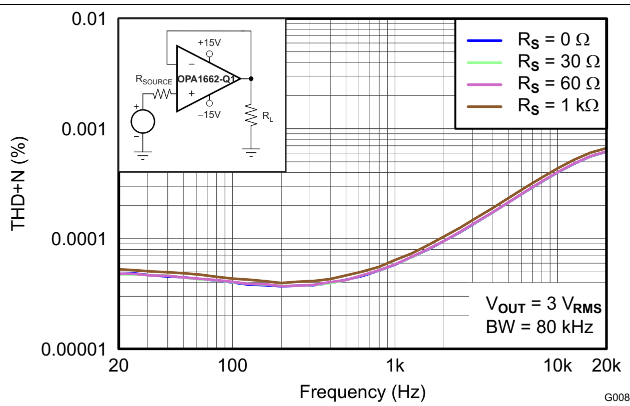


Figure 11. THD+N Ratio vs Frequency

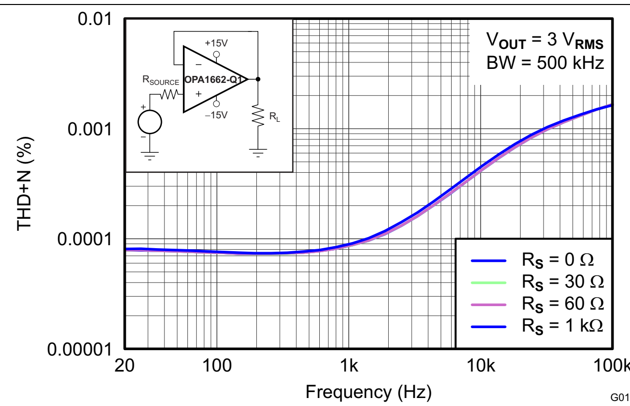


Figure 12. THD+N Ratio vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

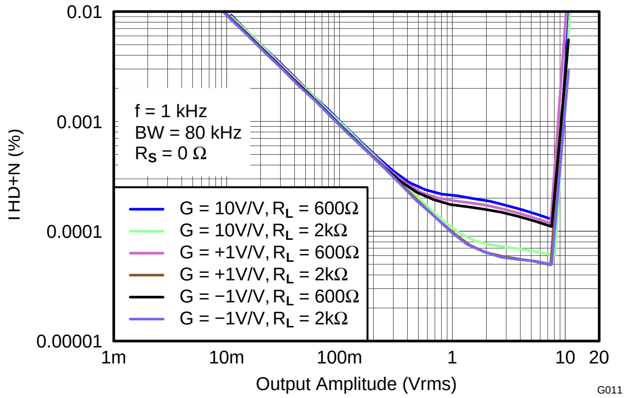


Figure 13. THD+N Ratio vs Output Amplitude

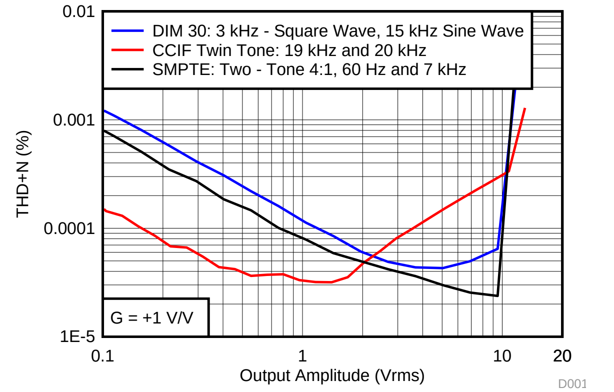


Figure 14. Intermodulation Distortion vs Output Amplitude

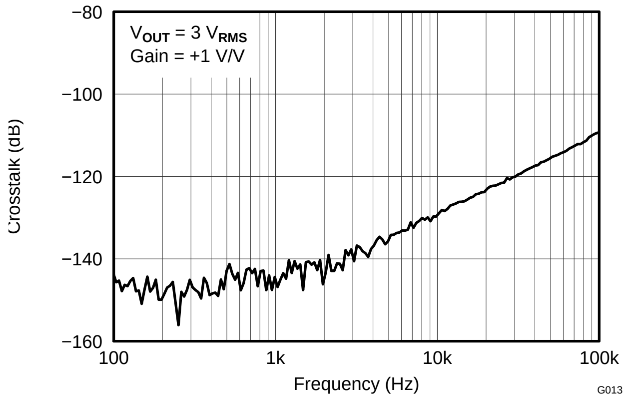


Figure 15. Channel Separation vs Frequency

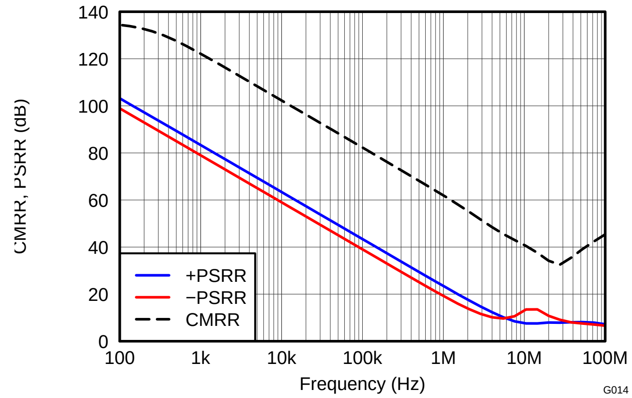


Figure 16. CMRR and PSRR vs Frequency (Referred to Input)

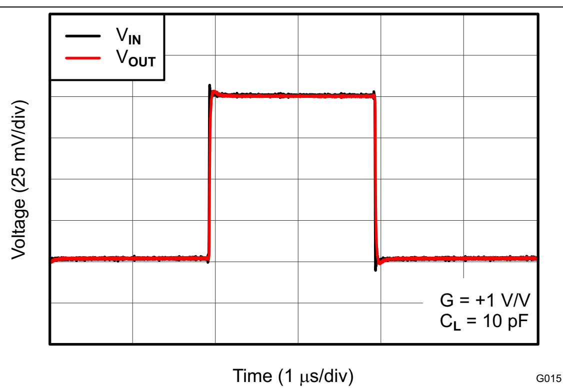


Figure 17. Small-Signal Step Response

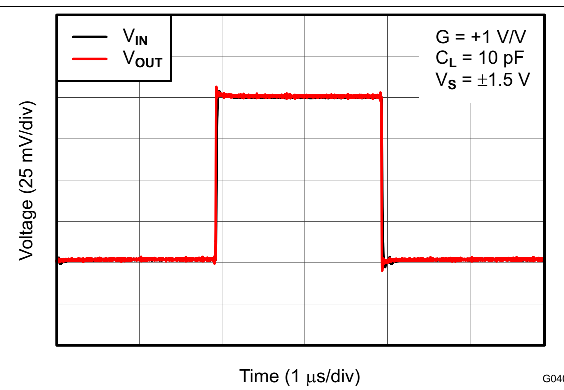


Figure 18. Small-Signal Step Response

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

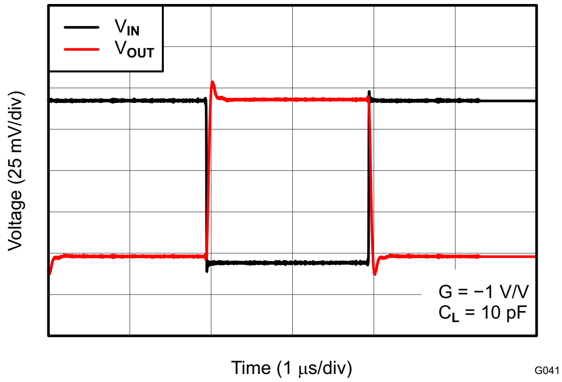


Figure 19. Small-Signal Step Response

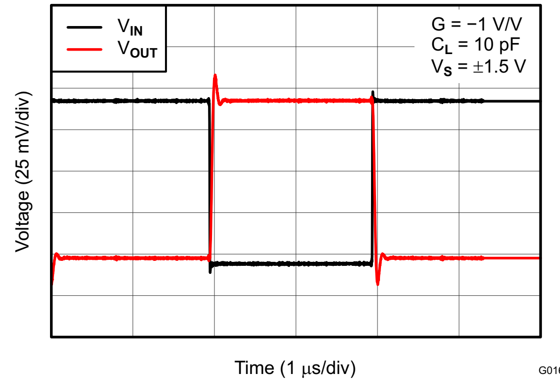


Figure 20. Small-Signal Step Response

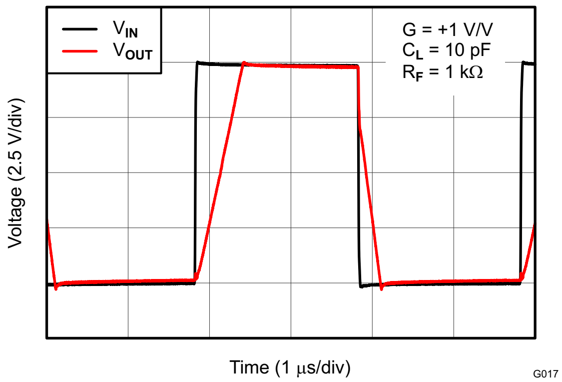


Figure 21. Large-Signal Step Response

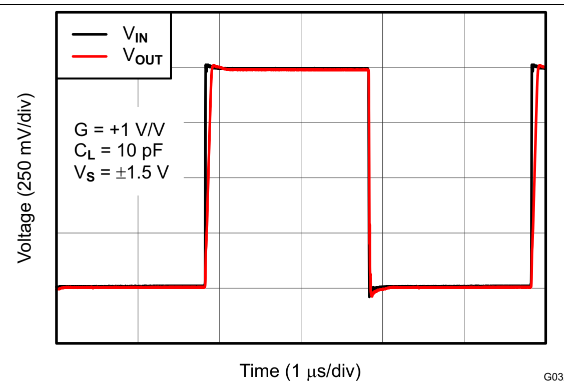


Figure 22. Large-Signal Step Response

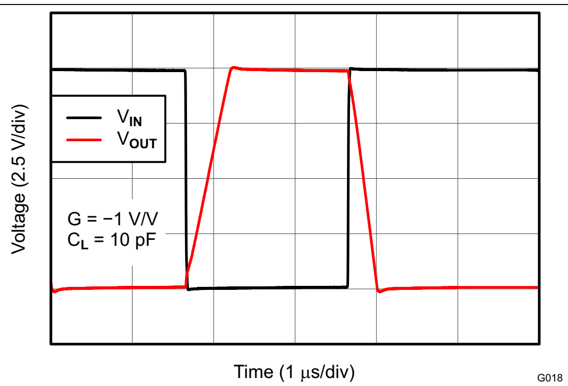


Figure 23. Large-Signal Step Response

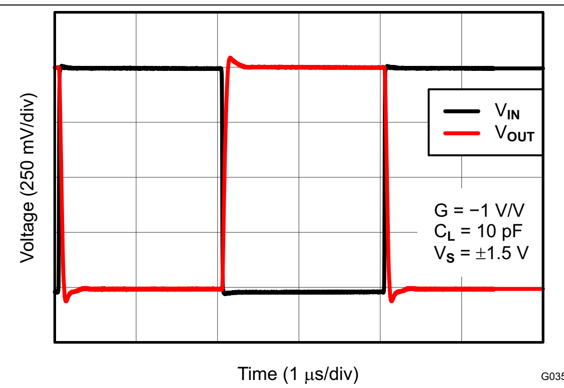


Figure 24. Large-Signal Step Response

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

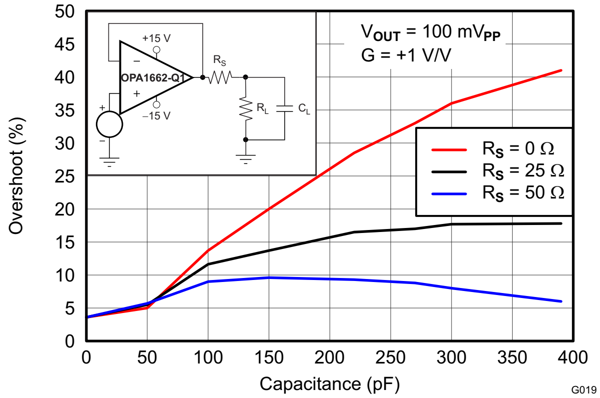


Figure 25. Small-Signal Overshoot vs Capacitive Load

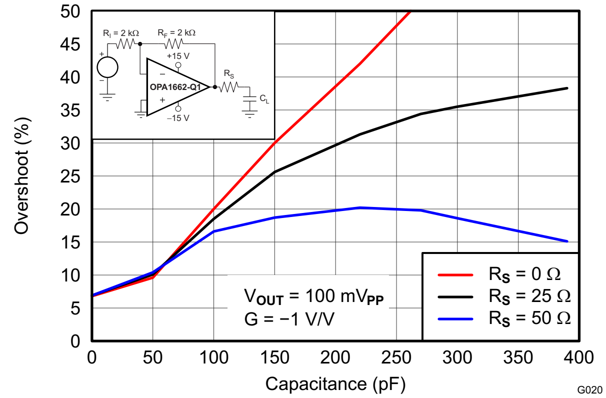


Figure 26. Small-Signal Overshoot vs Capacitive Load

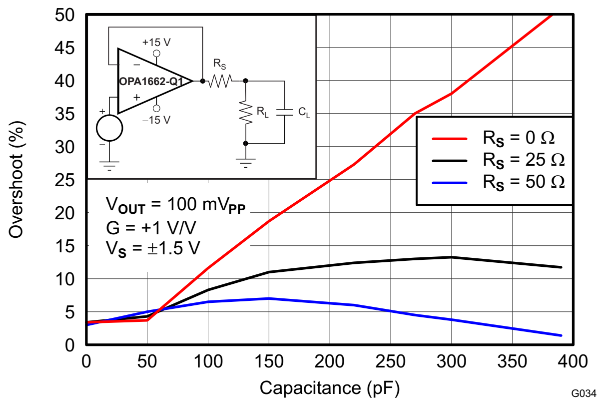


Figure 27. Small-Signal Overshoot vs Capacitive Load

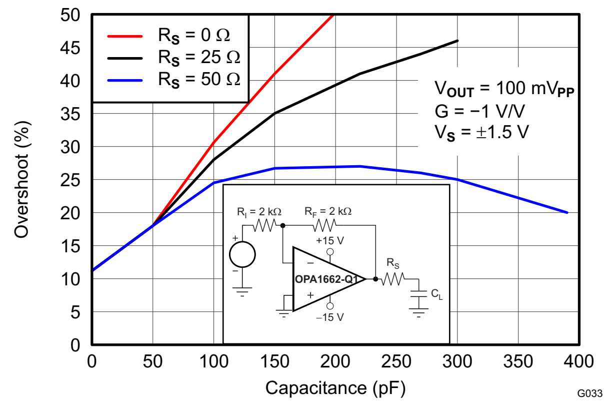


Figure 28. Small-Signal Overshoot vs Capacitive Load

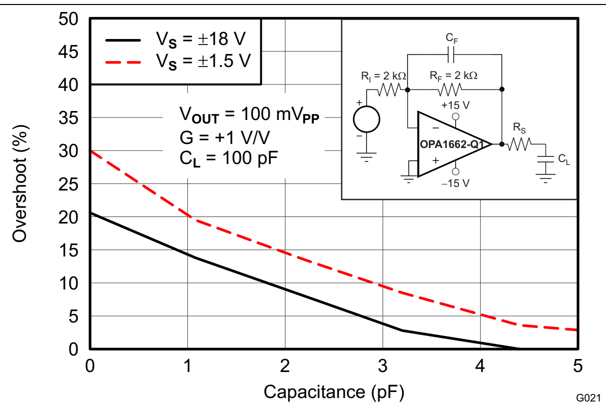


Figure 29. Small-Signal Overshoot vs Feedback Capacitor

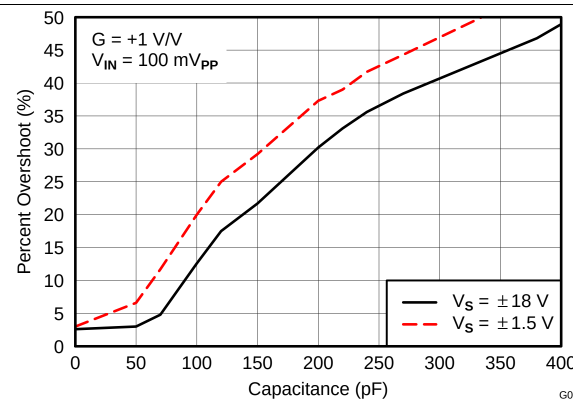


Figure 30. Percent Overshoot vs Capacitive Load

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

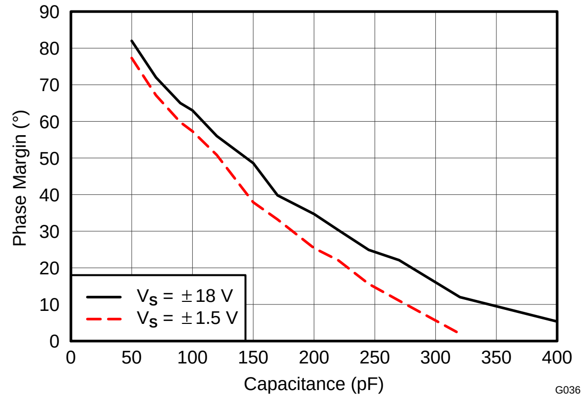


Figure 31. Phase Margin vs Capacitive Load

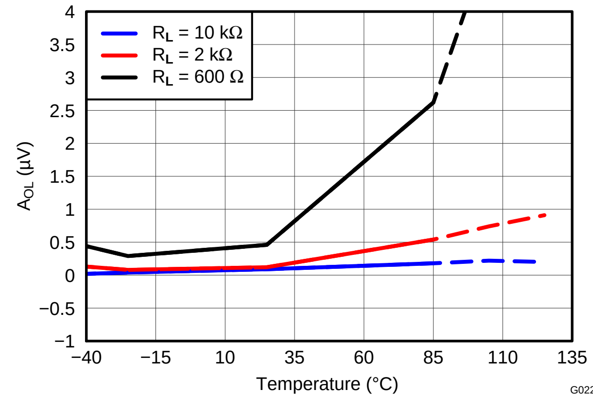


Figure 32. Open-Loop Gain vs Temperature

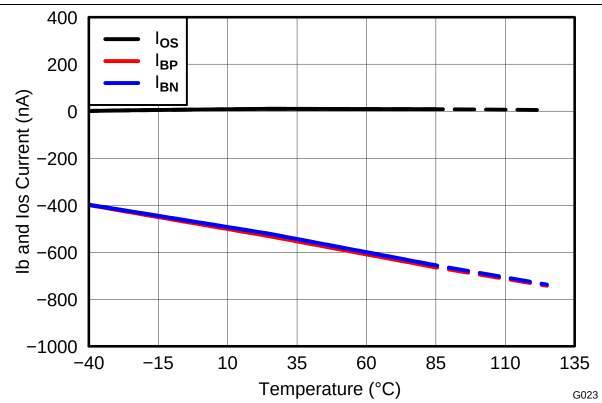


Figure 33. I_B and I_{OS} vs Temperature

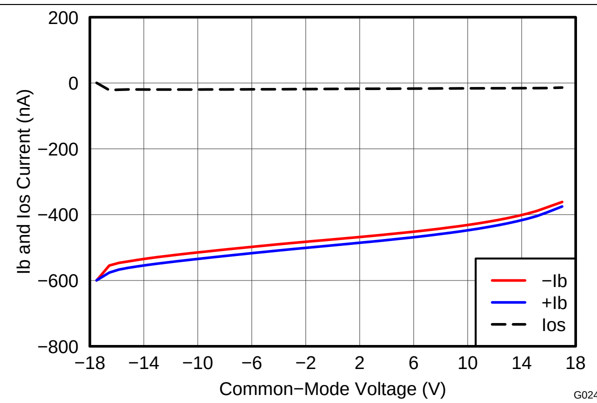


Figure 34. I_B and I_{OS} vs Common-Mode Voltage

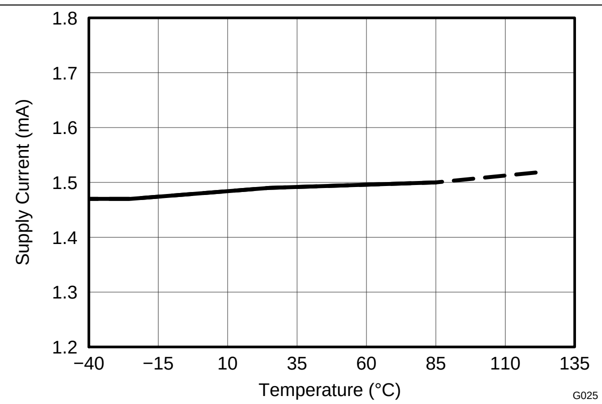


Figure 35. Supply Current vs Temperature

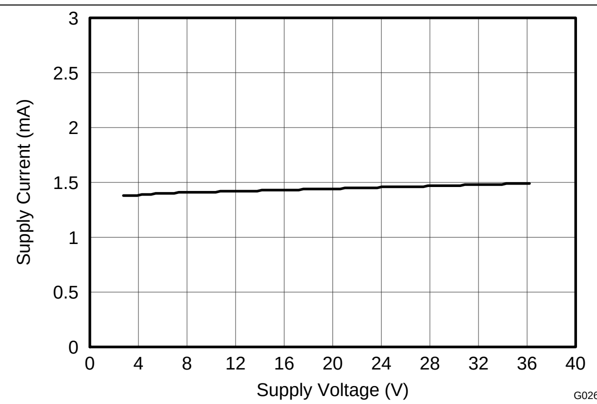


Figure 36. Supply Current vs Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

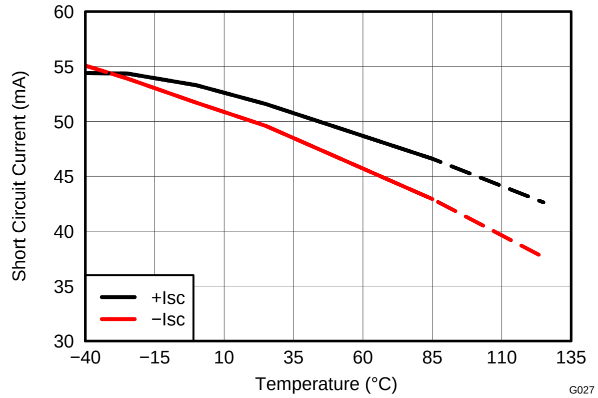


Figure 37. Short-Circuit Current vs Temperature

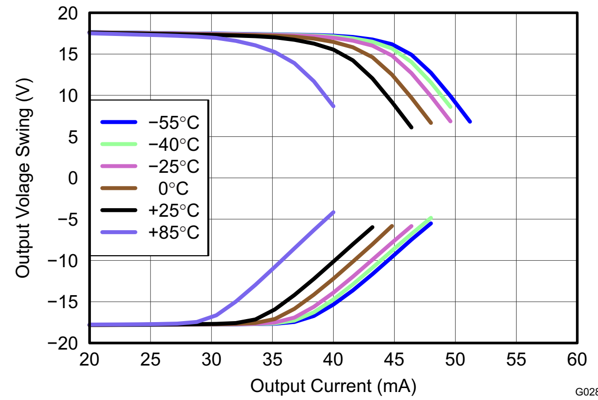


Figure 38. Output Voltage vs Output Current

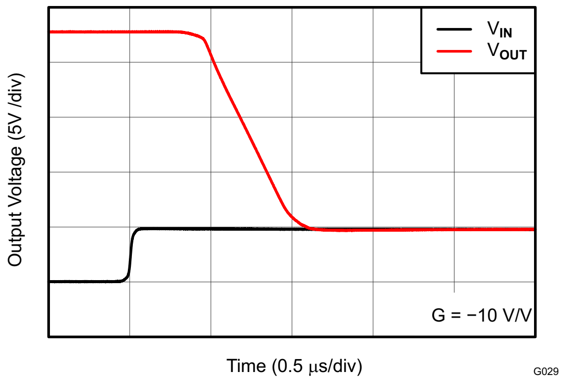


Figure 39. Positive Overload Recovery

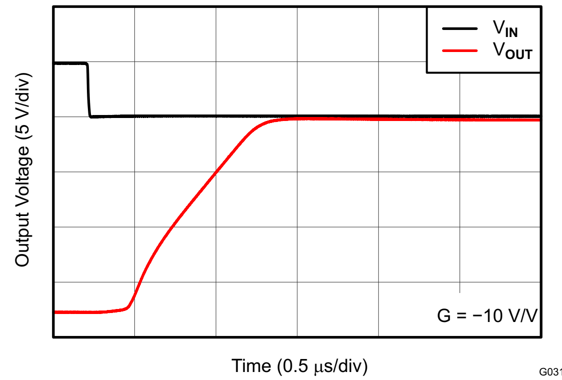


Figure 40. Negative Overload Recovery

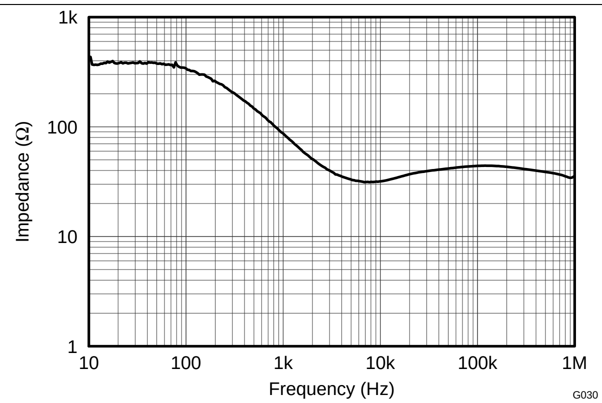


Figure 41. Open-Loop Output Impedance vs Frequency

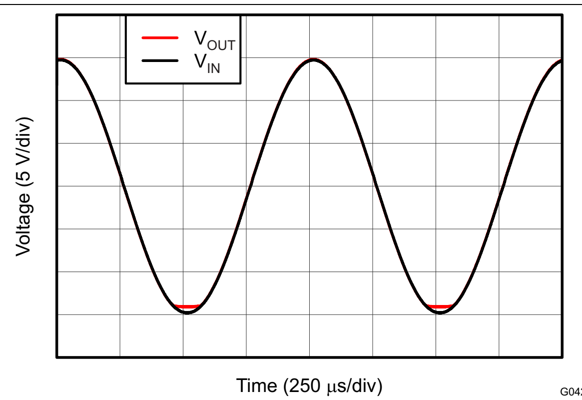


Figure 42. No Phase Reversal

8 Detailed Description

8.1 Overview

The OPA1662-Q1 operational amplifier achieves a low 3.3 nV/√Hz noise density with an ultra-low distortion of 0.00006% at 1 kHz that makes the device suitable for audio application. This device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery powered without regulation.

8.2 Functional Block Diagram

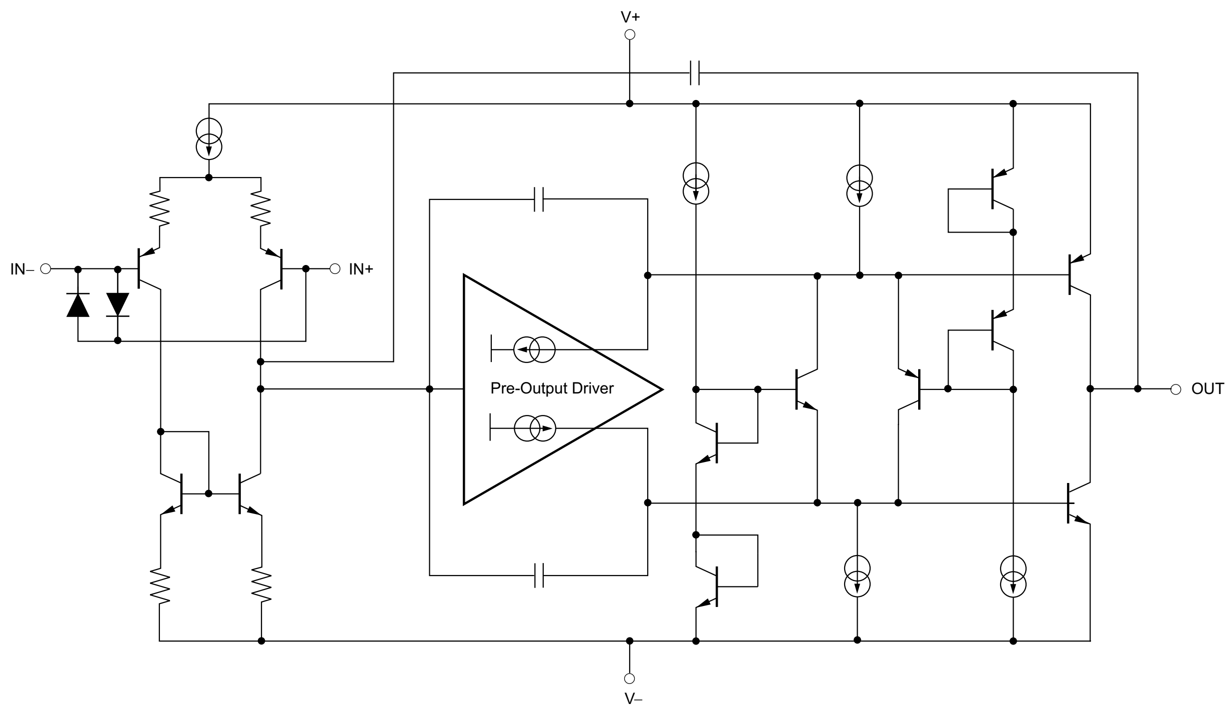


Figure 43. OPA1662-Q1 Simplified Schematic

8.3 Feature Description

8.3.1 Operating Voltage

The OPA1662-Q1 op amp operates from ±1.5-V to ±18-V supplies while maintaining excellent performance. The OPA1662-Q1 can operate with as little as 3 V between the supplies and up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA1662-Q1 device, power-supply voltages do not need to be equal. For example, the positive supply could be set to 25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature of T_A = –40°C to 85°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

Feature Description (continued)

8.3.2 Input Protection

The input terminals of the OPA1662-Q1 are protected from excessive differential voltage with back-to-back diodes, as Figure 44 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) or a feedback resistor (R_F) can be used to limit the signal input current. This resistor degrades the low-noise performance of the OPA1662-Q1 and is examined in *Noise Performance*. Figure 44 shows an example configuration when both current-limiting input and feedback resistors are used.

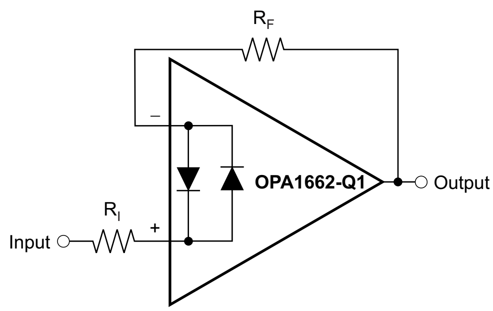
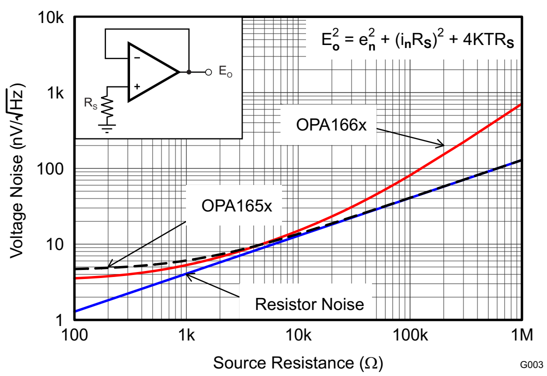


Figure 44. Pulsed Operation

8.3.3 Noise Performance

Figure 45 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA1662-Q1 (GBW = 22 MHz, G = 1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is similarly modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA1662-Q1 op amp makes them a better choice for low source impedances of less than 1 kΩ.



The equation calculates total circuit noise, where:

- e_n is the voltage noise
- i_n is the current noise
- R_S is the source impedance
- k is Boltzmann's constant = 1.38 × 10^{-23} J/K
- T is the temperature in Kelvins (K)

Figure 45. Noise Performance of the OPA1662-Q1 in Unity-Gain Buffer Configuration

Feature Description (continued)

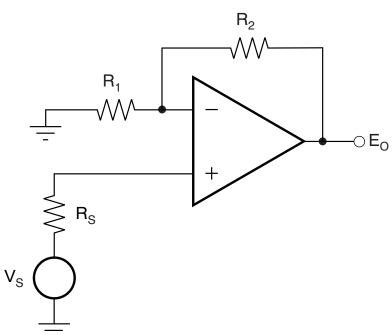
8.3.4 Basic Noise Calculations

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 45 plots this equation. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 46 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

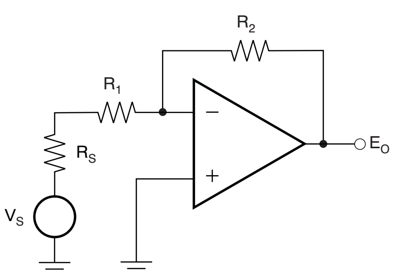
$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + \left[\frac{R_2}{R_1}\right]^2 e_1^2 + e_2^2 + \left[1 + \frac{R_2}{R_1}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_1^2 + e_2^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA1662-Q1 op amp at 1 kHz, $e_n = 3.3\ nV/\sqrt{Hz}$.

Figure 46. Noise Calculation in Gain Configurations

8.3.5 Total Harmonic Distortion Measurements

The OPA1662-Q1 op amp has excellent distortion characteristics. THD + noise is below 0.0006% (G = 1, $V_O = 3\ V_{RMS}$, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7 for characteristic performance).

The distortion produced by the OPA1662-Q1 op amp is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 47 shows) can be used to extend the measurement capabilities.

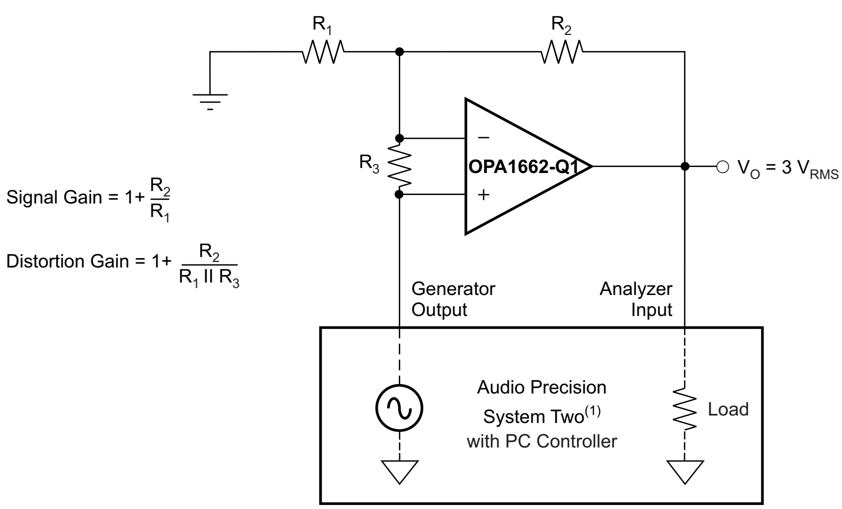
Op amp distortion can be considered an internal error source that can be referred to the input. Figure 47 shows a circuit that causes the op amp distortion to be gained up (see the table in Figure 47 for the distortion gain factor for various signal gains). The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by the distortion gain factor, thus extending the resolution by the same amount. The input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 must be kept small to minimize its effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion and noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

8.3.6 Capacitive Loads

The dynamic characteristics of the OPA1662-Q1 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 25 illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. Also see *Applications Bulletin: Feedback Plots Define Op Amp AC Performance* for details of analysis techniques and application circuits.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
+1	101	∞	1 kΩ	10 Ω
–1	101	4.99 kΩ	4.99 kΩ	49.9 Ω
+10	110	549 Ω	4.99 kΩ	49.9 Ω

(1) For measurement bandwidth, see Figure 7 through Figure 12.

Figure 47. Distortion Test Circuit

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 48 illustrates the ESD circuits contained in the OPA1662-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device internal to the OPA1662-Q1 triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, it quickly activates, clamping the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 48, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

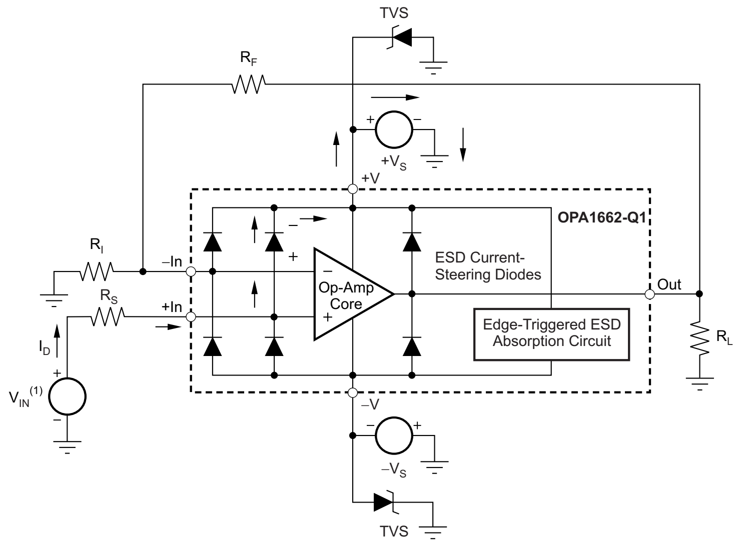
Figure 48 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, TI recommends that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 48.

The Zener voltage must be selected such that the diode does not turn on during normal operation. However, its Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500$ mV.

Figure 48. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application (Single Channel Shown)

8.4 Device Functional Modes

The OPA1662-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 3 V (±1.5 V). The maximum power supply voltage for the OPA1662-Q1 is 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA1662-Q1 is a unity-gain stable, precision dual op amp with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. Figure 43 shows a simplified schematic of the OPA1662-Q1 (one channel shown) while Figure 49 shows an additional application idea.

9.2 Typical Application

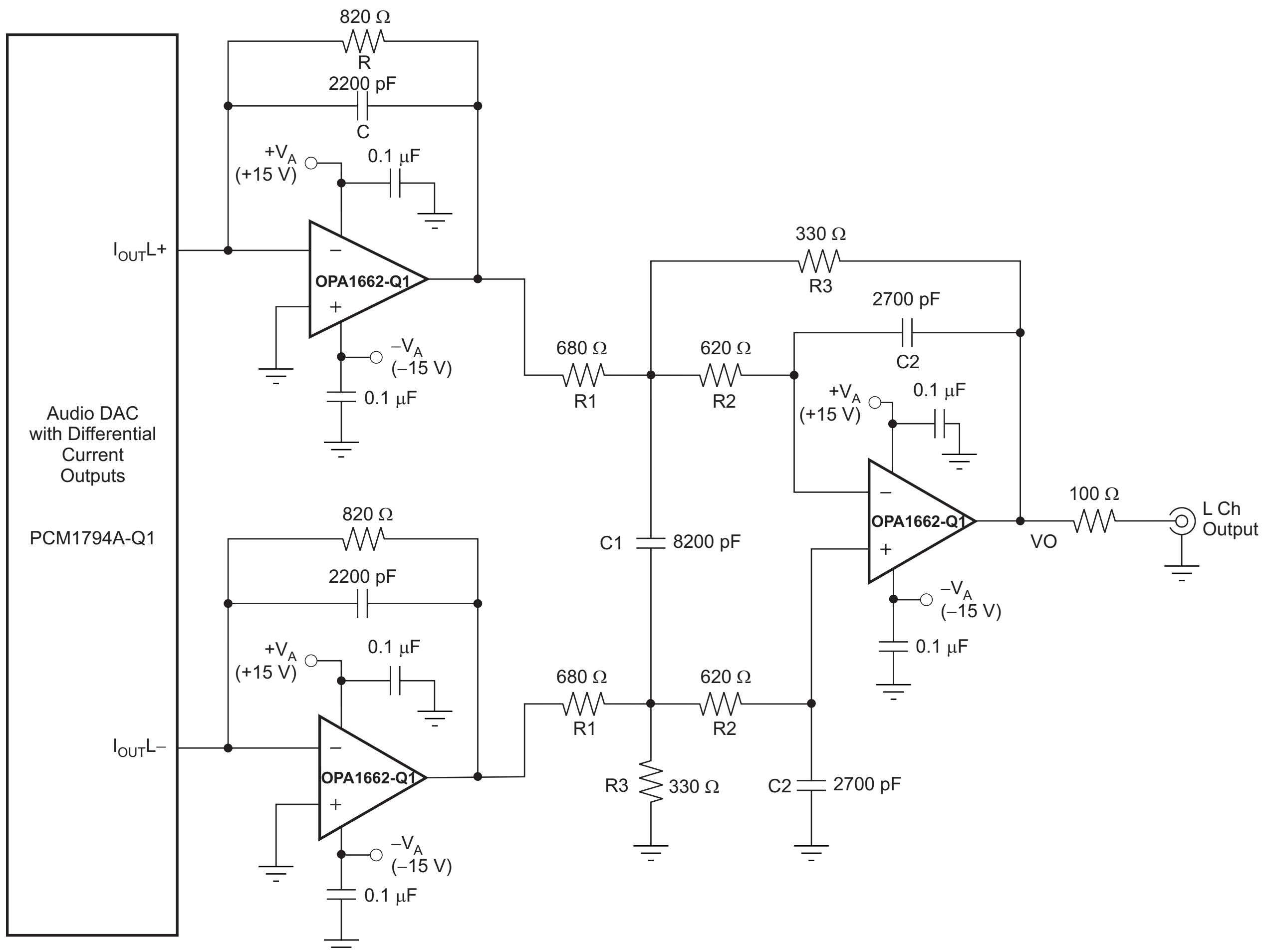


Figure 49. Audio DAC Current to Voltage Converter and Output Filter

Typical Application (continued)

9.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage	±15 V to ±36 V
Differential input currents	0 mA to 30 mA
Resistors value tolerance	1%
Ceramic capacitor	XR5 or XR7 50 V

9.2.2 Detailed Design Procedure

This circuit is designed for converting differential input current into a single ended output voltage. The resistor values are chosen to be relatively low for minimizing the total circuit noise. The filtering capacitors are chosen to maintain adequate bandwidth from 10 Hz to 20 kHz for audio signals.

The first stage converts the audio DAC output current into a voltage with a gain calculated by Equation 1:

$$\frac{R}{1+RCS}$$

where

- R = 820 Ω
- C = 2200 pF
- S is Laplace variable (1)

RC filters the audio DAC output ripple and cutoff frequency = $\frac{1}{2\pi RC}$ = 80 KHz

The second differential stage transfer function is calculated by Equation 2:

$$\frac{R3}{R1}\left(\frac{1}{1+\frac{R2R3}{R1//R2//R3}C2S+2R2R3C1C2S^2}\right) \quad (2)$$

The denominator of this transfer function $1+\frac{R2R3}{R1//R2//R3}C2S+2R2R3C1C2S^2$ is a quadratic equation and the general form is calculated by Equation 3:

$$1+\frac{S}{Q\omega o}+\frac{S^2}{Q\omega o^2}$$

where

- $\omega o = 2\pi Fo$ is the resonance frequency
- and Q is the quality factor (3)

The gain peak depends on the quality factor in Equation 4:

$$Q = R1//R2//R3\sqrt{2\frac{1}{R2R3}\times\frac{C1}{C2}} \quad (4)$$

The resonance frequency is calculated by Equation 5:

$$\omega o = 2\pi Fo = \sqrt{\frac{1}{2R2R3C1C2}} \quad (5)$$

These equations help to maintain adequate bandwidth and keep the differential gain flat so the quality factor is from 0.7 to 1. The resonance frequency must be at least twice the desired bandwidth.

The chosen components give a quality factor of 0.89 and a resonance frequency of 53 KHz.

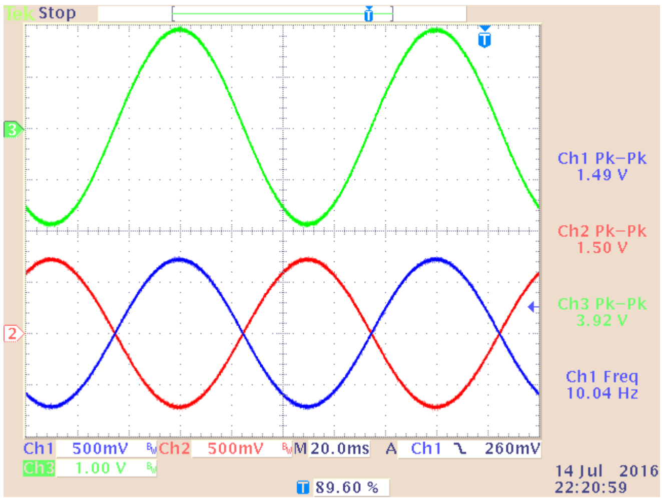
The overall transfer function is shown in Equation 6:

$$\frac{vo}{IoutL+\ -\ IoutL-} = \frac{R}{1+RCS} \times \frac{R3}{R1} \times \frac{1}{1+\frac{R2R3}{R1//R2//R3}C2S+2R2R3C1C2S^2} \quad (6)$$

The $DC\ gain = \frac{RR3}{R1}$ and is 398 mV/mA.

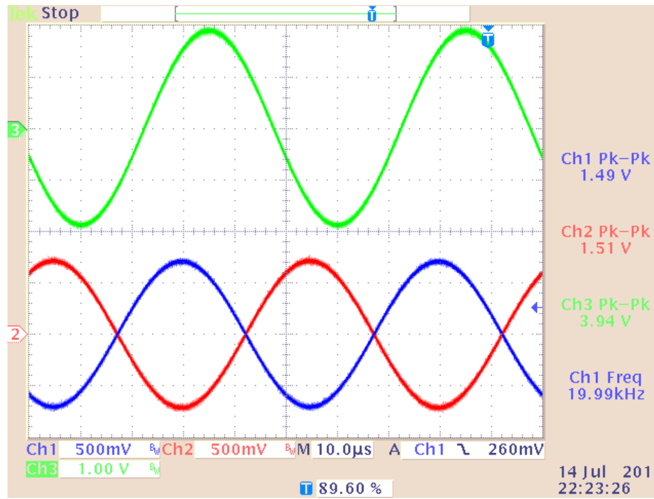
The poles are at 53 KHz and 80 KHz.

9.2.3 Application Curves



CH1 = positive input current $I_{OUT}L+$ = 1.5 V / 150 Ω
CH2 = negative input current $I_{OUT}L-$ = 1.5 V / 150 Ω
CH3 = output single-ended voltage

Figure 50. Output Voltage at 10 mApp and 10 Hz



CH1 = positive input current $I_{OUT}L+$ = 1.5 V / 150 Ω
CH2 = negative input current $I_{OUT}L-$ = 1.5 V / 150 Ω
CH3 = output single-ended voltage

Figure 51. Output Voltage at 10 mApp and 20 KHz

10 Power Supply Recommendations

The OPA1662-Q1 is specified for operation from 3 V to 36 V (±1.5 V to 18 V) and at an ambient operating temperature from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

11 Layout

11.1 Layout Guidelines

The OPA1662-Q1 is a unity-gain stable, precision dual op amp with very low noise. To realize the full operational performance of the device, good high-frequency printed-circuit board (PCB) layout practices are required. Low-loss, 0.1-µF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces must be designed for minimum inductance.

11.2 Layout Example

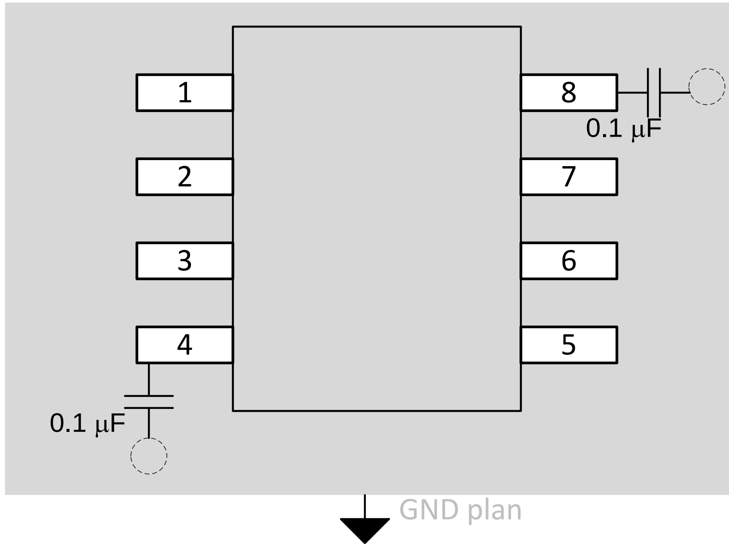


Figure 52. Layout Recommendation

11.3 Power Dissipation

The OPA1662-Q1 op amp is capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA1662-Q1 op amp improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《应用 公告：反馈曲线图定义运算放大器交流性能》*(SBOA015)
- *《用于电流输出音频 DAC 的高功率高保真耳机放大器参考设计》*(TIDU672)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA1662AIDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OUUI
OPA1662AIDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	OUUI
OPA1662AIDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O1662Q
OPA1662AIDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O1662Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA1662-Q1 :

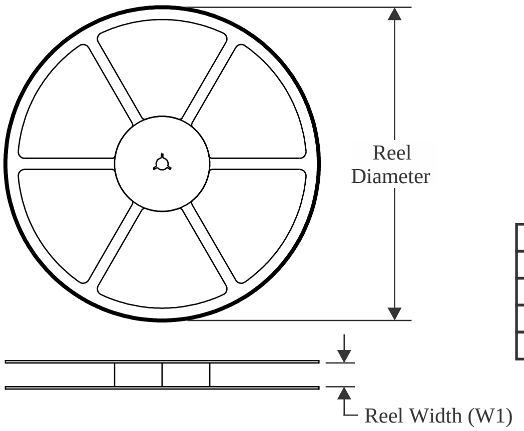
- Catalog : OPA1662

NOTE: Qualified Version Definitions:

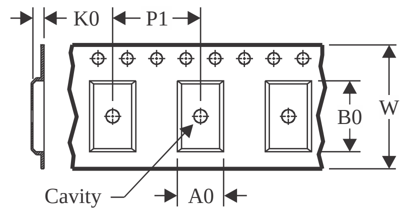
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

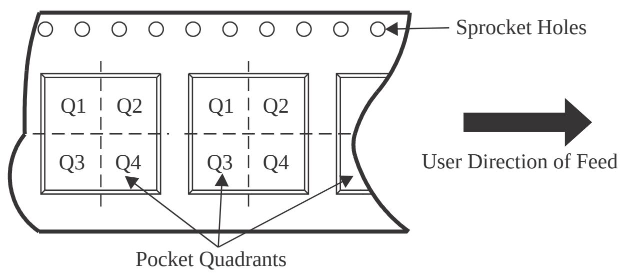


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

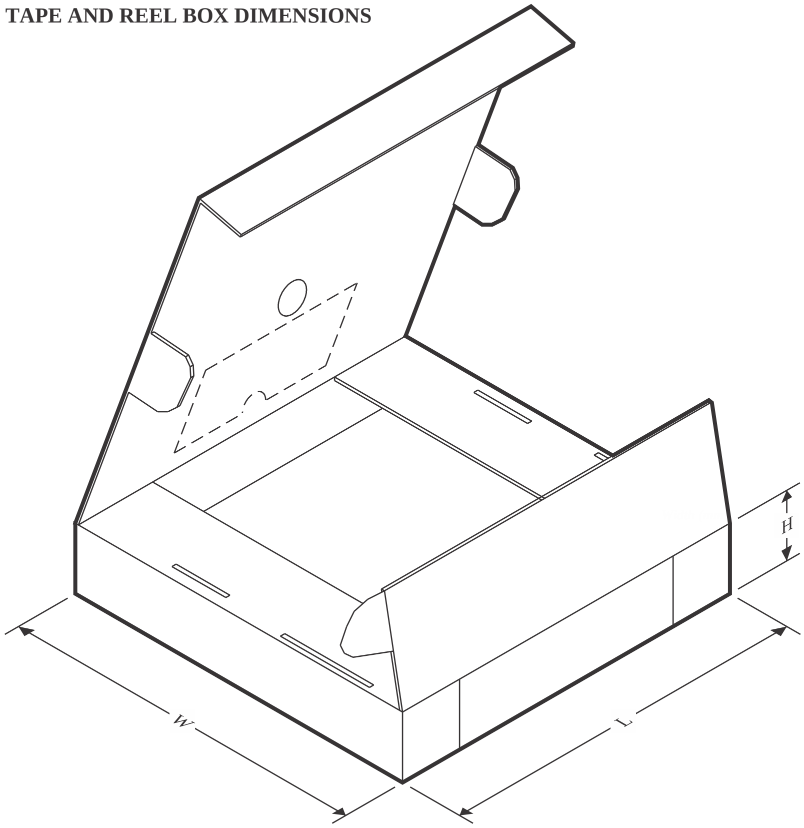
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

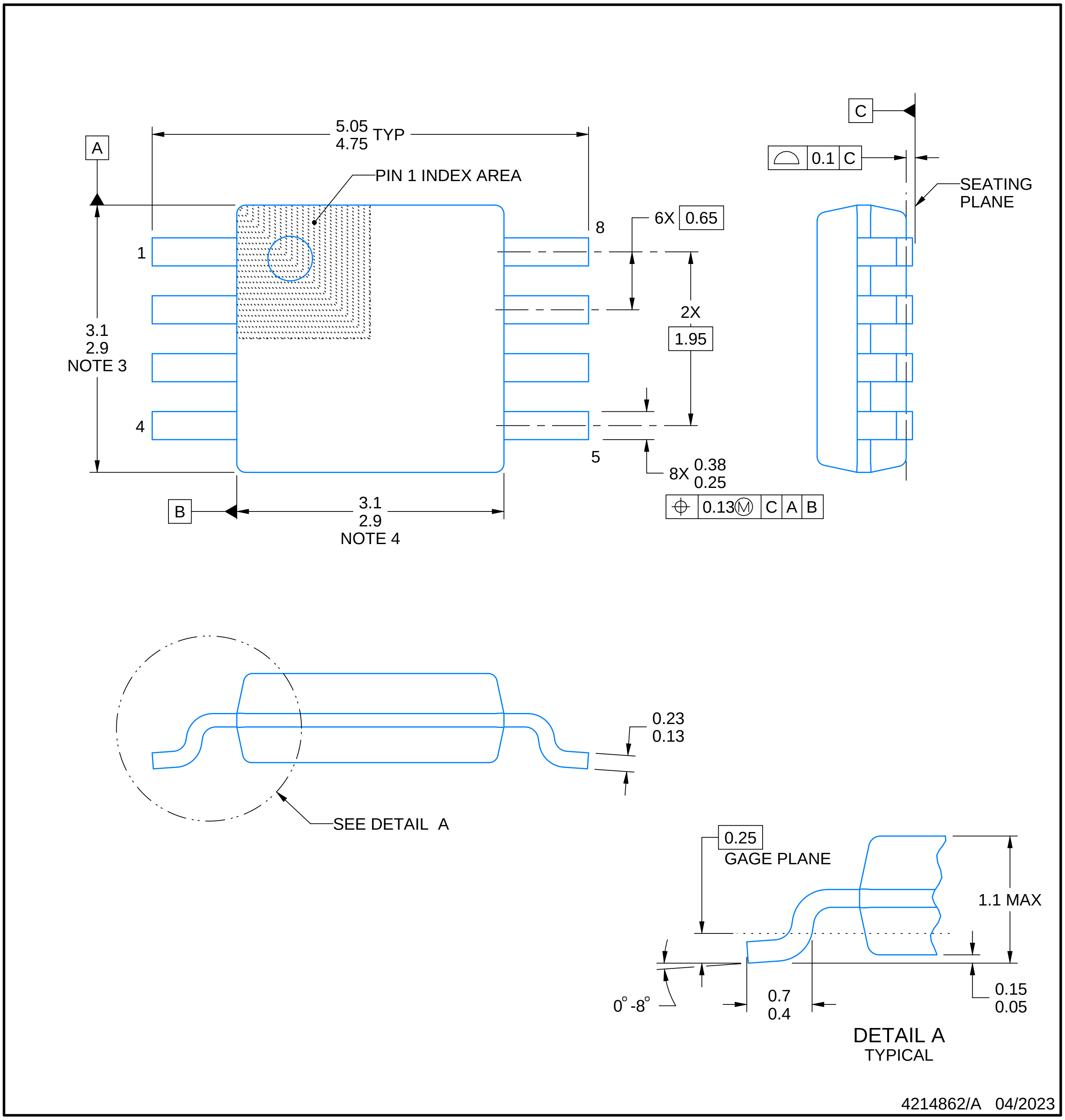
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1662AIDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1662AIDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1662AIDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1662AIDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1662AIDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1662AIDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

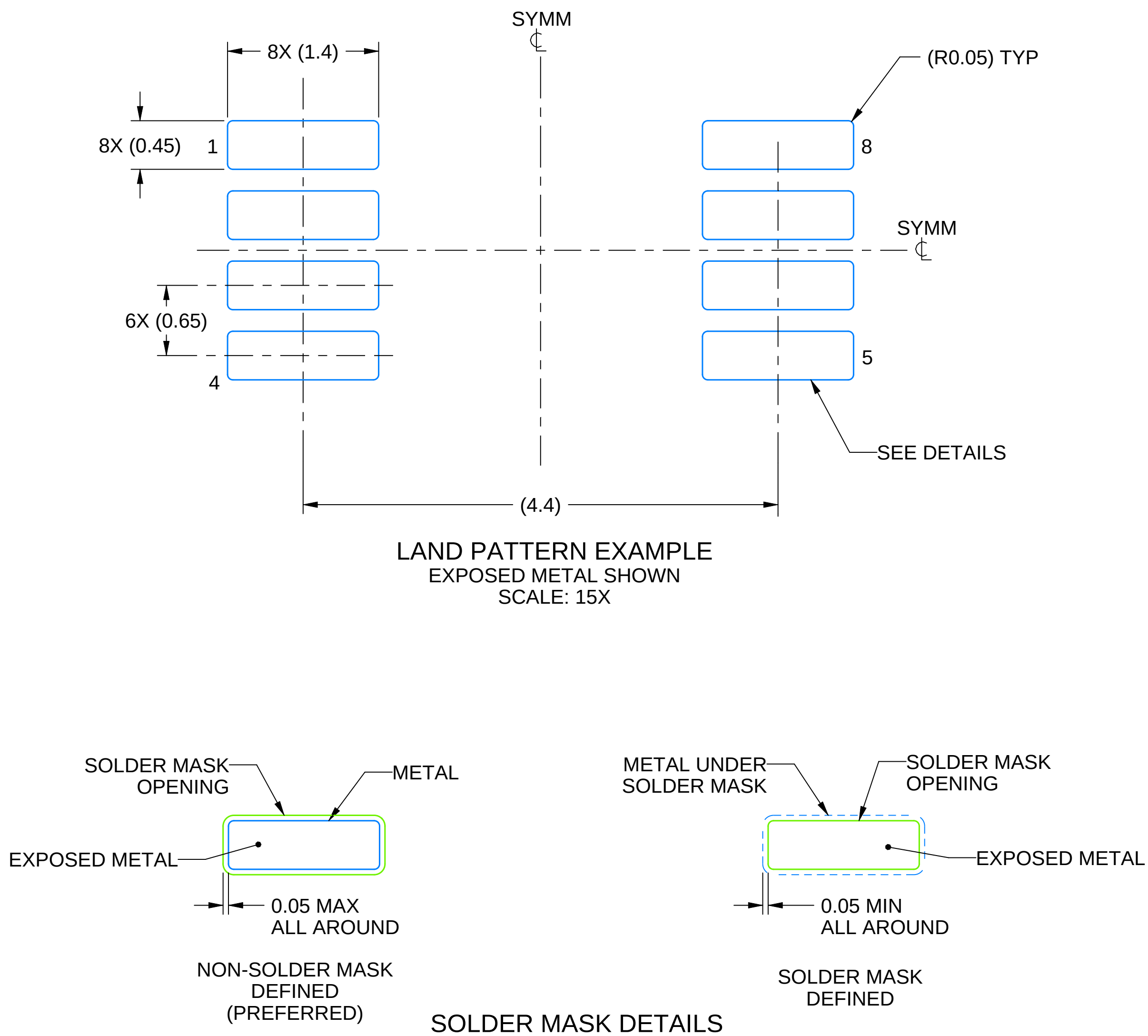


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



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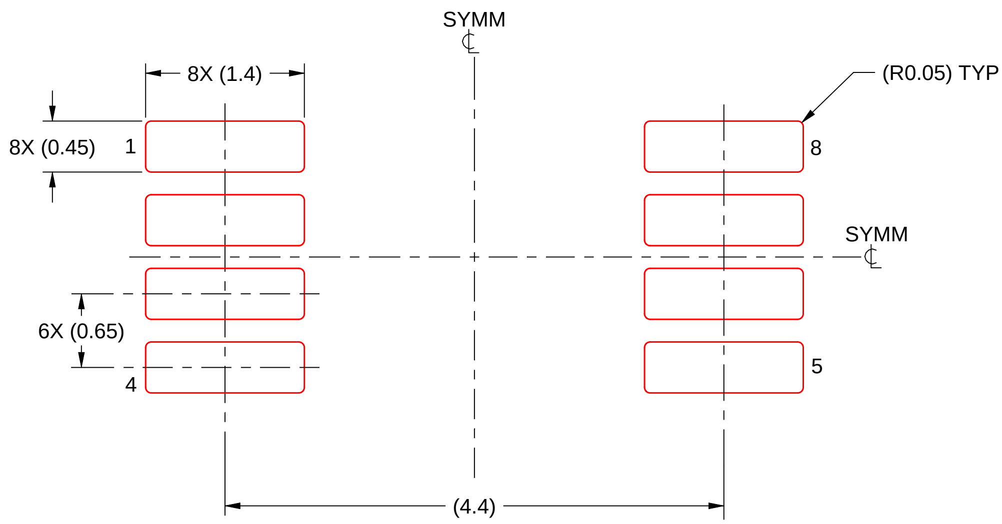
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

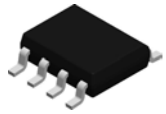


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

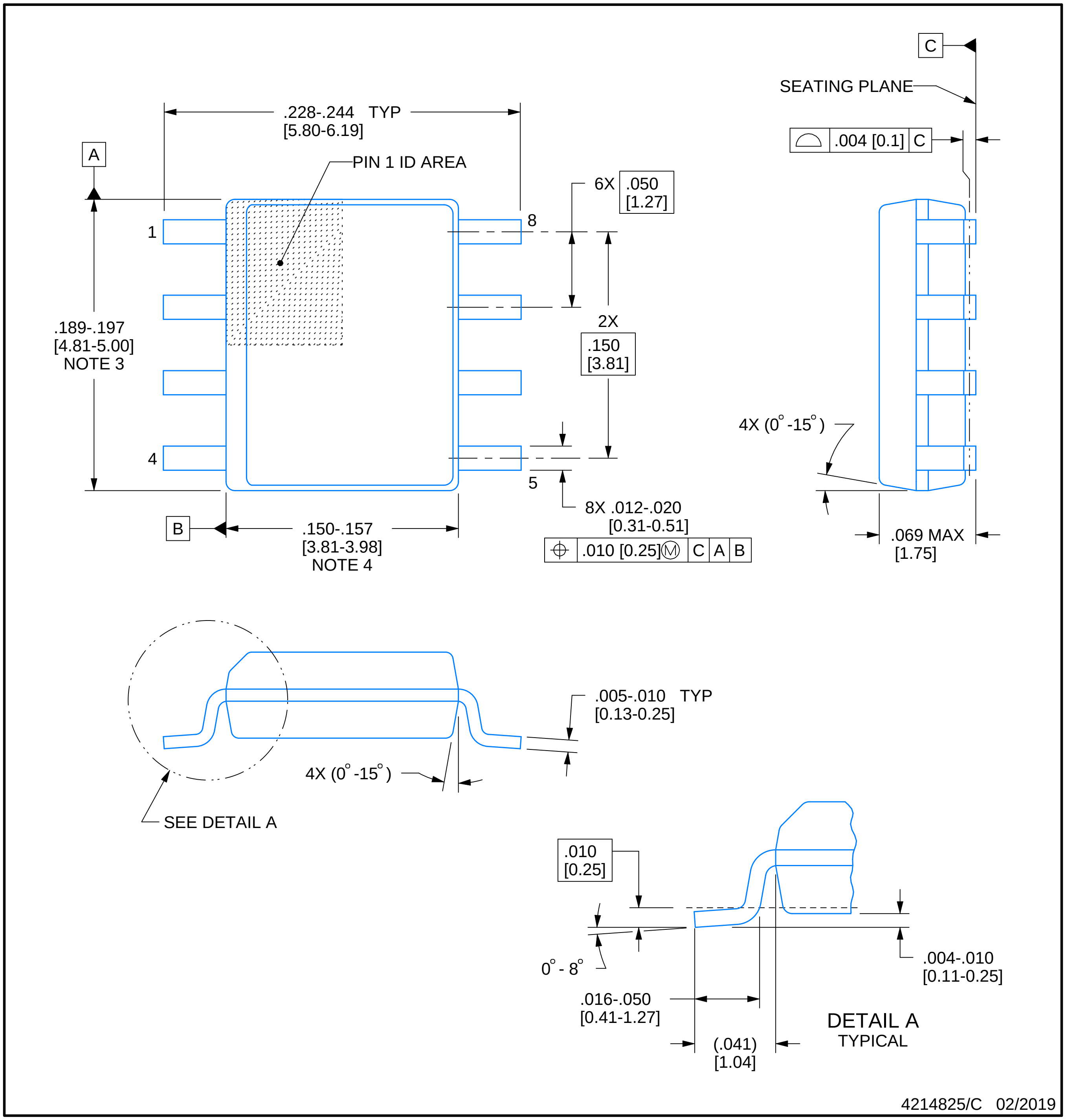
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

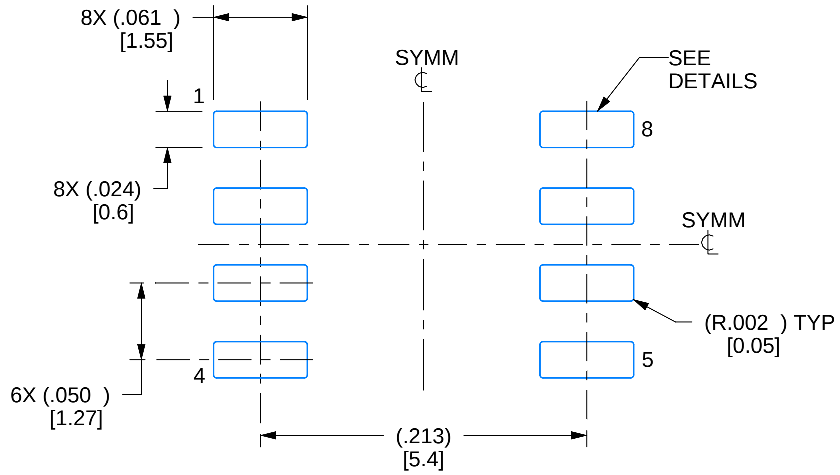
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

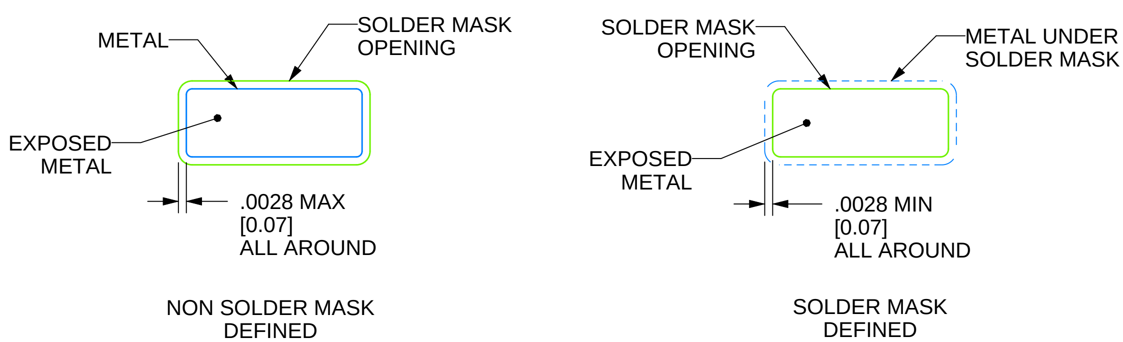


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

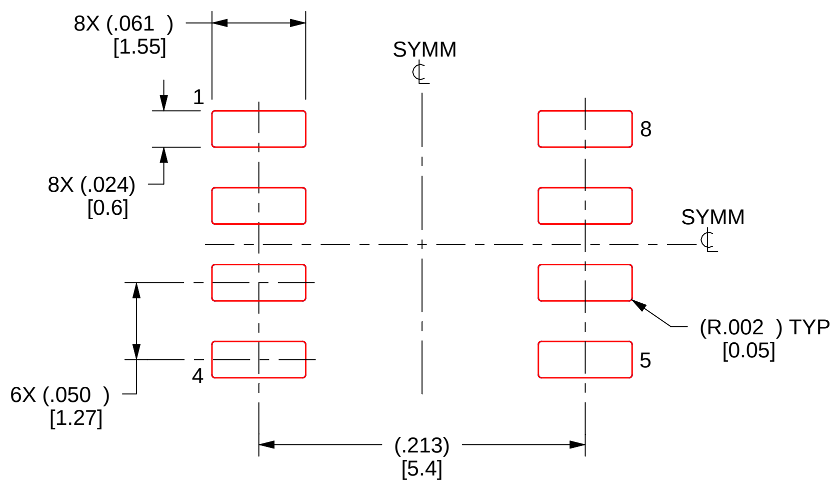


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明