具有输出波形整形的 11.35Gbps 差分调制器驱动器

查询样品: ONET1151M

特性

- **1.5V$_{PP}$**单端输出电压进入一个 **50Ω** 负载
- 可编程输入均衡器
- 输出预加重
- 可调上升和下降时间
- 交叉点控制
- 输出极性选择
- **2** 线制数字接口
- **3.3V** 单电源
- **-40°C** 至 **100°C** 运行
- 表明贴装 **3mm x 3mm 16** 引脚符合 **RoHS** 环保标准的四方扁平无引线 **(QFN)** 封装

应用范围

- **SONET OC-192/SDH STM-64** 光发射器
- **10G** 以太网光发射器
- **SFP+** 和 **XFP** 收发器模块

说明

ONET1151M 是一款高速，3.3V 调制器驱动器，此驱动器设计用来调制一个数据速率介于 1Gbps 到最高 11.35Gbps 的差分驱动马赫-曾德尔 (Mach Zehnder) 调制器。

可使用一个外部施加的电压来控制输出摆幅。 一个 2 线制接口可实现对均衡器、输出预加重、眼图交叉点、上升和下降时间以及摆幅的数字控制，从而免除了对于外部组件的需要。 提供以预加重、交叉点调整以及上升和下降时间调整的形式进行输出波形控制来改进光眼图模板容限。

一个 5GHz 时具有 10dB 提升的可选输入均衡器可被用于实现FR4 印刷电路板上微带线和带状线传输线路的高达 300mm（12 英寸）的均衡。

此调制器驱动器可在外壳温度介于 -40°C 至 100°C 时运行并采用一个小型封装 3mm x 3mm 16 引脚并与 RoHS 环保标准兼容的 QFN 封装。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM

Figure 1 shows a simplified block diagram of the ONET1151M. The modulator driver consists of an equalizer, a limiter, an output driver, power-on reset circuitry, a 2-wire serial interface including a control logic block, a modulation current generator, and an analog reference block.

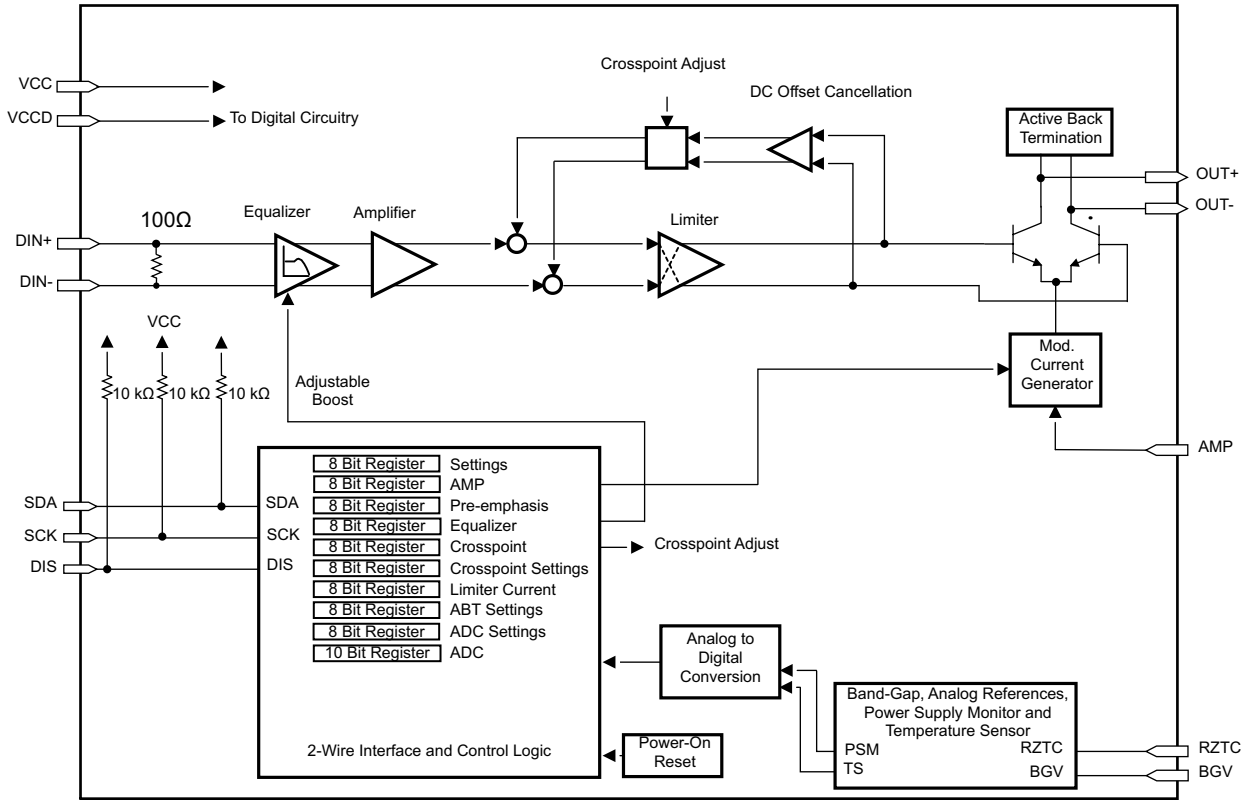


Figure 1. Simplified Block Diagram of the ONET1151M

PACKAGE

The ONET1151M is packaged in a small footprint 3-mm × 3-mm 16-pin RoHS compliant QFN package with a lead pitch of 0.5 mm.

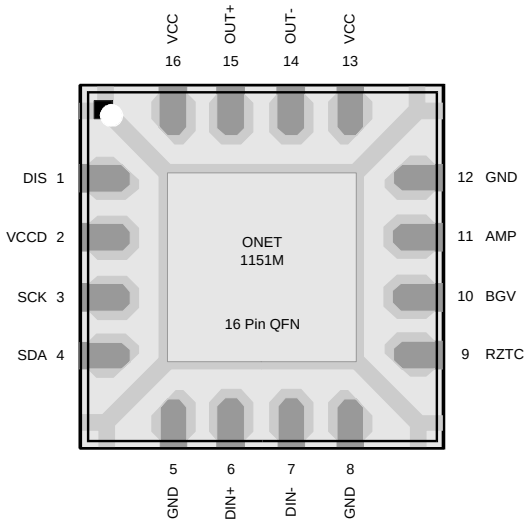


Figure 2. 16-Pin QFN Package, 3-mm x 3-mm (Top View)

Table 1. PIN DESCRIPTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
DIS	1	Digital–in	Disables bias, modulation, and peaking currents when set to high state. Includes a 10-kΩ or 40-kΩ pullup resistor to VCC.
VCCD	2	Supply	3.3 V ± 10% supply voltage for the digital logic. Connect to VCC.
SCK	3	Digital–in	2-wire interface serial clock. Includes a 10-kΩ or 40-kΩ pullup resistor to VCC.
SDA	4	Digital–in/out	2-wire interface serial data input. Includes a 10-kΩ or 40-kΩ pullup resistor to VCC.
GND	5, 8, 12	Supply	Circuit ground
DIN+	6	Analog–in	Non-inverted data input. On-chip differentially 100-Ω terminated to DIN–. Must be AC coupled.
DIN–	7	Analog–in	Inverted data input. On-chip differentially 100-Ω terminated to DIN+. Must be AC coupled.
RZTC	9	Analog	Connect external zero TC 28.7-kΩ resistor to ground (GND). Used to generate a defined zero TC reference current for internal DACs.
BGV	10	Analog–out	Buffered bandgap voltage with 1.16-V output. This is a replica of the bandgap voltage at RZTC.
AMP	11	Analog–in	Output amplitude control. Output amplitude can be adjusted by applying a voltage of 0 to 2.5 V to this pin.
VCC	13, 16	Supply	3.3 V ± 10% supply voltage. Connect to VCCD.
OUT-	14	CML–out (current)	Inverted data output
OUT+	15	CML–out (current)	Non-inverted data output
EP	EP	Thermal	Exposed die pad (EP) must be grounded.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VALUE		UNIT
		MIN	MAX	
V_{CC}	Supply voltage(2)	–0.3	4	V
V_{DIS}, V_{RZTC}, V_{SCK}, V_{SDA}, V_{BGV}, V_{AMP}, V_{DIN+}, V_{DIN-}, V_{OUT+}, V_{OUT-}	Voltage at DIS, RZTC, SCK, SDA, BGV, AMP, DIN+, DIN-, OUT+, OUT- (2)	–0.3	4	V
I_{DIN-}, I_{DIN+}	Max. current at input pins		25	mA
I_{MOD+}, $I_{MOD–}$	Max. current at output pins		35	mA
ESD	ESD rating at all pins except OUT+ and OUT-		2	kV (HBM)
	ESD rating at OUT+ and OUT-		1.5	kV (HBM)
$T_{J, max}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range	–65	150	°C
T_C	Case temperature	-40	110	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.97	3.3	3.63	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA	2			V
V_{IL}	Digital input low voltage	DIS, SCK, SDA			0.8	V
R_{RZTC}	Zero TC resistor value(1)	1.16-V bandgap bias across resistor, E96, 1% accuracy	28.4	28.7	29	kΩ
V_{IN}	Differential input voltage swing		150		1200	mV_{p-p}
V_{AMP}	Amplitude control input voltage range		0		2.5	V
t_{R-IN}	Input rise time	20%–80%		30	55	ps
t_{F-IN}	Input fall time	20%–80%		30	55	ps
T_C	Temperature at thermal pad		–40		100	°C

(1) Changing the value alters the DAC ranges and the current consumption.

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions with 50-Ω output load, V_{OUT+} = 1.5 V_{PP} and R_{RZTC} = 28.7 kΩ, unless otherwise noted. Typical operating condition is at 3.3 V and T_A = 25°C

PARAMETER		CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.97	3.3	3.63	V
I_{VCC}	Supply current	V_{CC} = 3.47 V, PKENA = 1			100	mA
		V_{CC} = 3.63 V, PKENA = 1			105	
P	Power Dissipation	V_{CC} = 3.47 V, PKENA = 1			347	mW
		V_{CC} = 3.63 V, PKENA = 1			381	
R_{IN}	Data input resistance	Differential between DIN+ / DIN-	80	100	120	Ω
I_{IH}	High level digital input current	SCK, SDA, DIS set to V_{CC} (1)	–10		10	µA
I_{IL}	Low level digital input current	SCK, SDA, DIS set to GND (1)	–500		500	µA
V_{CC-RST}	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset	2.3	2.5	2.8	V
$V_{CC-RSTHYS}$	V_{CC} reset threshold voltage hysteresis			100		mV

(1) Assured by simulation over process, supply and temperature variation

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions with 50-Ω output load, V_{OUT+} = 1.5 V_{PP} and R_{RZTC} = 28.7 kΩ unless otherwise noted. Typical operating condition is at V_{CC} =3.3 V and T_A = 25°C.

PARAMETER		CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
	Data rate				11.35	Gbps
SDD11	Differential input return gain	0.01 GHz < f < 5 GHz		–15		dB
		5 GHz < f < 11.1 GHz		–8		
SCD11	Differential to common mode conversion gain	0.01 GHz < f < 11.1 GHz		–15		dB
V_{O-MIN}	Minimum output amplitude	50-Ω load, single-ended			300	mV_{PP}
V_{O-MAX}	Maximum output amplitude	50-Ω load, single-ended, OASH0 = OASH1 = 0	1.4			V_{PP}
	Output amplitude stability	50-Ω load, single-ended			200	mV
t_{R-OUT}	Output rise time	20% – 80%, t_{R-IN} < 40 ps, 50-Ω load, single-ended, cross point = 50%. (1)		26	36	ps
t_{F-OUT}	Output fall time	20% – 80%, t_{F-IN} < 40 ps, 50-Ω load, single-ended, cross point = 50%. (1)		26	36	ps
ISI	Intersymbol interference (2)	EQENA = 0, K28.5 pattern at 11.35 Gbps, 150-mV_{PP}, 600-mV_{PP}, 1200-mV_{PP} differential input voltage, single-ended output. 750 $mV_{PP} \le V_{OUT} \le$ 1.5 V_{PP}		5	10	ps_{p-p}
		EQENA = 1, K28.5 pattern at 11.35 Gbps with 12-inch transmission line at the input, 150-mV_{PP}, 600-mV_{PP}, 1200-mV_{PP} input to transmission line, single-ended output. 750 $mV_{PP} \le V_{OUT} \le$ 1.5 V_{PP}.		6		
RJ	Random output jitter	EQENA = 0		0.3	0.6	ps_{RMS}
	High cross point control range	50-Ω load, single-ended		75		%
	Low cross point control range	50-Ω load, single-ended		25		%

(1) 1010 pattern with PKENA = 1 and PEADJ (Register 2) set to 0x0F.
(2) Jitter at the eye crossing point.

AC ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions with 50-Ω output load, V_{OUT+} = 1.5 V_{PP} and R_{RZTC} = 28.7 kΩ unless otherwise noted. Typical operating condition is at V_{CC} =3.3 V and T_A = 25°C.

PARAMETER		CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
	Cross point stability	50-Ω load, single-ended, V_{IN} = 180 mV_{PP}, 600 mV_{PP} and 1200 mV_{PP}, V_{OUT} = 1.2 V_{PP}		±5		pp
	Cross point stability vs. input amplitude	50-Ω load, single-ended, V_{IN} = 180 mV_{PP}, 600 mV_{PP} and 1200 mV_{PP}, V_{OUT} = 1.2 V_{PP}	–6		6	pp
BW_{AMP}	Bandwidth of AMP input			2.5		kHz
T_{OFF}	Transmitter disable time	Rising edge of DIS to V_{OUT+} ≤ 0.15 V_{PP} (3)		0.05	5	µs
T_{ON}	Disable negate time	Falling edge of DIS to V_{OUT+} ≥ 1.2 V_{PP} (3)			1	ms
T_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded(3)		1	10	ms
T_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data(3)			2	ms

(3) Assured by simulation over process, supply, and temperature variation.

DETAILED DESCRIPTION

EQUALIZER

The data signal is applied to an input equalizer by means of the input signal pins DIN+ / DIN–, which provide on-chip differential 100-Ω line-termination. The equalizer is enabled by setting EQENA to 1 (bit 1 of register 0). Equalization of up to 300-mm (12 in.) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is digitally controlled by the 2-wire interface and control logic block and is dependant on the register settings EQADJ[0..7] (register 3). The equalizer can be turned off and bypassed by setting EQENA to 0. For details about the equalizer settings, see Table 16.

LIMITER

By limiting the output signal of the equalizer to a fixed value, the limiter removes any overshoot after the input equalization and provides the input signal for the output driver. Adjustments to the limiter bias current and emitter follower current can be made to trade off the rise and fall times and supply current. The limiter bias current is adjusted through LIMCSGN (bit 7 of register 6) and LIMC[0..2] (bits 4, 5 and 6 of register 6). The emitter follower current is adjusted through EFCSGN (bit 3 of register 6) and EFC[0..2] (bits 0, 1 and 2 of register 6). In addition, the slope of the emitter follower current can be modified with the EFCRNG bit (bit 3 of register 5). Setting EFCRNG to 1 results in a steeper slope.

HIGH-SPEED OUTPUT DRIVER

The modulation current is sunk from the common emitter node of the limiting output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface. The collector nodes of the output stages are connected to the output pins OUT+ and OUT–. The collectors have internal active back termination. The outputs are optimized to drive a 50-Ω single-ended load and to obtain the maximum single-ended output voltage of 1.5 V_{PP}, AC coupling and inductive pullups to VCC are required. The active back termination emitter follower current is adjusted through ABTSGN (bit 3 of register 7) and ABTEF[0..2] (bits 0, 1 and 2 of register 7). ABTUP (bit 7 of register 7) and ABTDWN (bit 6 of register 7) can control the active back termination auxiliary buffer amplitude. Setting ABTUP to 1 increases the amplitude and setting ABTDWN to 1 decreases the amplitude. For most instances, these settings may be left in the default mode.

For waveform shaping, output pre-emphasis can be enabled by setting PKENA to 1 (bit 5 of register 0) and adjusting the peaking height through PEADJ[0..3] (register 2).

In addition, the polarity of the output pins can be inverted by setting the output polarity switch bit, POL (bit 2 of register 0) to 1.

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The modulation current generator is controlled by applying an analog voltage in the range of 0 to 2.5 V to the AMP pin, or it can be digitally controlled by the 2-wire interface block. The default method of control is through the AMP pin. To digitally control the output amplitude set AMPCTRL (bit 0 of register 0) to 1.

An 8-bit wide control bus, AMP[0..7] (register 1), can be used to set the desired modulation current, and therefore, the output voltage.

To decrease the output amplitude by approximately 18% set OARNG to 1 (bit 7 of register 5), to increase it by approximately 30 mV_{PP} set OASH0 (bit 5 of register 5) to 1, or to increase it by approximately 60 mV_{PP} set OASH1 (bit 6 of register 5) to 1.

The modulation current, and therefore the output signal, can be disabled by setting the DIS input pin to a high level or by setting ENA to 0 (bit 7 of register 0).

DC OFFSET CANCELATION AND CROSS POINT CONTROL

The ONET1151M has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled and the eye crossing point adjustment enabled by setting CPENA to 1 (bit 3 of register 0). The crossing point can be moved toward the one level by setting CPSGN to 0 (bit 7 of register 4) and it can be moved toward the zero level by setting CPSGN to 1. The percentage of shift depends upon the register settings CPADJ[0..6] (register 4) and the high cross point adjustment range bits HICP[0..1] (bits 0 and 1 of register 5). Setting HICP0 and HICP1 to 1 results in the maximum adjustment range but increases the supply current.

ANALOG REFERENCE AND TEMPERATURE SENSOR

The ONET1151M modulator driver is supplied by a single 3.3-V ± 10% supply voltage connected to the VCC and VCCD pins. This voltage is referred to ground (GND) and can be monitored as a 10-bit unsigned digital word through the 2-wire interface.

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground. This resistor is used to generate a precise, zero-TC current which is required as a reference current for the on-chip DACs.

In order to minimize the module component count, the ONET1151M provides an on-chip temperature sensor. The temperature can be monitored as a 10-bit unsigned digital word through the 2-wire interface.

POWER-ON RESET

The ONE1151M has power on reset circuitry which ensures that all registers are reset to zero during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. The part is ready to transmit data after the initialize to transmit time (t_{INIT2}), assuming that the chip enable bit ENA is set to 1 and the disable pin DIS is low. The DIS pin has an internal 10-kΩ pullup resistor so the pin must be pulled low to enable the outputs.

The ONET1151M can be disabled using either the ENA control register bit or the disable pin DIS. In both cases the internal registers are not reset. After the disable pin DIS is set low and/or the enable bit ENA is set back to 1, the part returns to its prior output settings.

ANALOG TO DIGITAL CONVERTER

The ONET1151M has an internal 10-bit analog to digital converter (ADC) that converts the analog monitors for temperature and power supply voltage into a 10-bit unsigned digital word. The first eight most significant bits (MSBs) are available in register 14 and the two least significant bits (LSBs) are available in register 15. Depending on the accuracy required, eight bits or 10 bits can be read. However, due to the architecture of the 2-wire interface, in order to read the two registers, two separate read commands have to be sent.

The ADC is enabled by default. To monitor a particular parameter, select the parameter with ADCSEL (bit 0 of register 13). Table 2 lists the ADCSEL bits and the monitored parameters.

Table 2. ADC Selection Bits and the Monitored Parameter

ADCSEL	Monitored Parameter
0	Temperature
1	Supply voltage

If it is not desired to use the ADC to monitor the two parameters then the ADC can be disabled by setting ADCDIS to 1 (bit 7 of register 13) and OSCDIS to 1 (bit 6 of register 13).

The digital word read from the ADC can be converted to its analog equivalent through the following formulas:

Temperature without a mid point calibration:

$$\text{Temperature } (°C) = \frac{(ADCx - 264)}{6}$$

Temperature with a mid point calibration:

$$\text{Temperature (°C)} = \frac{(\text{T\_cal (°C)} + 273) \times (\text{ADCx} + 1362)}{(\text{ADC\_cal} + 1362) - 273}$$

Power supply voltage:

$$\text{Power supply voltage (V)} = \frac{2.25 \times (\text{ADCx} + 1380)}{1409}$$

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET1151M uses a 2-wire serial interface for digital control. For example, the two circuit inputs, SDA and SCK, are respectively driven by the serial data and serial clock from a microprocessor. The SDA and SCK pins have internal 10-kΩ pullups to VCC. If a common interface is used to control multiple parts, the internal pullups can be set to 40 kΩ by setting HITERM to 1 (bit 6 of register 0). The internal pullup for the DIS pin is also set to 40 kΩ when HITERM is set to 1.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET1151M is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0001000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the ONET1151M is I^2C™ compatible. The typical timing is shown in Figure 3 and complete data write and read transfers are shown in Figure 4. Parameters for Figure 3 are defined in Table 3.

Bus Idle: Both SDA and SCK lines remain HIGH.

Start Data Transfer: A START condition (S) is defined by a change in the state of the SDA line from HIGH to LOW while the SCK line is HIGH. Each data transfer is initiated with a START condition.

Stop Data Transfer: A STOP condition (P) is defined by a change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH. Each data transfer is terminated with a STOP condition. However, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obligated to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

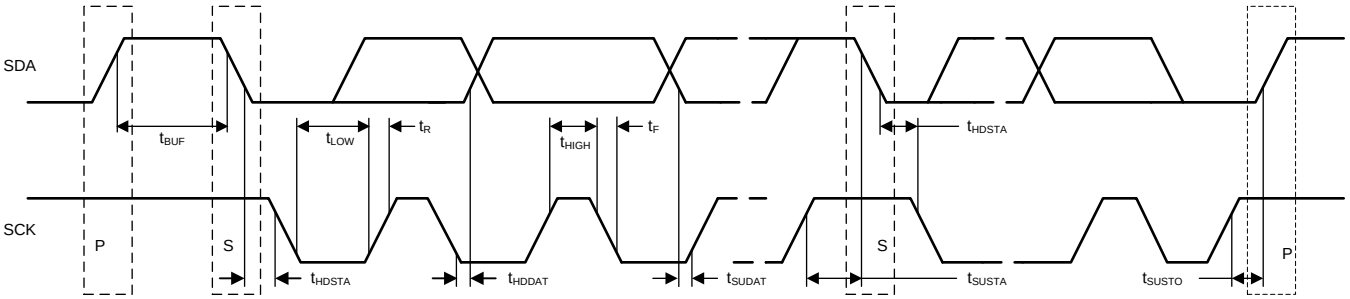


Figure 3. I²C Timing Diagram

Table 3. Timing Diagram Definitions

Parameter	Symbol	Min	Max	Unit
SCK clock frequency	f_{SCK}		400	kHz
Bus free time between STOP and START conditions	t_{BUF}	1.3		µs
Hold time after repeated START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6		µs
Low period of the SCK clock	t_{LOW}	1.3		µs
High period of the SCK clock	t_{HIGH}	0.6		µs
Setup time for a repeated START condition	t_{SUSTA}	0.6		µs
Data HOLD time	t_{HDDAT}	0		µs
Data setup time	t_{SUDAT}	100		ns
Rise time of both SDA and SCK signals	t_R		300	ns
Fall time of both SDA and SCK signals	t_F		300	ns
Setup time for STOP condition	t_{SUSTO}	0.6		µs

Write Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	Data Byte	A	P

Read Sequence

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	S	Slave Address	Rd	A	Data Byte	N	P

Legend

S	Start Condition
Wr	Write Bit (bit value = 0)
Rd	Read Bit (bit value = 1)
A	Acknowledge
N	Not Acknowledge
P	Stop Condition

Figure 4. Programming Sequence

REGISTER MAPPING

The register mapping for register addresses 0 (0x00) through 15 (0x0F) are listed in Table 4 through Table 15. Table 16 describes the circuit functionality based on the register settings.

Table 4. Register 0 (0x00) Mapping – Control Settings

Register Address 0 (0x00)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ENA	HITERM	PKENA	PKRNG	CPENA	POL	EQENA	AMPCTRL

Table 5. Register 1 (0x01) Mapping – Modulation Amplitude

Register Address 1 (0x01)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
AMP7	AMP6	AMP5	AMP4	AMP3	AMP2	AMP1	AMP0

Table 6. Register 2 (0x02) Mapping – Pre-Emphasis Adjust

Register Address 2 (0x02)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	-	-	-	PEADJ3	PEADJ2	PEADJ1	PEADJ0

Table 7. Register 3 (0x03) Mapping – Equalizer Adjust

Register Address 3 (0x03)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
EQADJ7	EQADJ6	EQADJ5	EQADJ4	EQADJ3	EQADJ2	EQADJ1	EQADJ0

Table 8. Register 4 (0x04) Mapping – Cross Point Adjust

Register Address 4 (0x04)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CPSGN	CPADJ6	CPADJ5	CPADJ4	CPADJ3	CPADJ2	CPADJ1	CPADJ0

Table 9. Register 5 (0x05) Mapping – CPA Settings

Register Address 5 (0x05)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
OARNG	OASH1	OASH0	-	EFCRNG	-	HICP1	HICP0

Table 10. Register 6 (0x06) Mapping – Limiter Bias Current Adjust

Register Address 6 (0x06)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
LIMCSGN	LIMC2	LIMC1	LIMC0	EFCSGN	EFC2	EFC1	EFC0

Table 11. Register 7 (0x07) Mapping – ABT – Emitter Follower Control

Register Address 7 (0x07)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ABTUP	ABTDWN	-	-	ABTSGN	ABTEF2	ABTEF1	ABTEF0

Table 12. Register 8 (0x08) – Register 12 (0x0C) Mapping – Not Used

Register Address 8 (0x08)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	-	-	-	-	-	-	-

Table 13. Register 13 (0x0D) Mapping – ADC Settings

Register Address 13 (0x0D)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ADCDIS	OSCDIS	-	-	-	-	-	ADCSEL

Table 14. Register 14 (0x0E) Mapping – ADC Output (Read Only)

Register Address 14 (0x0E)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2

Table 15. Register 15 (0x0F) Mapping – ADC Output (Read Only)

Register Address 15 (0x0F)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
-	-	-	-	-	-	ADC1	ADC0

Table 16. Register Functionality

Register	Bit	Symbol	Function
0	7	ENA	Enable chip bit: 1 = Chip enabled 0 = Chip disabled
	6	HITERM	SCK, SDA and DIS pin input termination select bit: 1 = 40 kΩ selected 0 = 10 kΩ selected
	5	PKENA	Output pre-emphasis enable bit: 1 = Pre-emphasis enabled (height controlled by register 2) 0 = Pre-emphasis disabled
	4	PKRNG	Output pre-emphasis range bit: 1 = High range enabled 0 = Default range
	3	CPENA	Cross point adjust enable bit: 1 = Cross point adjustment is enabled 0 = DC offset cancellation is enabled
	2	POL	Output polarity switch bit: 1: Pin 15 = OUT- and pin 14 = OUT+ 0: Pin 15 = OUT+ and pin 14 = OUT-
	1	EQENA	Input equalizer enable bit: 1 = Equalizer enabled (boost controlled by register 3) 0 = Equalizer disabled
	0	AMPCTRL	Amplitude control selection bit: 1 = Amplitude control through the serial interface 0 = Amplitude control by an analog voltage input at AMP pin
1	7	AMP7	Output amplitude setting Output voltage: 300 mV_{PP} to 1.5 V_{PP} in 256 steps
	6	AMP6	
	5	AMP5	
	4	AMP4	
	3	AMP3	
	2	AMP2	
	1	AMP1	
	0	AMP0	
2	7	-	
	6	-	
	5	-	
	4	-	
	3	PEADJ3	Pre-emphasis adjustment
	2	PEADJ2	0 = no pre-emphasis
	1	PEADJ1	> 0 = pre-emphasis added to output signal
	0	PEADJ0	
3	7	EQADJ7	Equalizer adjustment setting Maximum equalization for 00000000 Minimum equalization for 11111111
	6	EQADJ6	
	5	EQADJ5	
	4	EQADJ4	
	3	EQADJ3	
	2	EQADJ2	
	1	EQADJ1	
	0	EQADJ0	

Table 16. Register Functionality (continued)

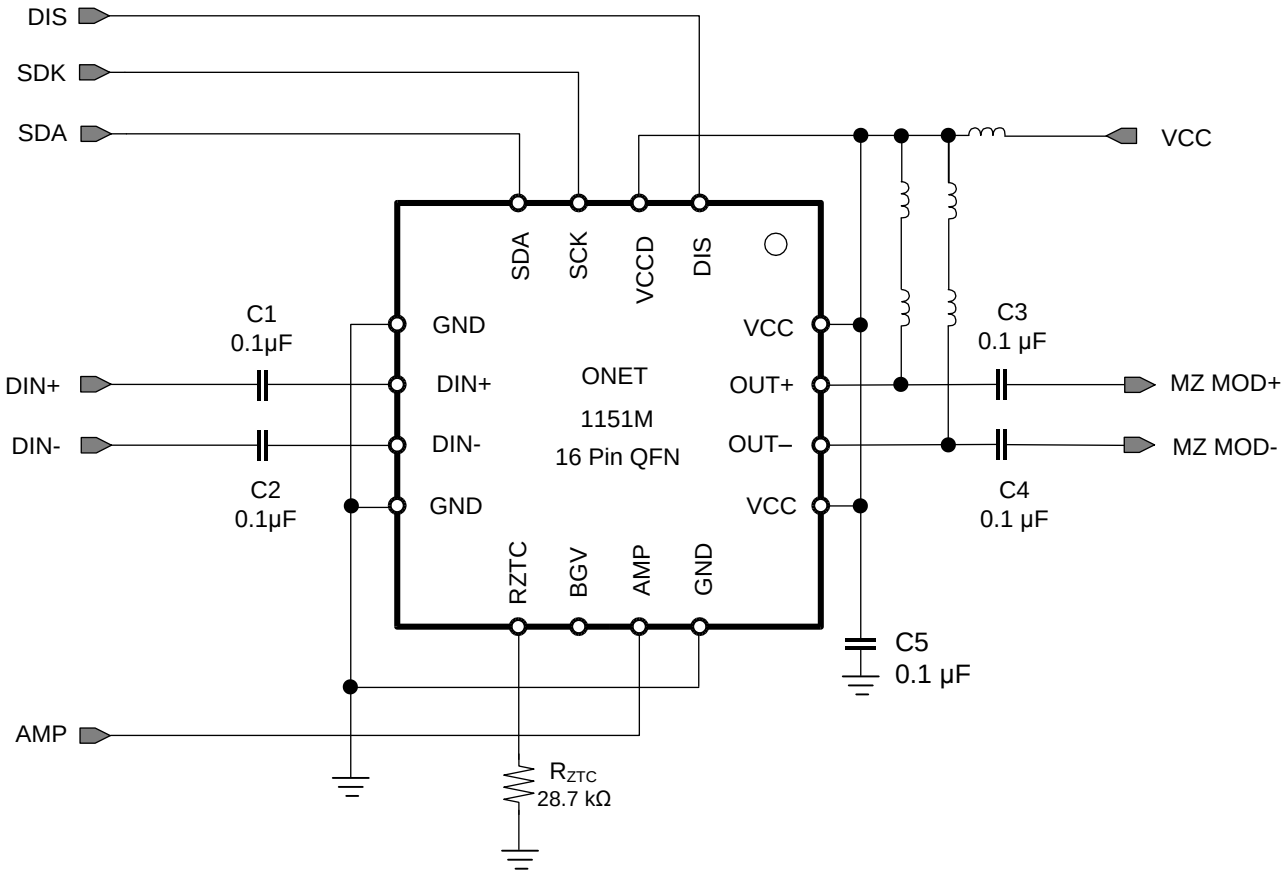
Register	Bit	Symbol	Function
4	7	CPSGN	Eye cross-point adjustment setting CPSGN = 0 (positive shift) Maximum shift for 1111111 Minimum shift for 0000000 CPSGN = 1 (negative shift) Maximum shift for 1111111 Minimum shift for 0000000
	6	CPADJ6	
	5	CPADJ5	
	4	CPADJ4	
	3	CPADJ3	
	2	CPADJ2	
	1	CPADJ1	
	0	CPADJ0	
5	7	OARNG	Output amplitude range bit: 1 = Decrease output amplitude by approximately 18% 0 = Default range
	6	OASH1	Upper output amplitude shift bit: 1 = Output amplitude shifted upwards by approximately 60 mV_{PP} 0 = Default
	5	OASH0	Lower output amplitude shift bit: 1 = Output amplitude shifted upwards by approximately 30 mV_{PP} 0 = Default
	4	-	
	3	EFCRNG	Emitter follower current slope selection: 1 = Step slope 0 = Shallow slope
	2	-	
	1 0	HICP1 HICP0	High cross point adjustment range bits: 00 = Default adjustment range 11 = Maximum increase in the adjustment range
6	7	LIMCSGN	Limiter bias current sign bit: 1 = Decrease limiter bias current 0 = Increase limiter bias current
	6 5 4	LIMC2 LIMC1 LIMC0	Limiter bias current selection bits: 000 = No change 111 = Maximum current change
	3	EFCSGN	Emitter follower current sign bit: 1 = Increase emitter follower current 0 = Decrease emitter follower current
	2 1 0	EFC2 EFC1 EFC0	Emitter follower current selection bits: 000 = No change 111 = Maximum current change
7	7	ABTUP	Active back termination auxiliary buffer amplitude control bit: 1 = Increase amplitude 0 = Default setting
	6	ABTDWN	Active back termination auxiliary buffer amplitude control bit: 1 = Decrease amplitude 0 = Default setting
	5	-	
	4	-	
	3	ABTSGN	Active back termination emitter follower current sign bit: 1 = Increase emitter follower current 0 = Decrease emitter follower current
	2 1 0	ABTEF2 ABTEF1 ABTEF0	Active back termination emitter follower current selection bits: 000 = No change 111 = Maximum current change

Table 16. Register Functionality (continued)

Register	Bit	Symbol	Function
13	7	ADCDIS	ADC disable bit: 1 = ADC disabled 0 = ADC enabled
	6	OSCDIS	ADC oscillator bit: 1 = Oscillator disabled 0 = Oscillator enabled
	5	-	
	4	-	
	3	-	
	2	-	
	1	-	
	0	ADCSEL	ADC input selection bits: 1 = Supply monitor 0 = Temperature sensor
14	7	ADC9 (MSB)	Digital representation of the ADC input source (read only)
	6	ADC8	
	5	ADC7	
	4	ADC6	
	3	ADC5	
	2	ADC4	
	1	ADC3	
	0	ADC2	
15	7	-	
	6	-	
	5	-	
	4	-	
	3	-	
	2	-	
	1	ADC1	Digital representation of the ADC input source (read only)
	0	ADC0 (LSB)	

APPLICATION INFORMATION

Figure 5 shows a typical application circuit using the ONET1151M. The modulator must be AC coupled to the driver for proper operation. The output amplitude is controlled through the AMP pin and the rest of the functions are controlled through the 2-wire interface (SDA or SCK) by a microcontroller.



Pullup inductors from MOD+ and MOD- to VCC are required.

Figure 5. Differential AC Coupled Drive

Layout Guidelines

For optimum performance, use 50-Ω transmission lines (100-Ω differential) for connecting the signal source to the DIN+ and DIN- pins and 50-Ω transmission lines (100-Ω differential) for connecting the OUT+ and OUT- modulation current outputs to the modulator. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter.

In addition, VCCD can be connected to VCC and filtered from a common supply.

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, V_{OUT} = 1.5 V_{PP} single ended, EQENA = 0, PKENA = 1 with PEADJ = 0x0F and V_{IN} = 600 mV_{PP} (unless otherwise noted).

DETERMINISTIC JITTER vs MODULATION CURRENT

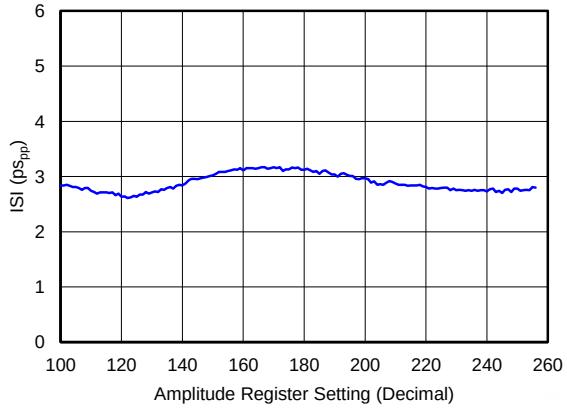


Figure 6.

DETERMINISTIC JITTER vs TEMPERATURE

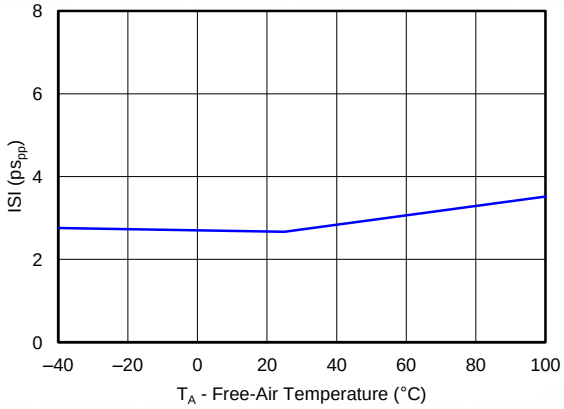


Figure 7.

RANDOM JITTER vs MODULATION CURRENT

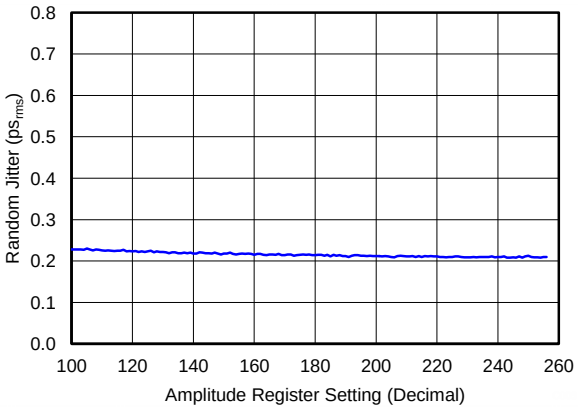


Figure 8.

RANDOM JITTER vs TEMPERATURE

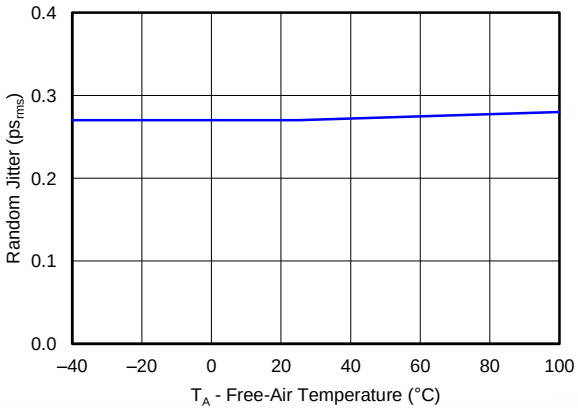


Figure 9.

RISE-TIME AND FALL-TIME vs MODULATION CURRENT

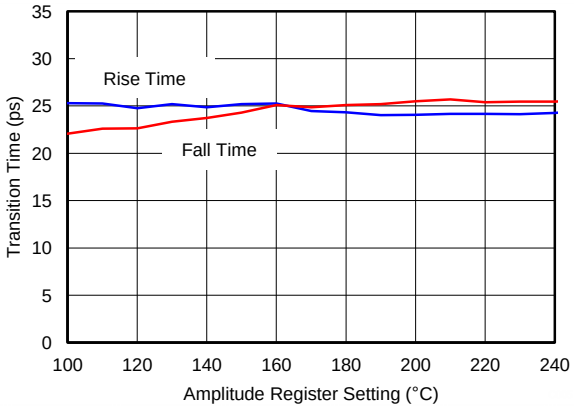


Figure 10.

RISE-TIME AND FALL-TIME vs TEMPERATURE

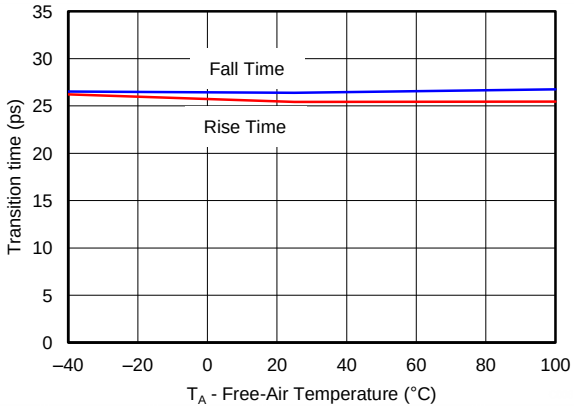


Figure 11.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, V_{OUT} = 1.5 V_{PP} single ended, EQENA = 0, PKENA = 1 with PEADJ = 0x0F and V_{IN} = 600 mV_{PP} (unless otherwise noted).

OUTPUT VOLTAGE vs AMP VOLTAGE

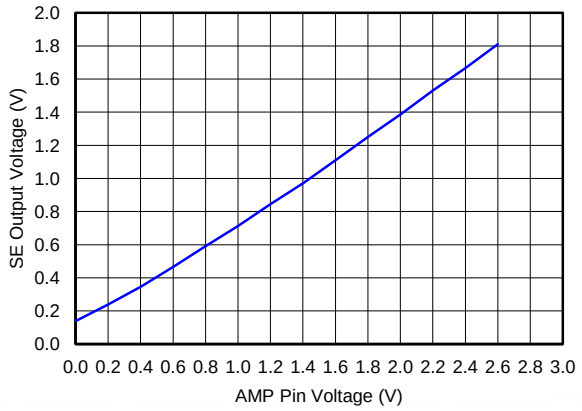


Figure 12.

OUTPUT VOLTAGE vs AMP REGISTER SETTING

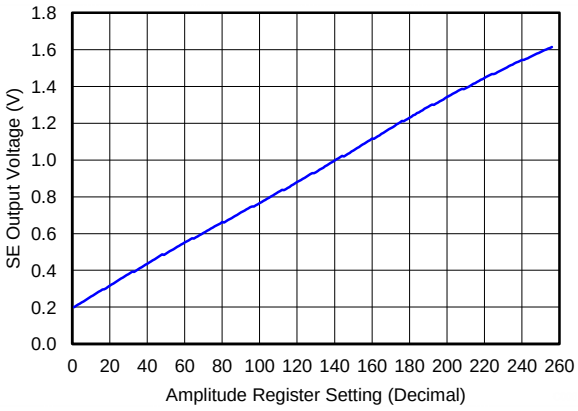


Figure 13.

SUPPLY CURRENT vs TEMPERATURE

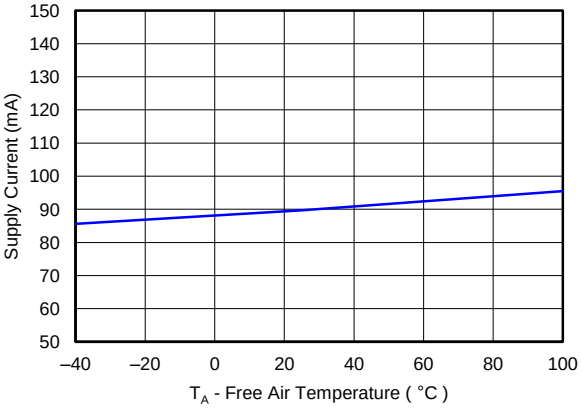


Figure 14.

EYE-DIAGRAM AT 10.3GBPS VOUT=1.5VPP

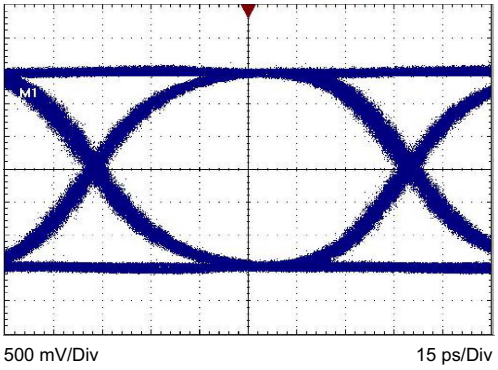


Figure 15.

EYE-DIAGRAM AT 11.3GBPS VOUT=1.5VPP, 50% CROSS POINT

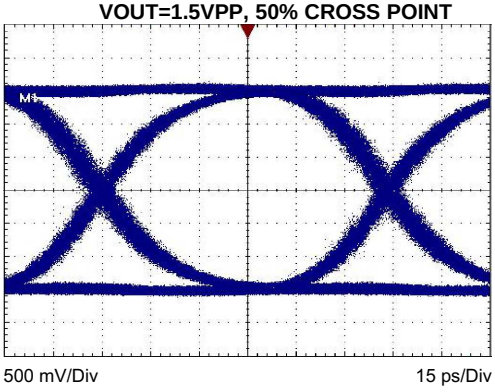


Figure 16.

EYE-DIAGRAM AT 11.3GBPS VOUT=1.5VPP, 30% CROSS POINT

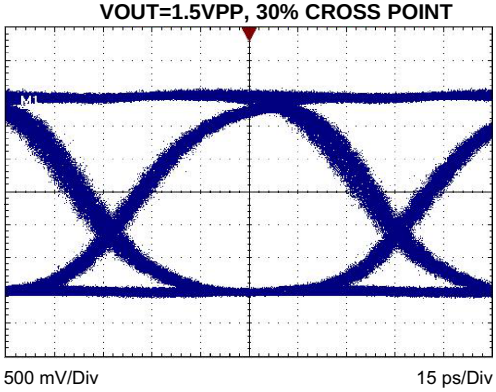


Figure 17.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, V_{OUT} = 1.5 V_{PP} single ended, EQENA = 0, PKENA = 1 with PEADJ = 0x0F and V_{IN} = 600 mV_{PP} (unless otherwise noted).

EYE-DIAGRAM AT 11.3GBPS VOUT=1.5VPP, 70% CROSS POINT

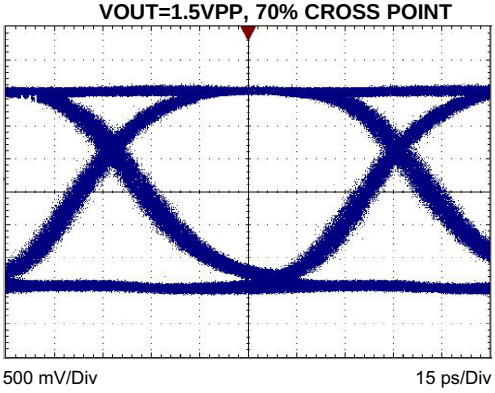


Figure 18.

EYE-DIAGRAM AT 11.3GBPS VOUT=1.5VPP, EQ SET TO 00, 12'' OF FR4 AT INPUTS

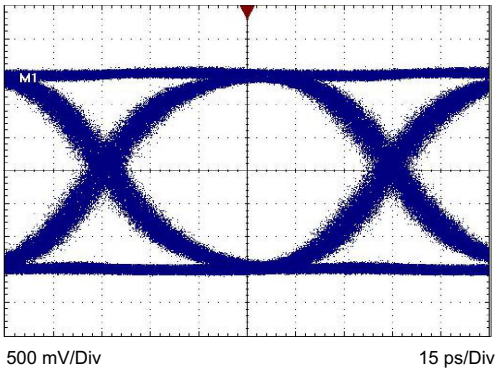


Figure 19.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ONET1151MRGTR	Obsolete	Production	VQFN (RGT) | 16	-	-	Call TI	Call TI	-40 to 100	1151M
ONET1151MRGTT	Obsolete	Production	VQFN (RGT) | 16	-	-	Call TI	Call TI	-40 to 100	1151M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

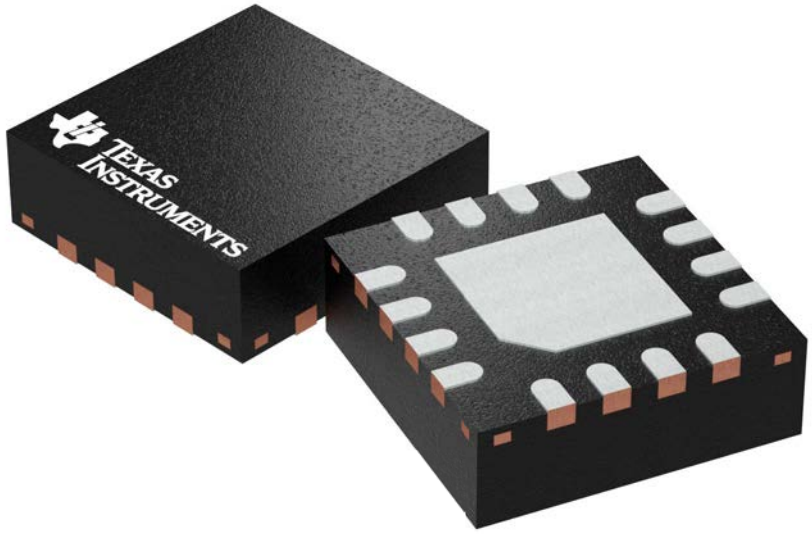
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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