LP503x 36/30 通道 12 位 PWM 超低静态电流 I²C RGB LED 驱动器

1 特性

- 工作电压范围：
  - V_{CC} 范围：2.7V 至 5.5V
  - 与 1.8V、3.3V 和 5V 电源轨兼容的 EN、SDA 和 SCL 引脚
  - 最大输出电压：6V
- 36 路高精度恒定电流阱
  - 在整个 V_{CC} 范围内，每个通道的最大电流为 25.5mA
  - 当 V_{CC} ≥ 3.3V 时，每个通道的最大电流为 35mA
  - 器件间的误差为 ±5%；通道间的误差为 ±5%
- 超低静态电流：
  - 关断模式：1μA（最大值），EN 处于低电平
  - 省电模式：12μA（最大值），EN 处于高电平，所有 LED 关断时间大于 30ms
- 每个通道具有一个集成式 12 位 29kHz PWM 发生器：
  - 每个通道具有一个独立的色彩混合寄存器
  - 每个 RGB LED 模块具有一个独立的亮度控制寄存器
  - 可选的对数或线性标度亮度控制
  - 集成式三相相移 PWM 方案
- 3 个可编程组（R、G、B），可轻松对每种颜色进行软件控制
- 2 个外部硬件地址引脚允许连接多达 4 个器件
- 广播从地址允许同时配置多个器件
- 自动递增允许在一次传输期间写入或读取多个连续的寄存器
- 高达 400kHz 的快速模式 I²C 速度

2 应用

用于以下设备的 LED 照明、指示灯和闪烁光：

- 智能扬声器
- 智能家用电器
- 可视门铃
- 电子智能锁
- 烟雾探测器
- 机顶盒
- 智能路由器
- 手持设备

3 说明

高效、高性能的 LED 响应效果，如闪烁，呼吸和追逐，对于改善许多人机界面 (HMI) 应用中的最终用户体验 至关重要。

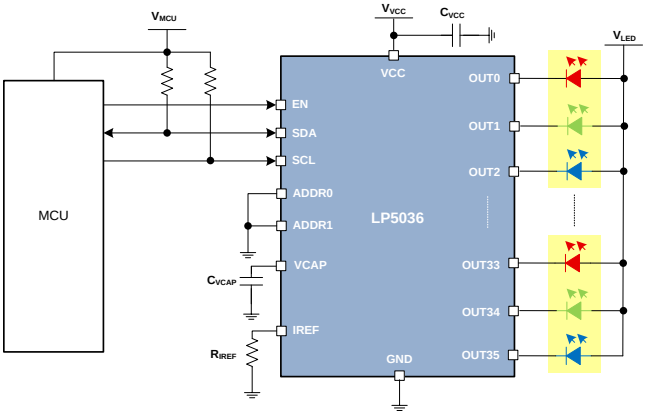
LP503x 器件是一款 30 或 36 通道恒定电流阱 LED 驱动器。LP503x 具有适用于每个通道的 29kHz、12 位 PWM 发生器以及通道/模块独立的色彩混合和*强度控制*（之前被称为亮度控制寄存器），能够达到可闻噪声为零的生动 LED 效果。用户可以受益于器件的超低关断 Iq 省电模式，而设计人员可以借助 LP503x 的三个可编程组 (R G B) 非常轻松地为软件编码。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LP5030	VQFN (46)	6.00mm × 5.00mm
LP5036		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2018) to Revision B **Page**

- Changed max standy current from 10uA to 12uA ... 8
- Changed power-save mode current from 10uA to 12uA ... 8
- 已更改 from LED3 to LED11 ... 28

Changes from Original (September 2018) to Revision A **Page**

- 首次发布生产数据数据表 ... 1

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5 说明（续）

LP503x 器件以 12 位 PWM 分辨率和 29kHz 开关频率控制每个 LED 输出。这种控制有助于获得可平缓降低的强度并消除可闻噪声。该器件具有不同的色彩混合和强度控制寄存器，使得编写软件代码变得非常简单。在以淡入淡出类型的呼吸效果为目标时，全局 R、G、B 组控制可显著减轻微控制器负载。LP503x 器件还可以实现 PWM 相移功能，以帮助在多个 LED 同时打开时降低输入功率预算。

LP503x 器件具有自动省电模式，可实现超低静态电流。当所有通道都关断 30ms 时，该器件的总功耗会降至 10μA，这使得 LP503x 器件成为电池供电终端设备的可能替代产品。

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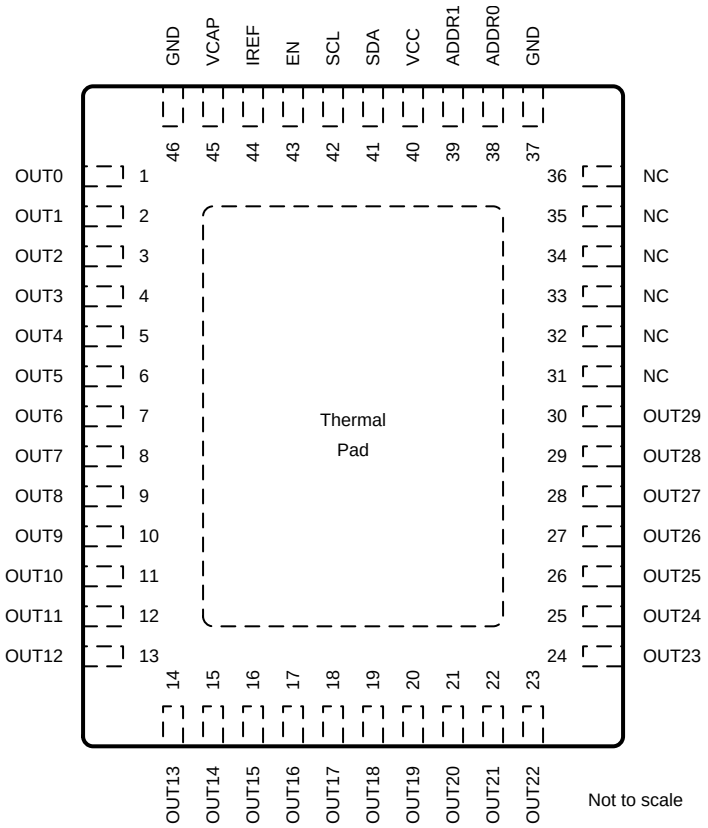
6 Pin Configuration and Functions

LP5030 RJV Package
46-Pin VQFN With Exposed Thermal Pad
Top View



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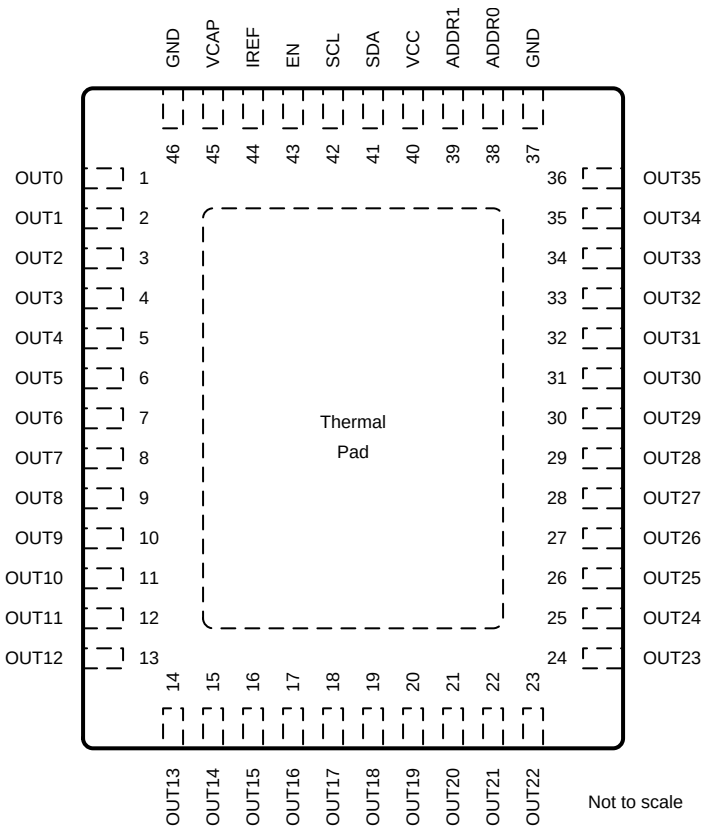
LP5036 RJV Package
46-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	LP5030	LP5036		
ADDR0	38	38	—	I^2C slave-address selection pin. This pin must not be left floating.
ADDR1	39	39	—	I^2C slave-address selection pin. This pin must not be left floating.
EN	43	43	I	Chip enable input pin
IREF	44	44	—	Output current-reference global-setting pin
NC	31	—	—	No internal connection
NC	32	—	—	No internal connection
NC	33	—	—	No internal connection
NC	34	—	—	No internal connection
NC	35	—	—	No internal connection
NC	36	—	—	No internal connection
OUT0	1	1	O	Current sink output 0. If not used, this pin can be left floating.
OUT1	2	2	O	Current sink output 1. If not used, this pin can be left floating.
OUT2	3	3	O	Current sink output 2. If not used, this pin can be left floating.
OUT3	4	4	O	Current sink output 3. If not used, this pin can be left floating.
OUT4	5	5	O	Current sink output 4. If not used, this pin can be left floating.
OUT5	6	6	O	Current sink output 5. If not used, this pin can be left floating.
OUT6	7	7	O	Current sink output 6. If not used, this pin can be left floating.

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Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	LP5030	LP5036		
OUT7	8	8	O	Current sink output 7. If not used, this pin can be left floating.
OUT8	9	9	O	Current sink output 8. If not used, this pin can be left floating.
OUT9	10	10	O	Current sink output 9. If not used, this pin can be left floating.
OUT10	11	11	O	Current sink output 10. If not used, this pin can be left floating.
OUT11	12	12	O	Current sink output 11. If not used, this pin can be left floating.
OUT12	13	13	O	Current sink output 12. If not used, this pin can be left floating.
OUT13	14	14	O	Current sink output 13. If not used, this pin can be left floating.
OUT14	15	15	O	Current sink output 14. If not used, this pin can be left floating.
OUT15	16	16	O	Current sink output 15. If not used, this pin can be left floating.
OUT16	17	17	O	Current sink output 16. If not used, this pin can be left floating.
OUT17	18	18	O	Current sink output 17. If not used, this pin can be left floating.
OUT18	19	19	O	Current sink output 18. If not used, this pin can be left floating.
OUT19	20	20	O	Current sink output 19. If not used, this pin can be left floating.
OUT20	21	21	O	Current sink output 20. If not used, this pin can be left floating.
OUT21	22	22	O	Current sink output 21. If not used, this pin can be left floating.
OUT22	23	23	O	Current sink output 22. If not used, this pin can be left floating.
OUT23	24	24	O	Current sink output 23. If not used, this pin can be left floating.
OUT24	25	25	O	Current sink output 24. If not used, this pin can be left floating.
OUT25	26	26	O	Current sink output 25. If not used, this pin can be left floating.
OUT26	27	27	O	Current sink output 26. If not used, this pin can be left floating.
OUT27	28	28	O	Current sink output 27. If not used, this pin can be left floating.
OUT28	29	29	O	Current sink output 28. If not used, this pin can be left floating.
OUT29	30	30	O	Current sink output 29. If not used, this pin can be left floating.
OUT30	—	31	O	Current sink output 30. If not used, this pin can be left floating.
OUT31	—	32	O	Current sink output 31. If not used, this pin can be left floating.
OUT32	—	33	O	Current sink output 32. If not used, this pin can be left floating.
OUT33	—	34	O	Current sink output 33. If not used, this pin can be left floating.
OUT34	—	35	O	Current sink output 34. If not used, this pin can be left floating.
OUT35	—	36	O	Current sink output 35. If not used, this pin can be left floating.
SCL	42	42	I	I^2C bus clock line. If not used, this pin must be connected to GND or VCC.
SDA	41	41	I/O	I^2C bus data line. If not used, this pin must be connected to GND or VCC.
VCAP	45	45	—	Internal LDO output pin, this pin must be connected to a 1-µF capacitor to GND.
VCC	40	40	I	Input power.
GND	37	37	—	The ground pin for the device.
GND	46	46	—	The ground pin for the device.
Thermal pad	GND	GND	—	Exposed thermal pad also serves as a ground for the device.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage on EN, IREF, OUTx, SCL, SDA, VCC	–0.3	6	V
Voltage on ADDRx	–0.3	VCC+0.3	V
Voltage on VCAP	–0.3	2	V
Continuous power dissipation	Internally limited		
Junction temperature, T_{J-MAX}	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage on VCC	2.7	5.5	V
Voltage on OUTx	0	5.5	V
Voltage on ADDRx, EN, SDA, SCL	0	5.5	V
Operating ambient temperature, T_A	–40	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		LP5030 or LP5036 RJV (QFN) 46 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and ICPackage Thermal Metrics*.

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7.5 Electrical Characteristics

over operating ambient temperature range (–40°C < T_A<85°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCC)						
V_{VCC}	Supply voltage(1)		2.7		5.5	V
I_{VCC}	Shutdown supply current	V_{EN} = 0 V		0.2	1	µA
	Standby supply current	V_{EN} = 3.3 V, Chip_EN = 0 (bit)		6	12	µA
	Normal-mode supply current	With 10-mA LED current per OUTx		6.5	10	mA
	Power-save mode supply current	V_{EN} = 3.3 V, Chip_EN = 1 (bit), Power_Save_EN = 1 (bit), all the LEDs off duration > t_{PSM}		6	12	µA
V_{UVR}	Undervoltage restart	V_{VCC} rising			2.5	V
V_{UVF}	Undervoltage shutdown	V_{VCC} falling	2			V
V_{UV_HYS}	Undervoltage shutdown hysteresis			0.2		V
OUTPUT STAGE (OUTx)						
I_{MAX}	Maximum sink current (OUT0 – OUT35)	V_{VCC} in full range, Max_Current_Option = 0 (bit), PWM = 100%			25.5	mA
	Maximum sink current (OUT0 – OUT35)	V_{VCC} ≥ 3.3 V, Max_Current_Option = 1 (bit), PWM = 100%			35	mA
I_{LIM}	Internal sink current limit (OUT0 – OUT35)	V_{VCC} in full range, Max_Current_Option = 0 (bit), V_{IREF} = 0 V	35	55	80	mA
	Internal sink current limit (OUT0 – OUT35)	V_{VCC} ≥ 3.3V, Max_Current_Option=1 (bit), V_{IREF} = 0 V	40	75	120	mA
I_{LKG}	Leakage current (OUT0 – OUT35)	PWM = 0%		0.1	1	µA
I_{ERR_DD}	Device to device current error, $I_{ERR\_DD}=(I_{AVE}-I_{SET})/I_{SET}\times100\%$	V_{VCC} = 3.3V. All channels' current set to 10 mA. PWM = 100%. Already includes the V_{IREF} and K_{IREF} tolerance	–5%		5%	
I_{ERR_CC}	Channel to channel current error, $I_{ERR\_CC}=(I_{OUTX}-I_{AVE})/I_{AVE}\times100\%$	V_{VCC} = 3.3V. All channels' current set to 10 mA. PWM = 100%. Already includes the V_{IREF} and K_{IREF} tolerance	–5%		5%	
V_{IREF}	IREF voltage(1)			0.7		V
K_{IREF}	IREF ratio(1)			105		
f_{PWM}	PWM switching frequency(1)		21	29		kHz
V_{SAT}	Output saturation voltage	V_{VCC} in full range, Max_Current_Option = 0 (bit), output current set to 20 mA, the voltage when the LED current has dropped 5%		0.25	0.35	V
		V_{VCC} ≥ 3.3 V, Max_Current_Option = 1 (bit), output current set to 20 mA, the voltage when the LED current has dropped 5%		0.3	0.4	V
LOGIC INPUTS (EN, SCL, SDA, ADDRx)						
V_{IL}	Low level input voltage				0.4	V
V_{IH}	High level input voltage		1.4			V
I_{LOGIC}	Input current		–1		1	µA
V_{SDA}	SDA output low level	I_{PULLUP} = 5 mA			0.4	V

(1) Specified by design

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Electrical Characteristics (continued)

over operating ambient temperature range (–40°C < T_A<85°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS						
$T_{(TSD)}$	Thermal-shutdown junction temperature(1)			160		°C
$T_{(HYS)}$	Thermal shutdown temperature hysteresis(1)			15		°C

7.6 Timing Requirements

over operating ambient temperature range (-40°C < T_A< 85°C) (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{OSC}	Internal oscillator frequency(1)		15		MHz
t_{PSM}	Power save mode deglitch time(1)	20	30	40	ms
t_{EN_H}	EN first rising edge until first I^2C access(1)			500	µs
t_{EN_L}	EN first falling edge until first I^2C reset(1)			3	µs
f_{SCL}	I^2C clock frequency(1)			400	kHz
1	Hold time (repeated) START condition(1)	0.6			µs
2	Clock low time(1)	1.3			µs
3	Clock high time(1)	600			ns
4	Setup time for a repeated START condition(1)	600			ns
5	Data hold time(1)	0			ns
6	Data setup time(1)	100			ns
7	Rise time of SDA and SCL(1)	20 + 0.1 C_b			ns
8	Fall time of SDA and SCL(1)	15 + 0.1 C_b			ns
9	Setup time for STOP condition(1)	600			ns
10	Bus free time between a STOP and a START condition(1)	1.3			µs
C_b	Capacitive load parameter for each bus line Load of 1 pF corresponds to one nanosecond(1).	10		200	pF

(1) Specified by design

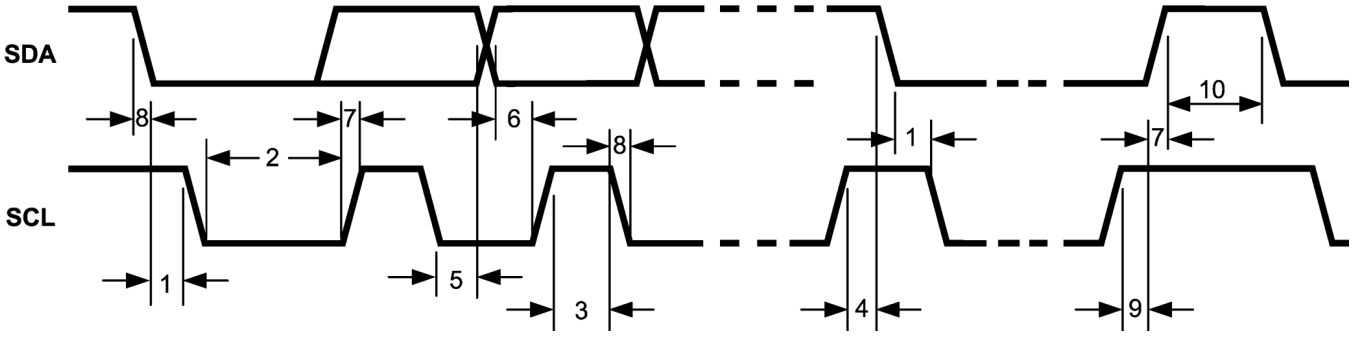


图 1. I^2C Timing Parameters

7.7 Typical Characteristics

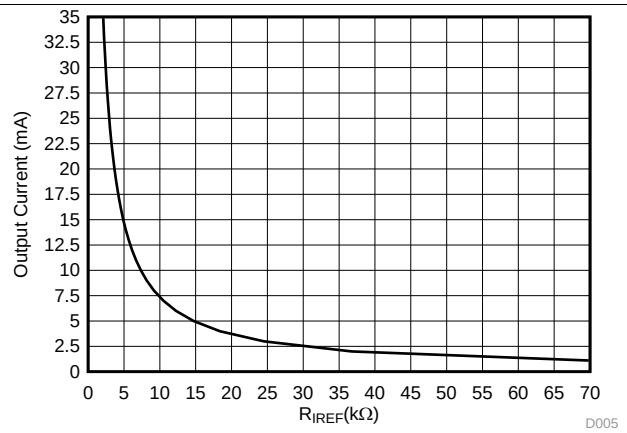
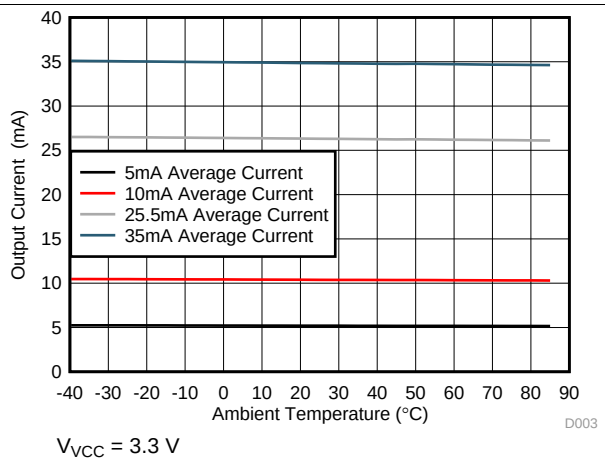
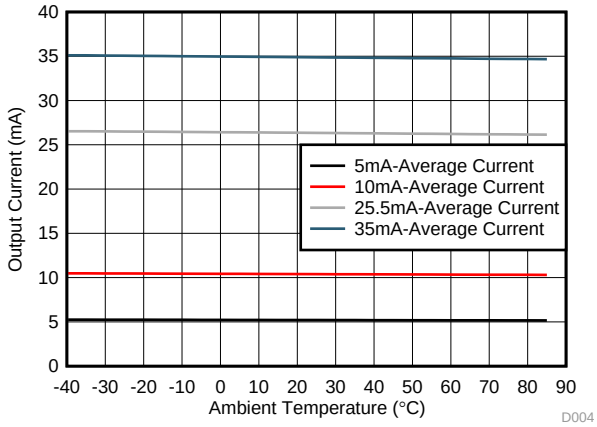


图 2. Output Current Target vs R_{IREF}



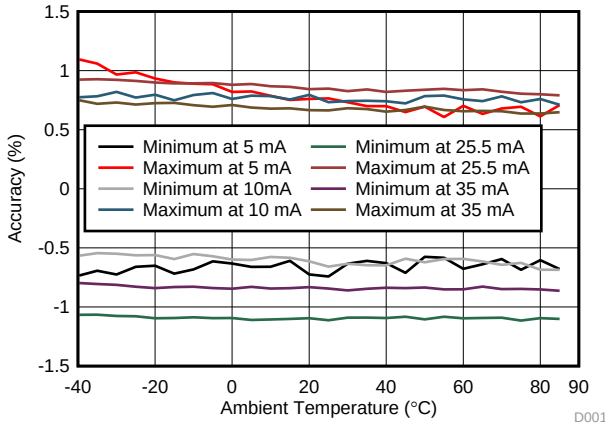
V_{VCC} = 3.3 V

图 3. Output Current vs Ambient Temperature



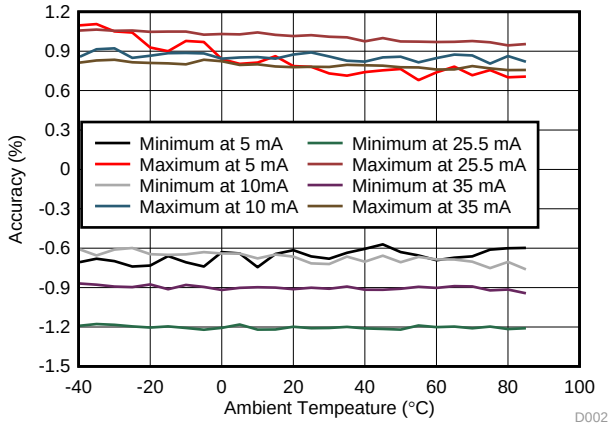
V_{VCC} = 5 V

图 4. Output Current vs Ambient Temperature



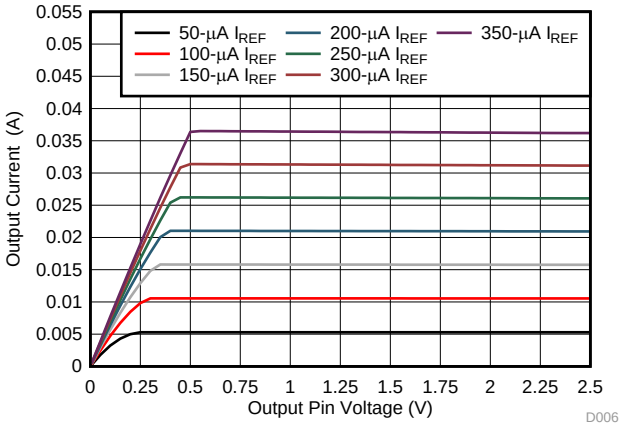
V_{VCC} = 3.3 V

图 5. Channel-to-Channel Accuracy



V_{VCC} = 5 V

图 6. Channel-to-Channel Accuracy



V_{VCC} = 3.3 V

图 7. OUT Pin Voltage vs Current

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Typical Characteristics (接下页)

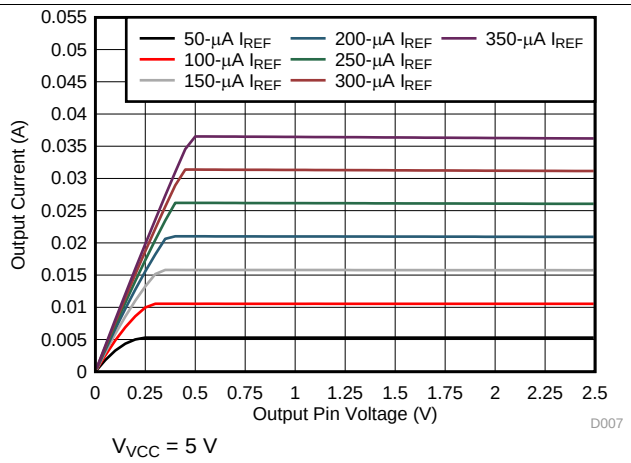


图 8. OUT Pin Voltage vs Current

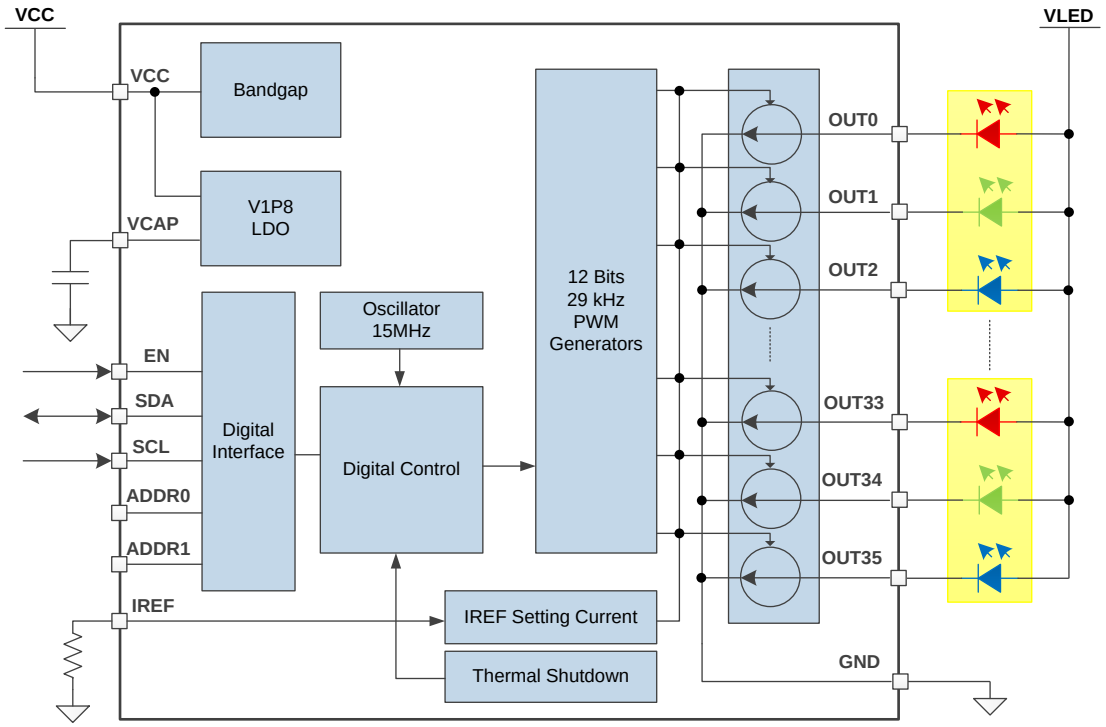
8 Detailed Description

8.1 Overview

The LP503x device is a 30- or 36-channel constant-current-sink LED driver. The LP503x device includes all necessary power rails, an on-chip oscillator, and a two-wire serial I^2C interface. The maximum constant-current value of all channels is set by a single external resistor. Two hardware address pins allow up to four devices on the same bus. An automatic power-saving mode is implemented to keep the total current consumption under 10 µA, which makes the LP503x device a potential choice for battery-powered end-equipment.

The LP503x device is optimized for RGB LEDs regarding both live effects and software efforts. The LP503x device controls each LED output with 12-bit PWM resolution at 29-kHz switching frequency, which helps achieve a smooth dimming effect and eliminates audible noise. The independent color-mixing and intensity-control registers make the software coding straightforward. When targeting a fade-in, fade-out type breathing effect, the global RGB bank control reduces the microcontroller loading significantly. The LP503x device also implements a PWM phase-shifting function to help reduce the input power budget when LEDs turn on simultaneously.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Each Channel PWM Control

Most traditional LED drivers are designed for the single-color LEDs, in which the high resolution PWM generator is used for intensity control only. However, for RGB LEDs, both the color mixing and intensity control should be addressed to achieve the target effect. With the traditional solution, the users must handle the color mixing and intensity control simultaneously with a single PWM register. Several undesired effects occur: the limited dimming steps, the complex software design, and the color distortion when using a logarithmic scale control.

The LP503x device is designed with independent color mixing and intensity control, which makes the RGB LED effects fancy and the control experience straightforward. With the inputs of the color-mixing register and the intensity-control register, the final PWM generator output for each channel is 12-bit resolution and 29-kHz dimming frequency, which helps achieve a smooth dimming effect and eliminates audible noise. See 图 9.

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Feature Description (接下页)

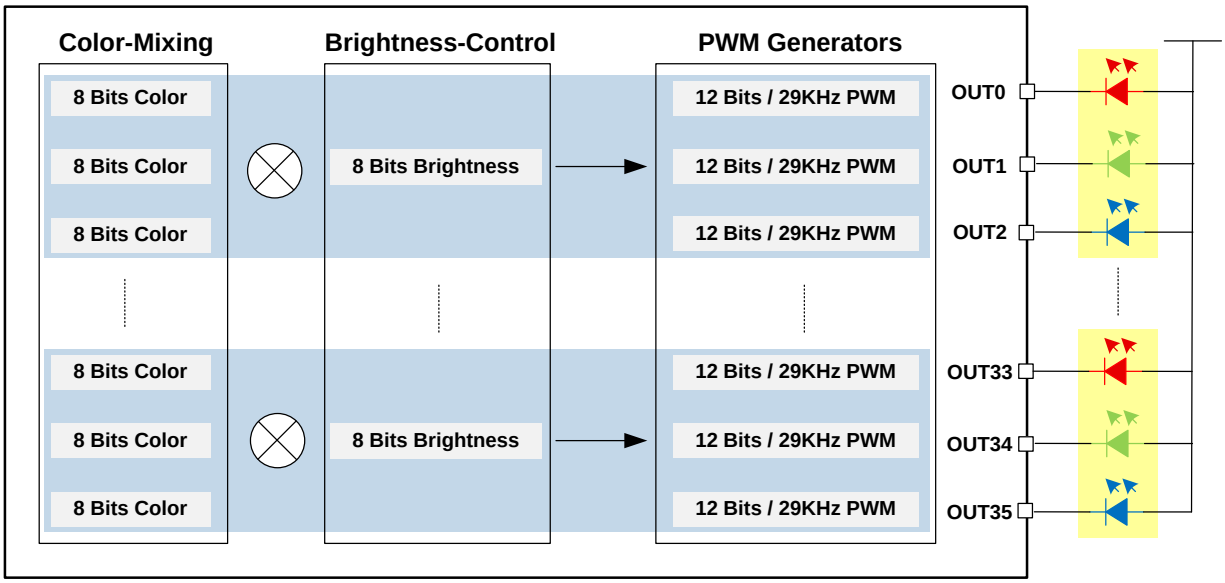

图 9. PWM Control Scheme for Each Channel

8.3.1.1 Independent Color Mixing Per RGB LED Module

Each output channel has its own individual 8-bit color-setting register (OUTx_COLOR). The device allows every RGB LED module to achieve >16 million (256 × 256 × 256) color-mixing.

8.3.1.2 Independent Intensity Control Per RGB LED Module

When color is fixed, the independent intensity-control is used to achieve accurate and flexible dimming control for every RGB LED module.

8.3.1.2.1 Intensity-Control Register Configuration

Every three consecutive output channels are assigned to their respective intensity-control register (LEDx_BRIGHTNESS). For example, OUT0, OUT1, and OUT2 are assigned to LED0_BRIGHTNESS, so it is recommended to connect the RGB LEDs in the sequence as shown in 表 1. The LP503x device allows 256-step intensity control for each RGB LED module, which helps achieve a smooth dimming effect.

Keeping FFh (default value) in the LED0_BRIGHTNESS register results in 100% dimming duty cycle. With this setting, the users can just configure the color mixing register by channel to achieve the target dimming effect in a single-color LED application.

8.3.1.2.2 Logarithmic- or Linear-Scale Intensity Control

For human-eye-friendly visual performance, a logarithmic-scale dimming curve is usually implemented in LED drivers. However, for RGB LEDs, if using a single register to achieve both color mixing and intensity control, color distortion can be observed easily when using a logarithmic scale. The LP503x device, with independent color-mixing and intensity-control registers, implements the logarithmic scale dimming control inside the intensity control function, which solves the color distortion issue effectively. See 图 10. Also, the LP503x device allows users to configure the dimming scale either logarithmically or linearly through the global Log_Scale_EN register bit. If a special dimming curve is desired, using the linear scale with software correction is the most flexible approach. See 图 11.

Feature Description (接下页)

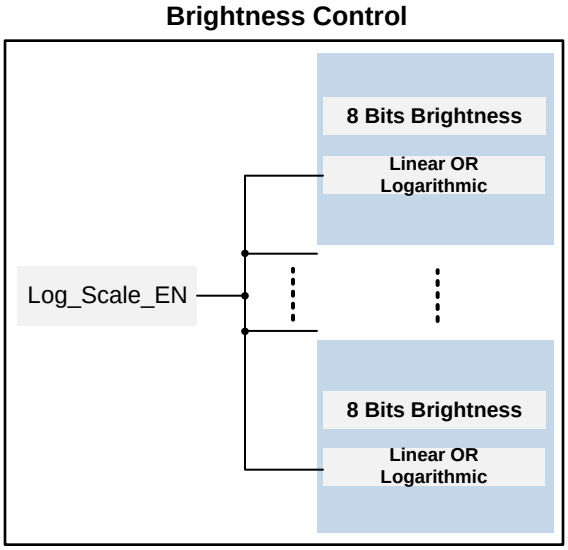

图 10. Logarithmic or Linear Scale Intensity Control

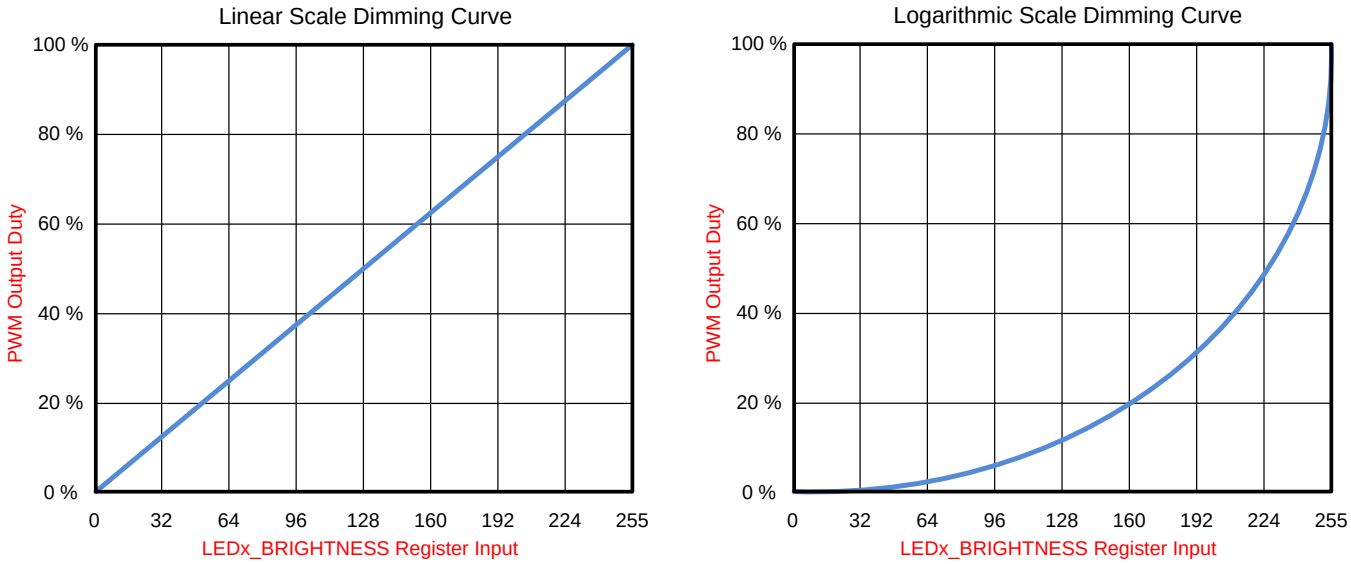

图 11. Logarithmic vs Linear Dimming Curve

8.3.1.3 12-Bit, 29-kHz PWM Generator Per Channel

8.3.1.3.1 PWM Generator

With the inputs of the color mixing and the intensity control, the final output PWM duty cycle is defined as the product obtained by multiplying the color-mixing register value by the related intensity-control register value. The final output PWM duty cycle has 12 bits of control accuracy, which is achieved by a 9 bits of pure PWM resolution and 3 bits of dithering digital control. For 3-bit dithering, every eighth pulse is made 1 LSB longer to increase the average value by 1 / 8th. The LP503x device allows the users to enable or disable the dithering function through the PWM_Dithering_EN register. When enabled (default), the output PWM duty-cycle accuracy is 12 bits. When disabled, the output PWM duty-cycle accuracy is 9 bits.

To eliminate the audible noise due to the PWM switching, the LP503x device sets the PWM switching frequency at 29-kHz, above the 20-kHz human hearing range.

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Feature Description (接下页)

8.3.1.4 PWM Phase-Shifting

A PWM phase-shifting scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. The scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases.

- Phase 1—the rising edge of the PWM pulse is fixed. The falling edge of the pulse is changed when the duty cycle changes. Phase 1 is applied to LED0, LED3, …, LED[3 × (n – 1)].
- Phase 2—the middle point of the PWM pulse is fixed. The pulse spreads in both directions when the PWM duty cycle is increased. Phase 2 is applied to LED1, LED4, …, LED[3 × (n – 1) + 1].
- Phase 3—the falling edge of the PWM pulse is fixed. The rising edge of the pulse is changed when the duty cycle changes. Phase 3 is applied to LED2, LED5, …, LED[3 × (n – 1) + 2].
- For LP5030, n = 10. For LP5036, n = 12.

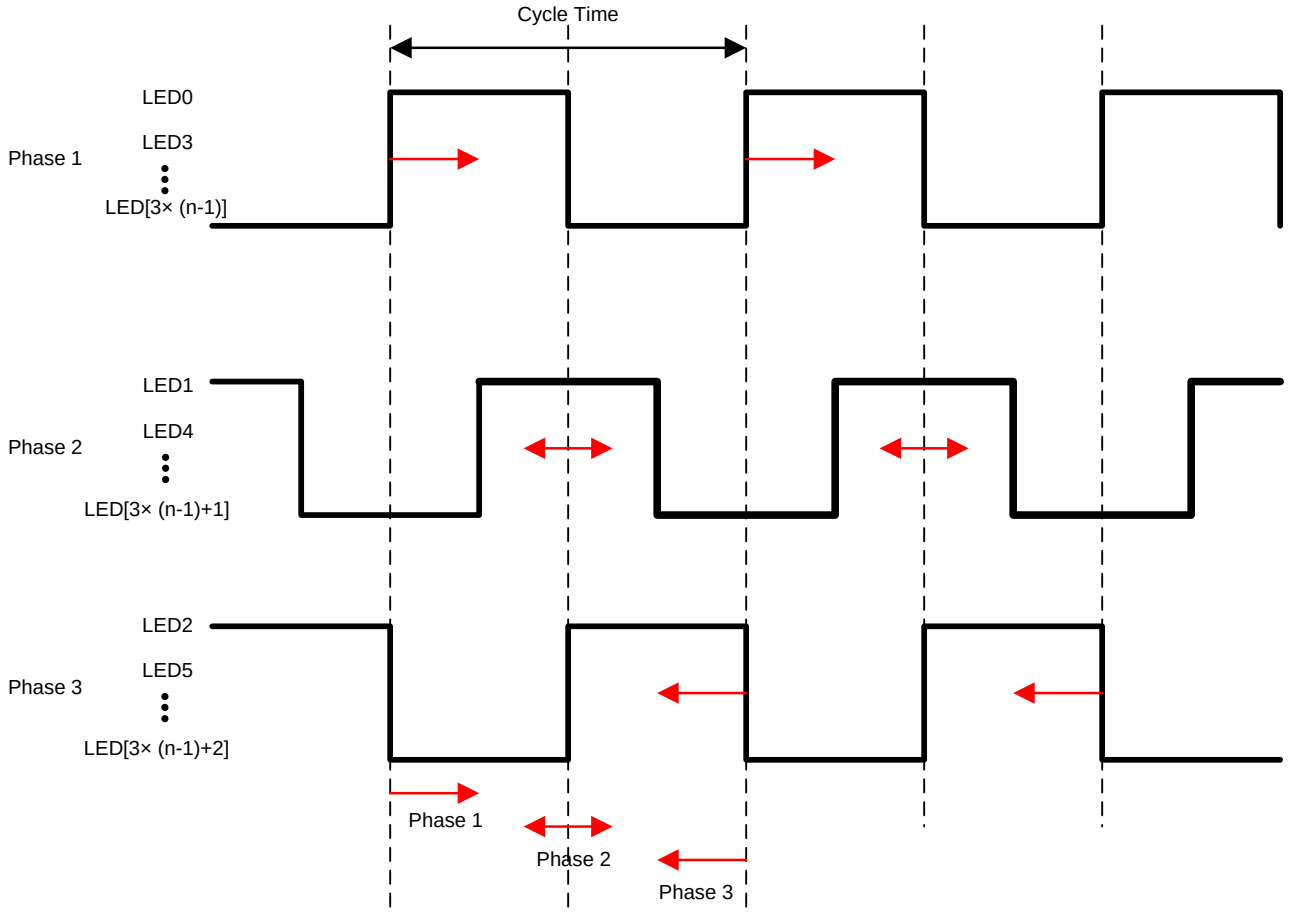

图 12. PWM Phase-Shifting

8.3.2 LED Bank Control

For most LED-animation effects, like blinking and breathing, all the RGB LEDs have the same lighting pattern. Instead of controlling the individual LED separately, which occupies the microcontroller resources heavily, the LP503x device provides an easy coding approach, the LED bank control.

Feature Description (接下页)

Each channel can be configured as either independent control or bank control through the LEDx_Bank_EN register. When LEDx_Bank_EN = 0 (default), the LED is controlled independently by the related color-mixing and intensity-control registers. When LEDx_Bank_EN = 1, the LP503x device drives the LED in LED bank-control mode. The LED bank has its own independent PWM control scheme, which is the same structure as the PWM scheme of each channel. See Each Channel PWM Control for more details. When a channel configured as LED bank-control mode, the related color mixing and intensity control is governed by the bank control registers (BANK_A_COLOR, BANK_B_COLOR, BANK_C_COLOR, and BANK_BRIGHTNESS) regardless of the inputs on its own color-mixing and intensity-control registers.

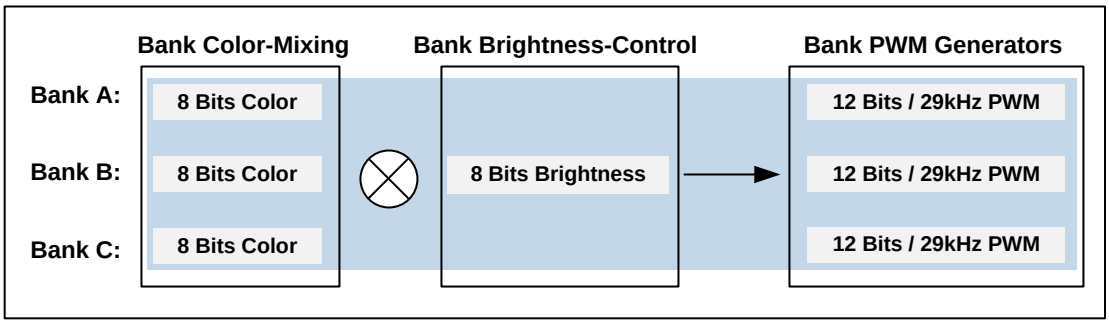

图 13. Bank PWM Control Scheme

表 1. Bank Number and LED Number Assignment

OUT NUMBER	BANK NUMBER	RGB LED MODULE NUMBER
OUT0	Bank A	LED0
OUT1	Bank B	
OUT2	Bank C	
OUT3	Bank A	LED1
OUT4	Bank B	
OUT5	Bank C	
OUT6	Bank A	LED2
OUT7	Bank B	
OUT8	Bank C	
OUT9	Bank A	LED3
OUT10	Bank B	
OUT11	Bank C	
OUT12	Bank A	LED4
OUT13	Bank B	
OUT14	Bank C	
OUT15	Bank A	LED5
OUT16	Bank B	
OUT17	Bank C	
OUT18	Bank A	LED6
OUT19	Bank B	
OUT20	Bank C	
OUT21	Bank A	LED7
OUT22	Bank B	
OUT23	Bank C	
OUT24	Bank A	LED8
OUT25	Bank B	
OUT26	Bank C	

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Feature Description (接下页)

表 1. Bank Number and LED Number Assignment (接下页)

OUT NUMBER	BANK NUMBER	RGB LED MODULE NUMBER
OUT27	Bank A	LED9
OUT28	Bank B	
OUT29	Bank C	
OUT30	Bank A	LED10(1)
OUT31	Bank B	
OUT32	Bank C	
OUT33	Bank A	LED11(1)
OUT34	Bank B	
OUT35	Bank C	

(1) For LP5036 only.

With the bank control configuration, the LP503x device enables users to achieve smooth and live LED effects globally with an ultra-simple software effort. 图 14 shows an example using LED0 as an independent RGB indicator and others with group breathing effect.

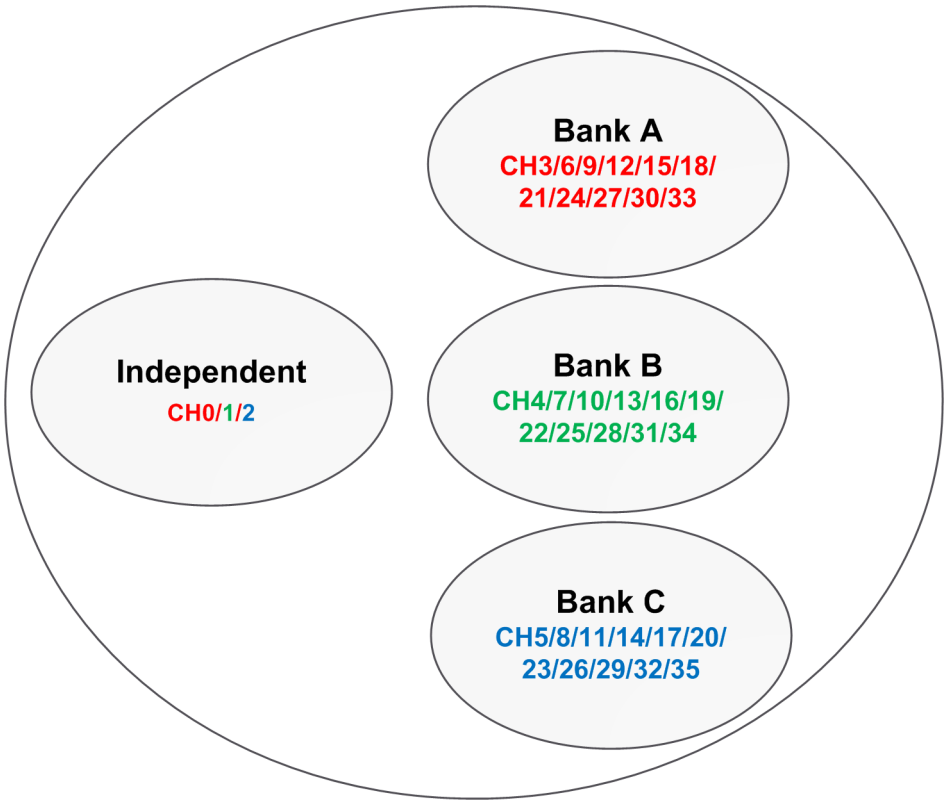

图 14. Bank PWM Control Example

8.3.3 Current Range Setting

The maximum constant-current value of all 30 or 36 channels is set by a single external resistor, R_{IREF}. The value of R_{IREF} can be calculated by 公式 1.

$$R_{IREF} = K_{IREF} \times \frac{V_{IREF}}{I_{SET}} \quad (1)$$

where:

- K_{IREF} = 105
- V_{IREF} = 0.7 V

With the IREF pin floating, the output current is close to zero. With the IREF pin shorted to GND, the LP503x device provides internal current-limit protection, and the output-channel maximum current is limited to I_{LIM}.

The LP503x device supports two levels of maximum output current, I_{MAX}.

- When V_{CC} is in the range from 2.7 V to 5.5 V, and the Max_Current_Option (bit) = 0, I_{MAX}= 25.5 mA.
- When V_{CC} is in the range from 3.3 V to 5.5 V, and the Max_Current_Option (bit) = 1, I_{MAX}= 35 mA.

8.3.4 Automatic Power-Save Mode

When all the LED outputs are inactive, the LP503x device is able to enter power-save mode automatically, thus lowering idle-current consumption down to 12 μA (maximum). Automatic power-save mode is enabled when register bit Power_Save_EN = 1 (default) and all the LEDs are off for a duration of >30 ms. Almost all analog blocks are powered down in power-save mode. If any I^2C command to the device occurs, the LP503x device returns to NORMAL mode.

8.3.5 Protection Features

8.3.5.1 Thermal Shutdown

The LP503x device implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160°C (typical), the device switches into shutdown mode. The LP503x device releases thermal shutdown when the junction temperature of the device is reduced to 145°C (typical).

8.3.5.2 UVLO

The LP503x device has an internal comparator that monitors the voltage at V_{CC}. When V_{CC} is below V_{UVF}, reset is active and the LP503x device is in the INITIALIZATION state.

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8.4 Device Functional Modes

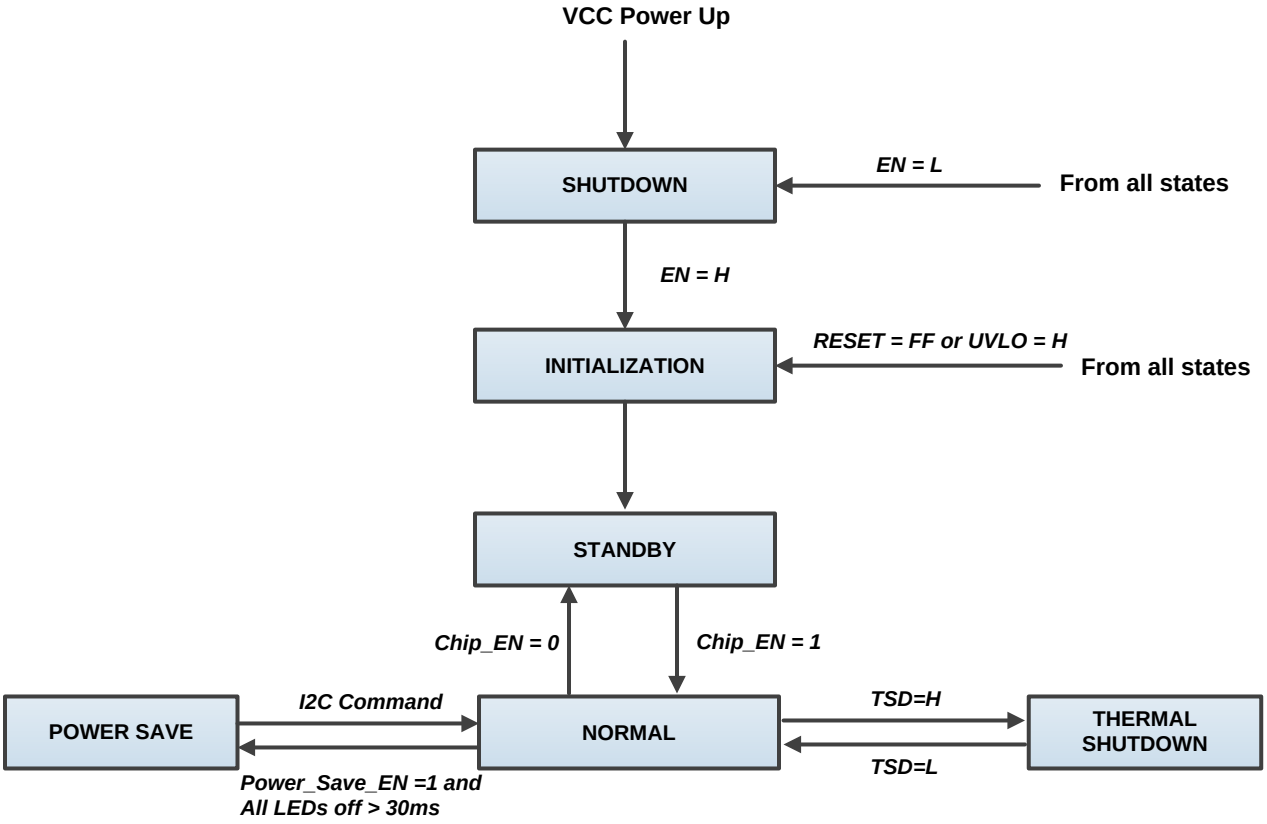

图 15. Functional Modes

- **INITIALIZATION**: The device enters into INITIALIZATION mode when EN = H. In this mode, all the registers are reset. Entry can also be from any state, if the RESET (register) = FFh or UVLO is active.
- **NORMAL**: The device enters the NORMAL mode when Chip_EN (register) = 1. I_{CC} is 10 mA (typical).
- **POWER SAVE**: The device automatically enters the POWER SAVE mode when Power_Save_EN (register) = 1 and all the LEDs are off for a duration of >30 ms. In POWER SAVE mode, analog blocks are disabled to minimize power consumption, but the registers retain the data and keep it available via I^2C. I_{CC} is 12 µA (maximum). In case of any I^2C command to this device, it goes back to the NORMAL mode.
- **SHUTDOWN**: The device enters into SHUTDOWN mode from all states on V_{CC} power up or when EN = L. I_{CC} is < 1 µA (max).
- **STANDBY**: The device enters the STANDBY mode when Chip_EN (register bit) = 0. In this mode, all the OUTx are shut down, but the registers retain the data and keep it available via I^2C. STANDBY is the low-power-consumption mode, when all circuit functions are disabled. I_{CC} is 10 µA (maximum).
- **THERMAL SHUTDOWN**: The device automatically enters the THERMAL SHUTDOWN mode when the junction temperature exceeds 160°C (typical). In this mode, all the OUTx outputs are shut down. If the junction temperature decreases below 145°C (typical), the device returns to the NORMAL mode.

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8.5 Programming

8.5.1 I²C Interface

The I²C-compatible two-wire serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock, SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle.

8.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when the clock signal is LOW.

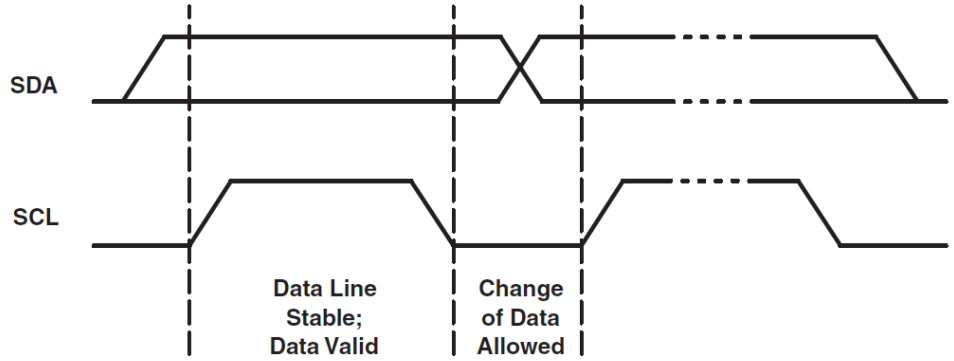

图 16. Data Validity

8.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus master always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

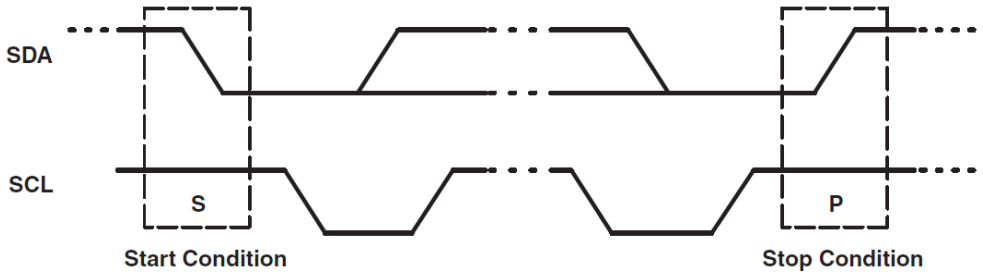

图 17. Start and Stop Conditions

8.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most-significant bit (MSB) being transferred first. Each byte of data must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

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Programming (接下页)

There is one exception to the acknowledge-after-every-byte rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit, which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

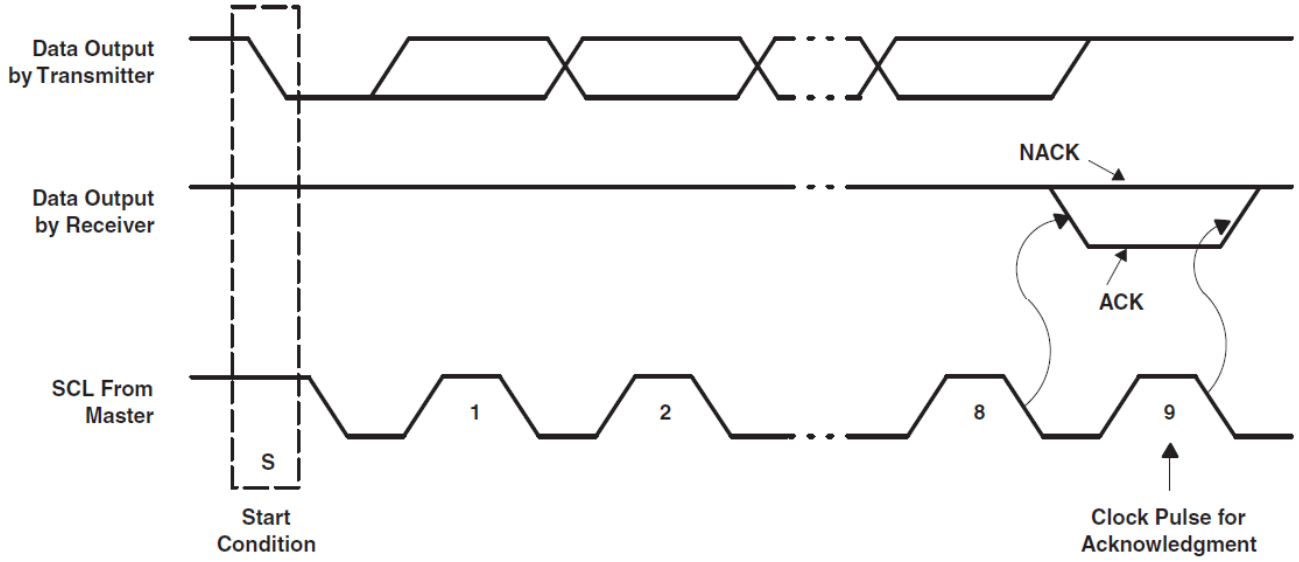

图 18. Acknowledge and Not Acknowledge on I²C Bus

8.5.1.4 I²C Slave Addressing

The device slave address is defined by connecting GND or VCC to the ADDR0 and ADDR1 pins. A total of four independent slave addresses can be realized by combinations when GND or VCC is connected to the ADDR0 and ADDR1 pins (see 表 2 and 表 3).

The device responds to a broadcast slave address regardless of the setting of the ADDR0 and ADDR1 pins. Global writes to the broadcast address can be used for configuring all devices simultaneously. The device supports global read using a broadcast address; however, the data read is only valid if all devices on the I²C bus contain the same value in the addressed register.

表 2. Slave-Address Combinations

ADDR1	ADDR0	SLAVE ADDRESS	
		INDEPENDENT	BROADCAST
GND	GND	011 0000	001 1100
GND	VCC	011 0001	
VCC	GND	011 0010	
VCC	VCC	011 0011	

表 3. Chip Address

	SLAVE ADDRESS							R/$\overline{W}$
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	0	1	1	0	0	ADDR1	ADDR0	1 or 0

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表 3. Chip Address (接下页)

	SLAVE ADDRESS							R/$\overline{W}$
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Broadcast	0	0	1	1	1	0	0	1 or 0

8.5.1.5 Control-Register Write Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/$\overline{W}$ = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device sends the data byte to be written to the addressed register.
- The slave device sends an acknowledge signal.
- If the master device sends further data bytes, the control register address of the slave is incremented by 1 after the acknowledge signal. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The write cycle ends when the master device creates a stop condition.

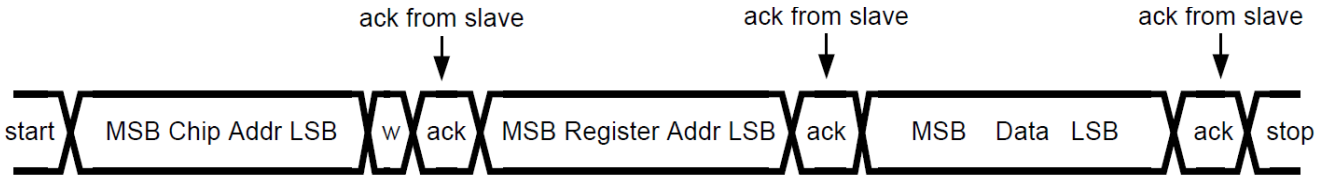

图 19. Write Cycle

8.5.1.6 Control-Register Read Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/$\overline{W}$ = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device generates a repeated-start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/$\overline{W}$ = 1).
- The slave device sends an acknowledge signal if the slave address is correct.
- The slave device sends the data byte from the addressed register.
- If the master device sends an acknowledge signal, the control-register address is incremented by 1. The slave device sends the data byte from the addressed register. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The read cycle ends when the master device does not generate an acknowledge signal after a data byte and generates a stop condition.

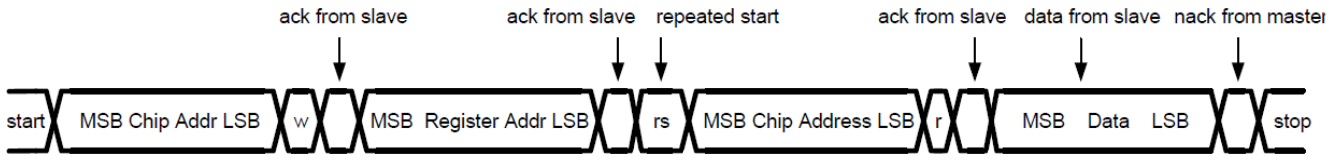

图 20. Read Cycle

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8.5.1.7 Auto-Increment Feature

The auto-increment feature allows writing or reading several consecutive registers within one transmission. For example, when an 8-bit word is sent to the device, the internal address index counter is incremented by 1, and the next register is written. The auto-increment feature is enabled by default and can be disabled by setting the Auto_Incr_EN bit = 0 in the DEVICE_CONFIG1 register. The auto-increment feature is applied for the full register address from 0h to FFh.

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8.6 Register Maps

表 4 lists the memory-mapped registers of the device.

表 4. Register Maps

REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
DEVICE_CONFIG0	00h	R/$\overline{W}$	RESERVED	Chip_EN	RESERVED						00h
DEVICE_CONFIG1	01h	R/$\overline{W}$	RESERVED		Log_Scale_EN	Power_Save_EN	Auto_Incr_EN	PWM_Dithering_EN	Max_Current_Option	LED_Global Off	3Ch
LED_CONFIG0	02h	R/$\overline{W}$	LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN	00h
LED_CONFIG1	03h	R/$\overline{W}$	RESERVED				LED11_Bank_EN	LED10_Bank_EN	LED9_Bank_EN	LED8_Bank_EN	00h
BANK_BRIGHTNESS	04h	R/$\overline{W}$	Bank_Brightness								FFh
BANK_A_COLOR	05h	R/$\overline{W}$	Bank_A_Color								00h
BANK_B_COLOR	06h	R/$\overline{W}$	Bank_B_Color								00h
BANK_C_COLOR	07h	R/$\overline{W}$	Bank_C_Color								00h
LED0_BRIGHTNESS	08h	R/$\overline{W}$	LED0_Brightness								FFh
LED1_BRIGHTNESS	09h	R/$\overline{W}$	LED1_Brightness								FFh
LED2_BRIGHTNESS	0Ah	R/$\overline{W}$	LED2_Brightness								FFh
LED3_BRIGHTNESS	0Bh	R/$\overline{W}$	LED3_Brightness								FFh
LED4_BRIGHTNESS	0Ch	R/$\overline{W}$	LED4_Brightness								FFh
LED5_BRIGHTNESS	0Dh	R/$\overline{W}$	LED5_Brightness								FFh
LED6_BRIGHTNESS	0Eh	R/$\overline{W}$	LED6_Brightness								FFh
LED7_BRIGHTNESS	0Fh	R/$\overline{W}$	LED7_Brightness								FFh
LED8_BRIGHTNESS	10h	R/$\overline{W}$	LED8_Brightness								FFh
LED9_BRIGHTNESS	11h	R/$\overline{W}$	LED9_Brightness								FFh

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Register Maps (接下页)

表 4. Register Maps (接下页)

REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
LED10_BRIGHTNESS	12h	R/$\overline{W}$	LED10_Brightness								FFh
LED11_BRIGHTNESS	13h	R/$\overline{W}$	LED11_Brightness								FFh
OUT0_COLOR	14h	R/$\overline{W}$	OUT0_Color								00h
OUT1_COLOR	15h	R/$\overline{W}$	OUT1_Color								00h
OUT2_COLOR	16h	R/$\overline{W}$	OUT2_Color								00h
OUT3_COLOR	17h	R/$\overline{W}$	OUT3_Color								00h
OUT4_COLOR	18h	R/$\overline{W}$	OUT4_Color								00h
OUT5_COLOR	19h	R/$\overline{W}$	OUT5_Color								00h
OUT6_COLOR	1Ah	R/$\overline{W}$	OUT6_Color								00h
OUT7_COLOR	1Bh	R/$\overline{W}$	OUT7_Color								00h
OUT8_COLOR	1Ch	R/$\overline{W}$	OUT8_Color								00h
OUT9_COLOR	1Dh	R/$\overline{W}$	OUT9_Color								00h
OUT10_COLOR	1Eh	R/$\overline{W}$	OUT10_Color								00h
OUT11_COLOR	1Fh	R/$\overline{W}$	OUT11_Color								00h
OUT12_COLOR	20h	R/$\overline{W}$	OUT12_Color								00h
OUT13_COLOR	21h	R/$\overline{W}$	OUT13_Color								00h
OUT14_COLOR	22h	R/$\overline{W}$	OUT14_Color								00h
OUT15_COLOR	23h	R/$\overline{W}$	OUT15_Color								00h
OUT16_COLOR	24h	R/$\overline{W}$	OUT16_Color								00h
OUT17_COLOR	25h	R/$\overline{W}$	OUT17_Color								00h
OUT18_COLOR	26h	R/$\overline{W}$	OUT18_Color								00h
OUT19_COLOR	27h	R/$\overline{W}$	OUT19_Color								00h
OUT20_COLOR	28h	R/$\overline{W}$	OUT20_Color								00h
OUT21_COLOR	29h	R/$\overline{W}$	OUT21_Color								00h
OUT22_COLOR	2Ah	R/$\overline{W}$	OUT22_Color								00h
OUT23_COLOR	2Bh	R/$\overline{W}$	OUT23_Color								00h
OUT24_COLOR	2Ch	R/$\overline{W}$	OUT24_Color								00h
OUT25_COLOR	2Dh	R/$\overline{W}$	OUT25_Color								00h
OUT26_COLOR	2Eh	R/$\overline{W}$	OUT26_Color								00h
OUT27_COLOR	2Fh	R/$\overline{W}$	OUT27_Color								00h

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Register Maps (接下页)

表 4. Register Maps (接下页)

REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
OUT28_COLOR	30h	R/$\overline{W}$	OUT28_Color								00h
OUT29_COLOR	31h	R/$\overline{W}$	OUT29_Color								00h
OUT30_COLOR	32h	R/$\overline{W}$	OUT30_Color								00h
OUT31_COLOR	33h	R/$\overline{W}$	OUT31_Color								00h
OUT32_COLOR	34h	R/$\overline{W}$	OUT32_Color								00h
OUT33_COLOR	35h	R/$\overline{W}$	OUT33_Color								00h
OUT34_COLOR	36h	R/$\overline{W}$	OUT34_Color								00h
OUT35_COLOR	37h	R/$\overline{W}$	OUT35_Color								00h
RESET	38h	W	Reset								00h

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表 5. Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 DEVICE_CONFIG0 (Address = 0h) [reset = 0h]

DEVICE_CONFIG0 is shown in 图 21 and described in 表 6.

Return to 表 4.

图 21. DEVICE_CONFIG0 Register

7	6	5	4	3	2	1	0
RESERVED	Chip_EN	RESERVED					
R/$\overline{W}$-0h	R/$\overline{W}$-0h	R/$\overline{W}$-0h					

表 6. DEVICE_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/$\overline{W}$	0h	Reserved
6	Chip_EN	R/$\overline{W}$	0h	0 = LP503x not enabled 1 = LP503x enabled
5–0	RESERVED	R/$\overline{W}$	0h	Reserved

8.6.2 DEVICE_CONFIG1 (Address = 1h) [reset = 3Ch]

DEVICE_CONFIG1 is shown in 图 22 and described in 表 7.

Return to 表 4.

图 22. DEVICE_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED		Log_Scale_EN	Power_Save_EN	Auto_Incr_EN	PWM_Dithering_EN	Max_Current_Option	LED_Global Off
R/$\overline{W}$-0h		R/$\overline{W}$-1h	R/$\overline{W}$-1h	R/$\overline{W}$-1h	R/$\overline{W}$-1h	R/$\overline{W}$-0h	R/$\overline{W}$-0h

表 7. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	RESERVED	R/$\overline{W}$	0h	Reserved
5	Log_Scale_EN	R/$\overline{W}$	1h	0 = Linear scale dimming curve enabled 1 = Logarithmic scale dimming curve enabled
4	Power_Save_EN	R/$\overline{W}$	1h	0 = Automatic power-saving mode not enabled 1 = Automatic power-saving mode enabled
3	Auto_Incr_EN	R/$\overline{W}$	1h	0 = Automatic increment mode not enabled 1 = Automatic increment mode enabled
2	PWM_Dithering_EN	R/$\overline{W}$	1h	0 = PWM dithering mode not enabled 1 = PWM dithering mode enabled
1	Max_Current_Option	R/$\overline{W}$	0h	0 = Output maximum current I_{MAX} = 25.5 mA. 1 = Output maximum current I_{MAX} = 35 mA.

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表 7. DEVICE_CONFIG1 Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
0	LED_Global Off	R/W	0h	0 = Normal operation 1 = Shut down all LEDs

8.6.3 LED_CONFIG0 (Address = 2h) [reset = 00h]

LED_CONFIG0 is shown in 图 23 and described in 表 8.

Return to 表 4.

图 23. LED_CONFIG0 Register

7	6	5	4	3	2	1	0
LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8. LED_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LED7_Bank_EN	R/W	0h	0 = LED7 independent control mode enabled 1 = LED7 bank control mode enabled
6	LED6_Bank_EN	R/W	0h	0 = LED6 independent control mode enabled 1 = LED6 bank control mode enabled
5	LED5_Bank_EN	R/W	0h	0 = LED5 independent control mode enabled 1 = LED5 bank control mode enabled
4	LED4_Bank_EN	R/W	0h	0 = LED4 independent control mode enabled 1 = LED4 bank control mode enabled
3	LED3_Bank_EN	R/W	0h	0 = LED3 Independent control mode enabled 1 = LED3 bank control mode enabled
2	LED2_Bank_EN	R/W	0h	0 = LED2 independent control mode enabled 1 = LED2 bank control mode enabled
1	LED1_Bank_EN	R/W	0h	0 = LED1 independent control mode enabled 1 = LED1 bank control mode enabled
0	LED0_Bank_EN	R/W	0h	0 = LED0 independent control mode enabled 1 = LED0 bank control mode enabled

8.6.4 LED_CONFIG1 (Address = 3h) [reset = 00h]

LED_CONFIG1 is shown in 图 23 and described in 表 8.

Return to 表 4.

图 24. LED_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED				LED11_Bank_EN	LED10_Bank_EN	LED9_Bank_EN	LED8_Bank_EN
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 9. LED_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
4–7	RESERVED	R/W	0h	Reserved
3	LED11_Bank_EN	R/W	0h	0 = LED11 Independent control mode enabled 1 =LED11 bank control mode enabled

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表 9. LED_CONFIG1 Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
2	LED10_Bank_EN	R/$\overline{W}$	0h	0 = LED10 independent control mode enabled 1 = LED10 bank control mode enabled
1	LED9_Bank_EN	R/$\overline{W}$	0h	0 =LED9 independent control mode enabled 1 = LED9 bank control mode enabled
0	LED8_Bank_EN	R/$\overline{W}$	0h	0 = LED8 independent control mode enabled 1 = LED8 bank control mode enabled

8.6.5 BANK_BRIGHTNESS (Address = 4h) [reset = FFh]

BANK_BRIGHTNESS is shown in 图 25 and described in 表 10.

Return to 表 4.

图 25. BANK_BRIGHTNESS Register

7	6	5	4	3	2	1	0
BANK_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 10. BANK_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	BANK_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full ... FFh = 100 % of full intensity

8.6.6 BANK_A_COLOR (Address = 5h) [reset = 00h]

BANK_A_COLOR is shown in 图 26 and described in 表 11.

Return to 表 4.

图 26. BANK_A_COLOR Register

7	6	5	4	3	2	1	0
BANK_A_COLOR							
R/$\overline{W}$-0h							

表 11. BANK_A_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	BANK_A_COLOR	R/$\overline{W}$	0h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.7 BANK_B_COLOR (Address = 6h) [reset = 00h]

BANK_B_COLOR is shown in 图 27 and described in 表 12.

Return to 表 4.

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图 27. BANK_B_COLOR Register

7	6	5	4	3	2	1	0
BANK_B_COLOR							
R/$\overline{W}$-0h							

表 12. BANK_B_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	BANK_B_COLOR	R/$\overline{W}$	0h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.8 BANK_C_COLOR (Address = 7h) [reset = 00h]

BANK_C_COLOR is shown in 图 28 and described in 表 13.

Return to 表 4.

图 28. BANK_C_COLOR Register

7	6	5	4	3	2	1	0
BANK_C_COLOR							
R/$\overline{W}$-0h							

表 13. BANK_C_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	BANK_C_COLOR	R/$\overline{W}$	0h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.9 LED0_BRIGHTNESS (Address = 8h) [reset = FFh]

LED0_BRIGHTNESS is shown in 图 29 and described in 表 14.

Return to 表 4.

图 29. LED0_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED0_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 14. LED0_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED0_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

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8.6.10 LED1_BRIGHTNESS (Address = 9h) [reset = FFh]

LED1_BRIGHTNESS is shown in 图 30 and described in 表 15.

Return to 表 4.

图 30. LED1_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED1_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 15. LED1_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED1_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.11 LED2_BRIGHTNESS (Address = 0Ah) [reset = FFh]

LED2_BRIGHTNESS is shown in 图 31 and described in 表 16.

Return to 表 4.

图 31. LED2_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED2_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 16. LED2_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED2_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.12 LED3_BRIGHTNESS (Address = 0Bh) [reset = FFh]

LED3_BRIGHTNESS is shown in 图 32 and described in 表 17.

Return to 表 4.

图 32. LED3_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED3_BRIGHTNESS							
R/$\overline{W}$-FFh							

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表 17. LED3_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED3_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.13 LED4_BRIGHTNESS (Address = 0Ch) [reset = FFh]

LED4_BRIGHTNESS is shown in 图 33 and described in 表 18.

Return to 表 4.

图 33. LED4_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED4_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 18. LED4_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED4_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.14 LED5_BRIGHTNESS (Address = 0Dh) [reset = FFh]

LED5_BRIGHTNESS is shown in 图 34 and described in 表 19.

Return to 表 4.

图 34. LED5_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED5_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 19. LED5_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED5_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.15 LED6_BRIGHTNESS (Address = 0Eh) [reset = FFh]

LED6_BRIGHTNESS is shown in 图 35 and described in 表 20.

Return to 表 4.

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图 35. LED6_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED6_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 20. LED6_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED6_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.16 LED7_BRIGHTNESS (Address = 0Fh) [reset = FFh]

LED7_BRIGHTNESS is shown in 图 36 and described in 表 21.

Return to 表 4.

图 36. LED7_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED7_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 21. LED7_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED7_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.17 LED8_BRIGHTNESS (Address = 10h) [reset = FFh]

LED8_BRIGHTNESS is shown in 图 37 and described in 表 22.

Return to 表 4.

图 37. LED8_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED8_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 22. LED8_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED8_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

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8.6.18 LED9_BRIGHTNESS (Address = 11h) [reset = FFh]

LED9_BRIGHTNESS is shown in 图 38 and described in 表 23.

Return to 表 4.

图 38. LED9_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED9_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 23. LED9_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED9_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.19 LED10_BRIGHTNESS (Address = 12h) [reset = FFh]

LED10_BRIGHTNESS is shown in 图 39 and described in 表 24.

Return to 表 4.

图 39. LED10_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED10_BRIGHTNESS							
R/$\overline{W}$-FFh							

表 24. LED10_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED10_BRIGHTNESS	R/$\overline{W}$	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.20 LED11_BRIGHTNESS (Address = 13h) [reset = FFh]

LED11_BRIGHTNESS is shown in 图 40 and described in 表 25.

Return to 表 4.

图 40. LED11_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED11_BRIGHTNESS							
R/$\overline{W}$-FFh							

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表 25. LED11_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	LED11_BRIGHTNESS	R/W	FFh	00h = 0% of full intensity ... 80h = 50% of full intensity ... FFh = 100 % of full intensity

8.6.21 OUT0_COLOR (Address = 14h) [reset = 00h]

OUT0_COLOR is shown in 图 41 and described in 表 26.

Return to 表 4.

图 41. OUT0_COLOR Register

7	6	5	4	3	2	1	0
OUT0_COLOR							
R/W-00h							

表 26. OUT0_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT0_COLOR	R/W	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.22 OUT1_COLOR (Address = 15h) [reset = 00h]

OUT1_COLOR is shown in 图 42 and described in 表 27.

Return to 表 4.

图 42. OUT1_COLOR Register

7	6	5	4	3	2	1	0
OUT1_COLOR							
R/W-00h							

表 27. OUT1_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT1_COLOR	R/W	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.23 OUT2_COLOR (Address = 16h) [reset = 00h]

OUT2_COLOR is shown in 图 43 and described in 表 28.

Return to 表 4.

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图 43. OUT2_COLOR Register

7	6	5	4	3	2	1	0
OUT2_COLOR							
R/$\overline{W}$-00h							

表 28. OUT2_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT2_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.24 OUT3_COLOR (Address = 17h) [reset = 00h]

OUT3_COLOR is shown in 图 44 and described in 表 29.

Return to 表 4.

图 44. OUT3_COLOR Register

7	6	5	4	3	2	1	0
OUT3_COLOR							
R/$\overline{W}$-00h							

表 29. OUT3_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT3_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.25 OUT4_COLOR (Address = 18h) [reset = 00h]

OUT4_COLOR is shown in 图 45 and described in 表 30.

Return to 表 4.

图 45. OUT4_COLOR Register

7	6	5	4	3	2	1	0
OUT1_COLOR							
R/$\overline{W}$-00h							

表 30. OUT4_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT4_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

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8.6.26 OUT5_COLOR (Address = 19h) [reset = 00h]

OUT5_COLOR is shown in 图 46 and described in 表 31.

Return to 表 4.

图 46. OUT5_COLOR Register

7	6	5	4	3	2	1	0
OUT5_COLOR							
R/$\overline{W}$-00h							

表 31. OUT5_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT5_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.27 OUT6_COLOR (Address = 1Ah) [reset = 00h]

OUT6_COLOR is shown in 图 47 and described in 表 32.

Return to 表 4.

图 47. OUT6_COLOR Register

7	6	5	4	3	2	1	0
OUT6_COLOR							
R/$\overline{W}$-00h							

表 32. OUT6_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT6_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.28 OUT7_COLOR (Address = 1Bh) [reset = 00h]

OUT7_COLOR is shown in 图 48 and described in 表 33.

Return to 表 4.

图 48. OUT7_COLOR Register

7	6	5	4	3	2	1	0
OUT7_COLOR							
R/$\overline{W}$-00h							

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表 33. OUT7_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT7_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.29 OUT8_COLOR (Address = 1Ch) [reset = 00h]

OUT8_COLOR is shown in 图 49 and described in 表 34.

Return to 表 4.

图 49. OUT8_COLOR Register

7	6	5	4	3	2	1	0
OUT8_COLOR							
R/$\overline{W}$-00h							

表 34. OUT8_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT8_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.30 OUT9_COLOR (Address = 1Dh) [reset = 00h]

OUT9_COLOR is shown in 图 50 and described in 表 35.

Return to 表 4.

图 50. OUT9_COLOR Register

7	6	5	4	3	2	1	0
OUT9_COLOR							
R/$\overline{W}$-00h							

表 35. OUT9_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT9_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.31 OUT10_COLOR (Address = 1Eh) [reset = 00h]

OUT10_COLOR is shown in 图 51 and described in 表 36.

Return to 表 4.

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图 51. OUT10_COLOR Register

7	6	5	4	3	2	1	0
OUT10_COLOR							
R/$\overline{W}$0-0h							

表 36. OUT10_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT10_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.32 OUT11_COLOR (Address = 1Fh) [reset = 00h]

OUT11_COLOR is shown in 图 52 and described in 表 37.

Return to 表 4.

图 52. OUT11_COLOR Register

7	6	5	4	3	2	1	0
OUT11_COLOR							
R/$\overline{W}$-00h							

表 37. OUT11_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT11_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.33 OUT12_COLOR (Address = 20h) [reset = 00h]

OUT12_COLOR is shown in 图 53 and described in 表 38.

Return to 表 4.

图 53. OUT12_COLOR Register

7	6	5	4	3	2	1	0
OUT12_COLOR							
R/$\overline{W}$-00h							

表 38. OUT12_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT12_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

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8.6.34 OUT13_COLOR (Address = 21h) [reset = 00h]

OUT13_COLOR is shown in 图 54 and described in 表 39.

Return to 表 4.

图 54. OUT13_COLOR Register

7	6	5	4	3	2	1	0
OUT13_COLOR							
R/$\overline{W}$-00h							

表 39. OUT13_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT13_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.35 OUT14_COLOR (Address = 22h) [reset = 00h]

OUT14_COLOR is shown in 图 55 and described in 表 40.

Return to 表 4.

图 55. OUT14_COLOR Register

7	6	5	4	3	2	1	0
OUT14_COLOR							
R/$\overline{W}$-00h							

表 40. OUT14_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT14_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.36 OUT15_COLOR (Address = 23h) [reset = 00h]

OUT15_COLOR is shown in 图 56 and described in 表 41.

Return to 表 4.

图 56. OUT15_COLOR Register

7	6	5	4	3	2	1	0
OUT15_COLOR							
R/$\overline{W}$-00h							

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表 41. OUT15_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT15_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.37 OUT16_COLOR (Address = 24h) [reset = 00h]

OUT16_COLOR is shown in 图 57 and described in 表 42.

Return to 表 4.

图 57. OUT16_COLOR Register

7	6	5	4	3	2	1	0
OUT16_COLOR							
R/$\overline{W}$-00h							

表 42. OUT16_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT16_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.38 OUT17_COLOR (Address = 25h) [reset = 00h]

OUT17_COLOR is shown in 图 58 and described in 表 43.

Return to 表 4.

图 58. OUT17_COLOR Register

7	6	5	4	3	2	1	0
OUT17_COLOR							
R/$\overline{W}$-00h							

表 43. OUT17_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT17_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.39 OUT18_COLOR (Address = 26h) [reset = 00h]

OUT18_COLOR is shown in 图 59 and described in 表 44.

Return to 表 4.

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图 59. OUT18_COLOR Register

7	6	5	4	3	2	1	0
OUT18_COLOR							
R/$\overline{W}$-00h							

表 44. OUT18_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT18_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.40 OUT19_COLOR (Address = 27h) [reset = 00h]

OUT19_COLOR is shown in 图 60 and described in 表 45.

Return to 表 4.

图 60. OUT19_COLOR Register

7	6	5	4	3	2	1	0
OUT19_COLOR							
R/$\overline{W}$-00h							

表 45. OUT19_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT19_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.41 OUT20_COLOR (Address = 28h) [reset = 00h]

OUT20_COLOR is shown in 图 61 and described in 表 46.

Return to 表 4.

图 61. OUT20_COLOR Register

7	6	5	4	3	2	1	0
OUT20_COLOR							
R/$\overline{W}$-00h							

表 46. OUT20_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT20_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

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8.6.42 OUT21_COLOR (Address = 29h) [reset = 00h]

OUT21_COLOR is shown in 图 62 and described in 表 47.

Return to 表 4.

图 62. OUT21_COLOR Register

7	6	5	4	3	2	1	0
OUT21_COLOR							
R/$\overline{W}$-00h							

表 47. OUT21_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT21_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.43 OUT22_COLOR (Address = 2Ah) [reset = 00h]

OUT22_COLOR is shown in 图 63 and described in 表 48.

Return to 表 4.

图 63. OUT22_COLOR Register

7	6	5	4	3	2	1	0
OUT22_COLOR							
R/$\overline{W}$-00h							

表 48. OUT22_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT22_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.44 OUT23_COLOR (Address = 2Bh) [reset = 00h]

OUT23_COLOR is shown in 图 64 and described in 表 49.

Return to 表 4.

图 64. OUT23_COLOR Register

7	6	5	4	3	2	1	0
OUT23_COLOR							
R/$\overline{W}$-00h							

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表 49. OUT23_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT23_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.45 OUT24_COLOR (Address = 2Ch) [reset = 00h]

OUT24_COLOR is shown in 图 65 and described in 表 50.

Return to 表 4.

图 65. OUT24_COLOR Register

7	6	5	4	3	2	1	0
OUT24_COLOR							
R/$\overline{W}$-00h							

表 50. OUT24_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT24_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.46 OUT25_COLOR (Address = 2Dh) [reset = 00h]

OUT25_COLOR is shown in 图 66 and described in 表 51.

Return to 表 4.

图 66. OUT25_COLOR Register

7	6	5	4	3	2	1	0
OUT25_COLOR							
R/$\overline{W}$-00h							

表 51. OUT25_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT25_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.47 OUT26_COLOR (Address = 2Eh) [reset = 00h]

OUT26_COLOR is shown in 图 67 and described in 表 52.

Return to 表 4.

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图 67. OUT26_COLOR Register

7	6	5	4	3	2	1	0
OUT26_COLOR							
R/$\overline{W}$-00h							

表 52. OUT26_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT26_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.48 OUT27_COLOR (Address = 2Fh) [reset = 00h]

OUT27_COLOR is shown in 图 68 and described in 表 53.

Return to 表 4.

图 68. OUT27_COLOR Register

7	6	5	4	3	2	1	0
OUT27_COLOR							
R/$\overline{W}$-00h							

表 53. OUT27_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT27_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.49 OUT28_COLOR (Address = 30h) [reset = 00h]

OUT28_COLOR is shown in 图 69 and described in 表 54.

Return to 表 4.

图 69. OUT28_COLOR Register

7	6	5	4	3	2	1	0
OUT28_COLOR							
R/$\overline{W}$-00h							

表 54. OUT28_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT28_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

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8.6.50 OUT29_COLOR (Address = 31h) [reset = 00h]

OUT29_COLOR is shown in 图 70 and described in 表 55.

Return to 表 4.

图 70. OUT29_COLOR Register

7	6	5	4	3	2	1	0
OUT29_COLOR							
R/$\overline{W}$-00h							

表 55. OUT29_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT29_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.51 OUT30_COLOR (Address = 32h) [reset = 00h]

OUT30_COLOR is shown in 图 71 and described in 表 56.

Return to 表 4.

图 71. OUT30_COLOR Register

7	6	5	4	3	2	1	0
OUT30_COLOR							
R/$\overline{W}$-00h							

表 56. OUT30_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT30_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.52 OUT31_COLOR (Address = 33h) [reset = 00h]

OUT31_COLOR is shown in 图 72 and described in 表 57.

Return to 表 4.

图 72. OUT31_COLOR Register

7	6	5	4	3	2	1	0
OUT31_COLOR							
R/$\overline{W}$-00h							

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表 57. OUT31_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT31_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.53 OUT32_COLOR (Address = 34h) [reset = 00h]

OUT32_COLOR is shown in 图 73 and described in 表 58.

Return to 表 4.

图 73. OUT32_COLOR Register

7	6	5	4	3	2	1	0
OUT32_COLOR							
R/$\overline{W}$-00h							

表 58. OUT32_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT32_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.54 OUT33_COLOR (Address = 35h) [reset = 00h]

OUT33_COLOR is shown in 图 74 and described in 表 59.

Return to 表 4.

图 74. OUT33_COLOR Register

7	6	5	4	3	2	1	0
OUT33_COLOR							
R/$\overline{W}$-00h							

表 59. OUT33_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT33_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.55 OUT34_COLOR (Address = 36h) [reset = 00h]

OUT34_COLOR is shown in 图 75 and described in 表 60.

Return to 表 4.

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图 75. OUT34_COLOR Register

7	6	5	4	3	2	1	0
OUT34_COLOR							
R/$\overline{W}$-00h							

表 60. OUT34_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT34_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.56 OUT35_COLOR (Address = 37h) [reset = 00h]

OUT35_COLOR is shown in 图 76 and described in 表 61.

Return to 表 4.

图 76. OUT35_COLOR Register

7	6	5	4	3	2	1	0
OUT35_COLOR							
R/$\overline{W}$-00h							

表 61. OUT35_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	OUT35_COLOR	R/$\overline{W}$	00h	00h = The color mixing percentage is 0%. ... 80h = The color mixing percentage is 50%. ... FFh = The color mixing percentage is 100%.

8.6.57 RESET (Address = 38h) [reset = 00h]

RESET is shown in 图 77 and described in 表 62.

Return to 表 4.

图 77. RESET Register

7	6	5	4	3	2	1	0
RESET							
W-00h							

表 62. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	RESET	W	00h	FFh = Reset all the registers to default value.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP503x device is a 30- or 36-channel constant-current-sink LED driver. The LP503x device improves the user experience in color mixing and intensity control, for both live effects and coding effort. The optimized performance for RGB LEDs makes it a perfect fit for human-machine interaction applications.

9.2 Typical Application

The LP503x design supports up to four devices in parallel with different configurations on the ADDR0 and ADDR1 pins.

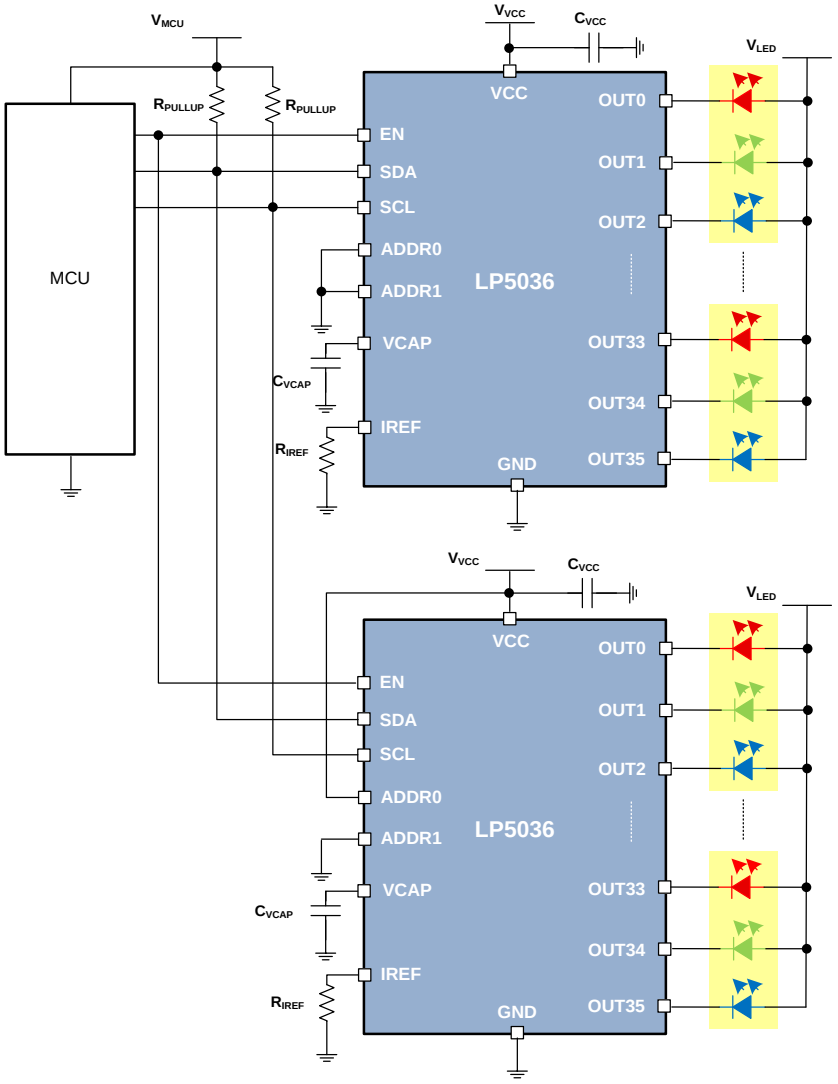

图 78. Driving Dual LP5036 Application Example

Typical Application (接下页)

9.2.1 Design Requirements

Set the LED current to 15 mA using the R_{IREF} resistor.

9.2.2 Detailed Design Procedure

The LP503x device scales up the reference current (I_{REF}) set by the external resistor (R_{IREF}) to sink the output current (I_{OUT}) at each output port. can be used to calculate the target output current I_{MAX_SET}:

$$R_{IREF} = \frac{K_{IREF} \times V_{IREF}}{I_{(MAX\_SET)}} = 105 \times 0.7 \div 0.015 = 4900\ \Omega$$

The SCL and SDA lines must each have a pullup resistor placed somewhere on the line (the pullup resistors are normally located on the bus master). In typical applications, values of 1.8 kΩ to 4.7 kΩ are used, depending on the bus capacitance, I/O voltage, and the desired communication speed. Selecting a smaller value increases the pullup speed, but slows the pulldown speed. If they want pull up quickly select the samller one but it will impact the pull down speed.

VCAP is the internal LDO output pin. This pin must be connected through a 1-μF capacitor to GND. Put the capacitor as close to the device as possible.

TI recommends having a 1-μF capacitor between VCC and GND to ensure proper operation. Put the capacitor as close to the device as possible.

9.2.3 Application Curves

The test condition for is that the testing is under bank control, using the following register values: 0x02 (0xFF), 0x04 (0xF0), 0x05 (0xF0), 0x06 (0xF0). The test condition for is that the testing is under bank control, using the following register values: 0x02 (0xFF), 0x04 (0x0F), 0x05 (0x0F), 0x06 (0x0F).

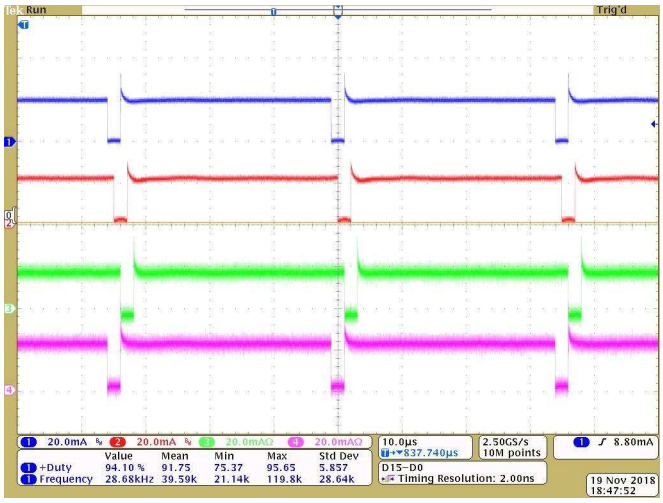

图 79. Current Waveform of OUT0, OUT1, OUT2 and OUT3

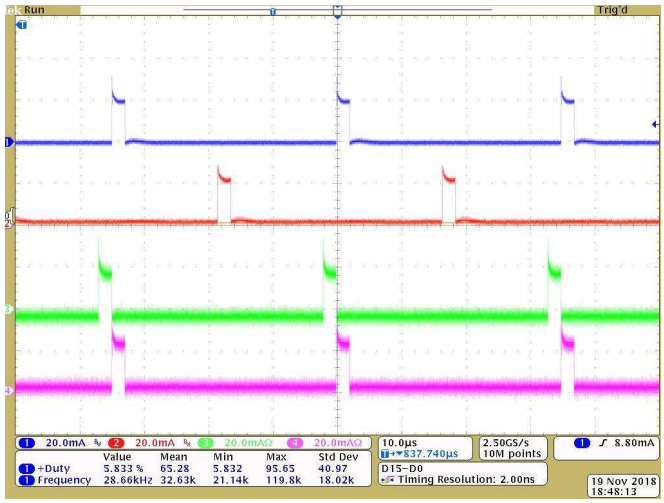

图 80. Current Waveform of OUT0, OUT1, OUT2 and OUT3

10 Power Supply Recommendations

The device is designed to operate from a V_{VCC} input-voltage supply range between 2.7 V and 5.5 V. This input supply must be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even in a load-transition condition (start-up or rapid intensity change). The resistance of the input supply rail must be low enough that the input-current transient does not cause a drop below the 2.7-V level in the LP503x V_{VCC} supply voltage.

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11 Layout

11.1 Layout Guidelines

To prevent thermal shutdown, the junction temperature, T_J, must be less than $T_{(TSD)}$. If the voltage drop across the output channels is high, the device power dissipation can be large. The LP503x device has very good thermal performance because of the thermal pad design; however, the PCB layout is also very important to ensure that the device has good thermal performance. Good PCB design can optimize heat transfer, which is essential for the long-term reliability of the device.

Use the following guidelines when designing the device layout:

- Put the C_{VCAP}, C_{VCC} and R_{IREF} as close as possible to the device. Also, TI recommends placing the ground plane as shown in 图 81 and 图 82.
- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through copper on the PCB. Maximum copper density is extremely important when no heat sinks are attached to the PCB on the other side from the package.
- Add as many thermal vias as possible directly under the package ground pad to maximize the thermal conductivity of the board.
- Use either plated-shut or plugged and capped vias for all the thermal vias on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

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11.2 Layout Examples

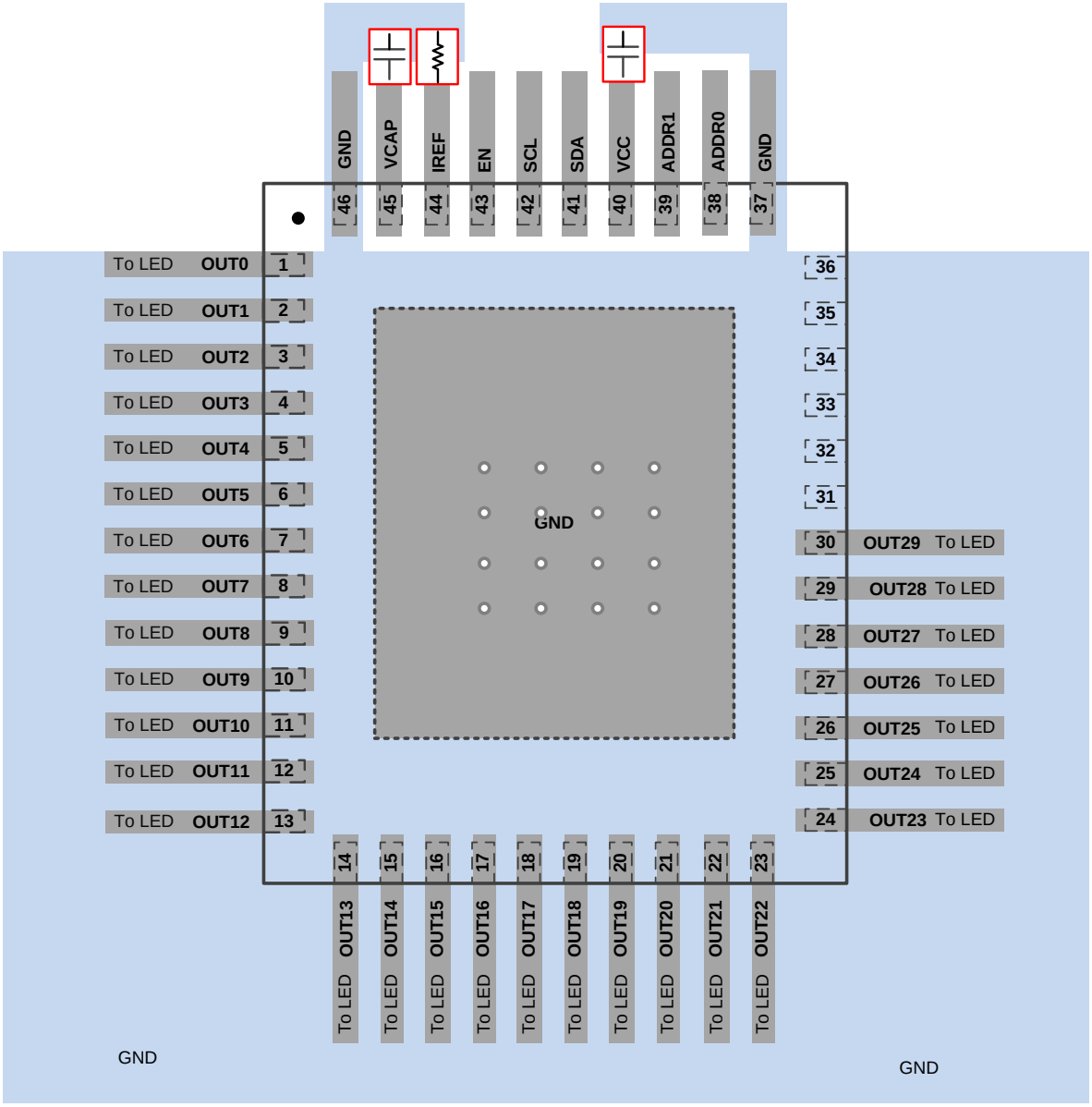

图 81. LP5030 Layout Example

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Layout Examples (接下页)

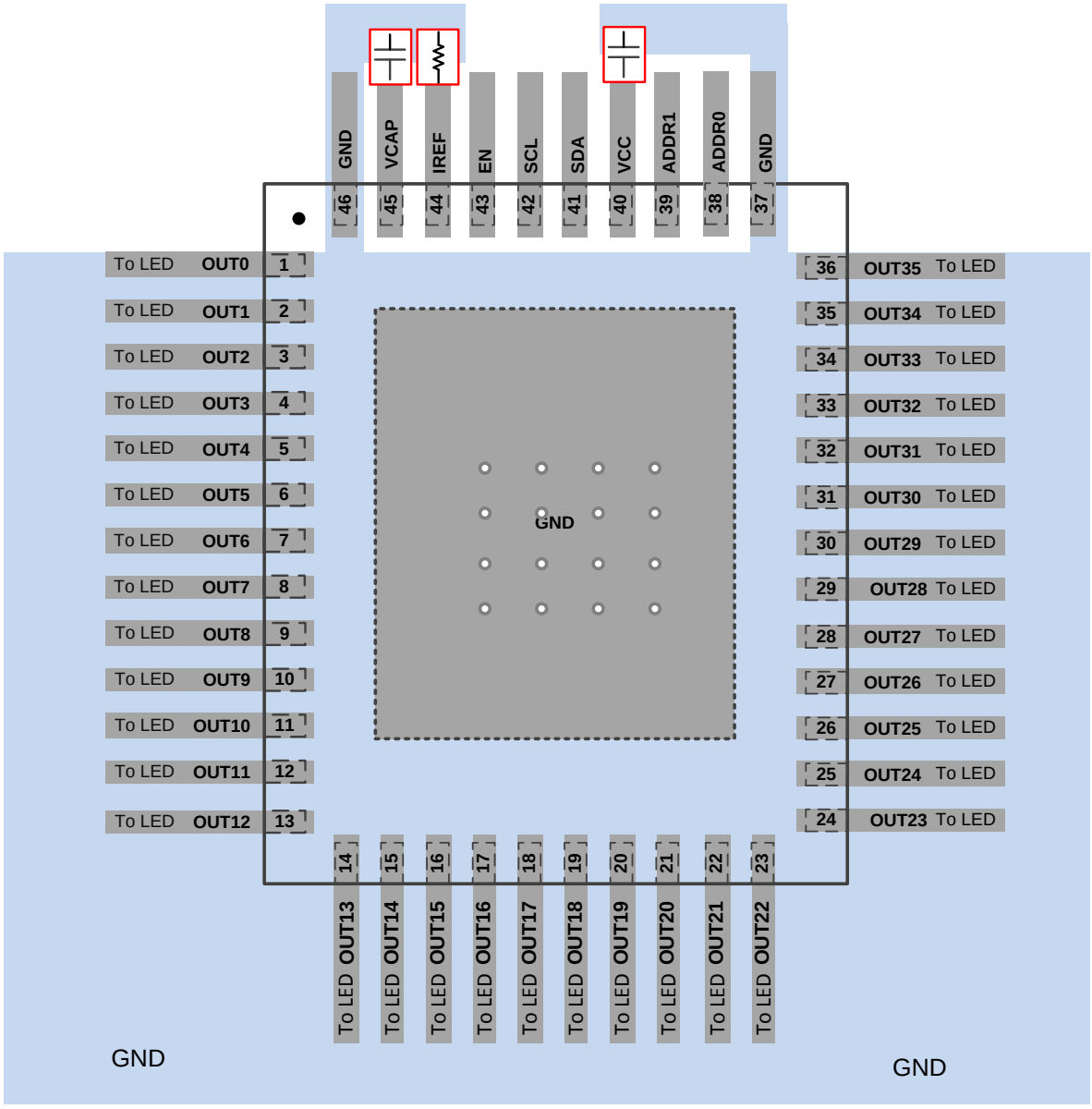

图 82. LP5036 Layout Example

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **63.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
LP5030	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LP5036	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5030RJVR	Active	Production	VQFN (RJV) | 46	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5030
LP5030RJVR.A	Active	Production	VQFN (RJV) | 46	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5030
LP5036RJVR	Active	Production	VQFN (RJV) | 46	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5036
LP5036RJVR.A	Active	Production	VQFN (RJV) | 46	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5036
LP5036RJVRG4	Active	Production	VQFN (RJV) | 46	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5036
LP5036RJVRG4.A	Active	Production	VQFN (RJV) | 46	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5036

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

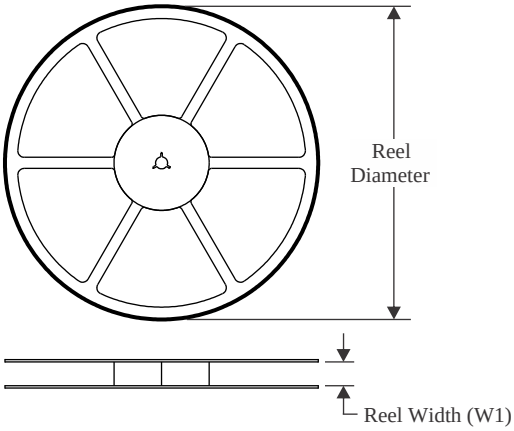
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

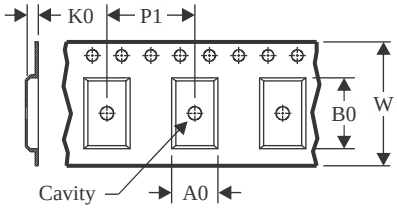
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

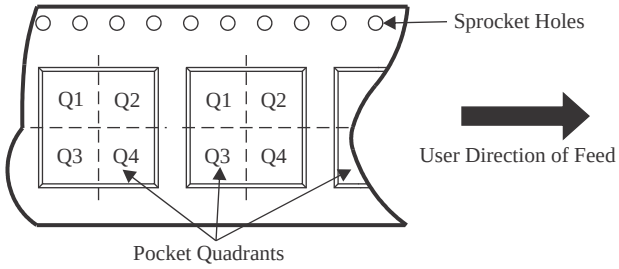


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

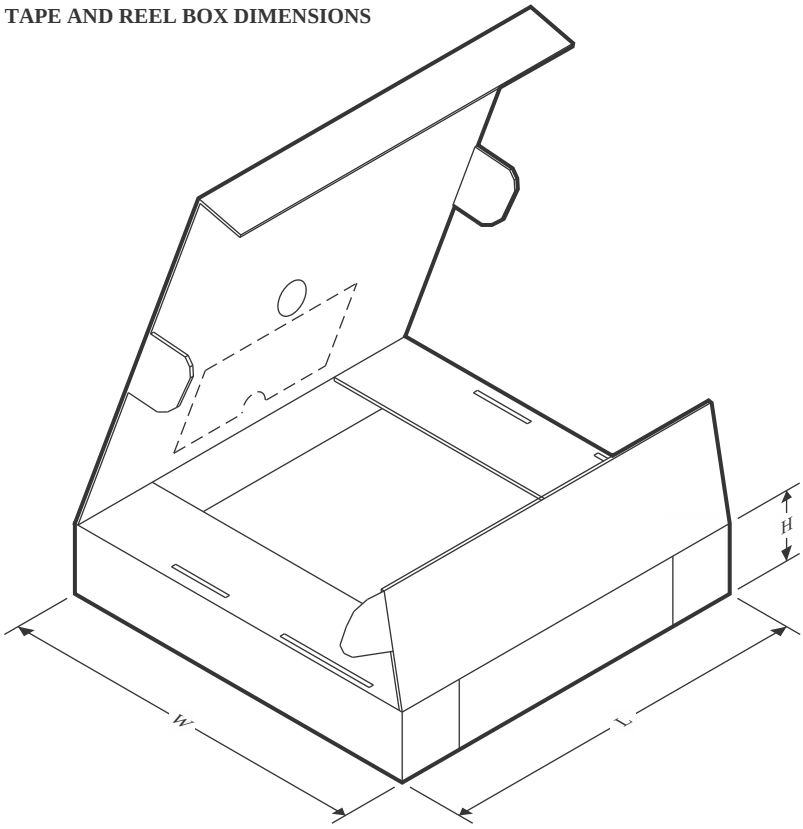
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5030RJVR	VQFN	RJV	46	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q1
LP5036RJVR	VQFN	RJV	46	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q1
LP5036RJVRG4	VQFN	RJV	46	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

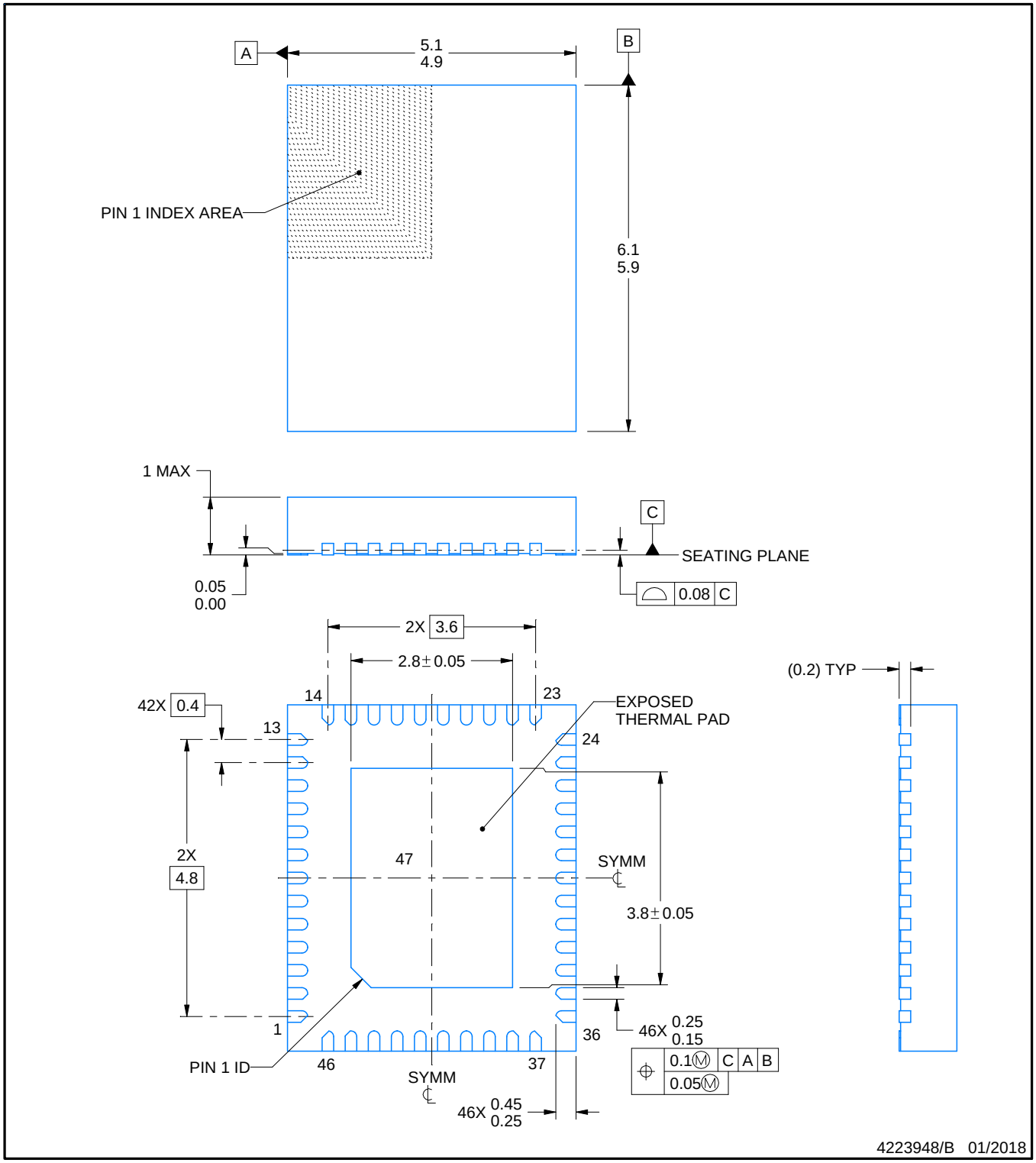
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5030RJVR	VQFN	RJV	46	3000	367.0	367.0	35.0
LP5036RJVR	VQFN	RJV	46	3000	367.0	367.0	35.0
LP5036RJVRG4	VQFN	RJV	46	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RJV0046A

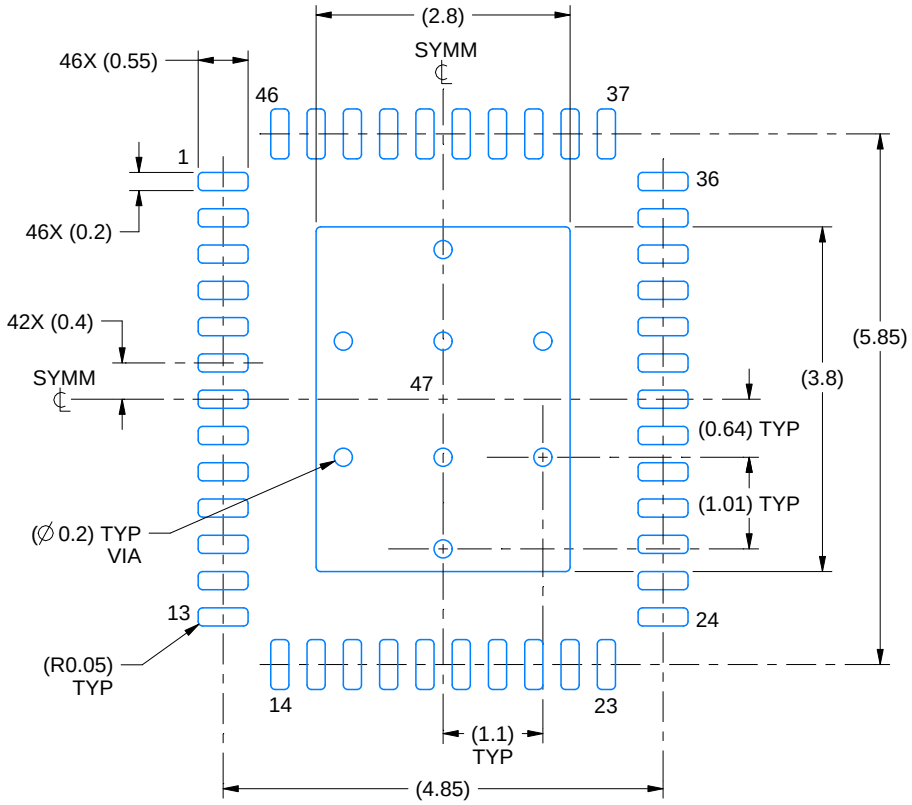
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

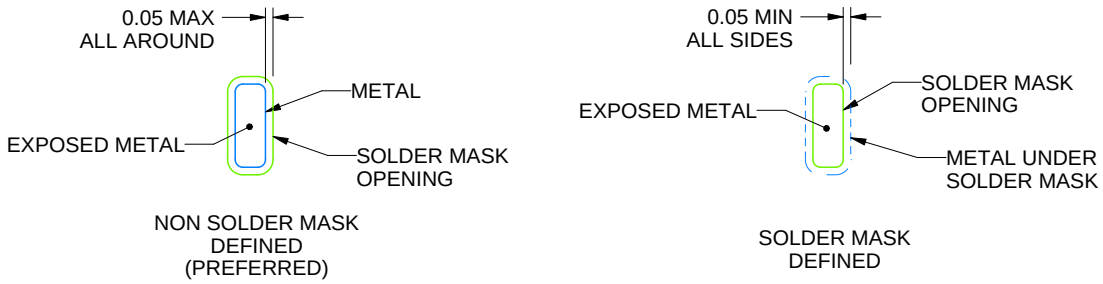


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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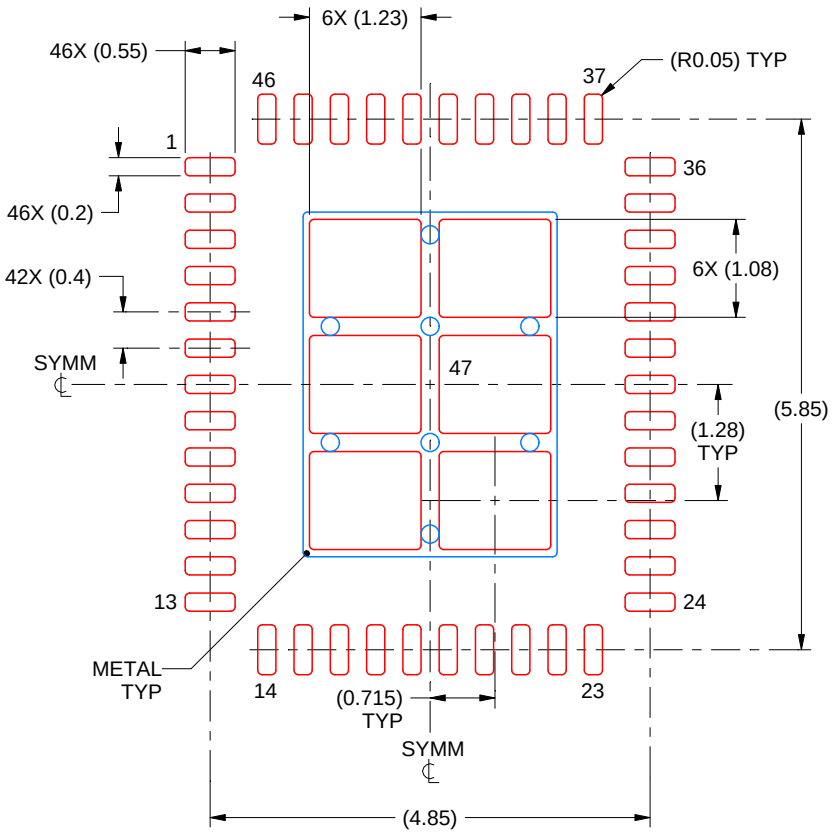
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 47:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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