

# LP3907-Q1 双路1 A 和600 mA 降压转换器和双路300 mA LDO 具有 I<sup>2</sup>C 接口用于汽车电子应用的

## 1 特性

- 符合汽车应用要求
- 具有符合 AEC Q100 的下列结果:
  - 器件温度等级 1: 环境工作温度范围为  $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$
- 输入电压范围: 2.8V 至 5.5V
- 兼容高级应用处理器和现场可编程门阵列 (FPGA)
- 2 个低压降线性稳压器 (LDO), 用于为内部处理器的运行和 I/O 供电
- 高速串行接口用于对器件功能和设置进行独立控制
- 精密的内部基准电压
- 热过载保护
- 电流过载保护
- 软件可编程稳压器
- 针对 Buck1 和 Buck2 的外部上电复位功能 (带延迟功能的电源正常指示)
- 配有欠压闭锁检测器, 用于监视输入电源电压
- 降压直流/直流转换器 (降压)
  - 可编程  $V_{\text{OUT}}$ :
    - Buck1: 1A 时为 0.8V 至 2V
    - Buck2: 600mA 时为 1V 至 3.5V
  - 效率高达 96%
  - 2.1MHz 脉冲宽度调制 (PWM) 开关频率
  - 低负载条件下从 PWM 模式自动切换到脉冲频率调制 (PFM) 模式
  - $\pm 3\%$  的输出电压精度
  - 自动软启动
- 线性稳压器 (LDO)
  - 可编程  $V_{\text{OUT}}$  1V 至 3.5V
  - 300mA 输出电流
  - 30mV (典型值) 压降

## 2 应用

- 适用于汽车和工业应用的 PMIC
- 现场可编程门阵列 (FPGA), 数字信号处理器 (DSP) 内核电源
- 应用处理器
- 外设 I/O 电源

## 3 说明

LP3907-Q1 器件是专为低功耗 FPGA、微处理器和 DSP 优化的多功能、可编程电源管理单元 (PMU)。该器件集成了两个具有动态电压调节 (DVS) 功能的高效 1A、600mA 降压直流/直流转换器、两个 300mA 线性稳压器和一个 400kHz I<sup>2</sup>C 接口, 使主机控制器可以访问该器件的内部控制寄存器。LP3907-Q1 还具有可编程的加电序列。该器件是一款经过 AECQ-100 1 级认证的汽车级产品。

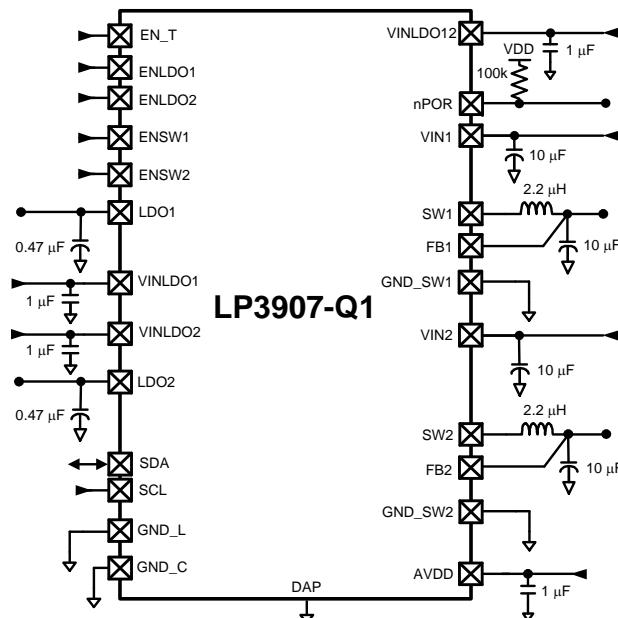
具备诸多功能, 其中包括可编程的加电序列、通信控制 (I<sup>2</sup>C)、动态电压调节、过流保护、电源正常指示、同步整流、热关断以及欠压锁定。对于需要轻负载的应用, 此款高效同步开关降压稳压器可进入 PFM 模式, 以较低的开关频率和电源电流运行, 从而在极轻负载下保持高效率。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
LP3907-Q1	WQFN (24)	4.00mm x 4.00mm
	DSBGA (25)	2.49mm x 2.49mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品目录。

### 典型应用电路



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

English Data Sheet: [SNVSA55](#)

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision B (November 2016) to Revision C</b>		<b>Page</b>
• 已删除	删除已过时的 OPN 表 3	3

<b>Changes from Revision A (May 2015) to Revision B</b>		<b>Page</b>
• 已更改	更改了改进的 SEO 的数据表标题，向“特性”中添加了所需的汽车项目符号，将动态电压“管理”更改为“调节”，向“说明”中添加了新段落	1

<b>Changes from Original (December 2014) to Revision A</b>		<b>Page</b>
• Added last sentence to "NOTE"		21

## 5 器件比较 台式机

表 1. 默认 I<sup>2</sup>C 地址

封装类型	默认 I <sup>2</sup> C 地址
24 引线 WQFN	60
25 凸点 DSBGA	61

表 2. 电源块

电源块输入	电源块运行		注释
	启用	禁用	
VINLDO12	VIN+ <sup>(1)</sup>	VIN+	始终供电
AVDD	VIN+	VIN+	始终供电
VIN1	VIN+	VIN+	
VIN2	VIN+	VIN+	
LDO1	≤ VIN+	≤ VIN+	如果启用, V <sub>IN</sub> 最小值为 1.74V
LDO2	≤ VIN+	≤ VIN+	如果启用, V <sub>IN</sub> 最小值为 1.74V

(1) VIN+ 是设备支持的最大电压。

表 3. 默认器件选项

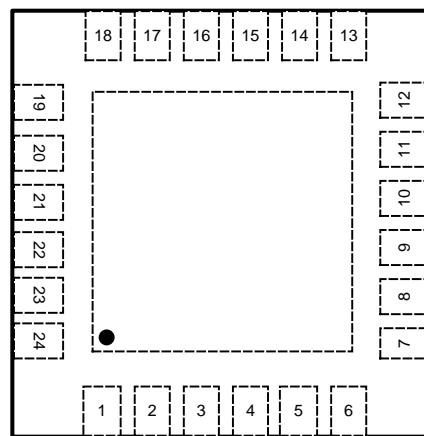
部件号 <sup>(1)(2)</sup>	BUCK1	BUCK2	LDO1	LDO2	降压模式	默认 EN_T 延迟	默认 UVLO
LP3907QSQ-JXIP/NOPB	1.2V	3.3V	1.8V	2.5V	强制 PWM	001	启用
LP3907QSQ-JXI7/NOPB	1.2V	3.3V	1.8V	2.5V	强制 PWM	001	禁用
LP3907QSQ-JJXP/NOPB	1.2V	1.8V	3.3V	2.5V	强制 PWM	010	禁用
LP3907QTL-VXSS/NOPB	1.8V	3.3V	2.8V	2.8V	强制 PWM	010	启用
LP3907QTLX-VXSS/NOPB	1.8V	3.3V	2.8V	2.8V	强制 PWM	010	启用

(1) 要获得最新的封装和订购信息, 请参见本文档末尾的封装选项附录, 或者浏览 TI 网站 [www.ti.com.cn](http://www.ti.com.cn)。

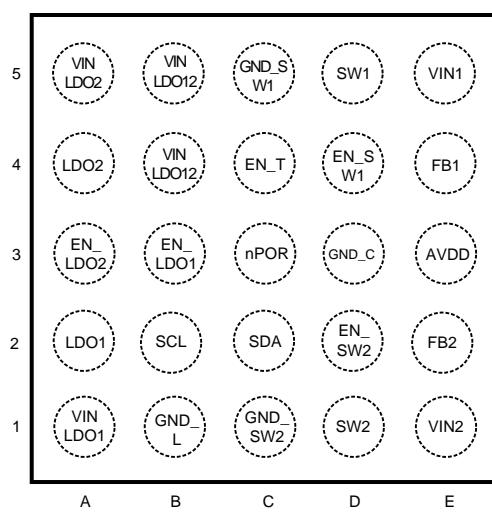
(2) 封装图样、散热数据和符号可从网站 [www.ti.com/packaging](http://www.ti.com/packaging) 中获取。

## 6 Pin Configuration and Functions

**WQFN (RTW)**  
24 Leads  
Top View



**DSBGA (YZR)**  
25 Pins  
Top View



**Pin Functions**

PIN			I/O	TYPE <sup>(1)</sup>	DESCRIPTION
WQFN NUMBER	DSBGA NUMBER	NAME			
1	B4, B5	VINLDO12	I	PWR	Analog Power for Internal Functions (VREF, BIAS, I <sup>2</sup> C, Logic)
2	C4	EN_T	I	D	Enable for preset power on sequence. (See .)
3	C3	nPOR	O	D	nPOR Power on reset pin for both Buck1 and Buck 2. Open drain logic output 100-kΩ pullup resistor. nPOR is pulled to ground when the voltages on these supplies are not good. See <i>Flexible Power-On Reset (Power Good with Delay)</i> section for more info.
4	C5	GND_SW1	G	G	Buck1 NMOS Power Ground
5	D5	SW1	O	PWR	Buck1 switcher output pin
6	E5	VIN1	I	PWR	Power in from either DC source or Battery to Buck1
7	D4	ENSW1	I	D	Enable Pin for Buck1 switcher, a logic HIGH enables Buck1
8	E4	FB1	I	A	Buck1 input feedback terminal
9	D3	GND_C	G	G	Non switching core ground pin
10	E3	AVDD	I	PWR	Analog Power for Buck converters
11	E2	FB2	I	A	Buck2 input feedback terminal
12	D2	ENSW2	I	D	Enable Pin for Buck2 switcher, a logic HIGH enables Buck2
13	E1	VIN2	I	PWR	Power in from either DC source or Battery to Buck2
14	D1	SW2	O	PWR	Buck2 switcher output pin
15	C1	GND_SW2	G	G	Buck2 NMOS Power ground
16	C2	SDA	I/O	D	I <sup>2</sup> C Data (bidirectional)
17	B2	SCL	I	D	I <sup>2</sup> C Clock
18	B1	GND_L	G	G	LDO ground
19	A1	VINLDO1	I	PWR	Power in from either DC source or battery to input terminal to LDO1
20	A2	LDO1	O	PWR	LDO1 Output
21	B3	ENLDO1	I	D	LDO1 enable pin, a logic HIGH enables the LDO1
22	A3	ENLDO2	I	D	LDO2 enable pin, a logic HIGH enables the LDO2
23	A4	LDO2	O	PWR	LDO2 Output
24	A5	VINLDO2	I	PWR	Power in from either DC source or battery to input terminal to LDO2.
DAP		DAP	GND	GND	Connection isn't necessary for electrical performance, but it is recommended for better thermal dissipation.

(1) **A:** Analog Pin    **D:** Digital Pin    **G:** Ground Pin    **PWR:** Power Pin    **I:** Input Pin    **I/O:** Input/Output Pin    **O:** Output Pin.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)</sup>

	MIN	MAX	UNIT
$V_{IN}$ , SDA, SCL	-0.3	6	V
GND to GND SLUG		$\pm 0.3$	V
Power dissipation (WQFN (RTW)) <sup>(3)</sup>		1.43	W
Power dissipation (DSBGA (YZR)) <sup>(3) (4)</sup>		0.78	W
Junction temperature, $T_{J-MAX}$		150	°C
Maximum lead temperature (soldering)		260	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions (Bucks)*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^{\circ}\text{C}$ ), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to-ambient thermal resistance of the part/package in the application ( $R_{\theta JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$ .
- (4) For  $T_A = 85^{\circ}\text{C}$ ,  $T_{J-MAX} = 125^{\circ}\text{C}$ .

### 7.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	$\pm 2000$
	Charged-device model (CDM), per AEC Q100-011	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions (Bucks)

over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)(3)(4)</sup>

	MIN	MAX	UNIT
$V_{IN}$	2.8	5.5	V
$V_{EN}$	0	$(V_{IN} + 0.3 \text{ V})$	V
Junction temperature, $T_J$	-40	125	°C
Ambient temperature, $T_A$ <sup>(5)</sup>	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) Minimum (Minimum) and Maximum (Maximum) limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
- (4) Buck  $V_{IN} \geq V_{OUT} + 1 \text{ V}$ .
- (5) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

## 7.4 Thermal Information

See<sup>(1)(2)(3)</sup>

THERMAL METRIC <sup>(4)</sup>		LP3907-Q1		UNIT
		RTW	YZR	
		24 PINS	25 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	58.7	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	31.2	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	8.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.2	0.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	11.2	8.0	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	1.4	N/A	°C/W

- (1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
- (2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J = 160^\circ\text{C}$  (typical) and disengages at  $T_J = 140^\circ\text{C}$  (typical).
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-\text{MAX}}$ ) is dependent on the maximum operating junction temperature ( $T_{J-\text{MAX-OP}} = 125^\circ\text{C}$ ), the maximum power dissipation of the device in the application ( $P_{D-\text{MAX}}$ ), and the junction-to-ambient thermal resistance of the part/package in the application ( $R_{\theta JA}$ ), as given by the following equation:  $T_{A-\text{MAX}} = T_{J-\text{MAX-OP}} - (R_{\theta JA} \times P_{D-\text{MAX}})$ .
- (4) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 General Electrical Characteristics

Unless otherwise noted,  $V_{IN} = 3.6\text{ V}$  and  $T_J = 25^\circ\text{C}$ .<sup>(1)(2)(3)(4)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_Q$	$V_{IN} = 3.6\text{ V}$		3		$\mu\text{A}$
$V_{POR}$	$V_{DD}$ falling edge <sup>(4)</sup>		1.9		V
$T_{SD}$	Thermal shutdown threshold		160		$^\circ\text{C}$
$T_{SDH}$	Thermal shutdown hysteresis		20		$^\circ\text{C}$
UVLO	Undervoltage lockout	Rising	2.9		V
		Falling	2.7		

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) This specification is ensured by design.
- (4) VPOR is voltage at which the EPROM resets. This is different from the UVLO on VINLDO12, which is the voltage at which the regulators shut off, and is also different from the nPOR function, which signals if the regulators are in a specified range.

## 7.6 Low Dropout Regulators, LDO1 And LDO2

Unless otherwise noted,  $V_{IN} = 3.6$  V,  $C_{IN} = 1$   $\mu$ F,  $C_{OUT} = 0.47$   $\mu$ F, and  $T_J = 25^\circ\text{C}$ .<sup>(1)(2)(3)(4)(5)(6)(7)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Operational voltage range	VINLDO1 and VINLDO2 PMOS pins <sup>(8)</sup>	1.74 <sup>(9)</sup>	5.5 <sup>(9)</sup>		V
$V_{OUT}$ Accuracy	Output voltage accuracy (default $V_{OUT}$ )	Load current = 1 mA	-3% <sup>(9)</sup>	3% <sup>(9)</sup>		
$\Delta V_{OUT}$	Line regulation	$V_{IN} = (V_{OUT} + 0.3$ V) to 5 V, <sup>(7)</sup> , load current = 1 mA		0.15 <sup>(9)</sup>		%/V
	Load regulation	$V_{IN} = 3.6$ V, Load current = 1 mA to $I_{MAX}$		0.011 <sup>(9)</sup>		%/mA
$I_{SC}$	Short circuit current limit	LDO1-2, $V_{OUT} = 0$ V		500		mA
$V_{IN} - V_{OUT}$	Dropout voltage	Load current = 50 mA <sup>(5)</sup>	30	200 <sup>(9)</sup>		mV
PSRR	Power supply ripple rejection	$f = 10$ kHz, load current = $I_{MAX}$		45		dB
$e_N$	Supply output noise	10 Hz < F < 100 kHz		80		$\mu$ Vrms
$I_Q$ <sup>(6)(10)</sup>	Quiescent current on	$I_{OUT} = 0$ mA		40		$\mu$ A
	Quiescent current on	$I_{OUT} = I_{MAX}$		60		$\mu$ A
	Quiescent current off	EN is de-asserted <sup>(11)</sup>		0.03		$\mu$ A
$T_{ON}$	Turnon time	Start-up from shutdown		300		$\mu$ s
$C_{OUT}$	Output capacitor	Capacitance for stability $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	0.33 <sup>(9)</sup>	0.47		$\mu$ F
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	0.68	1		$\mu$ F
		ESR	5 <sup>(9)</sup>	500 <sup>(9)</sup>		$\text{m}\Omega$

- (1) All voltages are with respect to the potential at the GND pin.
- (2) Minimum (MIN) and maximum (MAX) limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
- (3)  $C_{IN}$ ,  $C_{OUT}$ : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
- (4) The device maintains a stable, regulated output voltage without a load.
- (5) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
- (6) Quiescent current is defined here as the difference in current between the input voltage source and the load at  $V_{OUT}$ .
- (7)  $V_{IN}$  minimum for line regulation values is 1.8 V.
- (8) Pins 24, 19 can operate from  $V_{IN}$  min of 1.74 V to a  $V_{IN}$  max of 5.5 V. This rating is only for the series pass PMOS power FET. It allows the system design to use a lower voltage rating if the input voltage comes from a buck output.
- (9) Limits apply over the entire junction temperature range for operation,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .
- (10) The  $I_Q$  can be defined as the standing current of the LP3907-Q1 when the  $\text{I}^2\text{C}$  bus is active and all other power blocks have been disabled with the  $\text{I}^2\text{C}$  bus, or it can be defined as the  $\text{I}^2\text{C}$  bus active, and the other power blocks are active under no load condition. These two values can be used by the system designer when the LP3907-Q1 is powered using a battery.
- (11) The  $I_Q$  exhibits a higher current draw when the EN pin is de-asserted because the  $\text{I}^2\text{C}$  buffer pins draw an additional 2  $\mu$ A.

## 7.7 Buck Converters SW1, SW2

Unless otherwise noted,  $V_{IN} = 3.6$  V,  $C_{IN} = 10$   $\mu$ F,  $C_{OUT} = 10$   $\mu$ F,  $L_{OUT} = 2.2\text{-}\mu\text{H}$  ceramic, and  $T_J = 25^\circ\text{C}$ .<sup>(1)(2)(3)(4)(5)(6)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB}$	Feedback voltage		-3% <sup>(7)</sup>	3% <sup>(7)</sup>		
$V_{OUT}$	Line regulation	$2.8 \text{ V} < V_{IN} < 5.5 \text{ V}$ $I_{OUT} = 10 \text{ mA}$		0.089		%/V
	Load regulation	$100 \text{ mA} < I_{OUT} < I_{MAX}$		0.0013		%/mA
Eff	Efficiency	Load current = 250 mA		96%		
$I_{SHDN}$	Shutdown supply current	EN is de-asserted		0.01		$\mu$ A
$f_{osc}$	Internal oscillator frequency		1.7 <sup>(7)</sup>	2.1		MHz

- (1) All voltages are with respect to the potential at the GND pin.
- (2) Minimum (Min) and Maximum (Max) limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
- (3)  $C_{IN}$ ,  $C_{OUT}$ : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
- (4) The device maintains a stable, regulated output voltage without a load.
- (5) Quiescent current is defined here as the difference in current between the input voltage source and the load at  $V_{OUT}$ .
- (6) Buck  $V_{IN} \geq V_{OUT} + 1$  V.
- (7) Limits apply over the entire junction temperature range for operation,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

## Buck Converters SW1, SW2 (continued)

Unless otherwise noted,  $V_{IN} = 3.6 \text{ V}$ ,  $C_{IN} = 10 \mu\text{F}$ ,  $C_{OUT} = 10 \mu\text{F}$ ,  $L_{OUT} = 2.2\text{-}\mu\text{H}$  ceramic, and  $T_J = 25^\circ\text{C}$ .<sup>(1)(2)(3)(4)(5)(6)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PEAK}$	Buck1 peak switching current limit		1.5		1	A
	Buck2 peak switching current limit					
$I_Q^{(8)}$	Quiescent current “on”	No load PFM mode			33	$\mu\text{A}$
$R_{DS(ON)}(P)$	Pin-pin resistance PFET			200	$\text{m}\Omega$	
$R_{DS(ON)}(N)$	Pin-pin resistance NFET			180	$\text{m}\Omega$	
$T_{ON}$	Turnon time	Start up from shutdown			500	$\mu\text{s}$
$C_{IN}$	Input capacitor	Capacitance for stability			10	$\mu\text{F}$
$C_{OUT}$	Output capacitor	Capacitance for stability			10	$\mu\text{F}$

(8) The  $I_Q$  can be defined as the standing current of the LP3907-Q1 when the I<sup>2</sup>C bus is active and all other power blocks have been disabled with the I<sup>2</sup>C bus, or it can be defined as the I<sup>2</sup>C bus active, and the other power blocks are active under no load condition. These two values can be used by the system designer when the device is powered using a battery.

## 7.8 I/O Electrical Characteristics

Unless otherwise noted: Limits apply over the entire junction temperature range for operation,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL}$	Input low level			0.4	V
$V_{IH}$					

(1) This specification is ensured by design.

## 7.9 Power-On Reset (POR) Threshold/Function

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
nPOR	$nPOR = \text{Power on reset for Buck1 and Buck2}$	Default		50	ms
nPOR threshold	Percentage of target voltage Buck1 or Buck2	$V_{BUCK1}$ AND $V_{BUCK2}$ rising			
		$V_{BUCK1}$ OR $V_{BUCK2}$ falling			
VOL	Output level low	Load = $I_{oL} = 500 \text{ mA}$	0.23	0.5	V

## 7.10 I<sup>2</sup>C Interface Timing Requirements

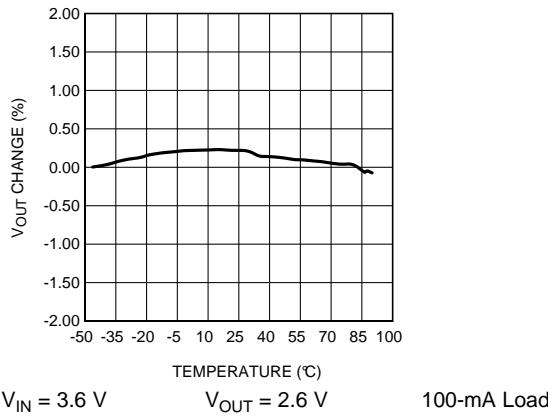
Unless otherwise noted,  $V_{IN} = 3.6 \text{ V}$  and  $T_J = 25^\circ\text{C}$ .<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
$f_{CLK}$	Clock frequency			400	kHz
$t_{BF}$	Bus-free time between start and stop	See <sup>(1)</sup>	1.3	$\mu\text{s}$	
$t_{HOLD}$	Hold time repeated start condition		0.6	$\mu\text{s}$	
$t_{CLKLP}$	CLK low period		1.3	$\mu\text{s}$	
$t_{CLKHP}$	CLK high period		0.6	$\mu\text{s}$	
$t_{SU}$	Set-up time repeated start condition		0.6	$\mu\text{s}$	
$t_{DATAHLD}$	Data hold time		0	$\mu\text{s}$	
$t_{DATASU}$	Data set-up time		100	ns	
$T_{SU}$	Set-up time for start condition		0.6	$\mu\text{s}$	
$T_{TRANS}$	Maximum pulse width of spikes that must be suppressed by the input filter of both DATA & CLK signals			50	ns

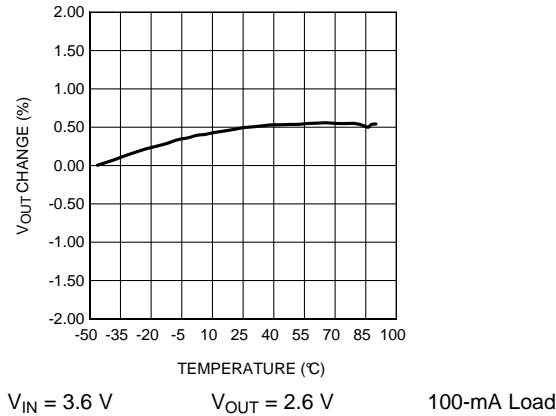
(1) This specification is ensured by design.

## 7.11 Typical Characteristics — LDO

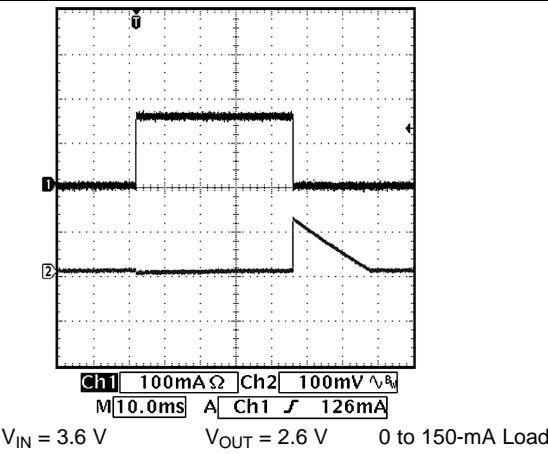
$T_A = 25^\circ\text{C}$  unless otherwise noted.



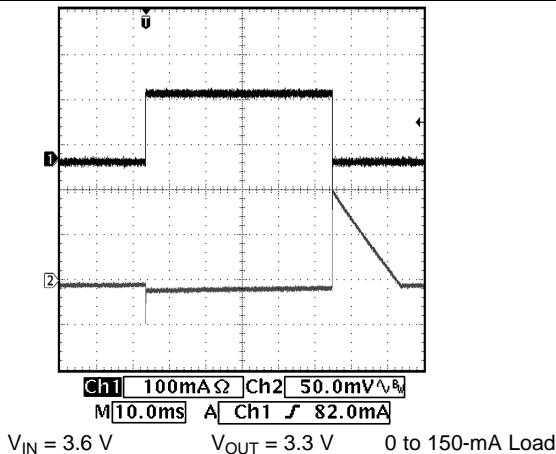
**Figure 1. Output Voltage Change vs Temperature (LDO1)**



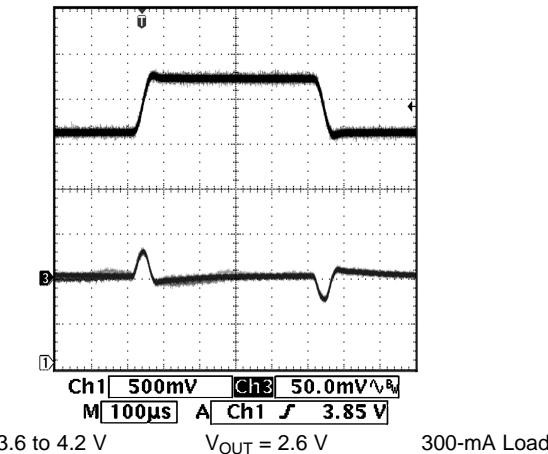
**Figure 2. Output Voltage Change vs Temperature (LDO2)**



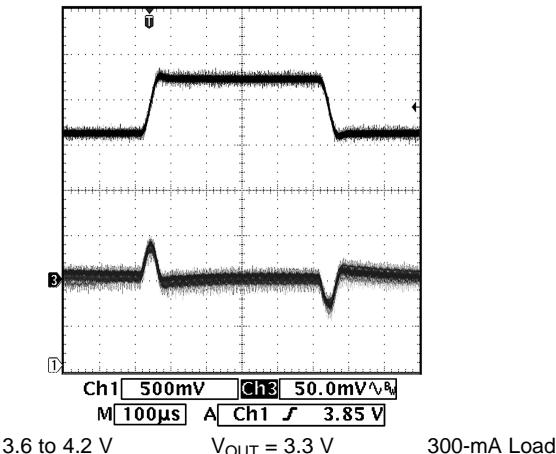
**Figure 3. Load Transient (LDO1)**



**Figure 4. Load Transient (LDO2)**



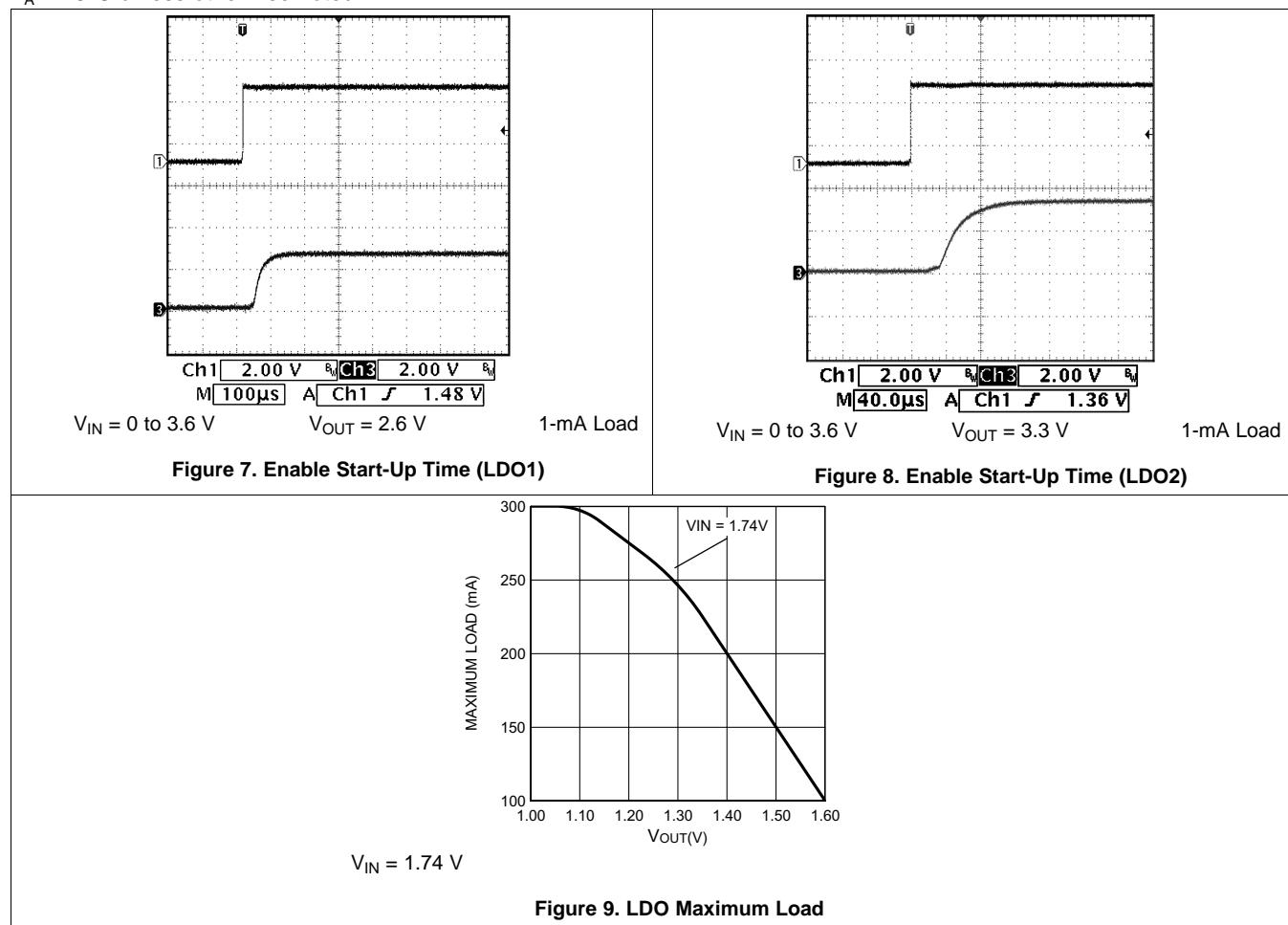
**Figure 5. Line Transient (LDO1)**



**Figure 6. Line Transient (LDO2)**

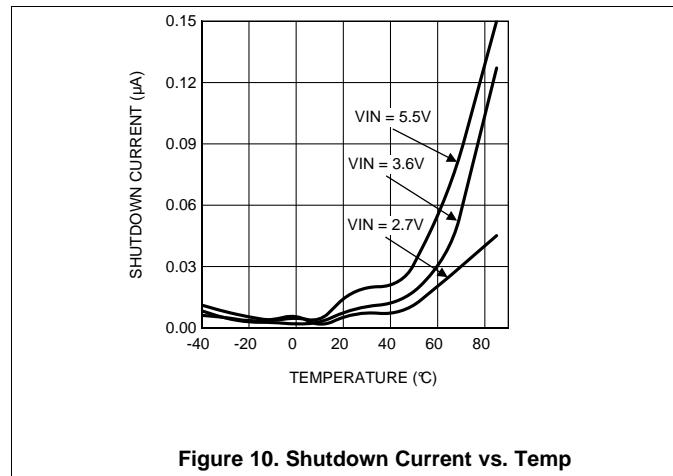
## Typical Characteristics — LDO (continued)

$T_A = 25^\circ\text{C}$  unless otherwise noted.

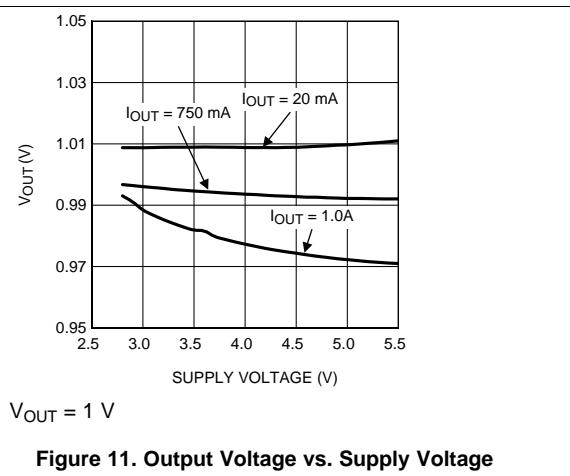


## 7.12 Typical Characteristics — Bucks

$V_{IN} = 2.8 \text{ V to } 5.5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

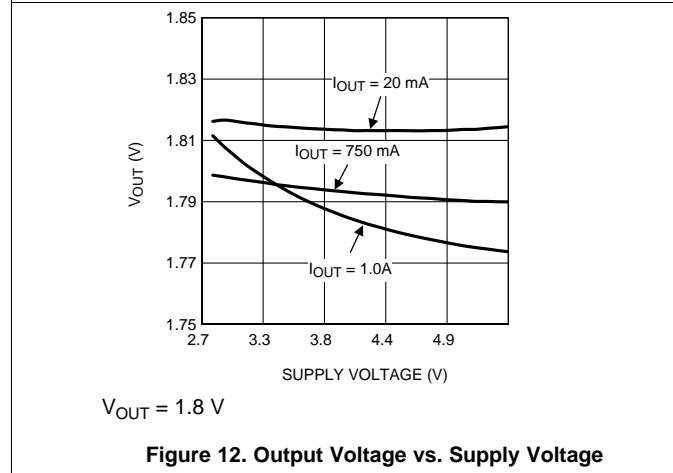


**Figure 10. Shutdown Current vs. Temp**



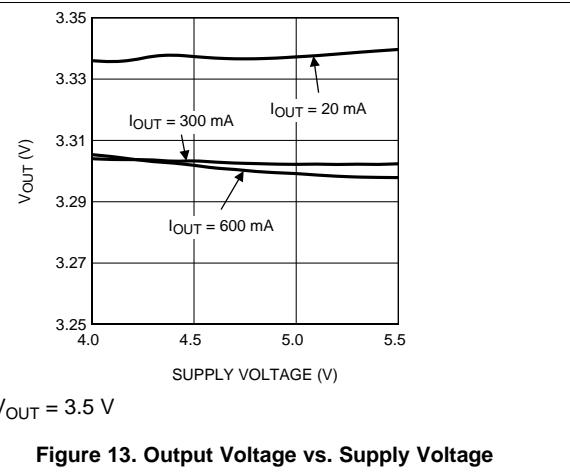
$V_{OUT} = 1 \text{ V}$

**Figure 11. Output Voltage vs. Supply Voltage**



$V_{OUT} = 1.8 \text{ V}$

**Figure 12. Output Voltage vs. Supply Voltage**

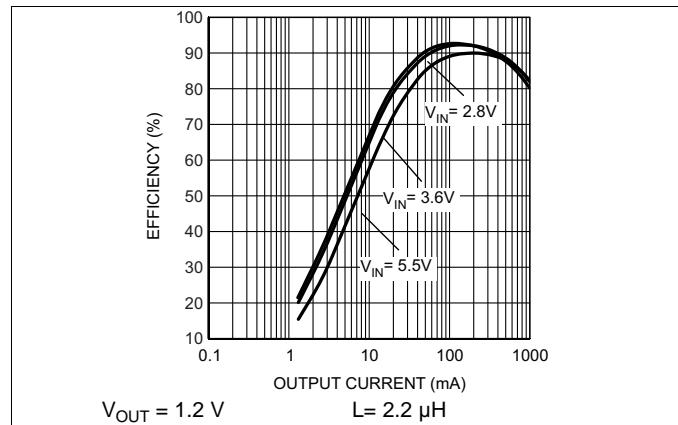


$V_{OUT} = 3.5 \text{ V}$

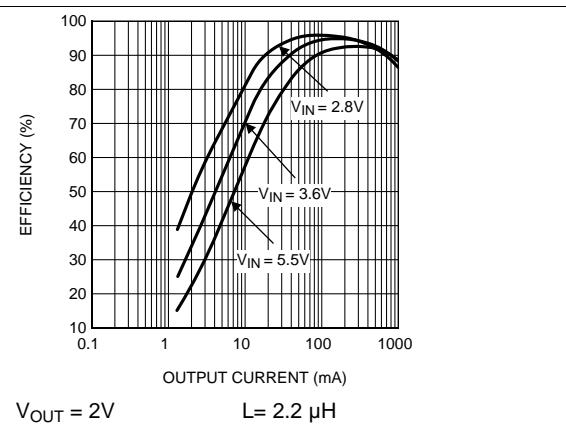
**Figure 13. Output Voltage vs. Supply Voltage**

## 7.13 Typical Characteristics — Buck1

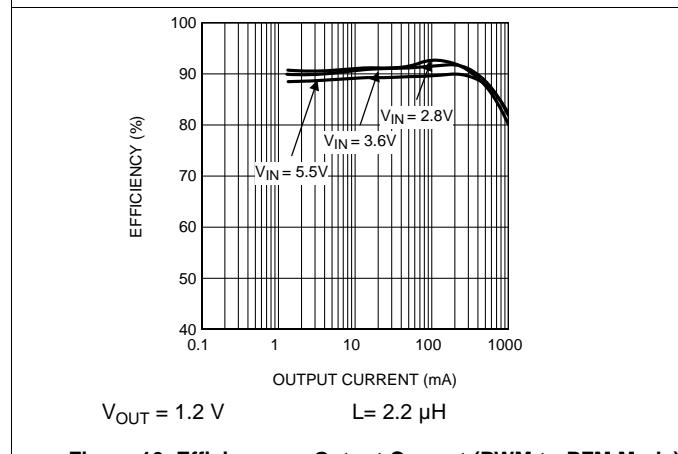
$V_{IN}$  = 2.8 V to 5.5 V,  $T_A$  = 25°C,  $V_{OUT}$  = 1.2 V, 2 V



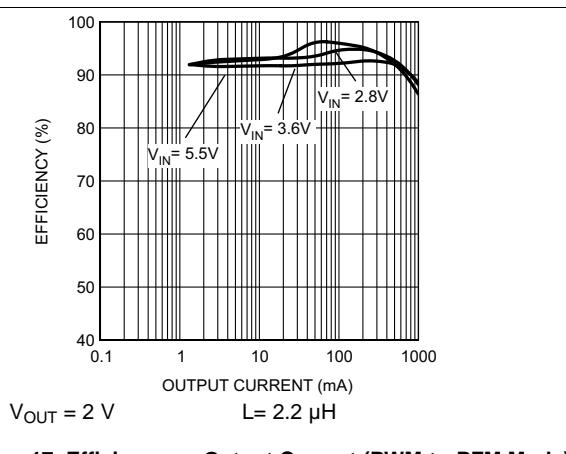
**Figure 14. Efficiency vs Output Current (Forced PWM Mode)**



**Figure 15. Efficiency vs Output Current (Forced PWM Mode)**



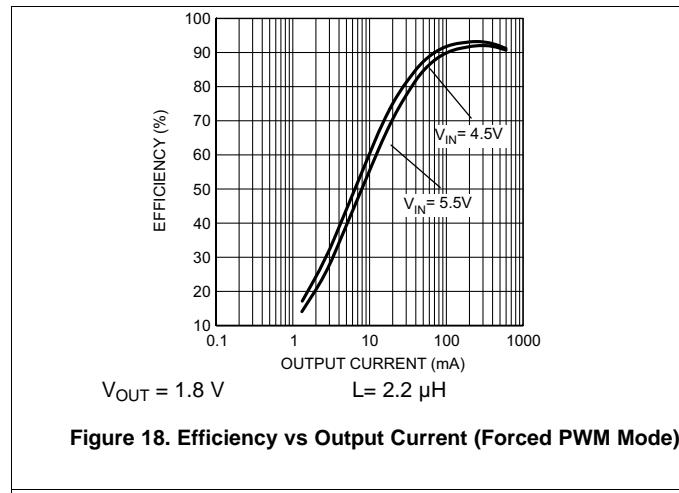
**Figure 16. Efficiency vs Output Current (PWM-to-PFM Mode)**



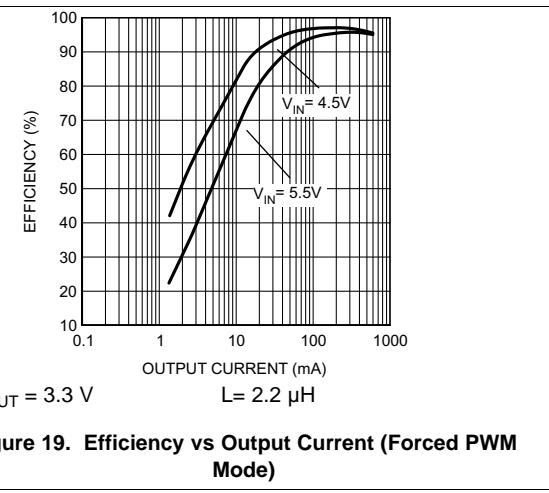
**Figure 17. Efficiency vs Output Current (PWM-to-PFM Mode)**

## 7.14 Typical Characteristics — Buck2

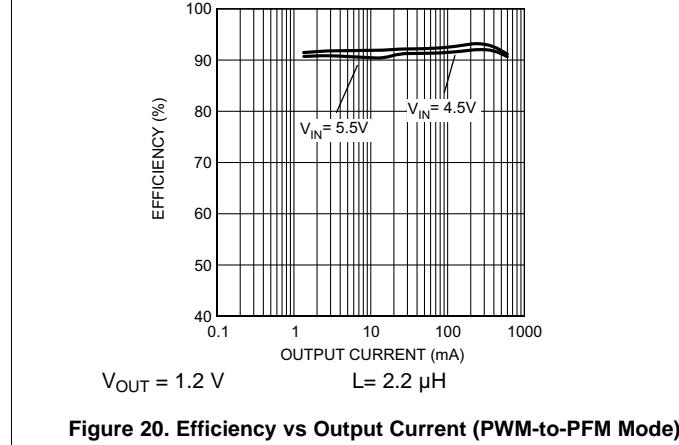
$V_{IN} = 4.5$  V to 5.5 V,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = 1.8$  V, 3.3 V



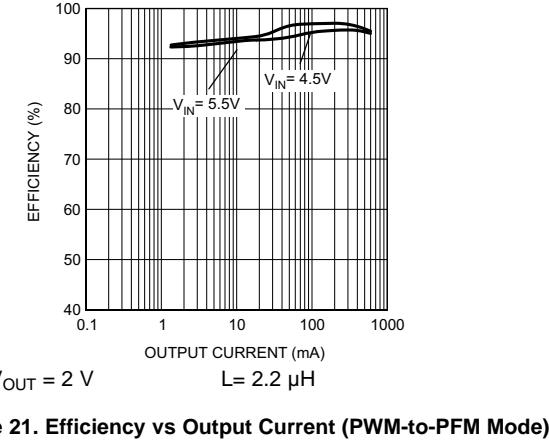
**Figure 18. Efficiency vs Output Current (Forced PWM Mode)**



**Figure 19. Efficiency vs Output Current (Forced PWM Mode)**



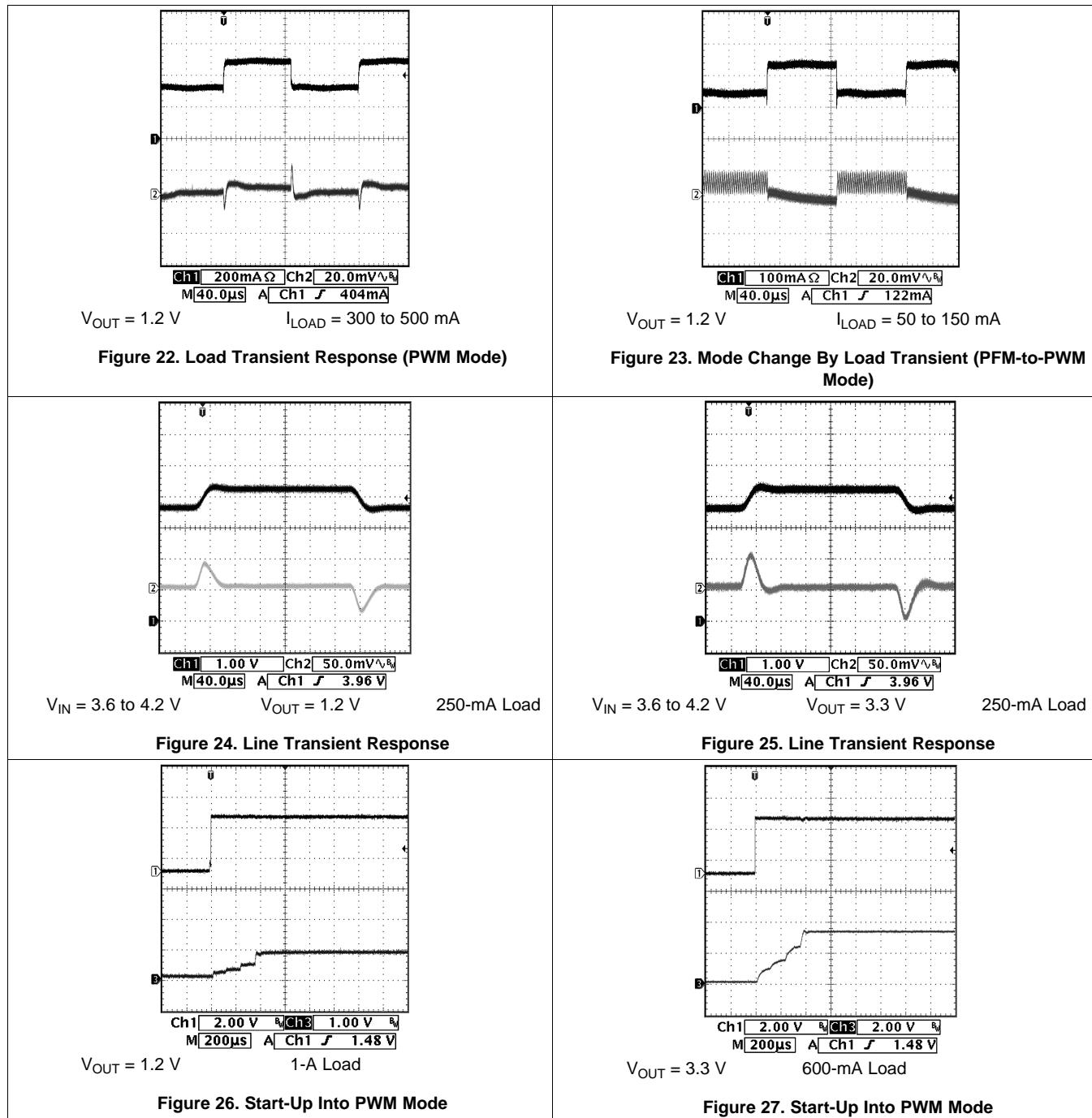
**Figure 20. Efficiency vs Output Current (PWM-to-PFM Mode)**



**Figure 21. Efficiency vs Output Current (PWM-to-PFM Mode)**

## 7.15 Typical Characteristics — Bucks

$V_{IN} = 3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = 1.2\text{ V}$  unless otherwise noted.



**Typical Characteristics — Bucks (continued)**

$V_{IN} = 3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = 1.2\text{ V}$  unless otherwise noted.

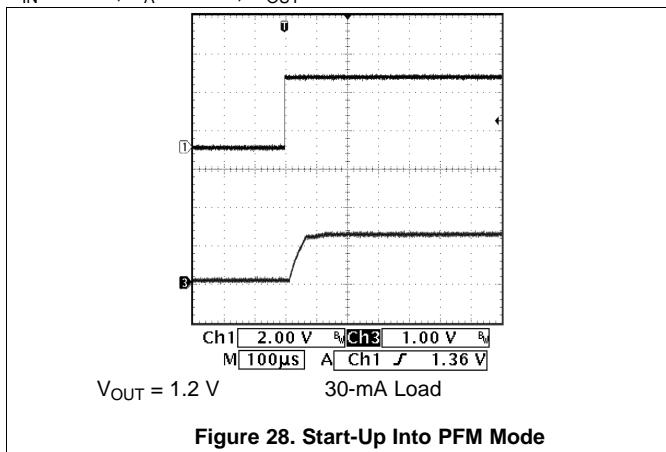


Figure 28. Start-Up Into PFM Mode

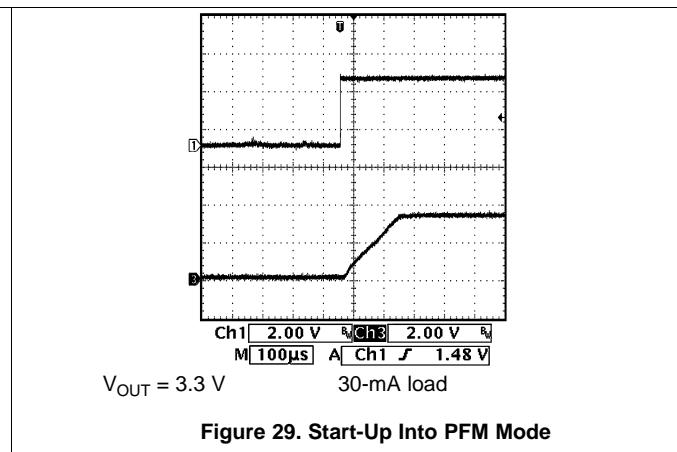


Figure 29. Start-Up Into PFM Mode

## 8 Detailed Description

### 8.1 Overview

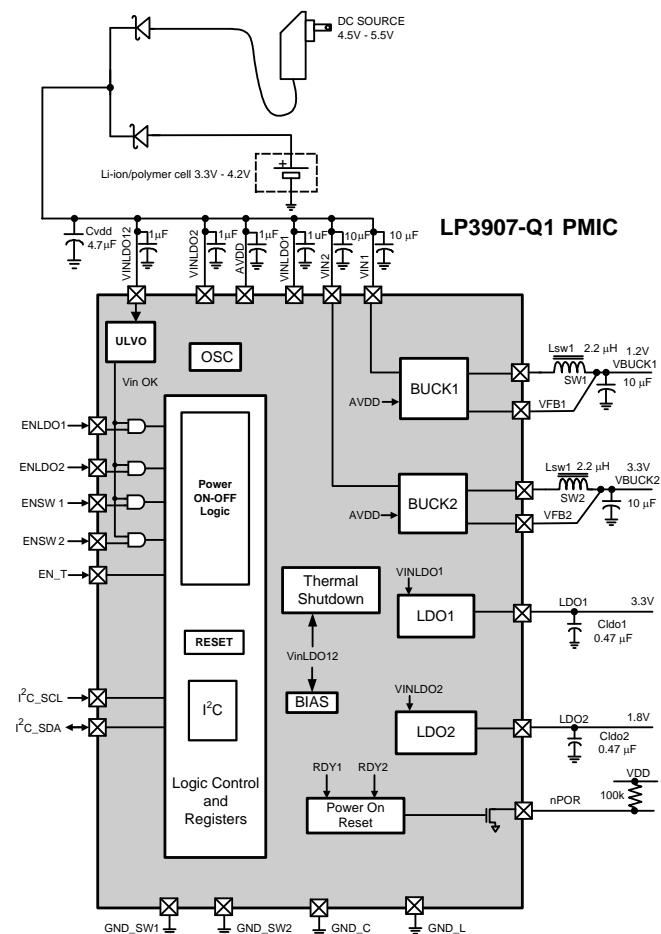
The LP3907 supplies the various power needs of the application by means of two linear low drop regulators (LDO1 and LDO2) and two buck converters (SW1 and SW2). [Table 4](#) lists the output characteristics of the various regulators.

**Table 4. Supply Specification**

SUPPLY <sup>(1)</sup>	LOAD	OUTPUT		
		V <sub>OUT</sub> RANGE (V)	RESOLUTION (mV)	I <sub>MAX</sub> MAXIMUM OUTPUT CURRENT (mA)
LDO1	analog	1 to 3.5	100	300
LDO2	analog	1 to 3.5	100	300
SW1	digital	0.8 to 2	50	1000
SW2	digital	1 to 3.5	100	600

(1) For default values of the regulators, consult [表 3](#).

### 8.2 Functional Block Diagram

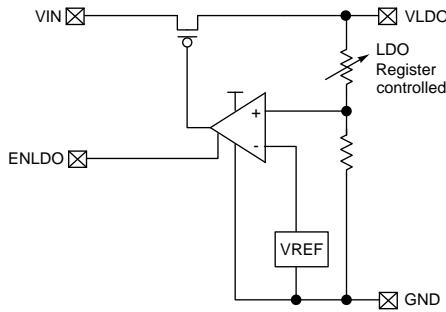


## 8.3 Feature Description

### 8.3.1 DC-DC Converters

#### 8.3.1.1 Linear Low Dropout Regulators (LDOs)

LDO1 and LDO2 are identical linear regulators targeting analog loads characterized by low noise requirements. LDO1 and LDO2 are enabled through the ENLDO pin or through the corresponding LDO1 or LDO2 control register. The output voltages of both LDOs are register programmable. The default output voltages are factory programmed during final test, which can be tailored to the specific needs of the system designer.



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**Figure 30. LDO Block Diagram**

#### 8.3.1.2 No-Load Stability

The LDOs remain stable and in regulation with no external load. This is an important consideration in some circuits, for example, CMOS RAM keep-alive applications.

#### 8.3.1.3 LDO and LDO2 Control Registers

LDO1 and LDO2 can be configured by means of the LDO1 and LDO2 control registers. The output voltage is programmable in steps of 100 mV from 1 V to 3.5 V by programming bits D4-D0 in the LDO Control registers. Both LDO1 and LDO2 are enabled by applying a logic 1 to the ENLDO1 and ENLDO2 pin. Enable/disable control is also provided through enable bit of the LDO1 and LDO2 control registers. The value of the enable LDO bit in the register is logic 1 by default. The output voltage can be altered while the LDO is enabled.

## 8.3.2 SW1, SW2: Synchronous Step-Down Magnetic DC-DC Converters

### 8.3.2.1 Functional Description

The LP3907-Q1 incorporates two high-efficiency synchronous switching buck regulators, SW1 and SW2, that deliver a constant voltage from a single Li-Ion battery to the portable system processors. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 1000 mA and 600 mA, respectively, depending on the input voltage and output voltage (voltage headroom), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required: PWM, PFM, and shutdown. PWM mode handles current loads of approximately 70 mA or higher, delivering voltage precision of  $\pm 3\%$  with 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption ( $I_Q = 15 \mu A$  typical) and a longer battery life. The standby operating mode turns off the device, offering the lowest current consumption. PWM or PFM mode is selected automatically or PWM mode can be forced through the setting of the buck control register.

Both SW1 and SW2 can operate up to a 100% duty cycle (PMOS switch always on) for low drop out control of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage.

Additional features include soft-start, undervoltage lockout, current overload protection, and thermal overload protection.

## Feature Description (continued)

### 8.3.2.2 Circuit Operation Description

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground (BCKGND pin) and a feedback path. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN} - V_{OUT}}{L} \quad (1)$$

by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

### 8.3.2.3 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward voltage inversely proportional to the input voltage is introduced.

### 8.3.2.4 Internal Synchronous Rectification

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

### 8.3.2.5 Current Limiting

A current limit feature allows the converter to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1.5 A for Buck1 and at 1 A for Buck2 (typical). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

### 8.3.2.6 PFM Operation

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

- The inductor current becomes discontinuous, or
- The peak PMOS switch current drops below the  $I_{MODE}$  level

$$\left( \text{Typically } I_{MODE} < 66 \text{ mA} + \frac{V_{IN}}{160\Omega} \right) \quad (3)$$

## Feature Description (continued)

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage with the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the *low* PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the ‘high’ PFM threshold or the peak current exceeds the  $I_{PFM}$  level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 66 \text{ mA} + \frac{V_{IN}}{80\Omega} \quad (4)$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the *high* PFM comparator threshold (see [Figure 31](#)), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the *high* PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this *sleep* mode is less than 30  $\mu\text{A}$ , which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the *low* PFM threshold, the cycle repeats to restore the output voltage to approximately 1.6% above the nominal PWM output voltage.

If the load current increases during PFM mode (see [Figure 31](#)) causing the output voltage to fall below the ‘low2’ PFM threshold, the part automatically transitions into fixed-frequency PWM mode.

### 8.3.2.7 SW1, SW2 Operation

SW1 and SW2 have selectable output voltages ranging from 0.8 V to 3.5 V (typical). Both SW1 and SW2 in the LP3907-Q1 are  $\text{I}^2\text{C}$  register controlled and are enabled by default through the internal state machine of the device following a power-on event that moves the operating mode to the Active state. (See [Flexible Power Sequencing of Multiple Power Supplies](#).) The SW1 and SW2 output voltages revert to default values when the power-on sequence has been completed. The default output voltage for each buck converter is factory programmable. (See [Application and Implementation](#).)

### 8.3.2.8 SW1, SW2 Control Registers

SW1, SW2 can be enabled/disabled through the corresponding control register.

The Modulation mode PWM/PFM is by default automatic and depends on the load as described above in the functional description. The modulation mode can be overridden by setting  $\text{I}^2\text{C}$  bit to a logic 1 in the corresponding buck control register, forcing the buck to operate in PWM mode regardless of the load condition.

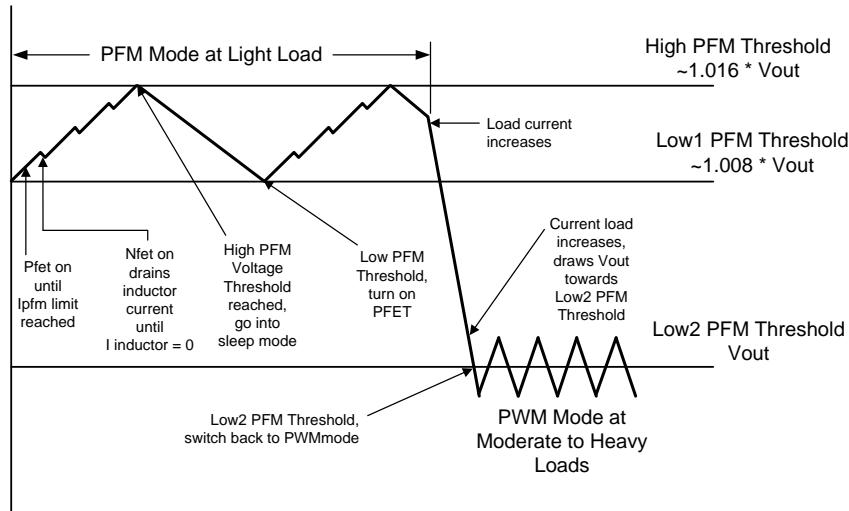


Figure 31. Operation in PFM Mode and Transfer to PWM Mode

## Feature Description (continued)

### 8.3.2.9 Soft Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The two LP3907-Q1 buck converters have a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after  $V_{IN}$  reaches 2.8V. Soft start is implemented by increasing switch current limit in steps of 180 mA, 300 mA, and 720 mA for Buck1; 161 mA, 300 mA, and 536 mA for Buck2 (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up.

### 8.3.2.10 Low Dropout Operation

The LP3907-Q1 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is:

$$V_{IN, MIN} = I_{LOAD} \times (R_{DSON, PFET} + R_{INDUCTOR}) + V_{OUT}$$

where

- $I_{LOAD}$  = Load current
- $R_{DSON, PFET}$  = Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$  = Inductor resistance

(5)

### 8.3.2.11 Flexible Power Sequencing of Multiple Power Supplies

The LP3907-Q1 provides several options for power on sequencing. The two bucks can be individually controlled with ENSW1 and ENSW2. The two LDOs can also be individually controlled with ENLDO1 and ENLDO2.

If the user desires a set power on sequence, the chip is programmable through I<sup>2</sup>C and raise EN\_T from LOW to HIGH to activate the power on sequencing.

### 8.3.2.12 Power-Up Sequencing Using the EN\_T Function

EN\_T assertion causes the LP3907-Q1 to emerge from Standby mode to Full Operation mode at a preset timing sequence. By default, the enables for the LDOs and Bucks (ENLDO1, ENLDO2, EN\_T, ENSW1, ENSW2) are 500 KΩ internally pulled down, which causes the part to stay OFF until enabled. If the user wishes to use the preset timing sequence to power on the regulators, transition the EN\_T pin from Low to High. Otherwise, simply tie the enables of each specific regulator HIGH to turn on automatically.

EN\_T is edge triggered with rising edge signaling the chip to power on. The EN\_T input is deglitched, and the default is set at 1 ms. As shown in [Figure 32](#) and [Figure 33](#), a rising EN\_T edge starts a power-on sequence, while a falling EN\_T edge starts a shutdown sequence. If EN\_T is high, toggling the external enables of the regulators has no effect on the chip.

The regulators can also be programmed through I<sup>2</sup>C to turn on and off. By default, I<sup>2</sup>C enables for the regulators turned ON.

The regulators are on following the pattern below:

Regulators on = (I<sup>2</sup>C enable) AND (External pin enable OR EN\_T high).

#### NOTE

The EN\_T power-up sequencing may also be employed immediately after  $V_{IN}$  is applied to the device. However,  $V_{IN}$  must be stable for approximately 8 ms minimum before EN\_T be asserted high to ensure internal bias, reference, and the Flexible POR timing are stabilized. This initial EN\_T delay is necessary only upon first time device power on for power sequencing function to operate properly. If the device is powered, the EN\_T logic must be stable for 12 ms minimum before switching state.

## Feature Description (continued)

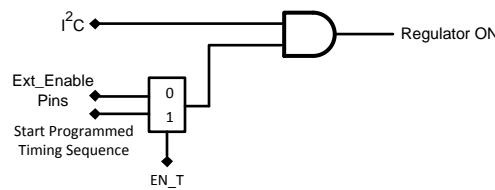


Figure 32. Power Rail Enable Logic

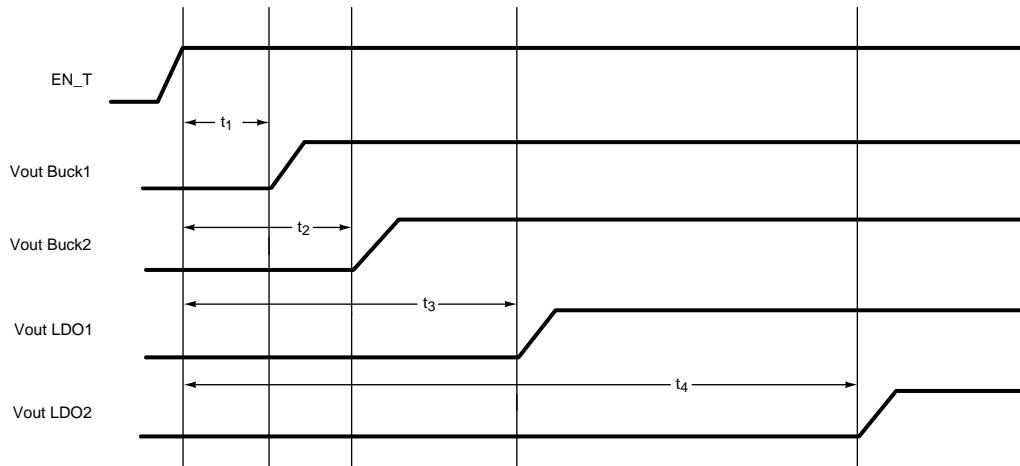


Figure 33. LP3907-Q1 Default Power-Up Sequence

Table 5. Power-On Timing Specification

	DESCRIPTION	MIN	NOM	TYP	UNIT
$t_1$	Programmable delay from EN_T assertion to $V_{CC\_Buck1}$ On			1.5	ms
$t_2$	Programmable delay from EN_T assertion to $V_{CC\_Buck2}$ On			2	ms
$t_3$	Programmable delay from EN_T assertion to $V_{CC\_LDO1}$ On			3	ms
$t_4$	Programmable delay from EN_T assertion to $V_{CC\_LDO2}$ On			6	ms

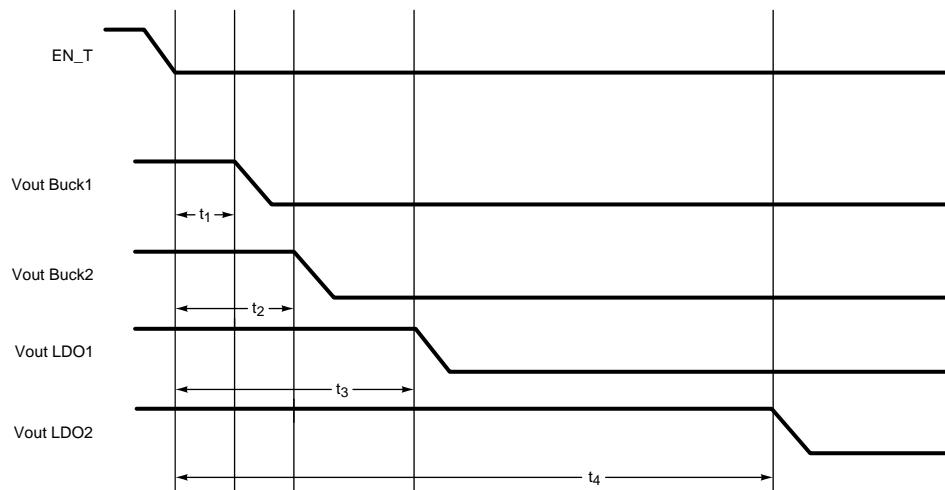


Figure 34. LP3907-Q1 Default Power-Off Sequence

**Table 6. Power-Off Timing Specification**

DESCRIPTION		MIN	NOM	MAX	UNIT
$t_1$	Programmable delay from EN_T deassertion to $V_{CC\_Buck1}$ Off		1.5		ms
$t_2$	Programmable delay from EN_T deassertion to $V_{CC\_Buck2}$ Off		2		ms
$t_3$	Programmable delay from EN_T deassertion to $V_{CC\_LDO1}$ Off		3		ms
$t_4$	Programmable delay from EN_T deassertion to $V_{CC\_LDO2}$ Off		6		ms

### 8.3.3 Flexible Power-On Reset (Power Good with Delay)

The LP3907-Q1 is equipped with an internal power-on-reset (POR) circuit which monitors the output voltage levels on Bucks 1 and 2. The nPOR is an open drain logic output which is logic LOW when either of the buck outputs are below 91% of the rising value, or when one or both outputs fall below 82% of the desired value. The time delay between output voltage level and nPOR is enabled is (50  $\mu$ s, 50 ms, 100 ms, 200 ms) 50 ms by default. The system designer can choose the external pullup resistor (that is, 100 k $\Omega$ ) for the nPOR pin.

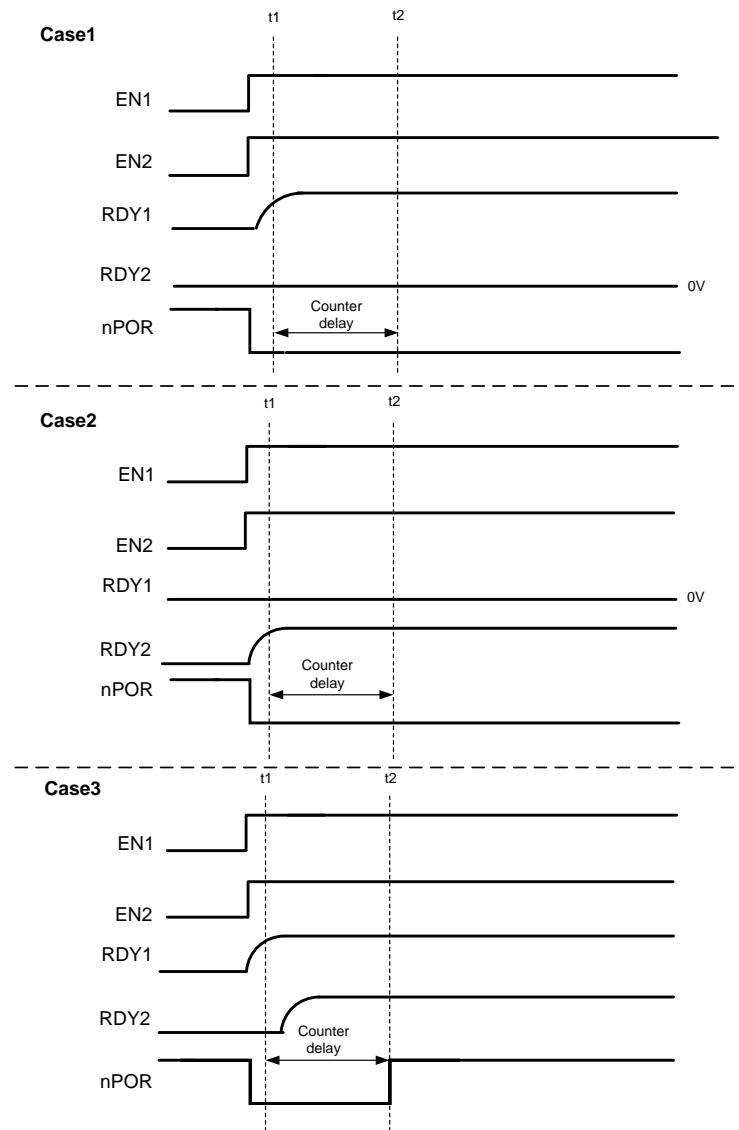
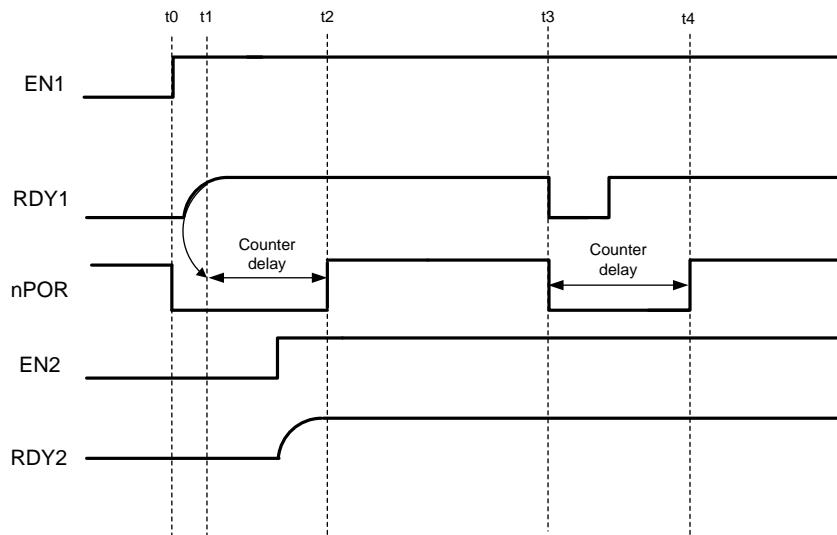

**Figure 35. nPOR with Counter Delay**

Figure 35 shows the simplest application of the POR, where both switcher enables are tied together. In Case 1, EN1 causes nPOR to transition LOW and triggers the nPOR delay counter. If the power supply for Buck2 does not come on within that period, nPOR stays LOW, indicating a power fail mode. Case 2 indicates the vice versa scenario if Buck1 supply did not come on. In both cases the nPOR remains LOW.

Case 3 shows a typical application of the POR, where both switcher enables are tied together. Even if RDY1 ramps up slightly faster than RDY2 (or vice versa), then nPOR signal triggers a programmable delay before going HIGH, as explained below.



**Figure 36. Faults Occurring in Counter Delay After Start-Up**

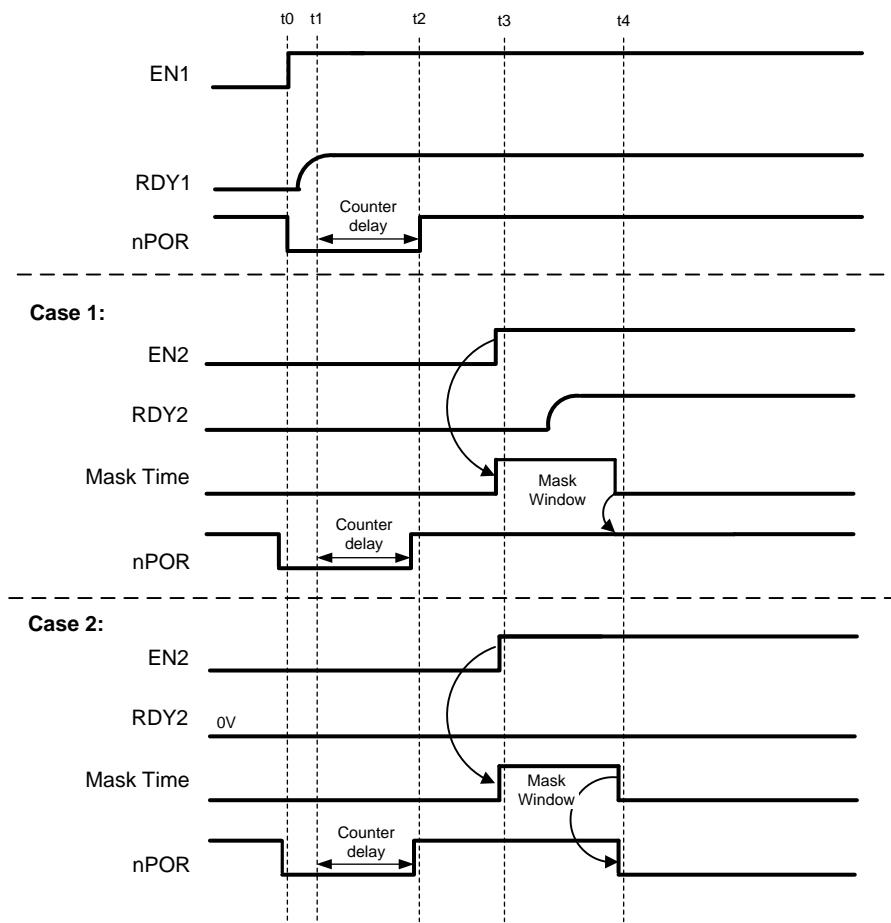
Figure 36 details the power good with delay with respect to the enable signals EN1, and EN2. The RDY1, RDY2 are internal signals derived from the output of two comparators. Each comparator has been trimmed as follows:

COMPARATOR LEVEL	BUCK SUPPLY LEVEL
HIGH	Greater than 94%
LOW	Less than 85%

The circuits for EN1 and RDY1 is symmetrical to EN2 and RDY2, so each reference to EN1 and RDY1 also works for EN2 and RDY2 and vice versa.

If EN1 and RDY1 signals are High at time t1, then the RDY1 signal rising edge triggers the programmable delay counter (50  $\mu$ s, 50 ms, 100 ms, 200 ms). This delay forces nPOR LOW between time interval t1 and t2. nPOR is then pulled high after the programmable delay is completed. Now if EN2 and RDY2 are initiated during this interval the nPOR signal ignores this event.

If either RDY1 or RDY2 were to go LOW at t3 then the programmable delay is triggered again.

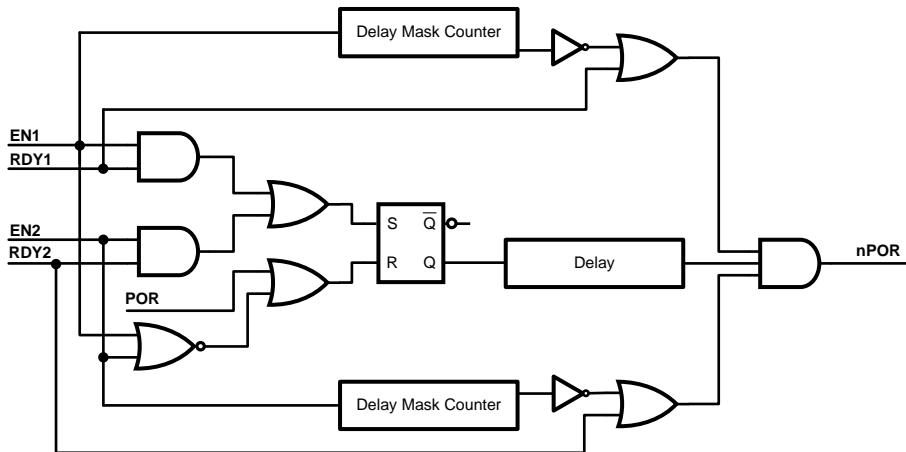


**Figure 37. nPOR Mask Window**

If the EN1 and RDY1 are initiated in normal operation, then nPOR is asserted and deasserted as explained in Figure 37.

Case 1 shows the case where EN2 and RDY2 are initiated after triggered programmable delay. To prevent the nPOR being asserted again, a masked window (5 ms) counter delay is triggered off the EN2 rising edge. nPOR is still held HIGH for the duration of the mask, whereupon the nPOR status afterwards depends on the status of both RDY1 and RDY2 lines.

Case 2 shows the case where EN2 is initiated after the RDY1 triggered programmable delay, but RDY2 never goes HIGH (Buck2 never turns on). Normal operation of nPOR occurs with respect to EN1 and RDY1, and the nPOR signal is held HIGH for the duration of the mask window. We see that nPOR goes LOW after the masking window has timed out because it is now dependent on RDY1 and RDY2, where RDY2 is LOW.



**Figure 38. Design Implementation of the Flexible Power-On Reset**

An internal power-on reset of the device is used with EN1, and EN2 to produce a reset signal (LOW) to the delay timer nPOR. EN1 and RDY1 or EN2 and RDY2 are used to generate the set signal (HIGH) to the delay timer. S = R = 1 never occurs. The mask timers are triggered off EN1 and EN2 which are gated with RDY1, and RDY2 to generate outputs to the final AND gate to generate the nPOR.

### 8.3.4 Undervoltage Lockout

The LP3907-Q1 features an undervoltage lockout circuit. The function of this circuit is to continuously monitor the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8 VDC.

The circuit incorporates a bandgap based circuit that establishes the reference used to determine the 2.8 VDC trip point for a  $V_{IN}$  OK – Not OK detector. This  $V_{IN}$  OK signal is then used to gate the enable signals to the four regulators of the device. When VINLDO12 is greater than 2.8 VDC the four enables control the four regulators, when VINLDO12 is less than 2.8 VDC the four regulators are disabled by the  $V_{IN}$  detector being in the “Not OK” state. The circuit has built-in hysteresis to prevent chattering occurring.

## 8.4 Device Functional Modes

### 8.4.1 Shutdown Mode

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch is on in shutdown to discharge the output. When the converter is enabled, soft start is activated. It is recommended to disable the converter during the system power up and undervoltage conditions when the supply is less than 2.8 V.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C-Compatible Serial Interface

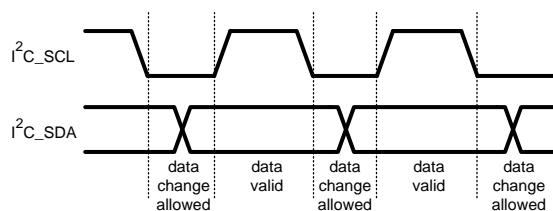
#### 8.5.1.1 I<sup>2</sup>C Signals

The LP3907-Q1 features an I<sup>2</sup>C-compatible serial interface, using two dedicated pins: SCL and SDA for I<sup>2</sup>C clock and data respectively. Both signals need a pullup resistor according to the I<sup>2</sup>C specification. The LP3907-Q1 interface is an I<sup>2</sup>C slave that is clocked by the incoming SCL clock.

Signal timing specifications are according to the I<sup>2</sup>C bus specification. The maximum bit rate is 400kbit/s. See I<sup>2</sup>C specification from NXP Semiconductors for further details.

#### 8.5.1.2 I<sup>2</sup>C Data Validity

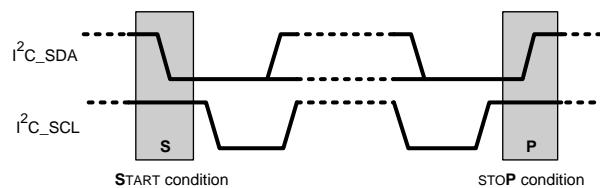
The data on the SDA line must be stable during the HIGH period of the clock signal (SCL); for example, the state of the data line can only be changed when CLK is LOW.



**Figure 39. I<sup>2</sup>C Signals: Data Validity**

#### 8.5.1.3 I<sup>2</sup>C Start and Stop Conditions

START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



**Figure 40. Start and Stop Conditions**

#### 8.5.1.4 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledged related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying acknowledgment. A receiver which has been addressed must generate an acknowledgment ("ACK") after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W).

## Programming (continued)

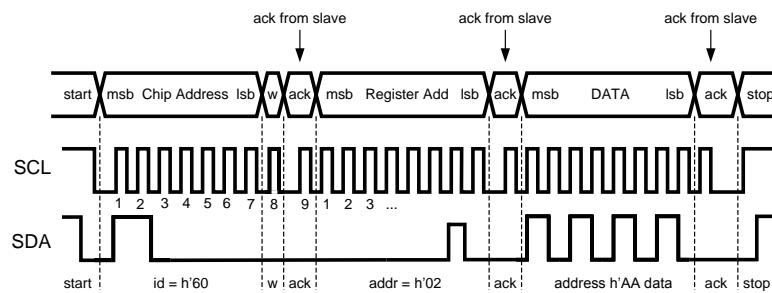
### NOTE

According to industry I<sup>2</sup>C standards for 7-bit addresses, the MSB of an 8-bit address is removed, and communication actually starts with the 7th most significant bit. For the eighth bit (LSB), a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

The LP3907-Q1 has factory-programmed I<sup>2</sup>C addresses. The WQFN chip has a chip address of 60'h, while the DSBGA chip has a chip address of 61'h.



Figure 41. I<sup>2</sup>C Chip Address (see note above)



w = write (SDA = 0)

r = read (SDA = 1)

ack = acknowledge (SDA pulled down by either master or slave)

rs = repeated start

id = LP3907-Q1 WQFN chip address: 0x60; DSBGA chip address: 0x61

Figure 42. I<sup>2</sup>C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

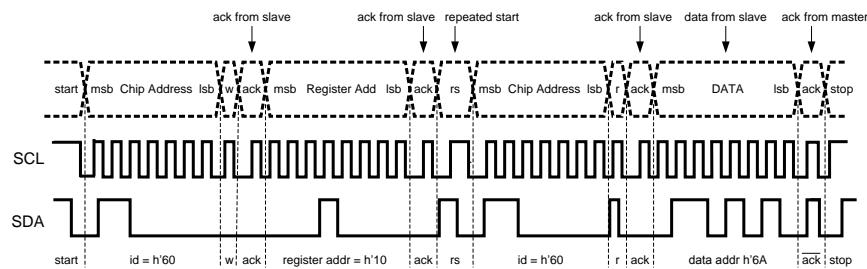


Figure 43. I<sup>2</sup>C Read Cycle

## Programming (continued)

### 8.5.2 Factory Programmable Options

Table 7 shows options EPROM programmed during final test of the LP3907-Q1. The system designer that needs specific options is advised to contact the TI sales office.

**Table 7. Factory-Programmable Options**

FACTORY PROGRAMMABLE OPTIONS	CURRENT VALUE
Enable delay for power on	code 010 (see <a href="#">Control 1 Register (SCR1) 0x07</a> )
SW1 ramp speed	8 mV/μs
SW2 ramp speed	8 mV/μs

The I<sup>2</sup>C Chip ID address is offered as a metal mask option. The current address for the WQFN chip equals 0x60, while the address for the DSBGA chip is 0x61.

## 8.6 Register Maps

### 8.6.1 LP3907-Q1 Control Registers

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
0x02	ICRA	R	Interrupt Status Register A
0x07	SCR1	R/W	System Control 1 Register
0x10	BKLDOEN	R/W	Buck and LDO Output Voltage Enable Register
0x11	BKLDOSR	R	Buck and LDO Output Voltage Status Register
0x20	VCCR	R/W	Voltage Change Control Register 1
0x23	B1TV1	R/W	Buck1 Target Voltage 1 Register
0x24	B1TV2	R/W	Buck1 Target Voltage 2 Register
0x25	B1RC	R/W	Buck1 Ramp Control
0x29	B2TV1	R/W	Buck2 Target Voltage 1 Register
0x2A	B2TV2	R/W	Buck2 Target Voltage 2 Register
0x2B	B2RC	R/W	Buck2 Ramp Control
0x38	BFCR	R/W	Buck Function Register
0x39	LDO1VCR	R/W	LDO1 Voltage Control Registers
0x3A	LDO2VCR	R/W	LDO2 Voltage Control Registers

#### 8.6.1.1 Interrupt Status Register (ISRA) 0x02

This register informs the System Engineer of the temperature status of the chip.

	D7-D2	D1	D0
Name	—	Temp 125°C	—
Access	—	R	—
Data	Reserved	Status bit for thermal warning PMIC T>125°C 0 – PMIC Temp. < 125°C 1 – PMIC Temp. > 125°C	Reserved
Reset	0	0	0

#### 8.6.1.2 Control 1 Register (SCR1) 0x07

This register allows the user to select the preset delay sequence for power-on timing, to switch between PFM and PWM mode for the bucks, and also to select between an internal and external clock for the bucks.

	D7	D6-D4	D3	D2	D1	D0
Name	—	EN_DLY	—	FPWM2	FPWM1	ECEN
Access	—	R/W	—	R/W	R/W	R/W
Data	Reserved	Selects the preset delay sequence from EN_T assertion (shown below)	Reserved	Buck2 PWM /PFM Mode select 0 – Auto Switch PFM - PWM operation 1 – PWM Mode Only	Buck 1 PWM /PFM Mode select 0 – Auto Switch PFM - PWM operation 1 – PWM Mode Only	Reserved
Reset	0	Factory-Programmed Default	1	Factory-Programmed Default	Factory-Programmed Default	0

### 8.6.1.3 EN\_DLY Preset Delay Sequence After EN\_T Assertion

EN_DLY<2:0>	DELAY (ms)			
	BUCK1	BUCK2	LDO1	LDO2
000	1	1	1	1
001	1	1.5	2	2
010	1.5	2	3	6
011	1.5	2	1	1
100	1.5	2	3	6
101	1.5	1.5	2	2
110	3	2	1	1.5
111	2	3	6	11

### 8.6.1.4 Buck and LDO Output Voltage Enable Register (BKLDOEN) – 0x10

This register controls the enables for the Bucks and LDOs.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	—	LDO2EN	—	LDO1EN	—	BK2EN	—	BK1EN
Access	—	R/W	—	R/W	—	R/W	—	R/W
Data	Reserved	0 – Disable 1 – Enable						
Reset	0	1	1	1	0	1	0	1

### 8.6.1.5 Buck and LDO Status Register (BKLDOSR) – 0x11

This register monitors whether the Bucks and LDOs meet the voltage output specifications.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	BKS_OK	LDOS_OK	LDO2_OK	LDO1_OK	—	BK2_OK	—	BK1_OK
Access	R	R	R	R	—	R	—	R
Data	0 – Buck 1-2 Not Valid 1 – Bucks Valid	0 – LDO 1-2 Not Valid 1 – LDOs Valid	0 – LDO2 Not Valid 1 – LDO2 Valid	0 – LDO1 Not Valid 1 – LDO1 Valid	Reserved	0 – Buck2 Not Valid 1 – Buck2 Valid	Reserved	0 – Buck1 Not Valid 1 – Buck1 Valid
Reset	0	0	0	0	0	0	0	0

### 8.6.1.6 Buck Voltage Change Control Register 1 (VCCR) – 0x20

This register selects and controls the output target voltages for the buck regulators.

	D7-6	D5	D4	D3-2	D1	D0
Name	—	B2VS	B2GO	—	B1VS	B1GO
Access	—	R/W	R/W	—	R/W	R/W
Data	Reserved	Buck2 Target Voltage Select 0 – B2VT1 1 – B2VT2	Buck2 Voltage Ramp CTRL 0 – Hold 1 – Ramp to B2VS selection	Reserved	Buck1 Target Voltage Select 0 – B1VT1 1 – B1VT2	Buck1 Voltage Ramp CTRL 0 – Hold 1 – Ramp to B1VS selection
Reset	00	0	0	00	0	0

### 8.6.1.7 Buck1 Target Voltage 1 Register (B1TV1) – 0x23

This register allows the user to program the output target voltage of Buck1.

	<b>D7-D5</b>	<b>D4-D0</b>	
Name	—	BK1_VOUT1	
Access	—	R/W	
Data	Reserved	Buck1 Output Voltage (V)	
		5'h00	Ext Ctrl
		5'h01	0.80
		5'h02	0.85
		5'h03	0.90
		5'h04	0.95
		5'h05	1.00
		5'h06	1.05
		5'h07	1.10
		5'h08	1.15
		5'h09	1.20
		5'h0A	1.25
		5'h0B	1.30
		5'h0C	1.35
		5'h0D	1.40
		5'h0E	1.45
		5'h0F	1.50
		5'h10	1.55
		5'h11	1.60
		5'h12	1.65
		5'h13	1.70
		5'h14	1.75
		5'h15	1.80
		5'h16	1.85
		5'h17	1.90
		5'h18	1.95
		5'h19	2.00
		5'h1A–5'h1F	2.00
Reset	000	Factory-Programmed Default	

### 8.6.1.8 Buck1 Target Voltage 2 Register (B1TV2) – 0x24

This register allows the user to program the output target voltage of Buck1.

	<b>D7-D5</b>	<b>D4-D0</b>	
Name	—	BK1_VOUT2	
Access	—	R/W	
Data	Reserved	Buck1 Output Voltage (V)	
		5'h00	Ext Ctrl <sup>(1)</sup>
		5'h01	0.80
		5'h02	0.85
		5'h03	0.90
		5'h04	0.95
		5'h05	1.00
		5'h06	1.05
		5'h07	1.10
		5'h08	1.15
		5'h09	1.20
		5'h0A	1.25
		5'h0B	1.30
		5'h0C	1.35
		5'h0D	1.40
		5'h0E	1.45
		5'h0F	1.50
		5'h10	1.55
		5'h11	1.60
		5'h12	1.65
		5'h13	1.70
		5'h14	1.75
		5'h15	1.80
		5'h16	1.85
		5'h17	1.90
		5'h18	1.95
		5'h19	2.00
		5'h1A–5'h1F	2.00
Reset	000	Factory-Programmed Default	

(1) If using Ext Ctrl, contact TI Sales for support.

### 8.6.1.9 Buck1 Ramp Control Register (B1RC) - 0x25

This register allows the user to program the rate of change between the target voltages of Buck1.

	D7	D6-D4	D3-D0	
Name	----	----	B1RS	
Access	----	----	R/W	
Data	Reserved	Reserved	Data Code	Ramp Rate mV/us
			4h'0	Instant
			4h'1	1
			4h'2	2
			4h'3	3
			4h'4	4
			4h'5	5
			4h'6	6
			4h'7	7
			<b>4h'8</b>	<b>8</b>
			4h'9	9
			4h'A	10
			4h'B - 4h'F	10
Reset	0	010	1000	

### 8.6.1.10 Buck2 Target Voltage 1 Register (B2TV1) – 0x29

This register allows the user to program the output target voltage of Buck2.

	<b>D7-D5</b>	<b>D4-D0</b>	
Name	—	BK2_VOUT1	
Access	—	R/W	
Data	Reserved	Buck2 Output Voltage (V)	
		5'h00	Ext Ctrl
		5'h01	1.0
		5'h02	1.1
		5'h03	1.2
		5'h04	1.3
		5'h05	1.4
		5'h06	1.5
		5'h07	1.6
		5'h08	1.7
		5'h09	1.8
		5'h0A	1.9
		5'h0B	2.0
		5'h0C	2.1
		5'h0D	2.2
		5'h0E	2.4
		5'h0F	2.5
		5'h10	2.6
		5'h11	2.7
		5'h12	2.8
		5'h13	2.9
		5'h14	3.0
		5'h15	3.1
		5'h16	3.2
		5'h17	3.3
		5'h18	3.4
		5'h19	3.5
		5'h1A–5'h1F	3.5
Reset	000	Factory-Programmed Default	

### 8.6.1.11 Buck2 Target Voltage 2 Register (B2TV2) – 0x2A

This register allows the user to program the output target voltage of Buck2.

	D7-5	D4-0	
Name	—	BK2_VOUT2	
Access	—	R/W	
Data	Reserved	Buck2 Output Voltage (V)	
		5'h00	Ext Ctrl <sup>(1)</sup>
		5'h01	1.0
		5'h02	1.1
		5'h03	1.2
		5'h04	1.3
		5'h05	1.4
		5'h06	1.5
		5'h07	1.6
		5'h08	1.7
		5'h09	1.8
		5'h0A	1.9
		5'h0B	2.0
		5'h0C	2.1
		5'h0D	2.2
		5'h0E	2.4
		5'h0F	2.5
		5'h10	2.6
		5'h11	2.7
		5'h12	2.8
		5'h13	2.9
		5'h14	3.0
		5'h15	3.1
		5'h16	3.2
		5'h17	3.3
		5'h18	3.4
		5'h19	3.5
		5'h1A–5'h1F	3.5
Reset	000	Factory-Programmed Default	

(1) If using Ext Ctrl, contact TI Sales for support.

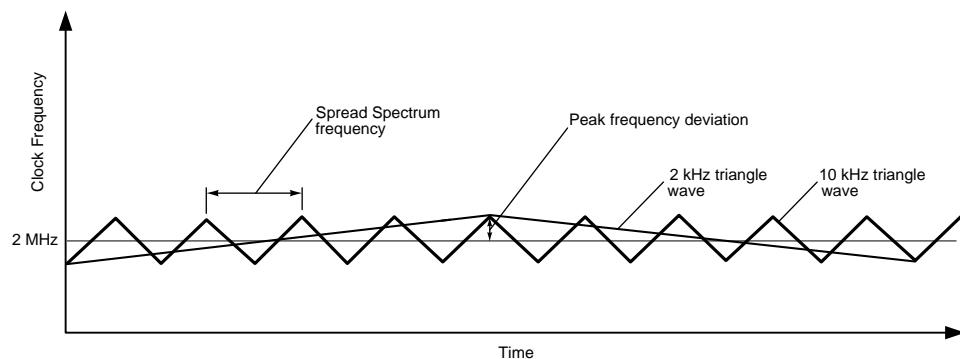
### 8.6.1.12 Buck2 Ramp Control Register (B2RC) - 0x2B

This register allows the user to program the rate of change between the target voltages of Buck2.

	D7	D6-D4	D3-D0	
Name	----	----	B2RS	
Access	----	----	R/W	
Data	Reserved	Reserved	Data Code	Ramp Rate mV/us
			4h'0	Instant
			4h'1	1
			4h'2	2
			4h'3	3
			4h'4	4
			4h'5	5
			4h'6	6
			4h'7	7
			<b>4h'8</b>	<b>8</b>
			4h'9	9
			4h'A	10
			4h'B - 4h'F	10
Reset	0	010	1000	

### 8.6.1.13 Buck Function Register (BFCR) – 0x38

This register allows the Buck switcher clock frequency to be spread across a wider range, allowing for less Electro-magnetic Interference (EMI). The spread spectrum modulation frequency refers to the rate at which the frequency ramps up and down, centered at 2 MHz.



**Figure 44. Spread Spectrum Modulation Frequency**

This register also allows dynamic scaling of the nPOR Delay Timing. The LP3907-Q1 is equipped with an internal POR circuit which monitors the output voltage levels on the buck regulators, allowing the user to more actively monitor the power status of the chip.

The UVLO feature continuously monitors the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8 VDC. This prevents the user from damaging the power source (such as battery), but can be disabled if the user wishes.

Note that if the supply to VDD\_M is close to 2.8 V with a heavy load current on the regulators, the chip is in danger of powering down due to UVLO. If the user wishes to keep the chip active under those conditions, enable the Bypass UVLO feature.

	<b>D7-D5</b>	<b>D4</b>	<b>D3-D2</b>	<b>D1</b>	<b>D0</b>
Name	—	BP_UVLO	TPOR	BK_SLOMOD	BK_SSEN
Access	—	R/W	R/w	R/W	R/W
Data	Reserved	Bypass UVLO monitoring 0 - Allow UVLO 1 - Disable UVLO	nPOR Delay Timing 00 - 50 µs 01 - 50 ms 10 - 100 ms 11 - 200 ms	Buck Spread Spectrum Modulation 0 – 10 kHz triangular wave 1 – 2 kHz triangular wave	Spread Spectrum Function Output 0 – Disabled 1 – Enabled
Reset	000	Factory-Programmed Default	01	1	0

#### **8.6.1.14 LDO1 Control Register (LDO1VCR) – 0x39**

This register allows the user to program the output target voltage of LDO 1.

	<b>D7-D5</b>	<b>D4-D0</b>	
Name	—	LDO1_OUT	
Access	—	R/W	
Data	Reserved	LDO1 Output voltage (V)	
		5'h00	1.0
		5'h01	1.1
		5'h02	1.2
		5'h03	1.3
		5'h04	1.4
		5'h05	1.5
		5'h06	1.6
		5'h07	1.7
		5'h08	1.8
		5'h09	1.9
		5'h0A	2.0
		5'h0B	2.1
		5'h0C	2.2
		5'h0D	2.3
		5'h0E	2.4
		5'h0F	2.5
		5'h10	2.6
		5'h11	2.7
		5'h12	2.8
		5'h13	2.9
		5'h14	3.0
		5'h15	3.1
		5'h16	3.2
		5'h17	3.3
		5'h18	3.4
		5'h19	3.5
		5'h1A–5'h1F	3.5
Reset	000	Factory-Programmed Default	

### 8.6.1.15 LDO2 Control Register (LDO2VCR) – 0x3A

This register allows the user to program the output target voltage of LDO 2.

	<b>D7-D5</b>	<b>D4-D0</b>	
Name	—	LDO2_OUT	
Access	—	R/W	
Data	Reserved	LDO2 Output voltage (V)	
		5'h00	1.0
		5'h01	1.1
		5'h02	1.2
		5'h03	1.3
		5'h04	1.4
		5'h05	1.5
		5'h06	1.6
		5'h07	1.7
		5'h08	1.8
		5'h09	1.9
		5'h0A	2.0
		5'h0B	2.1
		5'h0C	2.2
		5'h0D	2.3
		5'h0E	2.4
		5'h0F	2.5
		5'h10	2.6
		5'h11	2.7
		5'h12	2.8
		5'h13	2.9
		5'h14	3.0
		5'h15	3.1
		5'h16	3.2
		5'h17	3.3
		5'h18	3.4
		5'h19	3.5
		5'h1A–5'h1F	3.5
Reset	000	Factory-Programmed Default	

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP3907-Q1 provides three control methods to turn ON/OFF four power rails:

1. EN\_T Control: Provides pre-defined power up/down sequence. (Note:  $V_{IN}$ /Battery voltage must be settled approximately 8 ms, minimum, before EN\_T be asserted high).
2. Individual GPIO/EN pin control: four EN pins provide max control flexibility without  $I^2C$ .
3.  $I^2C$  control: besides simple ON/OFF control, also provides access to all the user programmable registers.

See [Register Maps](#) for details.

### 9.2 Typical Application

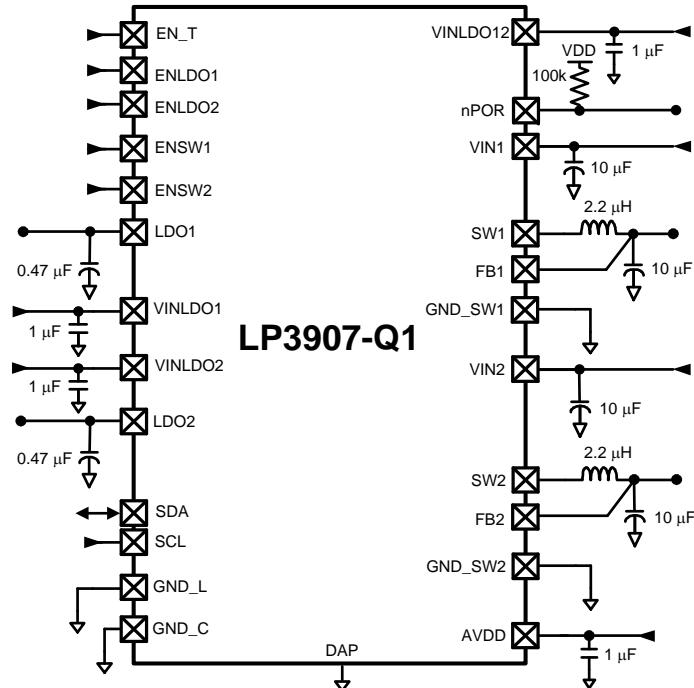


Figure 45. LP3907-Q1 Typical Application

#### 9.2.1 Design Requirements

Ten ceramic capacitors and two inductors are required for this application. These three external components must be selected very carefully for proper operation. See [Detailed Design Procedure](#).

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Component Selection

##### 9.2.2.1.1 Inductors for SW1 And SW2

There are two main considerations when choosing an inductor; the inductor must not saturate and the inductor current ripple is small enough to achieve the desired output voltage ripple. Care must be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application must be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating:

##### 9.2.2.1.1.1 Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average-to-peak inductor current. This can be written as follows:

$$I_{sat} > I_{outmax} + I_{ripple}$$

$$\text{where } I_{ripple} = \left(\frac{1}{f}\right) \times \left(\frac{V_{IN} - V_{OUT}}{2L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where

- $I_{RIPPLE}$  = Maximum load current
- $I_{OUTMAX}$  = Average to peak inductor current
- $V_{IN}$  = Maximum input voltage to the buck
- $L$  = Min inductor value including worse case tolerances (30% drop can be considered for method 1)
- $f$  = Minimum switching frequency (1.6 MHz)
- $V_{OUT}$  = Buck output voltage

(6)

##### 9.2.2.1.1.2 Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the maximum current limit of 1250 mA for Buck1 and 1750 mA for Buck2.

Given a peak-to-peak current ripple ( $I_{PP}$ ) the inductor needs to be at least

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$
(7)

**Table 8. Suggested Inductor Values**

INDUCTOR	VALUE (μH)	DESCRIPTION	NOTES
$L_{SW1,2}$	2.2	SW1,2 inductor	DCR: 70 mΩ

##### 9.2.2.1.2 External Capacitors

The regulators on the LP3907-Q1 require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

#### 9.2.2.2 LDO Capacitor Selection

##### 9.2.2.2.1 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-μF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failures due to surge currents when connected to a low impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains approximately 1  $\mu\text{F}$  over the entire operating temperature range.

#### 9.2.2.2.2 Output Capacitor

The LDOs on the LP3907-Q1 are designed specifically to work with very small ceramic output capacitors. A 0.47- $\mu\text{F}$  ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 m $\Omega$  to 500 m $\Omega$ , is suitable in the application circuit.

It is also possible to use tantalum or film capacitors at the device output,  $C_{\text{OUT}}$  (or  $V_{\text{OUT}}$ ), but these are not as attractive for reasons of size and cost.

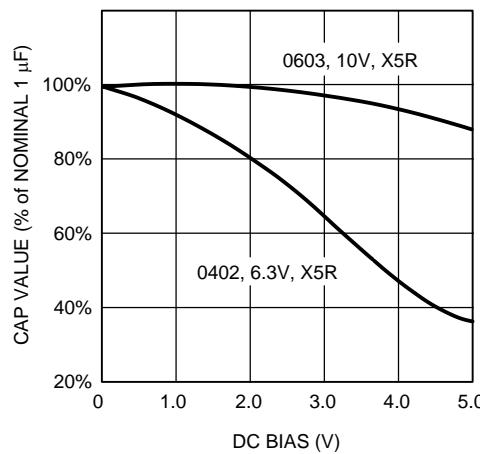
The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 m $\Omega$  to 500 m $\Omega$  for stability.

#### 9.2.2.2.3 Capacitor Characteristics

The LDOs are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47  $\mu\text{F}$  to 4.7  $\mu\text{F}$ , ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1- $\mu\text{F}$  ceramic capacitor is in the range of 20 m $\Omega$  to 40 m $\Omega$ , which easily meets the ESR requirement for stability for the LDOs.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependent on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, [Figure 46](#) is a typical graph comparing different capacitor case sizes.



**Figure 46. Graph Showing Typical Variation in Capacitance vs. DC Bias**

As shown in the graph, increasing the DC Bias condition can result in the capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , only varies the capacitance to within  $\pm 15\%$ . The capacitor type X5R has a similar tolerance over a reduced temperature range of  $-55^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Many large value ceramic capacitors, larger than  $1 \mu\text{F}$  are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from  $25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Therefore, X7R is recommended over Z5U and Y5V in applications where the ambient temperature changes significantly above or below  $25^{\circ}\text{C}$ .

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the  $0.47\text{-}\mu\text{F}$  to  $4.7\text{-}\mu\text{F}$  range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Note, also, that the ESR of a typical tantalum increases about 2:1 as the temperature goes from  $25^{\circ}\text{C}$  down to  $-40^{\circ}\text{C}$ , so some guard band must be allowed.

#### 9.2.2.2.4 Input Capacitor Selection for SW1 And SW2

A ceramic input capacitor of  $10 \mu\text{F}$ , 6.3 V is sufficient for the magnetic DC-DC converters. Place the input capacitor as close to the input of the device as possible. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the DC-DC converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to fast current transients. A capacitor with sufficient ripple current rating must be selected. The Input current ripple can be calculated as:

$$I_{\text{rms}} = I_{\text{outmax}} \sqrt{\frac{V_{\text{OUT}}}{V_{\text{IN}}}} \left( 1 + \frac{r^2}{12} \right) \text{ where } r = \frac{(V_{\text{in}} - V_{\text{out}}) \times V_{\text{out}}}{L \times f \times I_{\text{outmax}} \times V_{\text{in}}} \quad (8)$$

The worse case is when  $V_{\text{IN}} = 2 V_{\text{OUT}}$ .

#### 9.2.2.2.5 Output Capacitor Selection for SW1, SW2

A  $10\text{-}\mu\text{F}$ , 6.3-V ceramic capacitor must be used on the output of the SW1 and SW2 magnetic DC-DC converters. The output capacitor must be mounted as close to the output of the device as possible. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them and analyzed as part of the capacitor selection process.

The output filter capacitor of the magnetic DC-DC converter smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESD to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as follows:

$$V_{\text{PP-ESR}} = \frac{I_{\text{ripple}}}{4 \times f \times C} \quad (9)$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows:

$$V_{\text{PP-ESR}} = 2 \times I_{\text{RIPPLE}} \times R_{\text{ESR}} \quad (10)$$

Because the  $V_{\text{PP-C}}$  and  $V_{\text{PP-ESR}}$  are out of phase, the rms value can be used to get an approximate value of the peak-to-peak ripple:

$$V_{\text{pp-rms}} = \sqrt{V_{\text{pp-c}}^2 + V_{\text{pp-esr}}^2} \quad (11)$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor ( $R_{\text{ESR}}$ ). The  $R_{\text{ESR}}$  is frequency dependent as well as temperature dependent. Calculate the  $R_{\text{ESR}}$  with the applicable switching frequency and ambient temperature.

**Table 9. Suggested Capacitor Values**

CAPACITOR	MIN VALUE ( $\mu\text{F}$ )	DESCRIPTION	RECOMMENDED TYPE
$C_{\text{LDO1}}$	0.47	LDO1 output capacitor	Ceramic, 6.3 V, X5R
$C_{\text{LDO2}}$	0.47	LDO2 output capacitor	Ceramic, 6.3 V, X5R
$C_{\text{SW1}}$	10	SW1 output capacitor	Ceramic, 6.3 V, X5R
$C_{\text{SW2}}$	10	SW2 output capacitor	Ceramic, 6.3 V, X5R

#### 9.2.2.2.6 I<sup>2</sup>C Pullup Resistor

Both SDA and SCL pins must have pullup resistors connected to VINLDO12 or to the power supply of the I<sup>2</sup>C master. The values of the pullup resistors (typical approximately 1.8 k $\Omega$ ) are determined by the capacitance of the bus. A resistor that is too large, combined with a given bus capacitance, results in a rise time that would violate the maximum rise time specification. A too-small resistor results in a contention with the pulldown transistor on either slave(s) or master.

#### 9.2.2.3 Operation Without I<sup>2</sup>C Interface

Operation of the LP3907-Q1 without the I<sup>2</sup>C interface is possible if the system can operate with default values for the LDO and Buck regulators (see [Factory Programmable Options](#).) The I<sup>2</sup>C-less system must rely on the correct default output values of the LDO and Buck converters.

#### 9.2.2.3.1 High $V_{\text{IN}}$ High-Load Operation

Additional information is provided when the IC is operated at extremes of  $V_{\text{IN}}$  and regulator loads. These are described in terms of the junction temperature and, buck output ripple management.

### 9.2.2.3.2 Junction Temperature

The maximum junction temperature  $T_{J-MAX-OP}$  of 125°C of the device package [Equation 12](#) through [Equation 17](#) demonstrate junction temperature determination, ambient temperature  $T_{A-MAX}$ , and total chip power must be controlled to keep  $T_J$  below this maximum:

$$T_{J-MAX-OP} = T_{A-MAX} + (R_{\theta JA}) [^{\circ}\text{C}/\text{Watt}] \times (P_{D-MAX}) [\text{Watts}] \quad (12)$$

Total device power dissipation  $P_{D-MAX}$  is the sum of the individual power dissipation of the four regulators plus a minor amount for chip overhead. Chip overhead is Bias, TSD, and LDO analog.

$$P_{D-MAX} = P_{LDO1} + P_{LDO2} + P_{BUCK1} + P_{BUCK2} + (0.0001A \times V_{IN}) [\text{Watts}] \quad (13)$$

#### Power dissipation of LDO1:

$$P_{LDO1} = (V_{INLDO1} - V_{OUTLDO1}) \times I_{OUTLDO1} [\text{V} \times \text{A}] \quad (14)$$

#### Power dissipation of LDO2:

$$P_{LDO2} = (V_{INLDO2} - V_{OUTLDO2}) \times I_{OUTLDO2} [\text{V} \times \text{A}] \quad (15)$$

#### Power dissipation of Buck1:

$$P_{Buck1} = P_{IN} - P_{OUT} = V_{OUTBuck1} \times I_{OUTBuck1} \times (1 - \eta_1) / \eta_1 [\text{V} \times \text{A}]$$

where

- $\eta_1$  = efficiency of buck 1

#### Power dissipation of Buck2:

$$P_{Buck2} = P_{IN} - P_{OUT} = V_{OUTBuck2} \times I_{OUTBuck2} \times (1 - \eta_2) / \eta_2 [\text{V} \times \text{A}]$$

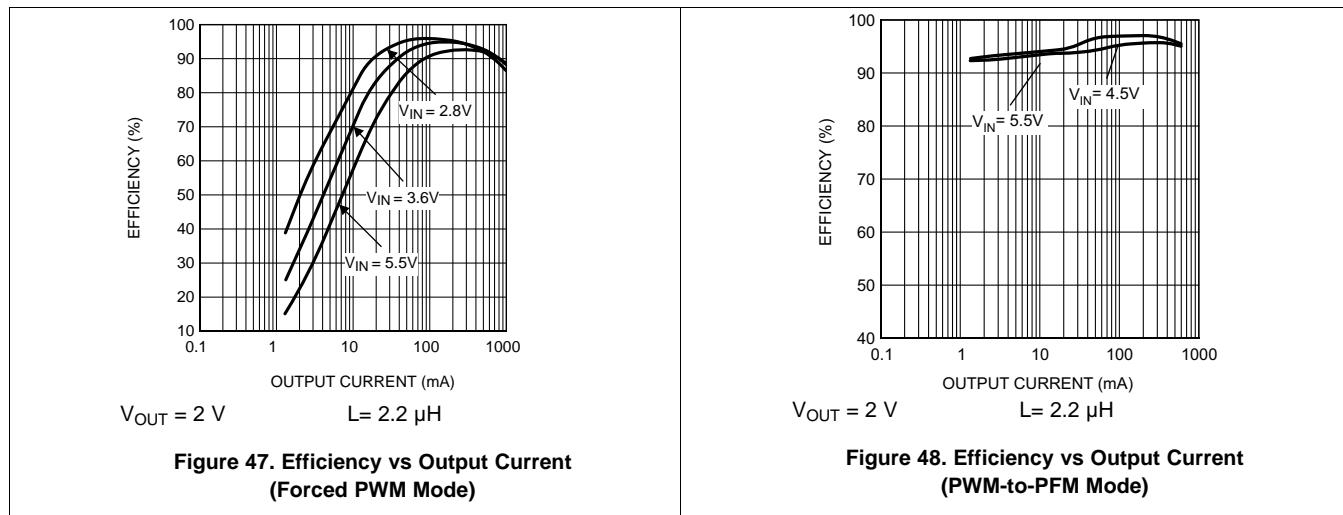
where

- $\eta_2$  = efficiency of Buck2

where

- $\eta$  is the efficiency for the specific condition taken from efficiency graphs.

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

If the EN\_T is used to power up the device instead individual ENs, then VIN must be stable for approximately 8 ms minimum before EN\_T be asserted high to ensure internal bias, reference, and the Flexible POR timing are stabilized. This initial EN\_T delay is necessary only upon first time device power on for power sequencing function to operate properly.

### 10.1 Analog Power Signal Routing

All power inputs must be tied to the main VDD source (for example, battery), unless the user wishes to power it from another source. (that is, external LDO output).

The analog VDD inputs power the internal bias and error amplifiers, so they must be tied to the main VDD. The analog VDD inputs must have an input voltage between 2.8 V and 5.5 V, as specified in the *Recommended Operating Conditions (Bucks)* table earlier in the data sheet.

The other VINs (VINLDO1, VINLDO2) can have inputs lower than 2.8 V, as long as the input is higher than the programmed output (0.3 V).

The analog and digital grounds must be tied together outside of the chip to reduce noise coupling.

## 11 Layout

### 11.1 DSBGA Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability.

Good layout for the LP3907-Q1 device bucks can be implemented by following a few simple design rules below. Refer to [Figure 49](#) for top-layer board buck layout.

1. *Place the LP3907 bucks, inductor, and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the VIN and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor through the LP3907-Q1 bucks and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LP3907-Q1 bucks by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LP3907-Q1 bucks and filter capacitors together using generous component-side copper fill as a pseudo-ground plane.* Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LP3907-Q1 bucks by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the circuit of the LP3907-Q1 buck and must be direct but must be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

For more detailed layout specifications and information, refer to [AN-1112 DSBGA Wafer Level Chip Scale Package](#).

## 11.2 Layout Example

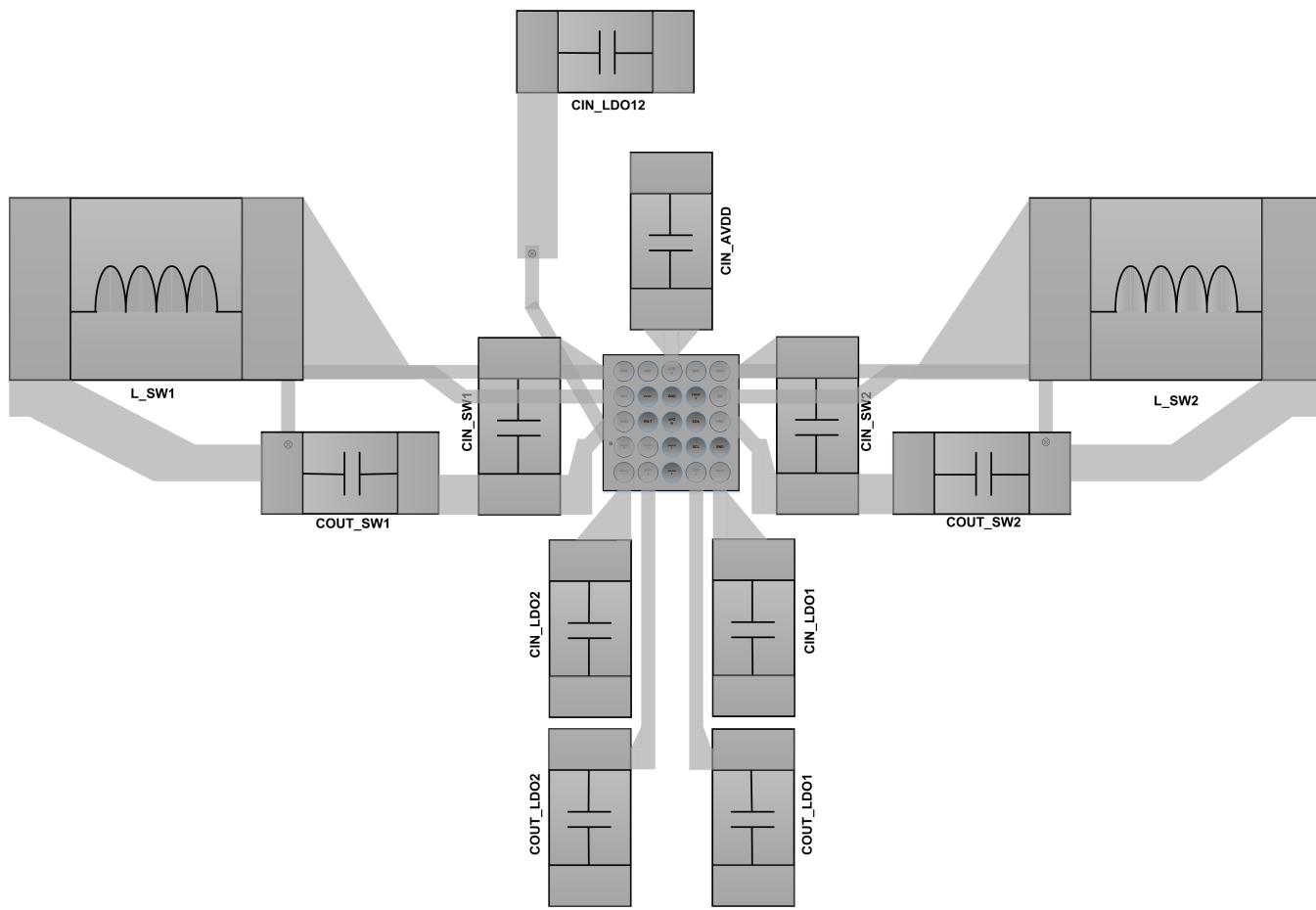


Figure 49. LP3907-Q1 DSBGA Layout Example

## 11.3 Thermal Considerations of WQFN Package

The LP3907-Q1 is a monolithic device with integrated power FETs. For that reason, it is important to pay special attention to the thermal impedance of the WQFN package and to the PCB layout rules in order to maximize power dissipation of the WQFN package.

The WQFN package is designed for enhanced thermal performance and features an exposed die attach pad at the bottom center of the package that creates a direct path to the PCB for maximum power dissipation. Compared to the traditional leaded packages where the die attach pad is embedded inside the molding compound, the WQFN reduces one layer in the thermal path.

The thermal advantage of the WQFN package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with thermal vias planted underneath the thermal land. Based on thermal analysis of the WQFN package, the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) can be improved by a factor of two when the die attach pad of the WQFN package is soldered directly onto the PCB with thermal land and thermal vias, as opposed to an alternative with no direct soldering to a thermal land. Typical pitch and outer diameter for thermal vias are 1.27 mm and 0.33 mm, respectively. Typical copper via barrel plating is 1 oz, although thicker copper may be used to further improve thermal performance. The LP3907-Q1 die attach pad is connected to the substrate of the device, and therefore, the thermal land and vias on the PCB board must be connected to ground (GND pin).

For more information on board layout techniques, refer to [AN-1187 Leadless Lead Frame Package \(LLP\)](#) on <http://www.ti.com>. This application note also discusses package handling, solder stencil, and the assembly process.

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：

- [AN-1112 DSBGA 晶圆级芯片级封装](#)
- [《AN-1187 无引线型引线框架封装 \(LLP\)》](#)

### 12.2 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.3 接收文档更新通知

如需接收文档更新通知，请导航至[ti.com](#) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** **TI 的工程师对工程师 (E2E) 社区。**此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 12.5 静电放电警告

 这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3907QSQ-JJXP/NO.A	Active	Production	WQFN (RTW)   24	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	07QJJXP
LP3907QSQ-JJXP/NOPB	Active	Production	WQFN (RTW)   24	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	07QJJXP
LP3907QSQ-JXI7/NO.A	Active	Production	WQFN (RTW)   24	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	07QJXI7
LP3907QSQ-JXI7/NOPB	Active	Production	WQFN (RTW)   24	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	07QJXI7
LP3907QSQ-JXIP/NO.A	Active	Production	WQFN (RTW)   24	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	07QJXIP
LP3907QSQ-JXIP/NOPB	Active	Production	WQFN (RTW)   24	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	07QJXIP
LP3907QTL-VXSS/NO.A	Active	Production	DSBGA (YZR)   25	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V025
LP3907QTL-VXSS/NOPB	Active	Production	DSBGA (YZR)   25	250   SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V025
LP3907QTLX-VXSS/NO.A	Active	Production	DSBGA (YZR)   25	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V025
LP3907QTLX-VXSS/NOPB	Active	Production	DSBGA (YZR)   25	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V025

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

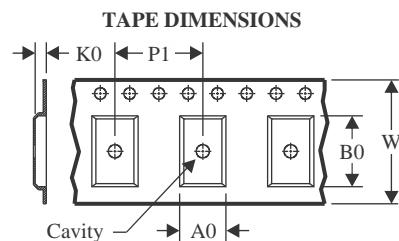
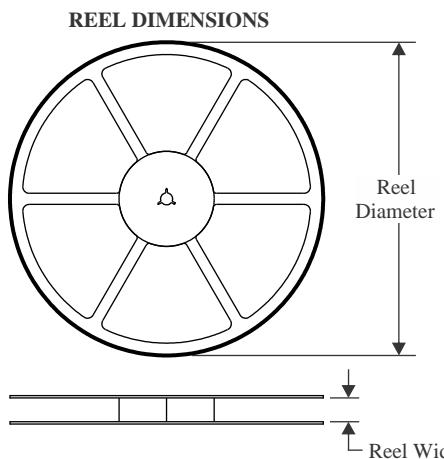
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LP3907-Q1 :**

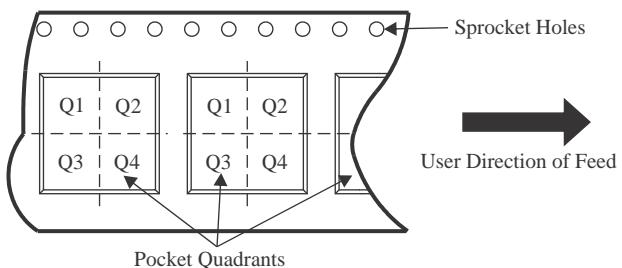
- Catalog : [LP3907](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

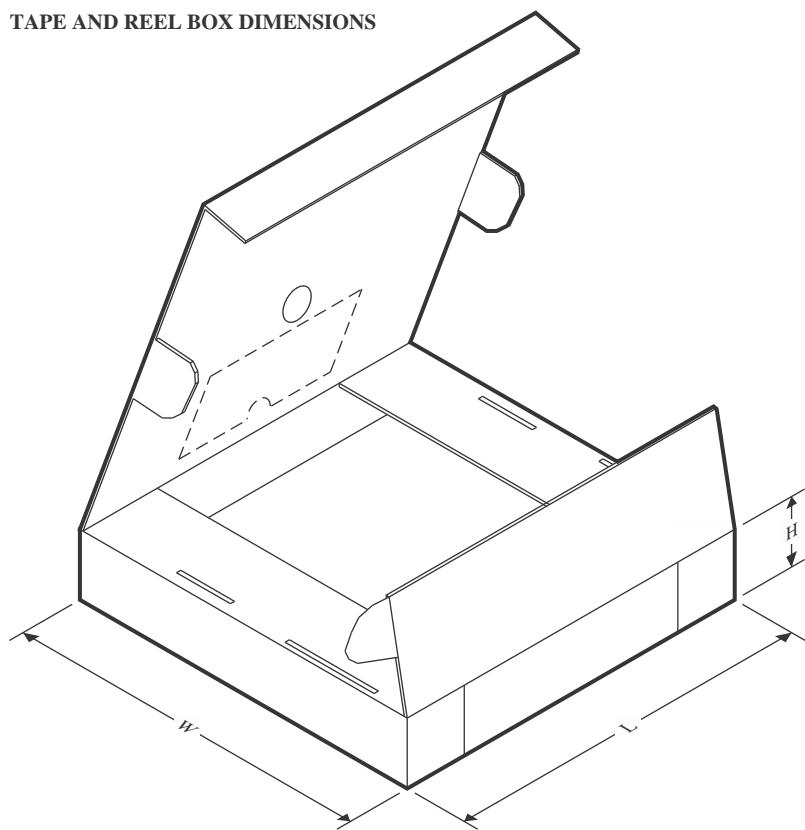
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


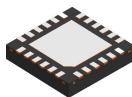
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3907QSQ-JJXP/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3907QSQ-JXI7/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3907QSQ-JXIP/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3907QTL-VXSS/NOPB	DSBGA	YZR	25	250	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1
LP3907QTLX-VXSS/NOPB	DSBGA	YZR	25	3000	178.0	8.4	2.69	2.69	0.76	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3907QSQ-JJXP/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LP3907QSQ-JX17/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LP3907QSQ-JX1P/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LP3907QTL-VXSS/NOPB	DSBGA	YZR	25	250	208.0	191.0	35.0
LP3907QTLX-VXSS/NOPB	DSBGA	YZR	25	3000	208.0	191.0	35.0

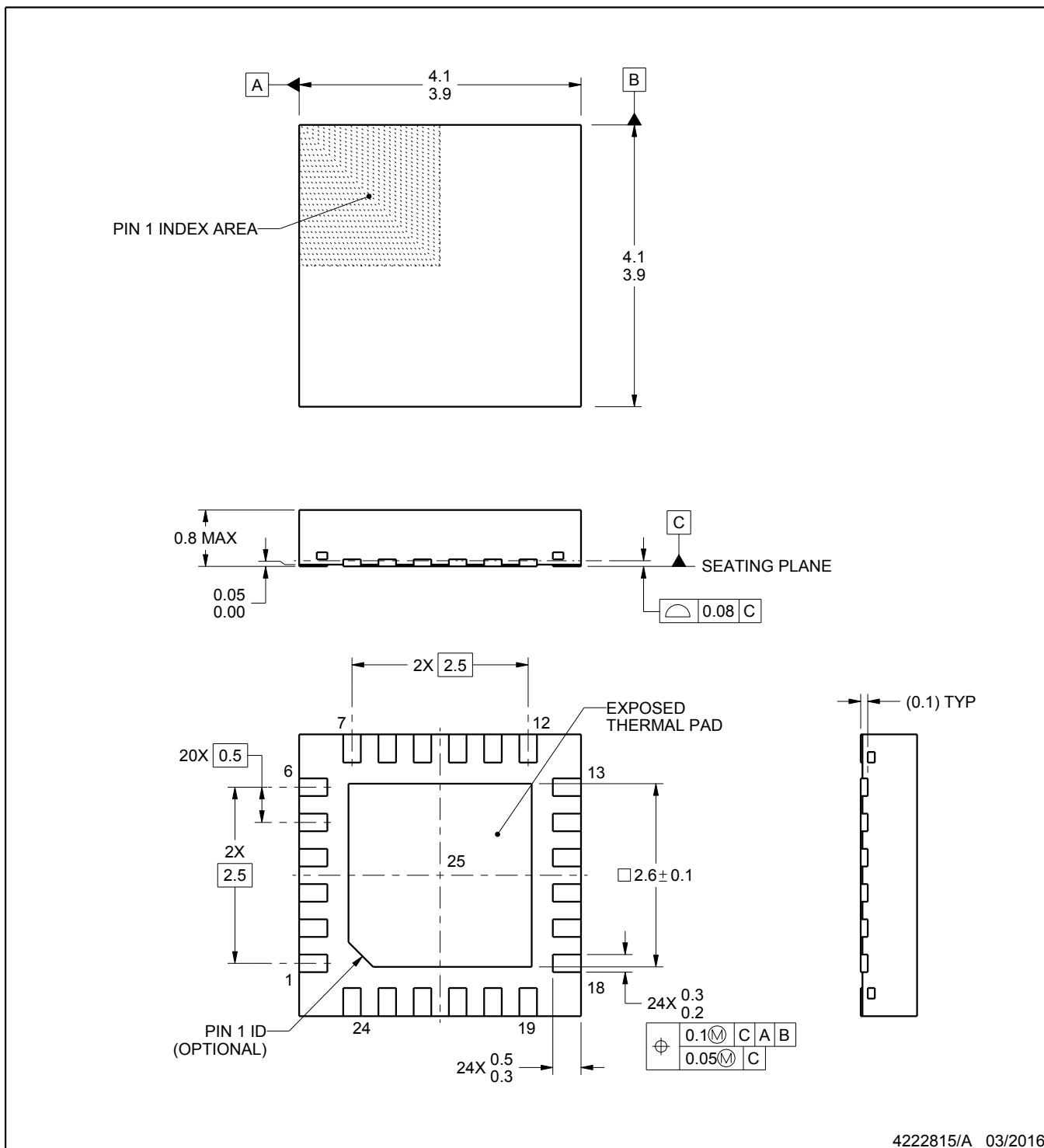


# PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222815/A 03/2016

## NOTES:

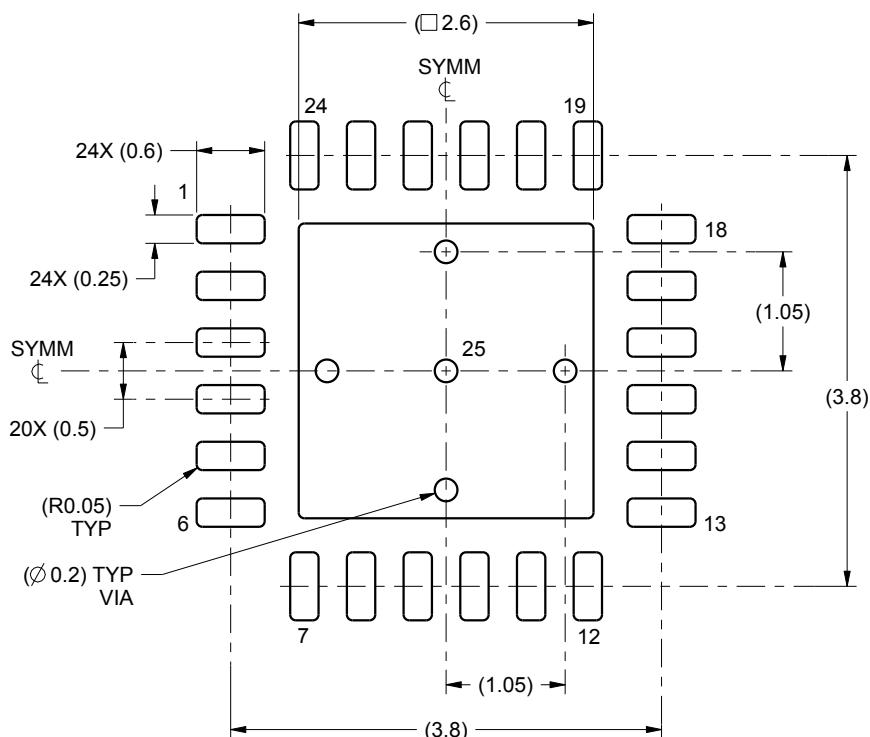
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**RTW0024A**

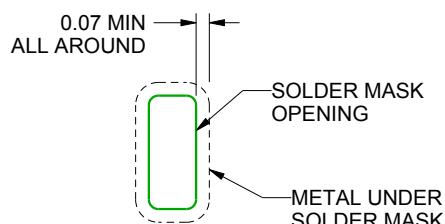
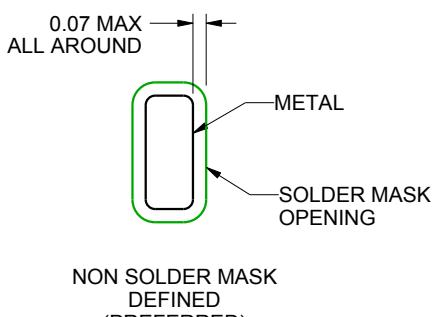
### **WQFN - 0.8 mm max height**

#### PLASTIC QUAD FLATPACK - NO LEAD



## LAND PATTERN EXAMPLE

SCALE:15X



## SOLDER MASK DETAILS

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#### NOTES: (continued)

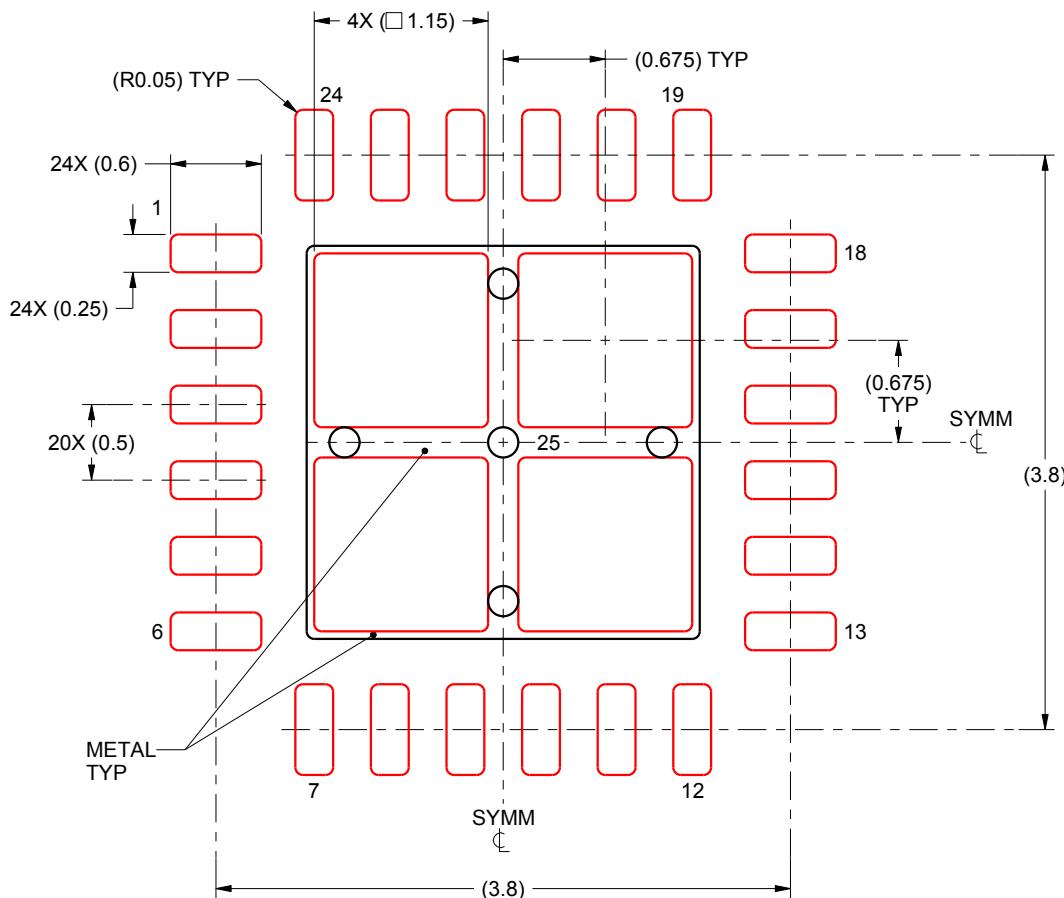
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

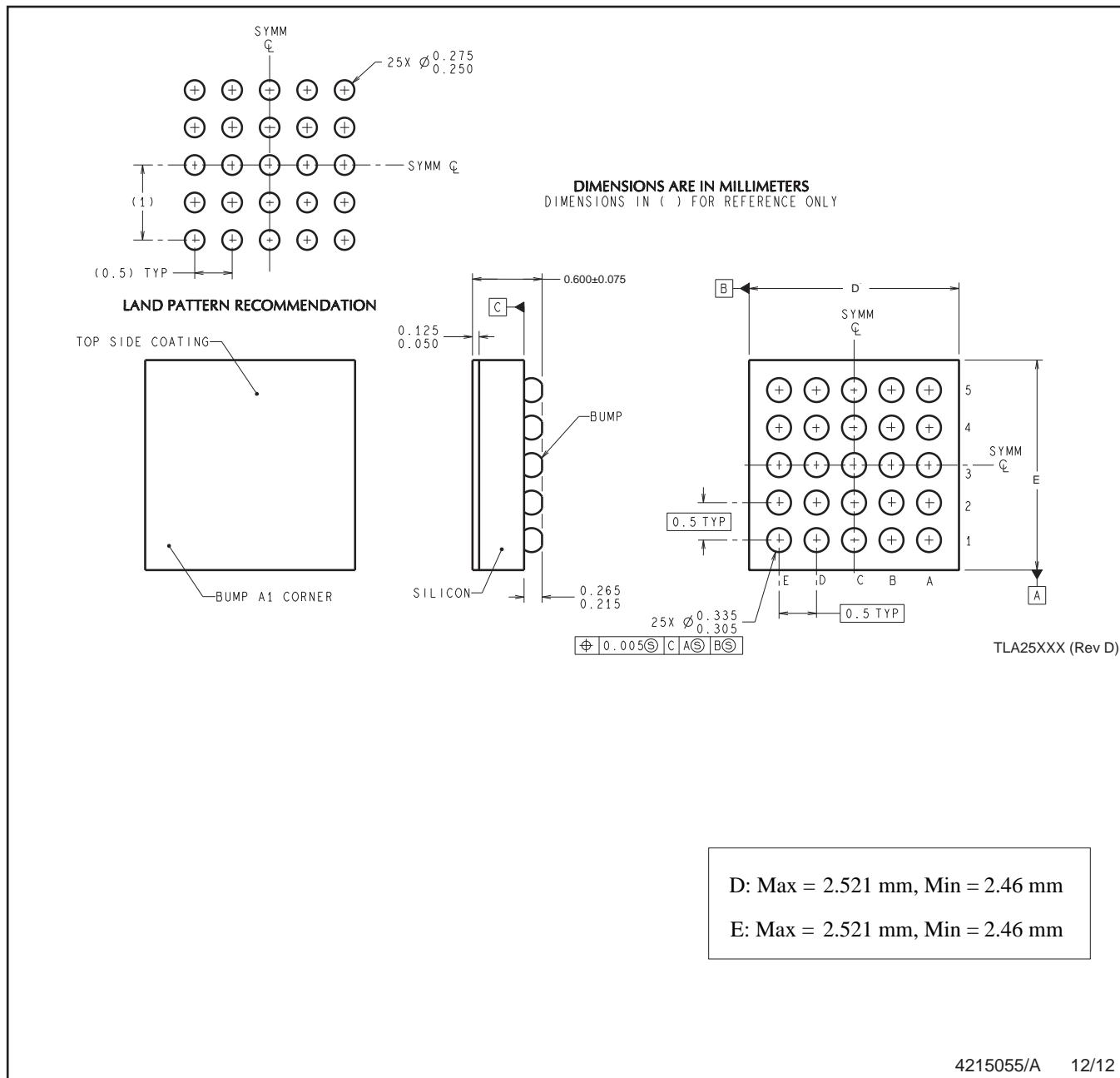
EXPOSED PAD 25:  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YZR0025



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.

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最后更新日期：2025 年 10 月