

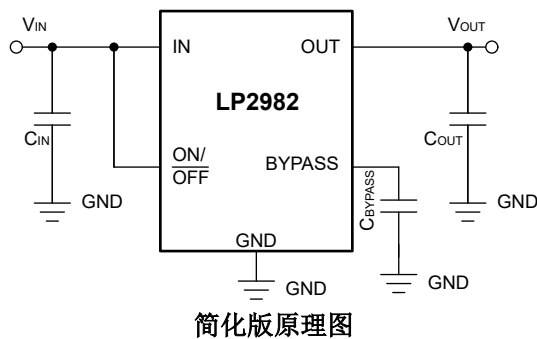
LP2982 采用 SOT-23 封装的 50mA 低噪声低压降稳压器

1 特性

- V_{IN} 范围 (新芯片) : 2.5V 至 16V
- V_{OUT} 范围 (新芯片) : 1.2V 至 5.0V
- V_{OUT} 精度 :
 - A 级 (旧芯片) 为 $\pm 1\%$
 - 标准级 (旧芯片) 为 $\pm 1.5\%$
 - $\pm 0.5\%$ (新芯片)
- 在整个负载和温度范围内的输出精度为 $\pm 1\%$ (新芯片)
- 输出电流 : 高达 50mA
- 低 I_Q (新芯片) : $I_{LOAD} = 0mA$ 时为 $69 \mu A$
- 低 I_Q (新芯片) : $I_{LOAD} = 50mA$ 时为 $380 \mu A$
- 关断电流 :
 - $1 \mu A$ (适用于旧芯片)
 - $2.25 \mu A$ (适用于新芯片)
- 低噪声 : $30 \mu V_{RMS}$ (具有 10nF 旁路电容器)
- 输出电流限制和热保护
- 与 2.2 μF 陶瓷电容器搭配使用时可保持稳定 (新芯片)
- 高 PSRR : 1kHz 频率下为 70dB, 1MHz 频率下为 40dB
- 工作结温 : -40°C 至 +125°C
- 封装 : 5 引脚 SOT-23 (DBV)

2 应用

- 工厂自动化和控制
- 工业运输 (非汽车、非轻型卡车)
- 电网基础设施
- 医疗



3 说明

LP2982 是一款固定输出、宽输入、低噪声、低压降稳压器,支持 2.5V 至 16V (对于新芯片) 的输入电压范围和高达 50mA 的负载电流。LP2982 支持 1.2V 至 5.0V 的输出范围 (新芯片)。

此外,LP2982 (新芯片) 在整个负载和温度范围内具有 $\pm 1\%$ 的输出精度,可满足低压微控制器 (MCU) 和处理器的需求。

30 μV_{RMS} 的低输出噪声 (带 10nF 旁路电容器) 以及 1kHz 时大于 70dB 和 1MHz 时大于 40dB 的宽带宽 PSRR 性能有助于衰减上游直流/直流转换器的开关频率,并尽可能减少后置稳压器滤波。

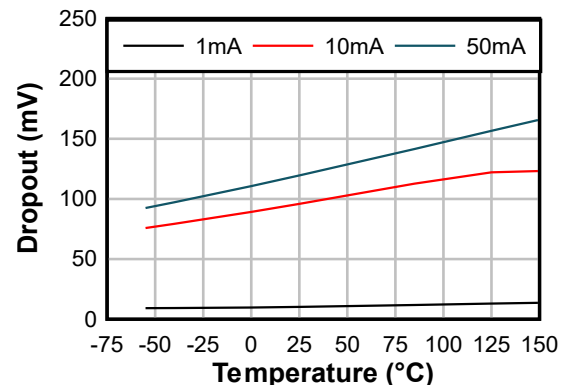
在新芯片中,内部软启动机制可减小启动期间的浪涌电流,从而最大限度降低输入电容。还包括标准保护特性,例如过流和过热保护。

LP2982 采用 5 引脚、2.9mm × 2.8mm SOT-23 (DBV) 封装。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
LP2982	DBV (SOT-23, 5)	2.9mm × 2.8mm

- (1) 如需更多信息,请参阅 [机械、封装和可订购信息](#)。
 (2) 封装尺寸 (长 × 宽) 为标称值,并包括引脚 (如适用)。



压降电压与温度间的关系 (新芯片)



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4 Pin Configuration and Functions

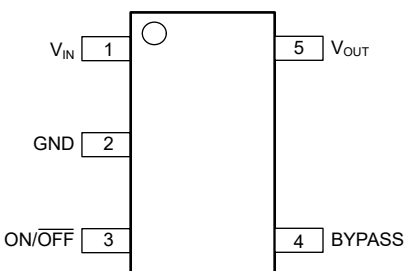


图 4-1. DBV Package, 5-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between BYPASS pin and ground reduces reference voltage noise. See the Recommended Operating Conditions section for more information.
GND	2	—	Ground
ON/OFF	3	I	Enable pin for the LDO. Driving the ON/OFF pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the Electrical Characteristics table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 μF or larger from this pin to ground. See the Input Capacitor Requirements section for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 2.2 μF or larger from this pin to ground. See the Input Capacitor Requirements section for more information. ⁽¹⁾

- (1) The nominal output capacitor for the new chip must be greater than 2.2 μF . Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 μF .

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	- 0.3	16	V
	Continuous input voltage range (for new chip)	- 0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	- 0.3	9	
	Output voltage range (for new chip)	- 0.3	$V_{IN} + 0.3$ or 9 (whichever is smaller)	
$V_{ON/OFF}$	ON/OFF pin voltage range (for legacy chip)	- 0.3	16	
	ON/OFF pin voltage range (for new chip)	- 0.3	18	
$V_{IN} - V_{OUT}$	Input-output voltage (for legacy chip)	- 0.3	16	
	Input-output voltage (for new chip)	- 0.3	18	
Current	Maximum output current	Internally limited		mA
Temperature	Operating junction, T_J	- 55	150	°C
	Storage, T_{stg}	- 65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages with respect to GND.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (Pin 1,2 and 5) ⁽¹⁾	±2000	±3000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (Pin 3 and 4) ⁽¹⁾	±1000		
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	N/A		

- (1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.1		16	V
	Supply input voltage (for new chip)	2.5		16	
$V_{IN} - V_{OUT}$	Input-output differential (for legacy chip)	0.7		11	
	Input-output differential (for new chip)	0		16	
V_{OUT}	Output voltage (for new chip)	1.2		5	
$V_{ON/OFF}$	Enable voltage (for legacy chip)	0		V_{IN}	
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		50	mA
$C_{IN}^{(1)}$	Input capacitor		1		μF
C_{OUT}	Output capacitor (for legacy chip)	2.2	4.7		
	Output capacitance (for new chip) ⁽¹⁾	1	2.2	200	
$C_{OUT} \text{ ESR}^{(2)}$	Output capacitor ESR (for new chip) ⁽³⁾	0		1	Ω
T_J	Operating junction temperature	- 40		125	$^{\circ}C$

- (1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 μF minimum for stability.
- (2) Maximum supported ESR range for new chip is 1 Ω . For output capacitor with higher ESR values, place a low ESR MLCC capacitor.
- (3) Details related to supported ESR range for the legacy chip are available in *Recommended Capacitors (Legacy Chip)*.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		Legacy Chip ⁽²⁾	New Chip ⁽²⁾	UNIT
		DBV (SOT23-5)	DBV (SOT23-5)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.7	178.6	$^{\circ}C/W$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.8	77.9	$^{\circ}C/W$
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	47.2	$^{\circ}C/W$
Ψ_{JT}	Junction-to-top characterization parameter	16.1	15.9	$^{\circ}C/W$
Ψ_{JB}	Junction-to-board characterization parameter	29.0	46.9	$^{\circ}C/W$

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the [Impact of board layout on LDO thermal performance](#) application report.

5.5 Electrical Characteristics

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	$I_L = 1\text{ mA}$	Legacy chip (standard grade)	- 1.5		1.5	%
			Legacy chip (A grade)	- 1.0		1.0	
			New chip	- 0.5		0.5	
		$1\text{ mA} < I_L < 50\text{ mA}$	Legacy chip (standard grade)	- 2		2	
			Legacy chip (A grade)	- 1.5		1.5	
			New chip	- 0.5		0.5	
		$1\text{ mA} < I_L < 50\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip (standard grade)	- 3.5		3.5	
			Legacy chip (A grade)	- 2		2	
			New chip	- 1		1	
$\Delta V_{OUT}(\Delta V_{IN})$	Line regulation	$V_{O(NOM)} + 1\text{ V} < V_{IN} < 16\text{ V}$	Legacy chip		0.007	0.014	%/V
			New chip		0.002	0.014	
		$V_{O(NOM)} + 1\text{ V} < V_{IN} < 16\text{ V}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip		0.007	0.032	
			New chip		0.002	0.032	
$\Delta V_{OUT}(\Delta I_{LOAD})$	Load regulation	$1\text{ mA} < I_L < 50\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 0.5\text{ V}$	New chip		0.1	0.5	%/A
V_{DO}	Dropout voltage	$I_{OUT} = 0\text{ mA}$	Legacy chip		1	3	mV
			New chip		1	2.75	
		$I_{OUT} = 0\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			5	
			New chip			3	
		$I_{OUT} = 1\text{ mA}$	Legacy chip		7	10	
			New chip		11.5	14	
		$I_{OUT} = 1\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			15	
			New chip			17	
		$I_{OUT} = 10\text{ mA}$	Legacy chip		40	60	
			New chip		98	115	
		$I_{OUT} = 10\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			90	
			New chip			148	
		$I_{OUT} = 50\text{ mA}$	Legacy chip		120	150	
			New chip		120	145	
		$I_{OUT} = 50\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			225	
			New chip			184	
		$I_{OUT} = 80\text{ mA}$	Legacy chip		180	225	
			New chip		150	165	
		$I_{OUT} = 80\text{ mA}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			325	
			New chip			204	

5.5 Electrical Characteristics (续)

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{GND}	GND pin current	I _{OUT} = 0 mA	Legacy chip		65	95	μA
			New chip		69	95	
		I _{OUT} = 0 mA, - 40°C ≤ T _J ≤ 125°C	Legacy chip			125	
			New chip			123	
		I _{OUT} = 1 mA	Legacy chip		80	110	
			New chip		78	110	
		I _{OUT} = 1 mA, - 40°C ≤ T _J ≤ 125°C	Legacy chip			170	
			New chip			140	
		I _{OUT} = 10 mA	Legacy chip		140	220	
			New chip		175	210	
		I _{OUT} = 10 mA, - 40°C ≤ T _J ≤ 125°C	Legacy chip			460	
			New chip			250	
		I _{OUT} = 50 mA	Legacy chip		375	600	
			New chip		380	440	
		I _{OUT} = 50 mA, - 40°C ≤ T _J ≤ 125°C	Legacy chip			1200	
			New chip			650	
		I _{OUT} = 80 mA	Legacy chip		525	750	
			New chip		575	720	
		I _{OUT} = 80 mA, - 40°C ≤ T _J ≤ 125°C	Legacy chip			1400	
						900	
		V _{ON/OFF} < 0.3 V, V _{IN} = 16 V	Legacy chip		0.01	0.8	
			New chip		1.25	1.75	
		V _{ON/OFF} < 0.15 V, V _{IN} = 16 V, - 40°C ≤ T _J ≤ 125°C	Legacy chip		0.1	2	
			New chip		1.12	2.75	
V _{UVLO+}	Rising bias supply UVLO	V _{IN} rising, - 40°C ≤ T _J ≤ 125°C	New chip		2.2	2.4	V
V _{UVLO-}	Falling bias supply UVLO	V _{IN} falling, - 40°C ≤ T _J ≤ 125°C		1.9			V
V _{UVLO(HYST)}	UVLO hysteresis	- 40°C ≤ T _J ≤ 125°C			0.130		V
I _{O(MAX)}	Short Output Current	R _L = 0 Ω (steady state)	Legacy chip		150		mA
			New chip		150		mA
I _{O(PK)}	Peak Output Current	V _{OUT} ≥ V _{O(NOM)} - 5% (steady state)	Legacy chip	100	150		mA
			New chip	100	150		mA
V _{ON/OFF}	ON/OFF input voltage	Low = Output OFF	Legacy chip		0.55		
			New chip		0.72		
		Low = Output OFF, V _{OUT} + 1 < V _{IN} < 16 V, - 40°C ≤ T _J ≤ 125°C	Legacy chip			0.15	
			New chip			0.15	
		High = Output ON	Legacy chip		1.4		
			New chip		0.85		
		High = Output ON, V _{OUT} + 1 < V _{IN} < 16 V, - 40°C ≤ T _J ≤ 125°C	Legacy chip		1.6		
			New chip		1.6		

5.5 Electrical Characteristics (续)

specified at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1.0\text{ V}$ or $V_{IN} = 2.5\text{ V}$ (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{ON/OFF} = 2\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{ON/OFF}$	ON/OFF input current	$V_{ON/OFF} = 0\text{ V}$	Legacy chip		0.01		μA
			New chip		0.42		
		$V_{ON/OFF} = 0\text{ V}$, $V_{OUT} + 1 < V_{IN} < 16\text{ V}$, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	Legacy chip			-2	μA
			New chip			-0.9	
		$V_{ON/OFF} = 5\text{ V}$	Legacy chip		5		μA
			New chip		0.011		
$\Delta V_O / \Delta V_{IN}$	Ripple rejection	$f = 1\text{ kHz}$, $C_{BYPASS} = 10\text{ nF}$, $C_{OUT} = 10\text{ }\mu\text{F}$ $f = 100\text{ kHz}$, $C_{BYPASS} = 10\text{ nF}$, $I_{LOAD} = 50\text{ mA}$	Legacy chip		45		dB
			New chip		78		
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, $C_{NR/SS} = 10\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $V_{OUT} = 1.8\text{ V}$, $I_{LOAD} = 150\text{ mA}$ Bandwidth = 10 Hz to 100 kHz, $C_{NR/SS} = 10\text{ nF}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $V_{OUT} = 3.3\text{ V}$, $I_{LOAD} = 150\text{ mA}$	Legacy chip		30		μVRMS
			New chip		30	50	
T_{sd+}	Thermal shutdown threshold	Shutdown, temperature increasing	New chip		170		$^\circ\text{C}$
T_{sd-}		Reset, temperature decreasing			150		

5.6 Typical Characteristics

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

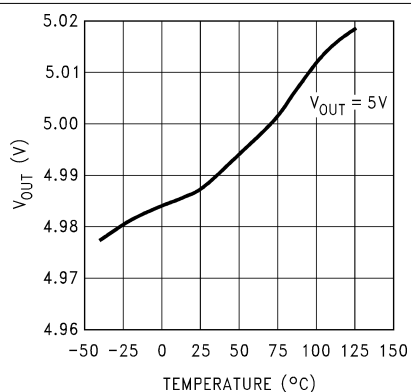


图 5-1. Output Voltage vs Temperature (Legacy Chip)

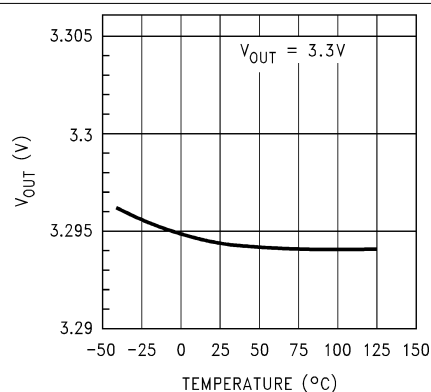


图 5-2. Output Voltage vs Temperature (Legacy Chip)

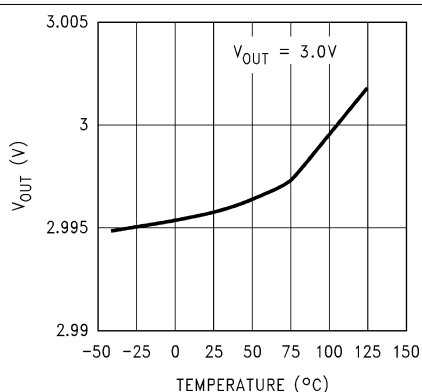


图 5-3. Output Voltage vs Temperature (Legacy Chip)

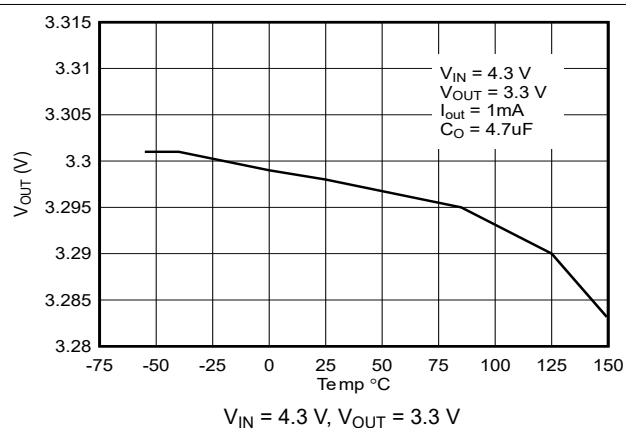


图 5-4. Output Voltage vs Temperature (New Chip)

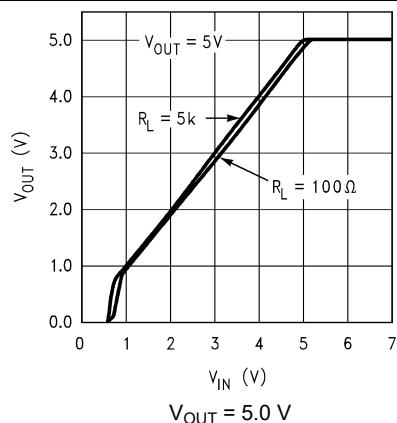


图 5-5. Output Voltage vs V_{IN} (Legacy Chip)

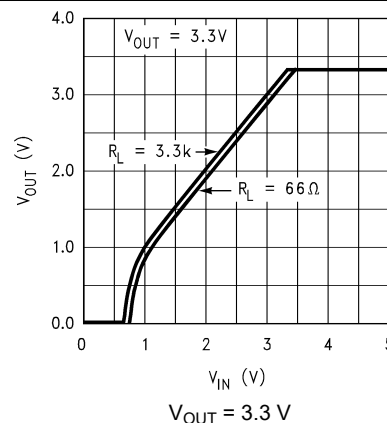


图 5-6. Output Voltage vs V_{IN} (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

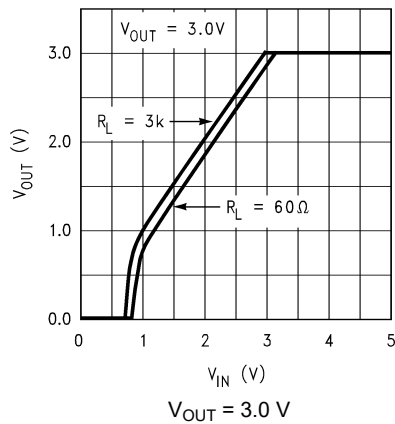


图 5-7. Output Voltage vs V_{IN} (Legacy Chip)

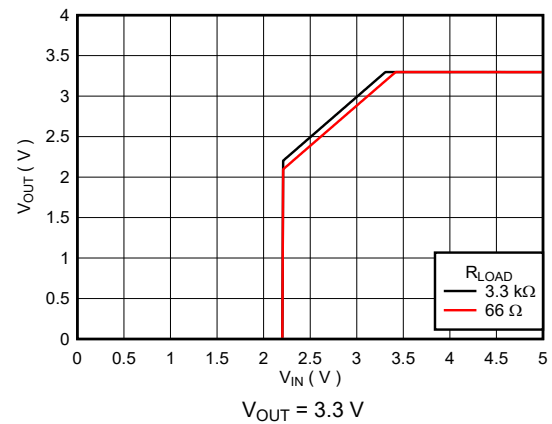


图 5-8. Output Voltage vs V_{IN} (New Chip)

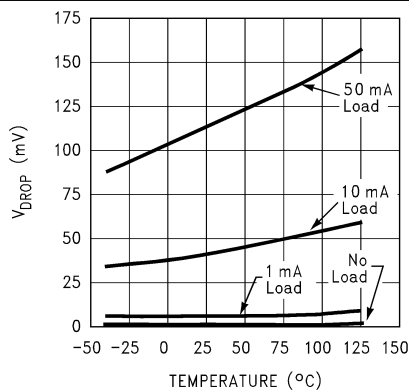


图 5-9. Dropout Voltage vs Temperature (Legacy Chip)

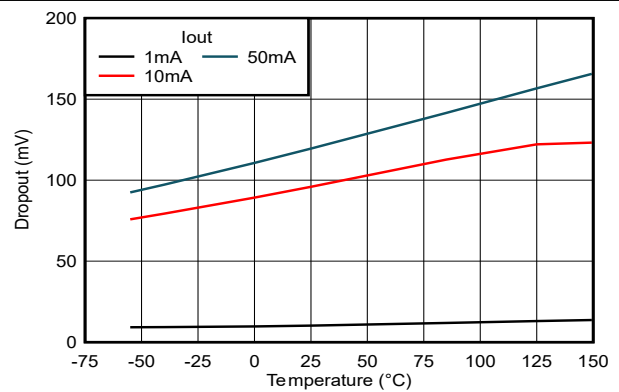


图 5-10. Dropout Voltage vs Temperature (New Chip)

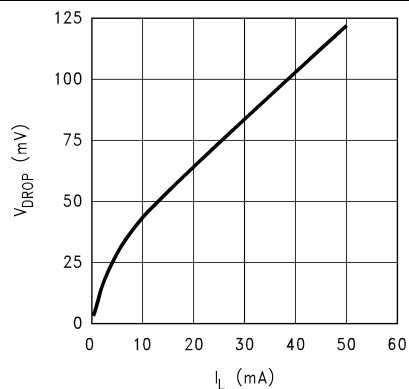


图 5-11. Dropout Voltage vs Load Current (Legacy Chip)

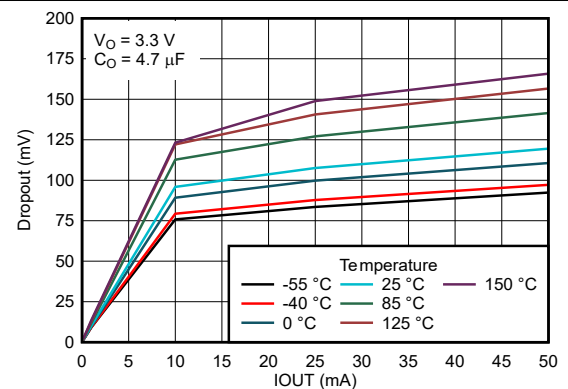


图 5-12. Dropout Voltage vs Load Current (New Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

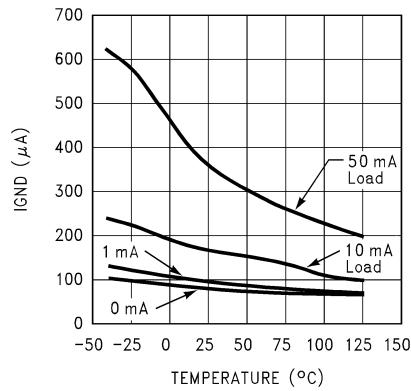


图 5-13. Ground Pin Current vs Temperature (Legacy Chip)

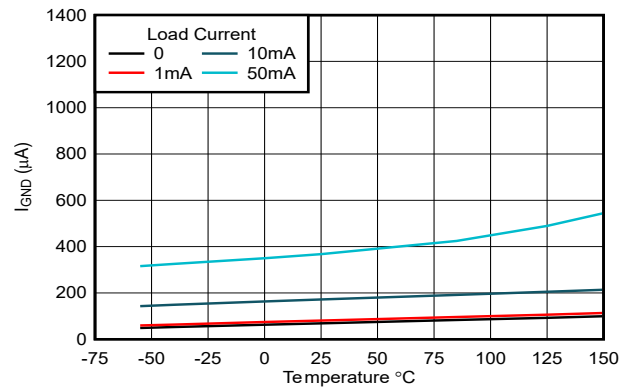


图 5-14. Ground Pin Current vs Temperature (New Chip)

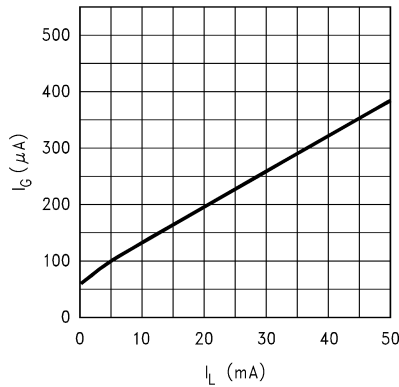


图 5-15. Ground Pin Current vs Load Current (Legacy Chip)

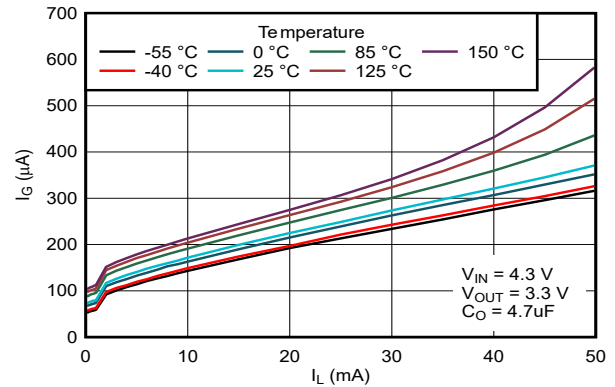


图 5-16. Ground Pin Current vs Load Current (New Chip)

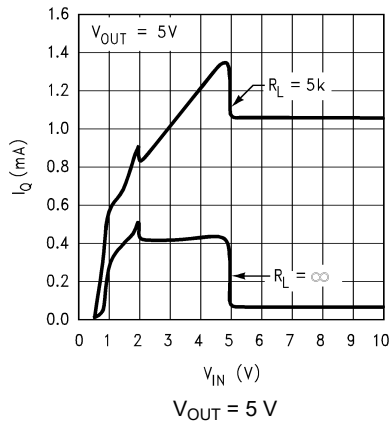


图 5-17. Input Current vs V_{IN} (Legacy Chip)

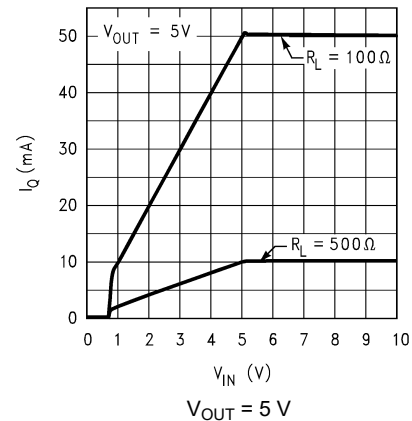


图 5-18. Input Current vs V_{IN} (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

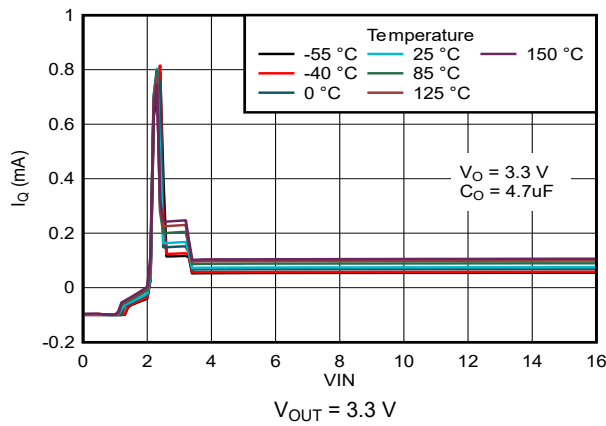


图 5-19. Input Current vs Input Voltage (New Chip)

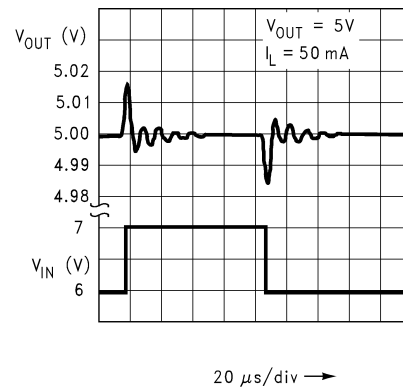


图 5-20. Line Transient Response (Legacy Chip)

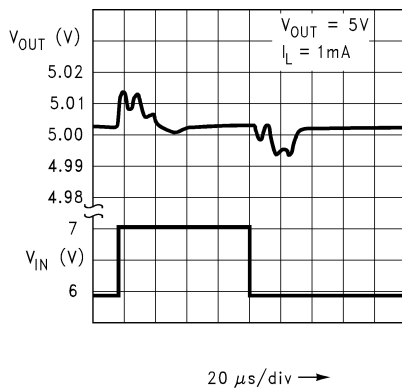
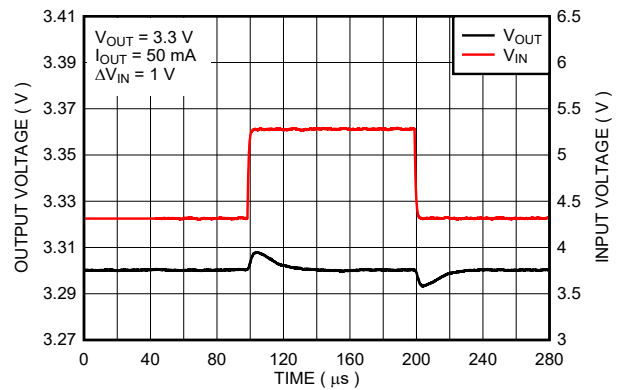


图 5-21. Line Transient Response (Legacy Chip)



$V_{OUT} = 3.3\text{ V}$, $\Delta V_{IN} = 1\text{ V}$, $I_{OUT} = 50\text{ mA}$, $dV/dt = 1\text{ V}/\mu\text{s}$

图 5-22. Line Transient Response (New Chip)

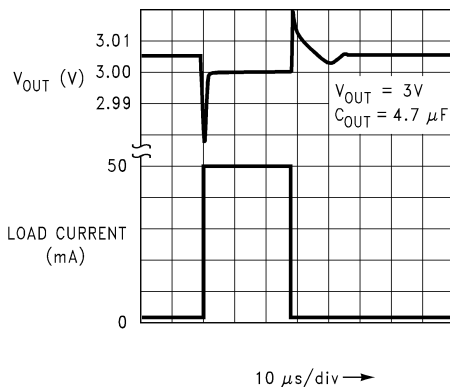


图 5-23. Load Transient Response (Legacy Chip)

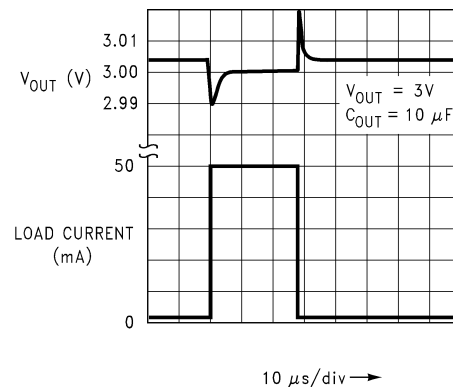


图 5-24. Load Transient Response (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

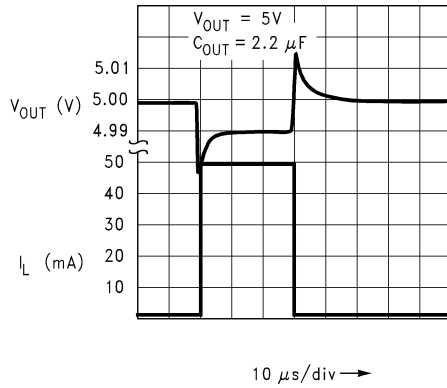


图 5-25. Load Transient Response (Legacy Chip)

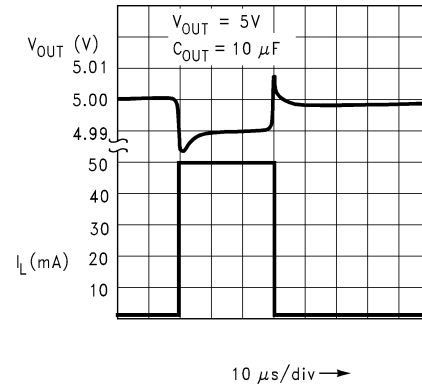


图 5-26. Load Transient Response (Legacy Chip)

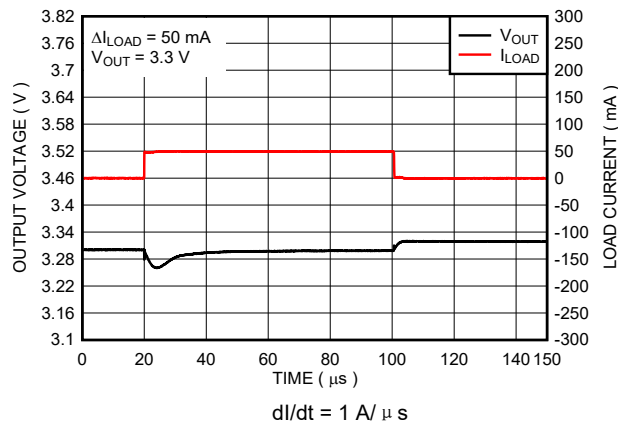


图 5-27. Load Transient Response (New Chip)

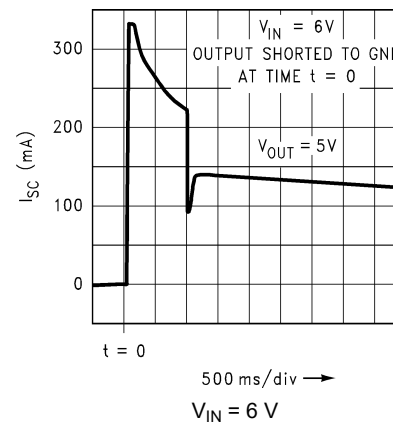


图 5-28. Short-Circuit Current vs Time (Legacy Chip)

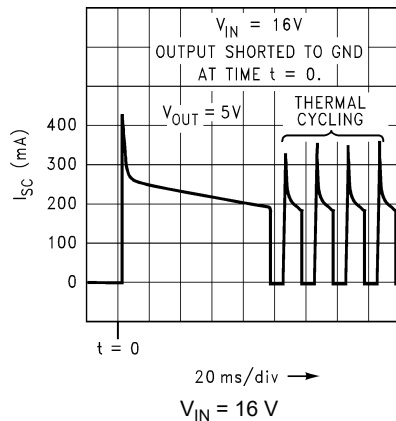


图 5-29. Short-Circuit Current vs Time (Legacy Chip)

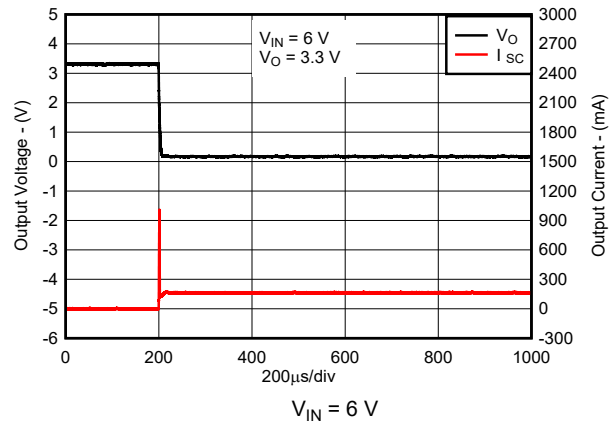


图 5-30. Short-Circuit Current vs Time (New Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

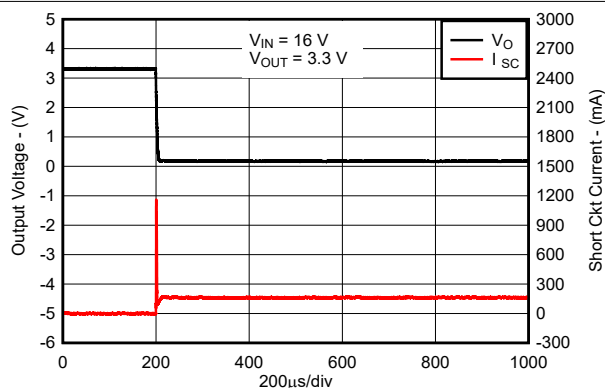


图 5-31. Short-Circuit Current vs Time (New Chip)

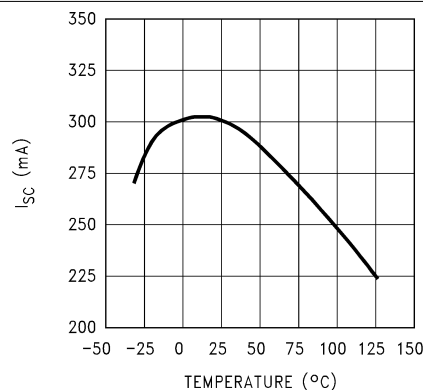


图 5-32. Instantaneous Short-Circuit Current vs Temperature (Legacy Chip)

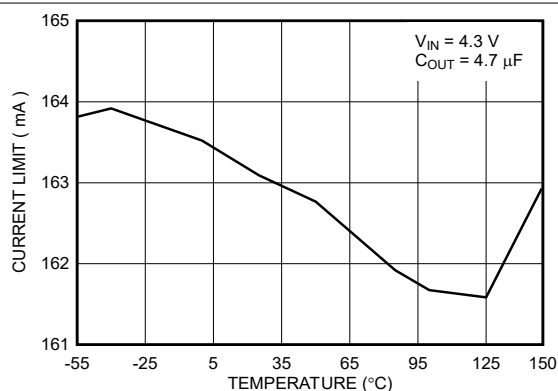


图 5-33. Short-Circuit Current vs Temperature (New Chip)

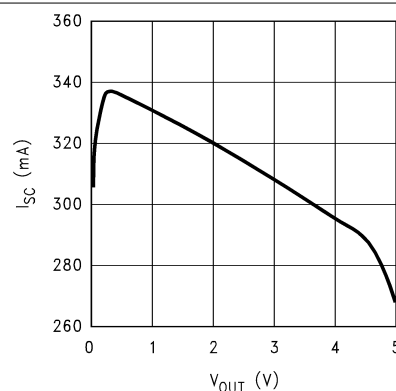


图 5-34. Instantaneous Short-Circuit Current vs Output Voltage (Legacy Chip)

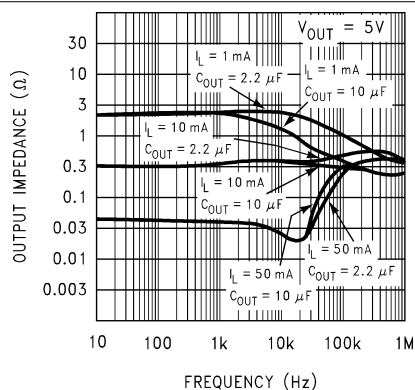


图 5-35. Output Impedance vs Frequency (Legacy Chip)

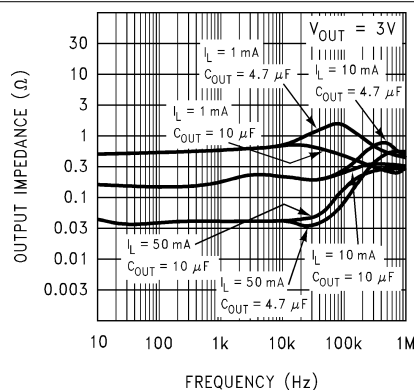


图 5-36. Output Impedance vs Frequency (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

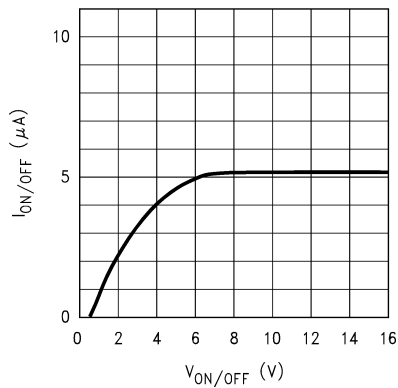


图 5-37. ON/OFF Pin Current vs $V_{ON/OFF}$ (Legacy Chip)

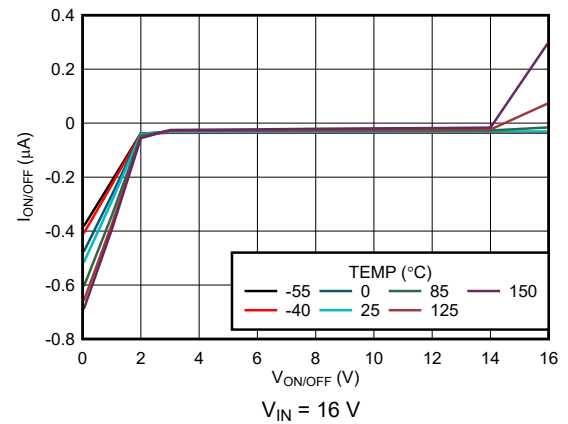


图 5-38. ON/OFF Pin Current vs $V_{ON/OFF}$ (New Chip)

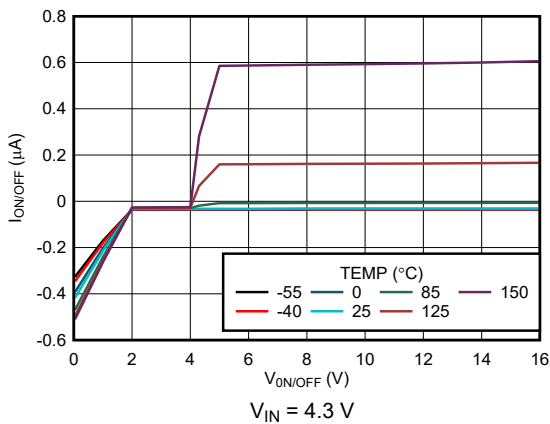


图 5-39. ON/OFF Pin Current vs $V_{ON/OFF}$ (New Chip)

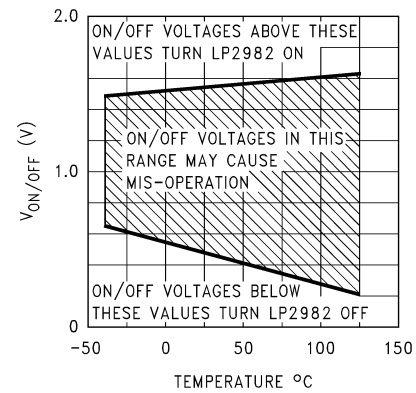


图 5-40. ON/OFF Threshold vs Temperature (Legacy Chip)

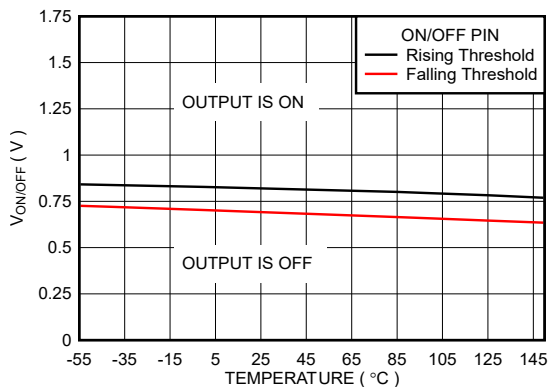


图 5-41. ON/OFF Threshold vs Temperature (New Chip)

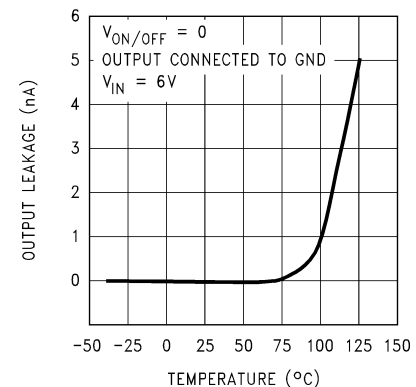


图 5-42. Input-to-Output Leakage vs Temperature (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

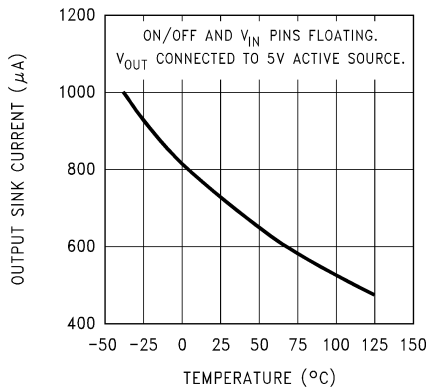


图 5-43. Output Reverse Leakage vs Temperature (Legacy Chip)

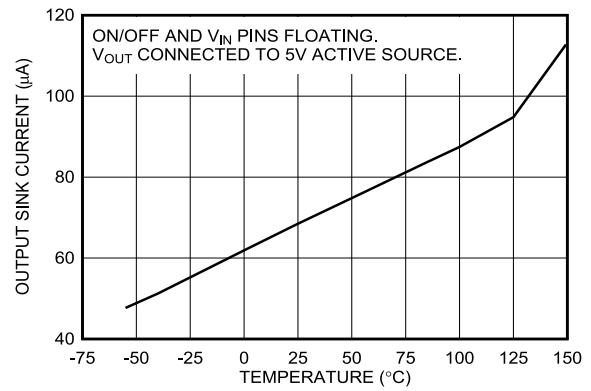


图 5-44. Output Reverse Leakage vs Temperature (New Chip)

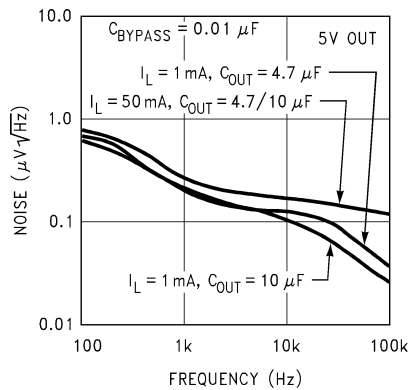


图 5-45. Output Noise Density (Legacy Chip)

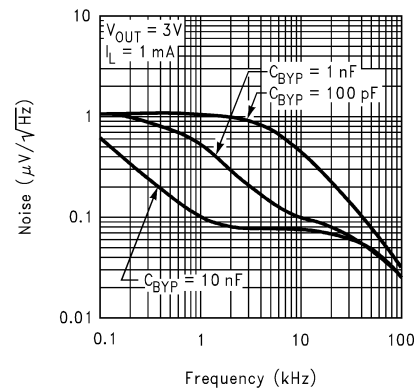


图 5-46. Output Noise Density (Legacy Chip)

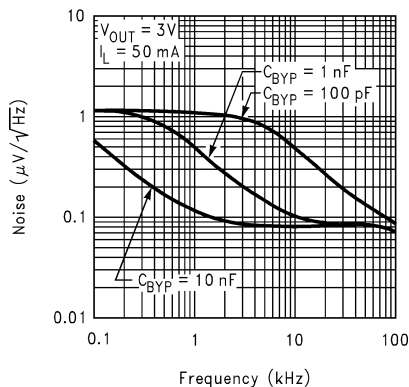


图 5-47. Output Noise Density (Legacy Chip)

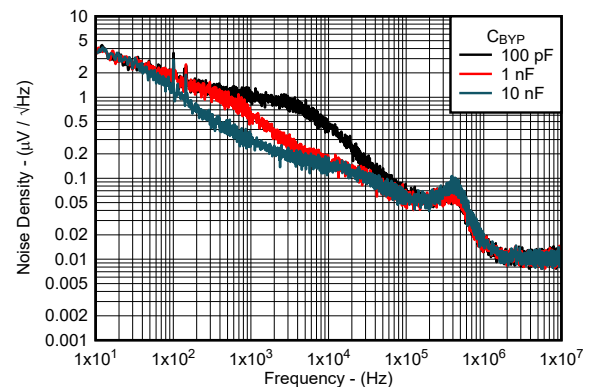


图 5-48. Output Noise Density vs Frequency (New Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

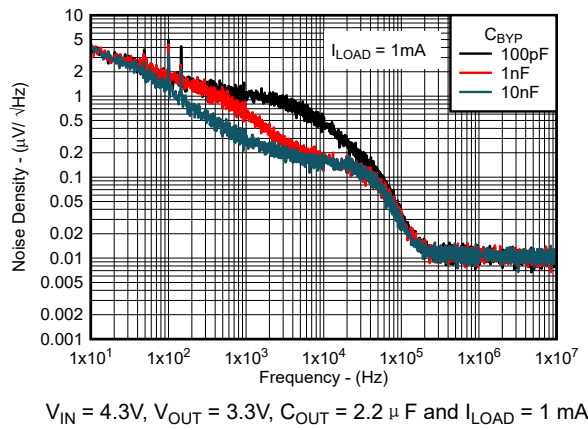


图 5-49. Output Noise Density vs Frequency (New Chip)

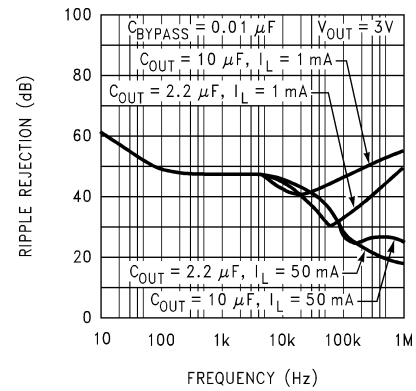


图 5-50. Ripple Rejection (Legacy Chip)

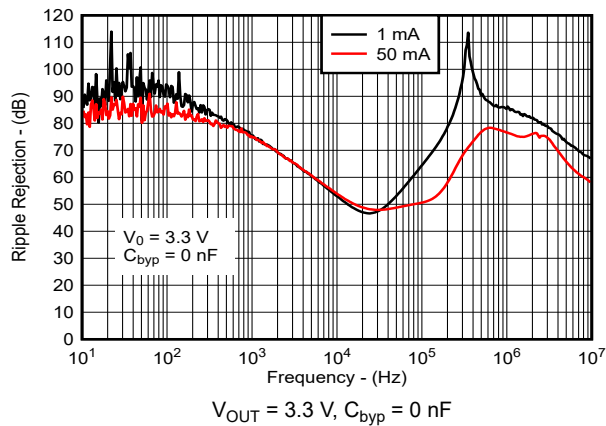


图 5-51. Ripple Rejection vs I_{OUT} (New Chip)

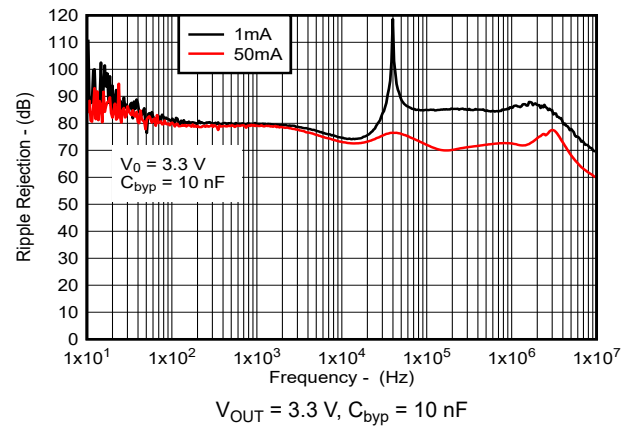


图 5-52. Ripple Rejection vs I_{OUT} (New Chip)

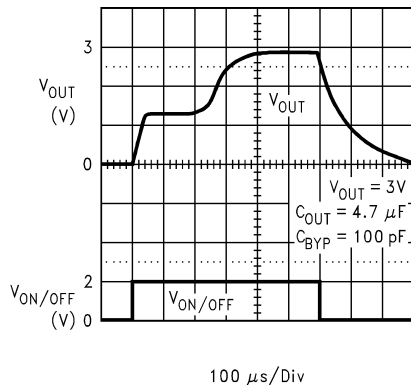


图 5-53. Turnon Waveform (Legacy Chip)

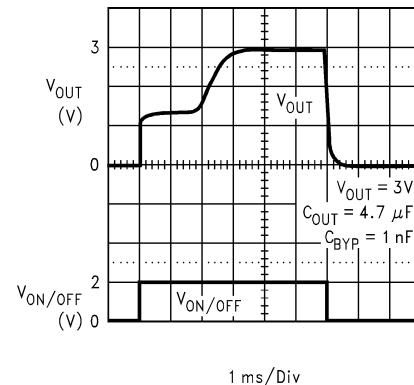


图 5-54. Turnon Waveform (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_{IN} = V_{O(NOM)} + 1\text{ V}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, all voltage options, ON/ OFF pin tied to V_{IN} .

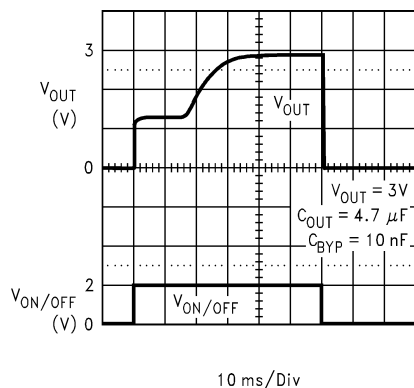


图 5-55. Turnon Waveform (Legacy Chip)

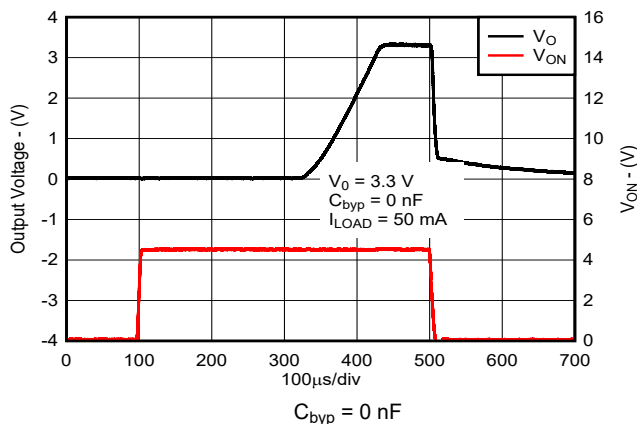


图 5-56. Turnon Waveform (New Chip)

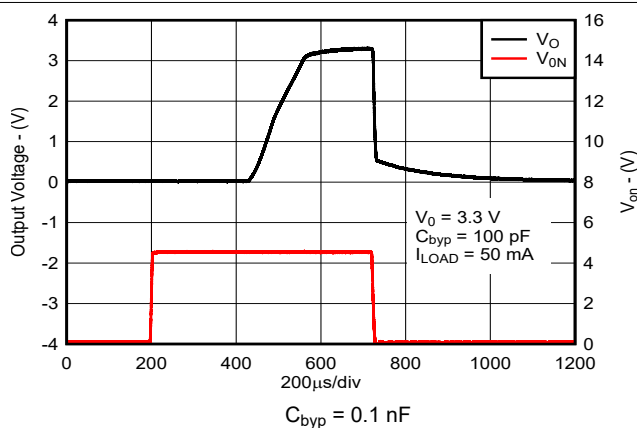


图 5-57. Turnon Waveform (New Chip)

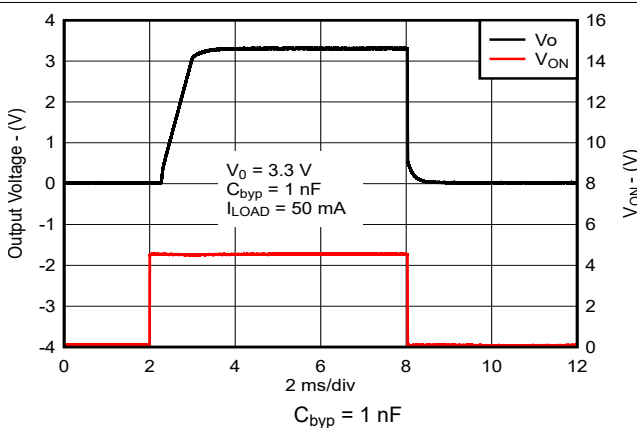


图 5-58. Turnon Waveform (New Chip)

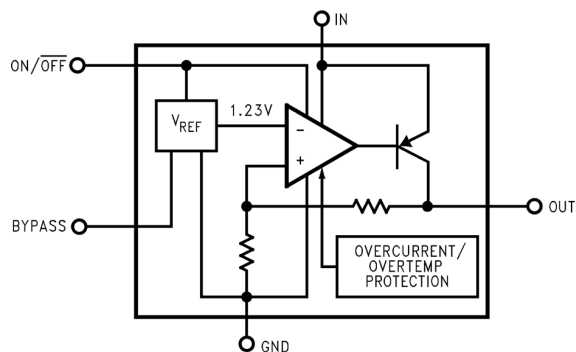
6 Detailed Description

6.1 Overview

The LP2982 is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2982 has an output tolerance of $\pm 1\%$ across load, and temperature variation (new chip) and is capable of delivering 50 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown and output enable. The new chip version of the LP2982 also features internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is -40°C to $+125^{\circ}\text{C}$.

6.2 Functional Block Diagrams



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图 6-1. Functional Block Diagram (Legacy Chip)

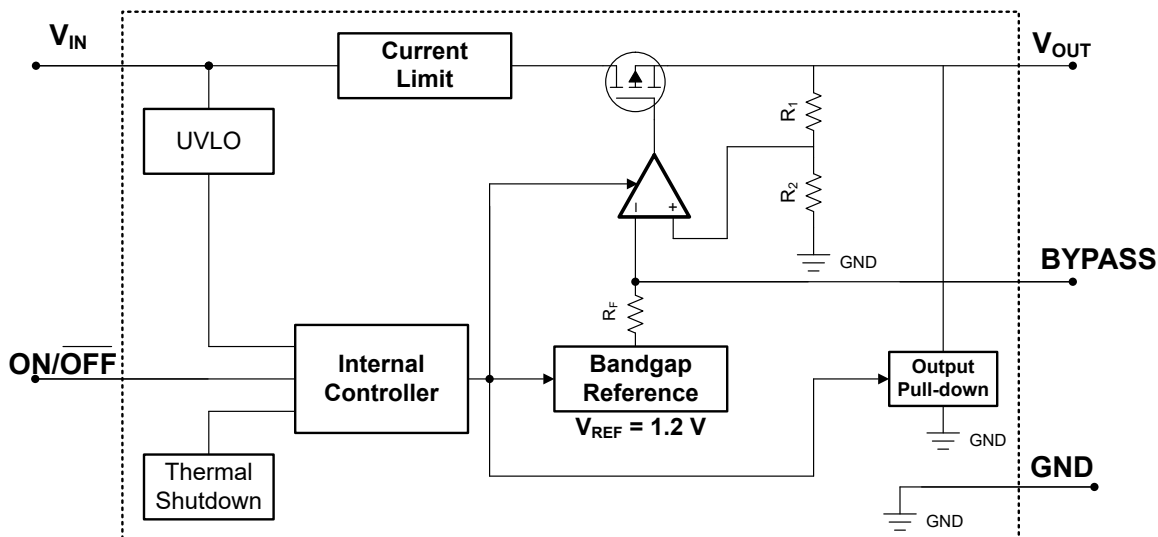


图 6-2. Functional Block Diagram (New Chip)

6.3 Feature Description

6.3.1 Output Enable

The ON/OFF pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/OFF pin is greater than the high-level input voltage of the ON/OFF pin and disabled with the ON/OFF pin voltage is less than the low-level input voltage of the ON/OFF pin. If independent control of the output voltage is not needed, connect the ON/OFF pin to the input of the device.

The new chip version of the device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/OFF pin voltage lower than the low-level input voltage of the ON/OFF pin, to actively discharge the output voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the [Recommended Operating Conditions](#) table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

For the legacy chip, the internal current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If V_{OUT} is forced below 0 V before ON/OFF goes high, and the load current required exceeds the foldback current limit, the device may not start up correctly.

For the new chip, the device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the [Electrical Characteristics](#) table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application note](#).

图 6-3 shows a diagram of the current limit.

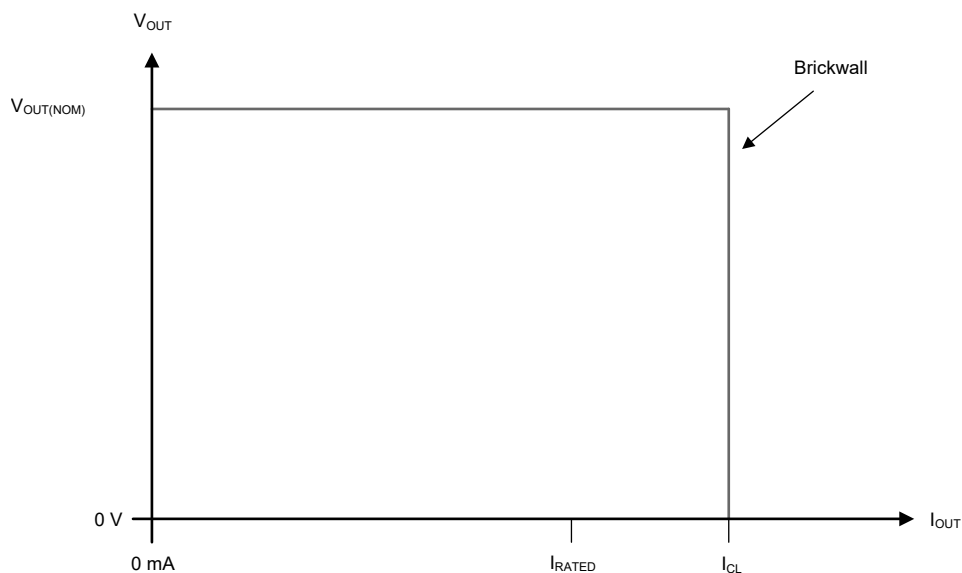


图 6-3. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The new chip version of the device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the [Electrical Characteristics](#) table.

6.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/OFF} < V_{ON/OFF(LOW)}$)
- If $1.0\text{ V} < V_{IN} < V_{UVLO}$

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the [Reverse Current](#) section for more details.

6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis enables the device to reset (turns on) when the temperature falls to $T_{SD(reset)}$ (typical). Thermal shutdown circuit limits are defined in [Electrical Characteristics](#) section.

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the [Recommended Operating Conditions](#) table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

[Device Functional Mode Comparison](#) shows the conditions that lead to the different modes of operation. See the [Electrical Characteristics](#) table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/OFF}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/OFF} > V_{ON/OFF(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/OFF} > V_{ON/OFF(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/OFF} < V_{ON/OFF(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/OFF voltage has previously exceeded the ON/OFF rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/OFF pin to less than the maximum ON/OFF pin low-level input voltage (see the [Electrical Characteristics](#) table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The LP2982 is a linear voltage regulator operating from 2.5 V to 16 V (for new chip) on the input and regulates voltages between 1.2 V to 5 V with $\pm 1\%$ accuracy (across load and temperature) and 50-mA maximum output current.

Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified for a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

7.1.1 Recommended Capacitor Types

7.1.1.1 Recommended Capacitors (Legacy Chip)

Tantalum Capacitors: Tantalum capacitors are the best choice for use with the LP2982. Most good quality tantalums can be used with the LP2982, but check the manufacturer's data sheet to be sure the ESR is in range. As the ESR increases at lower temperatures and a capacitor that is near the upper limit for stability at room temperature can cause instability when temperature gets cold.

In applications which must operate at very low temperatures, the output tantalum capacitor needs to be placed in parallel with a ceramic capacitor to prevent the ESR from going up too high (see ceramic capacitors discussion in this section for important information on ceramic capacitors).

Ceramic Capacitors: TI does not recommend use of ceramic capacitors at the output of the LP2982. This is because the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2982. A $2.2\ \mu\text{F}$ ceramic was measured and found to have an ESR of about $15\text{m}\Omega$, which is low enough to cause oscillations. If a ceramic capacitor is used on the output, a $1\ \Omega$ resistor must be placed in series with the capacitor.

Aluminum Capacitors: Because of large physical size, aluminum electrolytics are not typically used with the LP2982. The aluminum capacitors must meet the same ESR requirements over the operating temperature range, more difficult because of the ESR steep increase at cold temperature. An aluminum electrolytic can exhibit an ESR increase of as much as $50\times$ when going from 20°C to -40°C . Also, some aluminum electrolytics are not operational below -25°C because the electrolyte can freeze.

7.1.1.2 Recommended Capacitors (New Chip)

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas using Y5V-rated capacitors is discouraged because of large variations in capacitance.

The maximum supported ESR range across complete temperature (-40°C to $+125^\circ\text{C}$) and load current range (0mA-50mA) is less than $1\ \Omega$. If in an existing implementation, where different type of capacitors with higher ESR are being used, place a low ESR MLCC capacitor with a value of 100nF, as close as possible to the output (V_{OUT}) pin of the LP2982.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output

capacitors listed in the [Recommended Operating Conditions](#) table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input Capacitor Requirements

For the legacy chip, an input capacitor with a value $\geq 1 \mu\text{F}$ is required with the LP2982 (amount of capacitance can be increased without limit). This capacitor must be located a distance of not more than 0.5 inches from the input pin of the LP2982 and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.

For the new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω . A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

7.1.3 Output Capacitor Requirements

For the legacy chip, the output capacitor must meet both the requirement for minimum amount of capacitance and equivalent series resistance (ESR) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (see [图 7-1](#) and [图 7-2](#)).

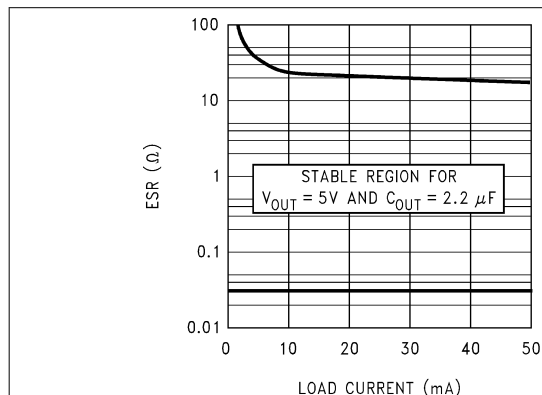


图 7-1. 5-V, 2.2- μF ESR Curves (Legacy Chip)

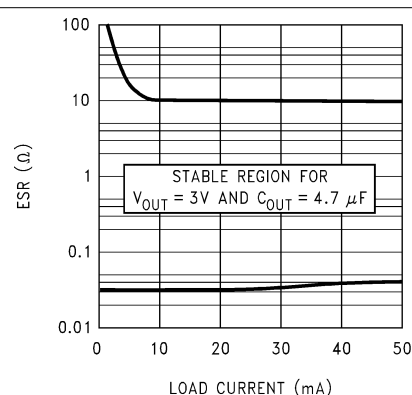


图 7-2. 3-V, 4.7- μF ESR Curves (Legacy Chip)

备注

The output capacitor must maintain its ESR in the stable region over the full operating temperature range to ensure stability. Also, capacitor tolerance and variation with temperature must be considered to ensure the minimum amount of capacitance is provided at all times.

This capacitor must be located not more than 0.5 inches from the OUT pin of the LP2982 and returned to a clean analog ground.

For the new chip, dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the [Recommended Operating Conditions](#) table for stability.

7.1.4 Noise Bypass Capacitor (C_{BYPASS})

The LP2982 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference with the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, the output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA. The C_{BYPASS} capacitor also impacts the start-up behavior of the regulator. Inrush current and start-up time increase with larger bypass capacitor values.

Use a 10-nF capacitor for C_{BYPASS} . Ceramic and film capacitors are good choices for this purpose.

7.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{\text{OUT}} \leq V_{\text{IN}} + 0.3 \text{ V}$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 7-3 shows one approach for protecting the device.

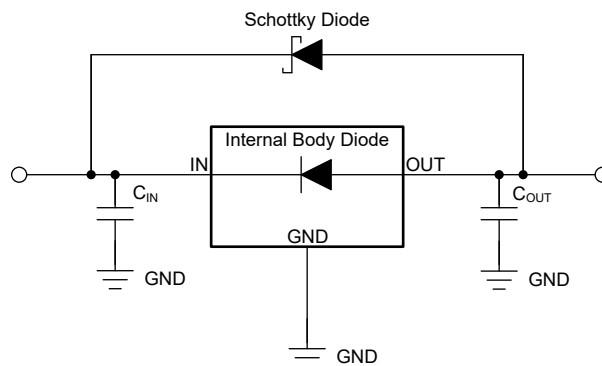


图 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} \quad (2)$$

备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the

junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the [Thermal Information](#) table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The [Thermal Information](#) table lists the primary thermal metrics, which are the junction-to-top characterization parameter (Ψ_{JT}) and junction-to-board characterization parameter (Ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (Ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (Ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \quad (4)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

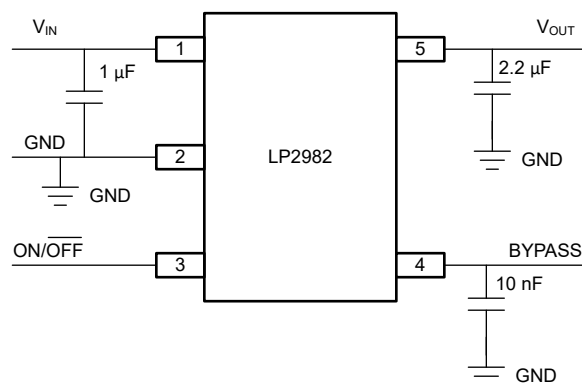
$$T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics application note](#).

7.2 Typical Application



ON/ OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used. Minimum output capacitance is shown to insure stability over full load current range. More capacitance provides better dynamic performance and additional stability margin (see the [Recommended Capacitor Types](#) section).

图 7-4. LP2982 Typical Application

7.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V $\pm 10\%$
Output voltage	3.3 V $\pm 1.5\%$
Output current	50 mA
Ambient temperature	85°C

7.2.2 Detailed Design Procedure

7.2.2.1 ON/ OFF Input Operation

The LP2982 is shut off by pulling the ON/ OFF input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input required to be tied to V_{IN} to keep the regulator on at all times (the ON/ OFF input must **not** be left floating).

For proper operation of the LDO, the signal source used to drive the ON/ OFF input must be able to swing above and below the specified turnon/turnoff voltage thresholds which specify an ON or OFF state.

The ON/ OFF signal can come from either a totem-pole output, or an open-collector output with pullup resistor to the LP2982 input voltage or another logic supply. The high-level voltage can exceed the LP2982 input voltage, but must remain within the absolute maximum ratings for the ON/ OFF pin.

It is also important that the turnon/turnoff voltage signals applied to the ON/ OFF input have a slew rate which is greater than 40 mV/ μ s.

备注

IMPORTANT: For the legacy chip, the regulator shutdown function does not operate correctly if a slow-moving signal is applied to the ON/ OFF input.

7.2.3 Application Curves

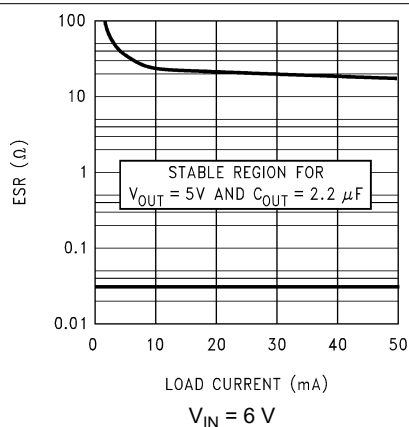


图 7-5. 5-V, 2.2- μF ESR Curves (Legacy chip)

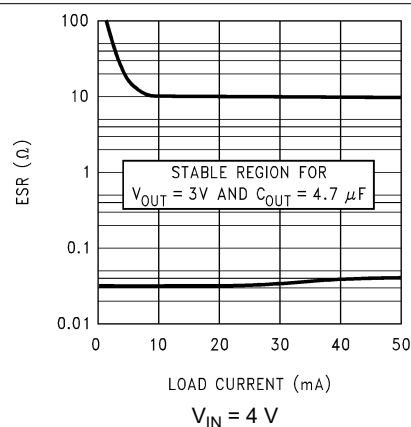


图 7-6. 3-V, 4.7- μF ESR Curves (Legacy chip)

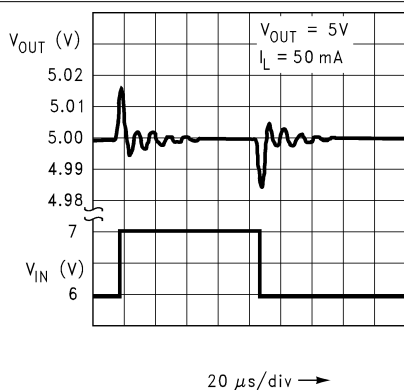


图 7-7. Line Transient Response (Legacy chip)

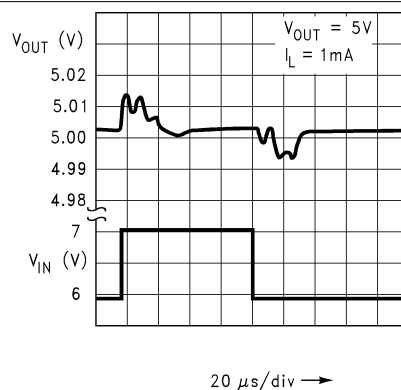


图 7-8. Line Transient Response (Legacy chip)

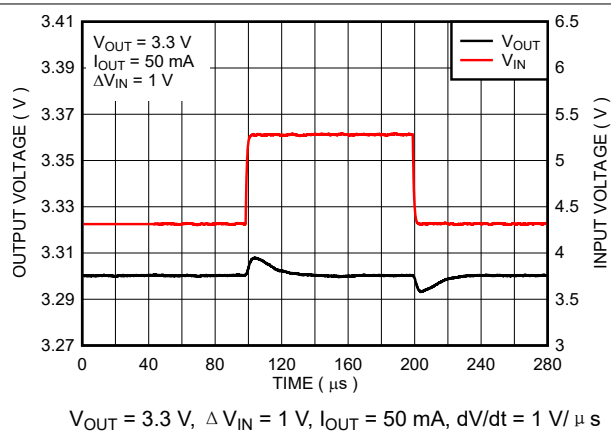


图 7-9. Line Transient Response (New Chip)

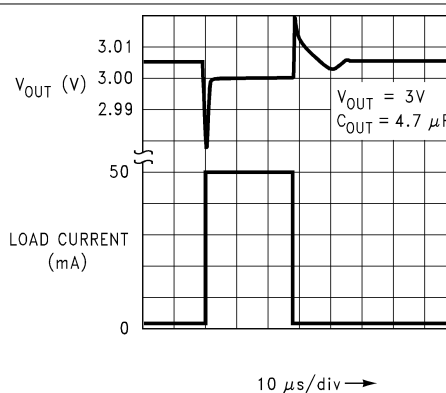


图 7-10. Load Transient Response (Legacy chip)

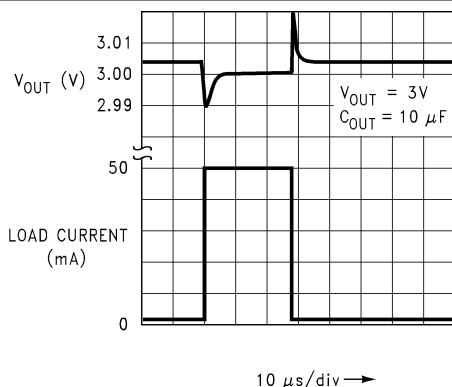


图 7-11. Load Transient Response (Legacy chip)

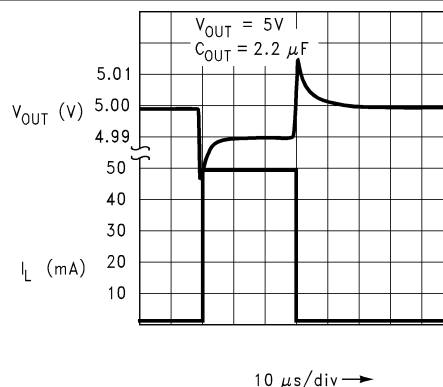


图 7-12. Load Transient Response (Legacy chip)

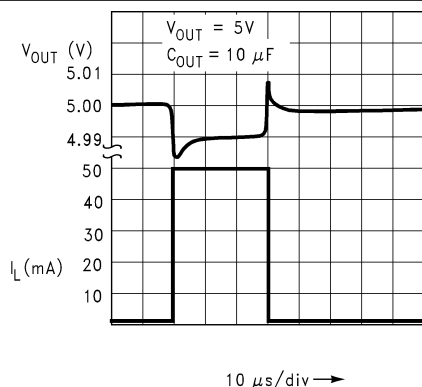


图 7-13. Load Transient Response (Legacy chip)

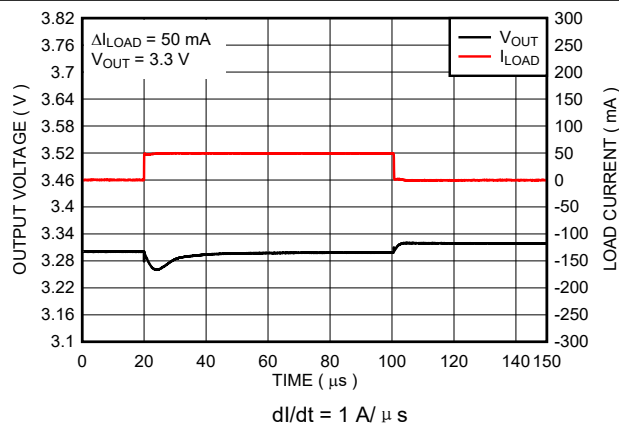


图 7-14. Load Transient Response (New Chip)

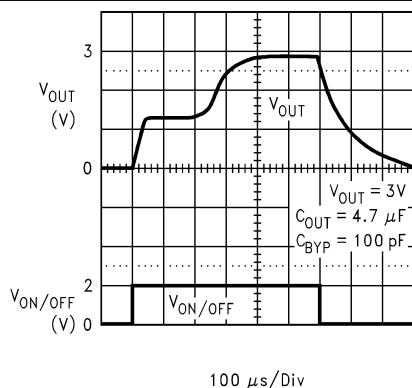


图 7-15. Turnon Waveform (Legacy chip)

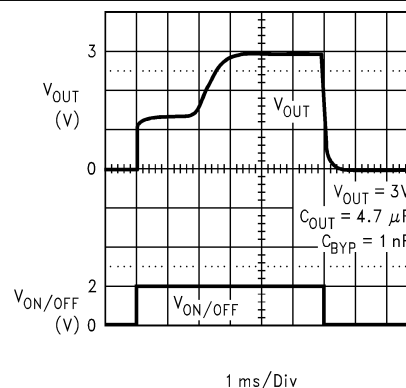


图 7-16. Turnon Waveform (Legacy chip)

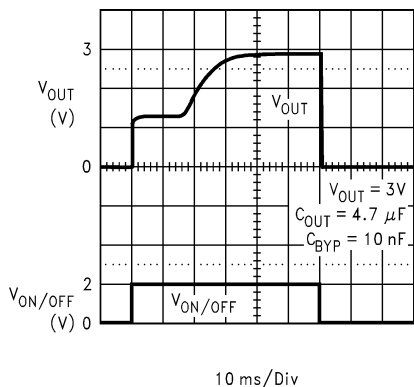


图 7-17. Turnon Waveform (Legacy chip)

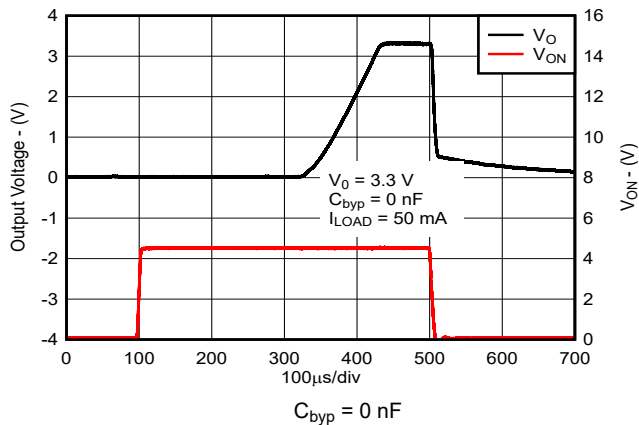


图 7-18. Turnon Waveform (New chip)

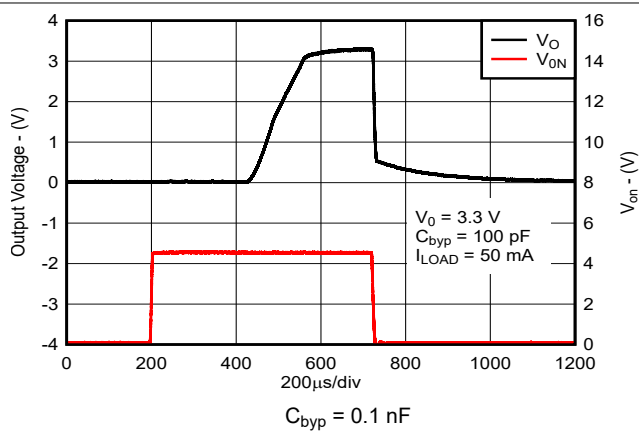


图 7-19. Turnon Waveform (New chip)

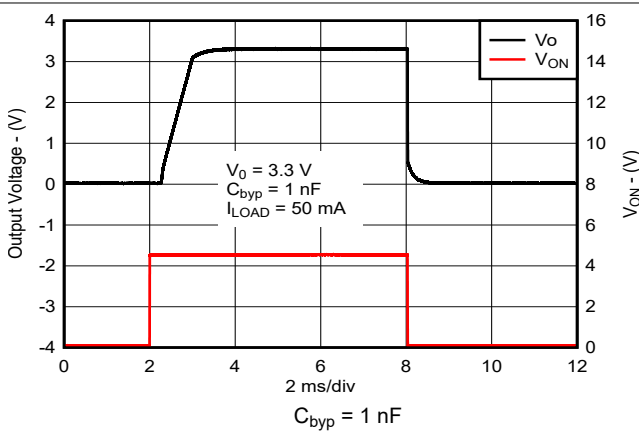


图 7-20. Turnon Waveform (New chip)

7.3 Power Supply Recommendations

The LP2982 is designed to operate from an input voltage supply range between $V_{OUT(NOM)} + 1\text{ V}$ and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves for better accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Example

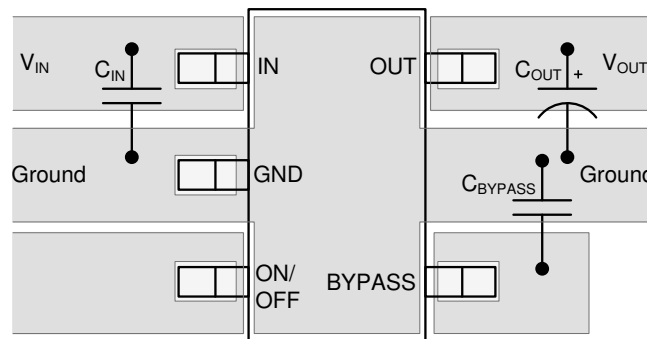


图 7-21. LP2982 Layout Example

8 器件和文档支持

8.1 器件命名规则

表 8-1. 提供的选项

产品 ⁽¹⁾	说明
LP2982vwxy-z.z/NOPB	v 是旧芯片 (A 或空白) 的精度规格。有关更多信息, 请参阅 节 5.5 。此特性对于新芯片而言无关紧要。 w 是工作温度范围 (I = -40°C 至 +125°C)。 xx 是封装指示符 (M5 = SOT-23)。 y 是卷带标识符尺寸。有关封装数量的更多信息, 请参阅封装附录。 z.z 是额定输出电压 (例如, 3.3 = 3.3V ; 5.0 = 5.0V)。 /NOPB 表示不使用铅 (Pb) 的材料结构。该器件可以随附旧芯片 (CSO : DLN 或 GF8) 或采用最新制造流程的新芯片 (CSO:RFB)。卷带封装标签提供 CSO 信息以区分正在使用的芯片。全篇对新芯片和旧芯片的器件性能进行了说明。

(1) 如需了解最新的封装及订购信息, 请参阅本文档末尾的封装选项附录, 或访问 www.ti.com 查看器件产品文件夹。

8.2 第三方产品免责声明

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8.3 文档支持

8.3.1 相关文档

更多信息, 请参见以下文档:

- 德州仪器 (TI), [半导体和 IC 封装热指标应用手册](#)
- 德州仪器 (TI), [使用新的热指标应用手册](#)
- 德州仪器 (TI), [采用 JEDEC PCB 设计的线性和逻辑封装的热特性应用手册](#)

8.4 接收文档更新通知

要接收文档更新通知, 请导航至 ti.com 上的器件产品文件夹。点击右上角的 [提醒我](#) 进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

8.5 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料, 可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题, 获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的 [使用条款](#)。

8.6 商标

TI E2E™ is a trademark of Texas Instruments.

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8.7 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.8 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision L (December 2023) to Revision M (June 2025)	Page
• 更改了整个文档，以识别旧芯片和新芯片的功能和差异.....	1
• 更改了 说明部分中与新芯片相关的软启动讨论.....	1
• Changed <i>Overview</i> section.....	19
• Changed <i>Functional Block Diagrams</i> section.....	19
• Changed <i>Current Limit</i> section.....	20
• Changed <i>Recommended Capacitors (Legacy Chip)</i> section.....	24
• Changed <i>Recommended Capacitors (New Chip)</i> section.....	24
• Changed <i>Input Capacitor Requirements</i> section.....	25
• Changed <i>Input and Output Capacitor Requirements</i> section.....	25
• 更改了 器件命名规则部分.....	33

Changes from Revision K (June 2016) to Revision L (December 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更改了整个文档以与当前系列格式保持一致.....	1
• 向文档添加了 M3 器件.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2982AIM5-3.0/NO.A	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5-3.0/NOPB	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5-3.3/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5-3.3/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5-5.0/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982AIM5-5.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982AIM5X-3.0/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5X-3.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5X-3.3/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5X-3.3/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5X-5.0/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982AIM5X-5.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982IM5-3.0/NOPB	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5-3.0/NOPB.A	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5-3.0/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5-3.3/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5-3.3/NOPB.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5-5.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B
LP2982IM5-5.0/NOPB.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B
LP2982IM5X-3.0/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5X-3.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5X-3.3/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5X-3.3/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5X-5.0/NO.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B
LP2982IM5X-5.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

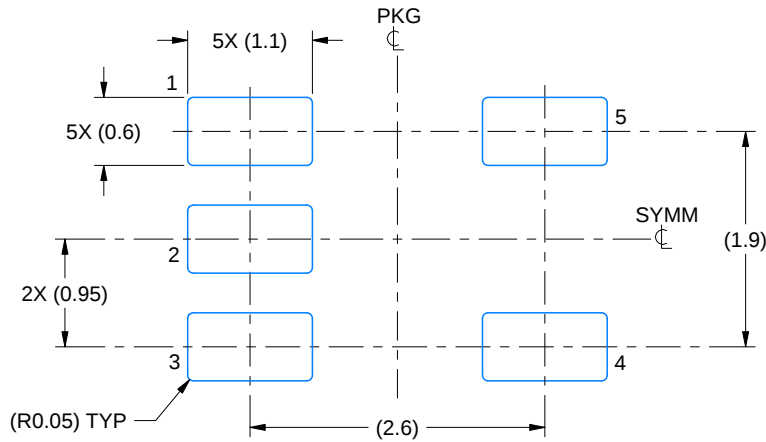
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

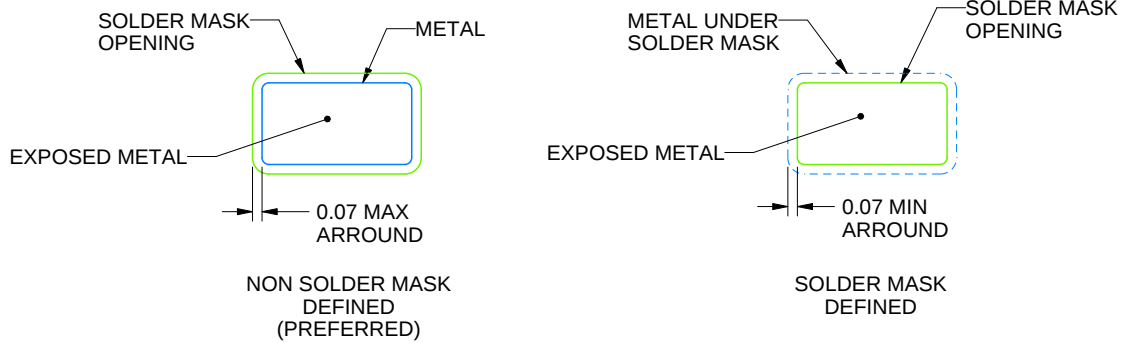
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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