LMK1C110x 1.8V、2.5V 和 3.3V LVCMOS 时钟缓冲器系列

1 特性

- 高性能 1:6 和 1:8 LVCMOS 时钟缓冲器
- 输出偏斜极低，< 55ps
- 附加抖动极低，标称值 < 25fs
  - V_{DD} = 3.3 V 时，典型值为 12fs
  - V_{DD} = 2.5 V 时，典型值为 15fs
  - V_{DD} = 1.8V 时，典型值为 28fs
- 传播延迟极低，< 3ns
- 同步输出使能
- 电源电压：3.3V、2.5V 或 1.8V
  - 在电源电压范围内输入端耐受 3.3V 电压
  - 失效防护输入
- 9000V HBM 的工业高 ESD 等级
- f_{max} = 250MHz (3.3V)
  f_{max} = 200MHz（2.5V 和 1.8V）
- 工作温度范围：–40°C 至 125°C
- 采用 14 引脚和 16 引脚 TSSOP 封装

2 应用

- 工厂自动化与控制
- 电信设备
- 数据中心和企业计算
- 电网基础设施
- 电机驱动器
- 医疗成像

3 说明

LMK1C110x 是德州仪器 (TI) 的一款模块化、高性能、低偏斜、通用时钟缓冲器系列器件。整个系列采用模块化方法设计。提供五个不同的扇出选项：1:2、1:3、1:4、1:6 和 1:8。

该系列所有器件均互相引脚兼容，并与 CDCLVC110x 系列向后兼容，从而易于处理。

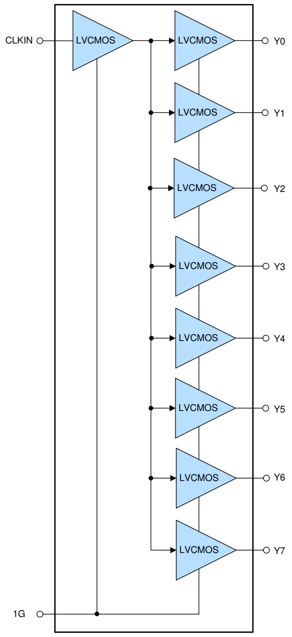
该系列所有器件均具有相同的高性能特性，如低附加抖动、低偏斜和宽工作温度范围。

LMK1C110x 具有同步输出使能控制端 (1G)，可在 1G 处于低电平时将输出切换为低电平状态。这些器件具有失效防护输入，可防止在没有输入信号的情况下输出发生振荡并允许在提供 VDD 之前提供输入信号。

LMK1C110x 系列可在 1.8V、2.5V 和 3.3V 电压下工作，额定工作温度范围为 –40°C 至 125°C。

器件信息

器件型号	封装	封装尺寸（标称值）
LMK1C1106	TSSOP (14)	5.00mm x 4.40mm
LMK1C1108	TSSOP (16)	5.00mm x 4.40mm



功能方框图

Table of Contents

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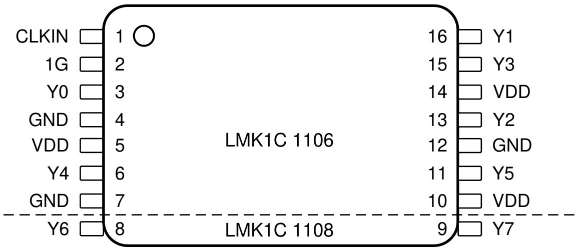
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2020) to Revision A (January 2022)	Page
• 向*说明*部分中添加失效防护输入详细信息	1
• 更改了第一页的重要图形	1
• Changed part-to-part skew maximum from 950 ps to 280 ps	5
• Added the *Fail-Safe Inputs* section	11

5 Pin Configuration and Functions



Not to scale

图 5-1. LMK1C1106 and LMK1C1108 PW Package 14-Pin TSSOP and 16-Pin TSSOP Top View

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	**LMK1C 1106**	**LMK1C 1108**		
LVCMOS CLOCK INPUT				
CLKIN	1	1	Input	Single-ended clock input with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
CLOCK OUTPUT ENABLE				
1G	2	2	Input	Global Output Enable with internal 300-kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
LVCMOS CLOCK OUTPUT				
Y0	3	3	Output	LVCMOS output. Typically connected to a receiver. Unused outputs can be left floating.
Y1	14	16		
Y2	11	13		
Y3	13	15		
Y4	6	6		
Y5	9	11		
Y6	–	8		
Y7	–	9		
SUPPLY VOLTAGE				
VDD	5	5	Power	Power supply terminal. Typically connected to a 3.3-V, 2.5-V, or 1.8-V supply. The VDD pin is typically connected to an external 0.1-µF capacitor near the pin.
	8	10		
	12	14		
GROUND				
GND	4	4	GND	Device ground.
	7	7		
	10	12		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	3.6	V
V_{CLKIN}	Input voltage (CLKIN)			
V_{IN}	Input voltage (1G)			
V_{Yn}	Output pins (Yn)	–0.5	V_{DD} + 0.3	
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±9000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMK1C1106	LMK1C1108	UNIT
		PW (TSSOP)	PW(TSSOP)	
		14 PINS	16 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	114.4	123.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	45.2	53.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	60.6	66.4	°C/W
Y_{JT}	Junction-to-top characterization parameter	5.9	8.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	60	65.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

VDD = 3.3 V ± 5 %, –40°C ≤ TA ≤ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{DD}	Core supply current, static	All-outputs disabled, f_{IN} = 0 V		25	45	µA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz, V_{DD} = 1.8 V		2	6	mA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz, V_{DD} = 2.5 V		6.5	10	mA
I_{DD}	Core supply current	All-outputs disabled, f_{IN} = 100 MHz, V_{DD} = 3.3 V		15	21	mA
I_{DD}	Output current	Per output, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 1.8 V		3.2	3.5	
		Per output, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 2.5 V		4.6	5.5	
		Per output, f_{IN} = 100 MHz, C_L = 5pF, V_{DD} = 3.3 V		6	7	
CLOCK INPUT						
f_{IN_SE}	Input frequency	V_{DD} = 3.3 V	DC		250	MHz
		V_{DD} = 2.5 V and 1.8 V	DC		200	
V_{IH}	Input high voltage		0.7 x V_{DD}			V
V_{IL}	Input low voltage				0.3 x V_{DD}	
dV_{IN}/dt	Input slew rate	20% - 80% of input swing	0.1			V/ns
I_{IN_LEAK}	Input leakage current		–50		50	uA
C_{IN_SE}	Input capacitance	at 25°C		7		pF
CLOCK OUTPUT FOR ALL V_{DD} LEVELS						
f_{OUT}	Output frequency	V_{DD} = 3.3 V			250	MHz
		V_{DD} = 2.5 V and 1.8 V			200	
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_{1G_ON}	Output enable time	See (1)			5	cycles
t_{1G_OFF}	Output disable time	See (2)			5	cycles
CLOCK OUTPUT FOR V_{DD} = 3.3 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	2.8			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2	
$t_{RISE\text{-}FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, fIN = 156.25 MHz		0.3	0.7	ns
$t_{OUTPUT\text{-}SKEW}$	Output-output skew	See (3)		35	55	ps
$t_{PART\text{-}SKEW}$	Part-to-part skew				280	
$t_{PROP\text{-}DELAY}$	Propagation delay	See (4)		1.3	2.2	ns
$t_{JITTER\text{-}ADD}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 1.6 V/ns, Integration range = 12 kHz - 20 MHz		12	20	fs, RMS
R_{OUT}	Output impedance			50		Ω
CLOCK OUTPUT FOR V_{DD} = 2.5 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	0.8 x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2 x V_{DD}	
$t_{RISE\text{-}FALL}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.33	0.8	ns
$t_{OUTPUT\text{-}SKEW}$	Output-output skew	See (3)			55	ps
$t_{PART\text{-}SKEW}$	Part-to-part skew				450	
$t_{PROP\text{-}DELAY}$	Propagation delay	See (4)		1.5	2.5	ns

VDD = 3.3 V ± 5 %, –40°C ⩽ TA ⩽ 125°C. Typical values are at VDD = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{JITTER-ADD}}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 1.2 V/ns, Integration range = 12 kHz - 20 MHz		15	27	fs, RMS
R_{OUT}	Output impedance			55		Ω
CLOCK OUTPUT FOR V_{DD} = 1.8 V ± 5%						
V_{OH}	Output high voltage	I_{OH} = 1 mA	0.8 x V_{DD}			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.2 x V_{DD}	
$t_{\text{RISE-FALL}}$	Output rise and fall time	20/80%, C_L= 5 pF, f_{IN} = 156.25 MHz		0.38	1	ns
$t_{\text{OUTPUT-SKEW}}$	Output-output skew	See [3]			55	ps
$t_{\text{PART-SKEW}}$	Part-to-part skew				930	ps
$t_{\text{PROP-DELAY}}$	Propagation delay	See [4]		1.5	3	ns
$t_{\text{JITTER-ADD}}$	Additive Jitter	f_{IN} = 156.25 MHz, Input slew rate = 1.2 V/ns, Integration range = 12 kHz - 20 MHz		28	60	fs, RMS
R_{OUT}	Output impedance			64		Ω
GENERAL PURPOSE INPUT (1G)						
V_{IH}	High-level input voltage		0.75 x V_{DD}			V
V_{IL}	Low-level input voltage				0.25 x V_{DD}	
I_{IH}	Input high-level current	V_{IH} = V_{DD_REF}	– 50		50	µA
I_{IL}	Input low-level current	V_{IL} = GND	– 50		50	

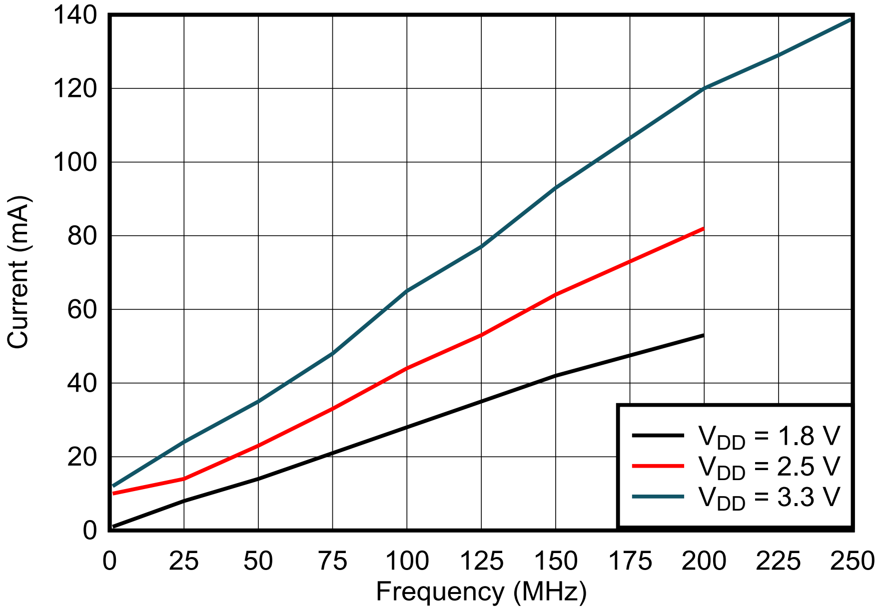
(1) Measured from 1G rising edge crossing VIH to first rising edge of Yn.
(2) Measured from 1G falling edge crossing VIL to last falling edge of Yn.
(3) Measured from rising edge of any Yn output to any other Ym output.
(4) Measured from rising edge of CLKIN to any Yn output.

6.6 Timing Requirements

VDD = 3.3 V ± 5 %, –40°C ⩽ TA ⩽ 125°C

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V/t_{RAMP}	V_{DD} ramp rate		0.1		50	V/ms

6.7 Typical Characteristics



Device Power Consumption vs. Clock Frequency (Load 5 pF)

7 Parameter Measurement Information

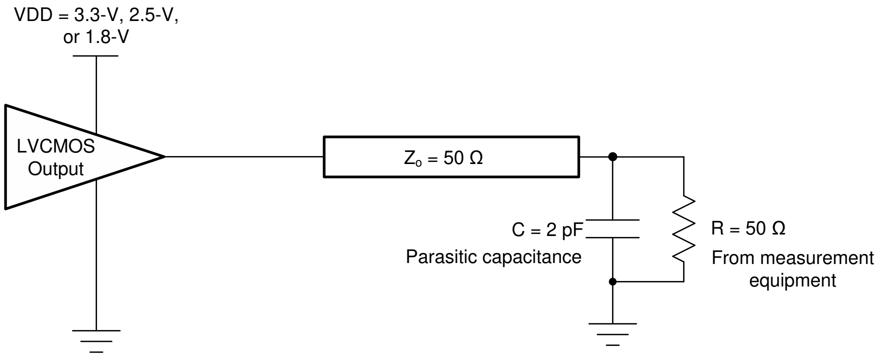


图 7-1. Test Load Circuit

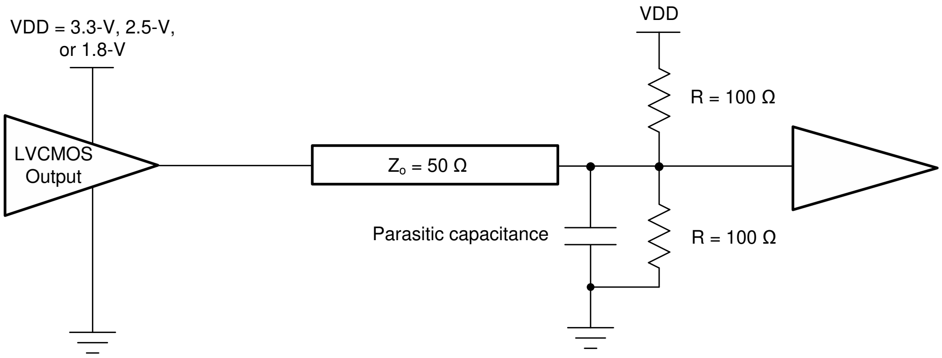


图 7-2. Application Load With 50-Ω Termination

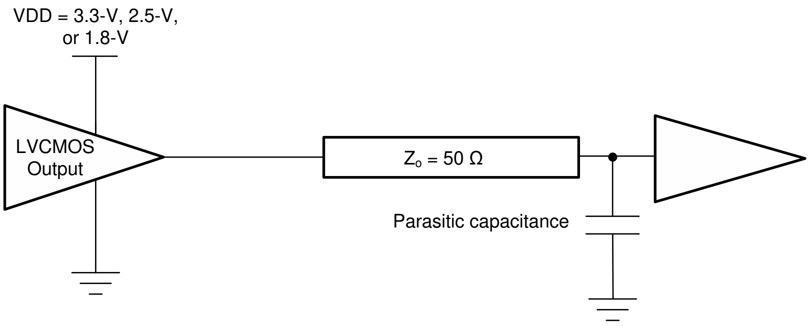


图 7-3. Application Load With Termination

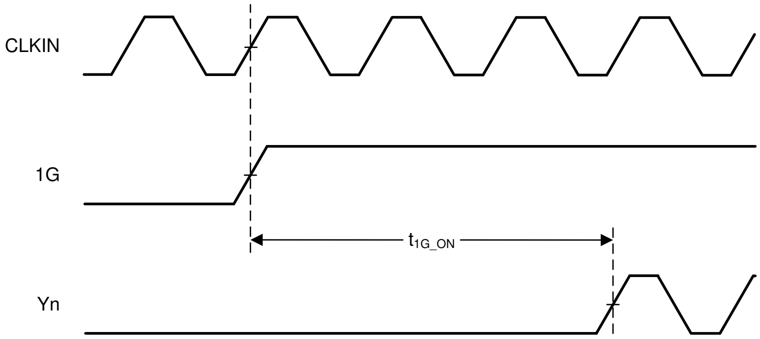


图 7-4. t_{1G_ON} Output Enable Time

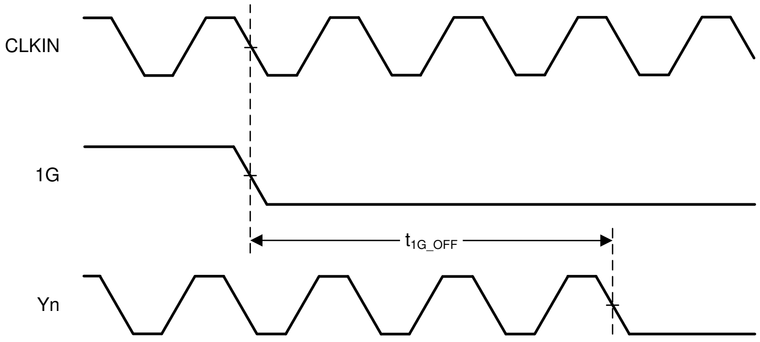


图 7-5. t_{1G_OFF} Output Disable Time

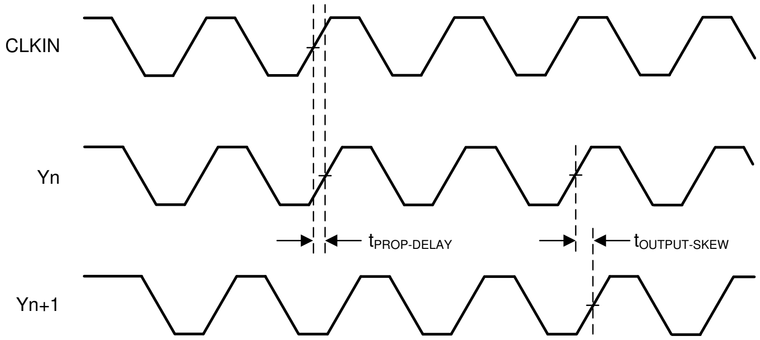


图 7-6. Propagation Delay $t_{PROP-DELAY}$ and Output Skew $t_{OUTPUT-SKEW}$

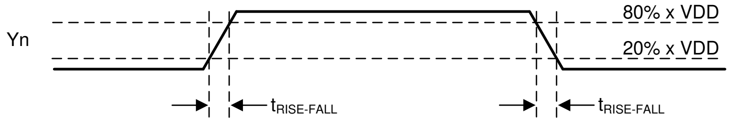


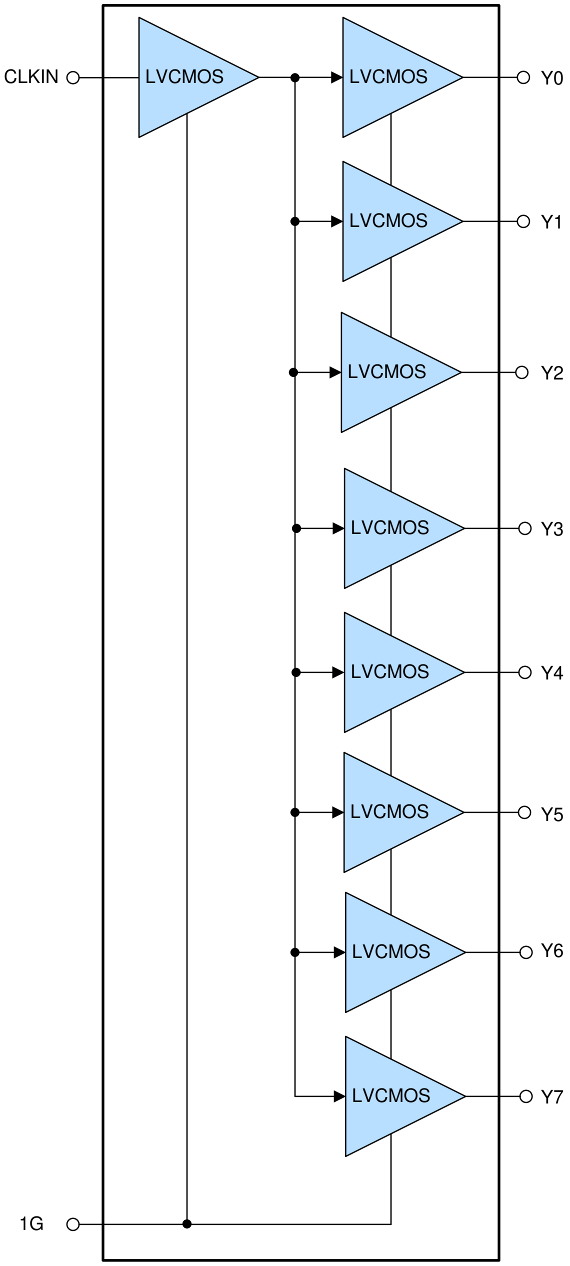
图 7-7. Rise and Fall Time $t_{RISE-FALL}$

8 Detailed Description

8.1 Overview

The LMK1C110x family of devices is part of a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the LMK1C110x's output driver with that of the transmission line.

8.2 Functional Block Diagram



8.3 Feature Description

The outputs of the LMK1C110x can be disabled by driving the synchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. Supply and ground pins must be connected to V_{DD} and GND, respectively.

8.3.1 Fail-Safe Inputs

The LMK1C110x family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to *Absolute Maximum Ratings* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis that prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

8.4 Device Functional Modes

The LMK1C110x operates from 1.8-V, 2.5-V, or 3.3-V supplies. 表 8-1 shows the output logics of the LMK1C110x.

表 8-1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	**1G**	**Yn**
X	L	L
L	H	L
H	H	H

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LMK1C110x family is a low additive jitter LVCMOS buffer solution that can operate up to 250-MHz at V_{DD} = 3.3 V and 200 MHz at V_{DD} = 2.5 V to 1.8 V. Low output skew as well as the ability for synchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

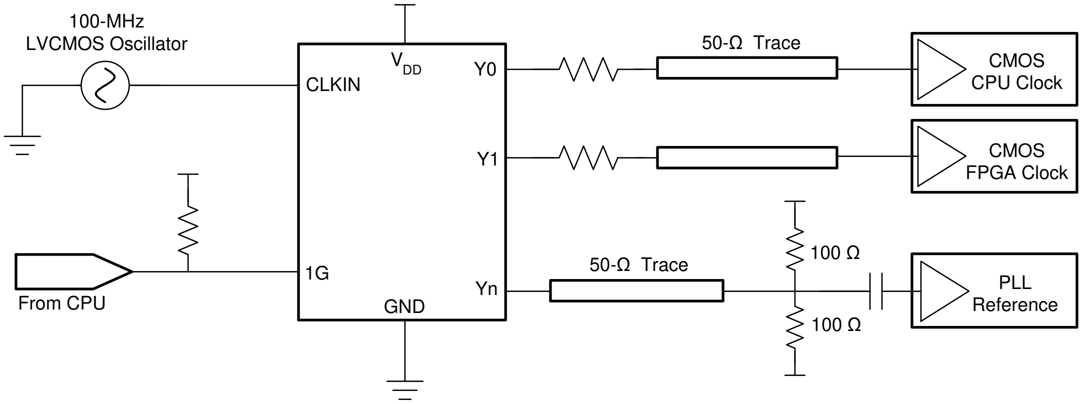


图 9-1. System Configuration Example

9.2.1 Design Requirements

The LMK1C110x shown in 图 9-1 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the LMK1C110x to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the LMK1C110x.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

9.2.2 Detailed Design Procedure

Unused outputs can be left floating. See *Power Supply Recommendations* for recommended filtering techniques.

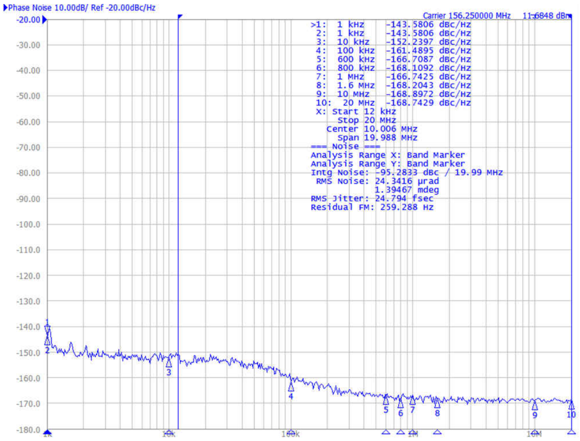
9.2.3 Application Curves

The low additive jitter of the LMK1C110x is shown in 图 9-2.

图 9-3 shows the low-noise 156.25-MHz reference source with 24.8-fs RMS jitter driving the LMK1C110x, resulting in 27.3-fs RMS jitter when integrated from 12 kHz to 20 MHz at 3.3-V supply. The resultant additive jitter measured is a low 11.4-fs RMS for this configuration.

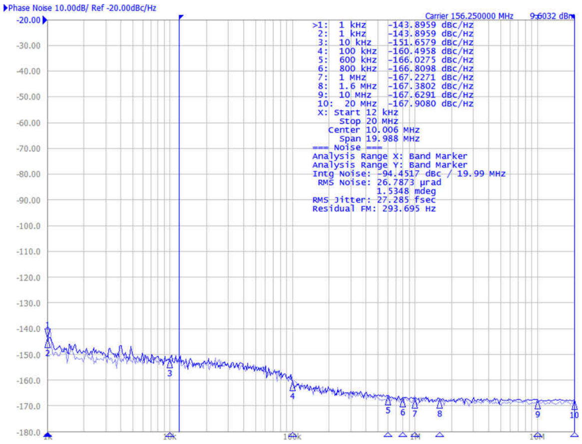
图 9-4 shows the low-noise 156.25-MHz reference source with 24.8-fs RMS jitter driving the LMK1C110x, resulting in 29-fs RMS jitter when integrated from 12 kHz to 20 MHz at 2.5-V supply. The resultant additive jitter measured is a low 15-fs RMS for this configuration.

图 9-5 shows the low-noise 156.25-MHz reference source with 24.8-fs RMS jitter driving the LMK1C110x, resulting in 34-fs RMS jitter when integrated from 12 kHz to 20 MHz at 1.8-V supply. The resultant additive jitter measured is a low 23.25-fs RMS for this configuration.



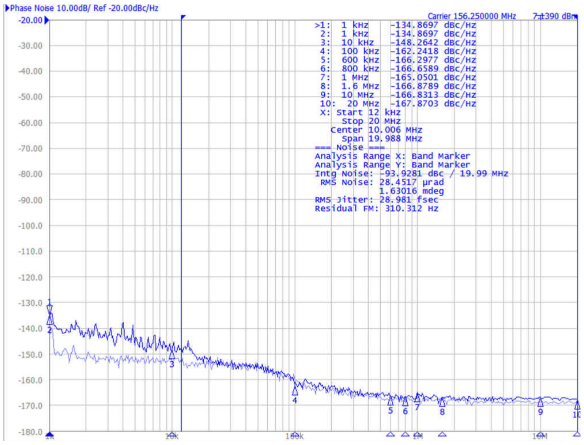
```
>1:  1 kHz    -143.5806 dBc/Hz
 2:  1 kHz    -143.5806 dBc/Hz
 3:  10 kHz   -152.2397 dBc/Hz
 4:  100 kHz  -161.4895 dBc/Hz
 5:  600 kHz  -166.7087 dBc/Hz
 6:  800 kHz  -168.1092 dBc/Hz
 7:  1 MHz    -166.7425 dBc/Hz
 8:  1.6 MHz  -168.2043 dBc/Hz
 9:  10 MHz   -168.8972 dBc/Hz
 10:  20 MHz  -168.7429 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -95.2833 dBc / 19.99 MHz
 RMS Noise: 24.3416 µrad
            1.39467 mdeg
RMS Jitter: 24.794 fsec
Residual FM: 259.288 Hz
```

图 9-2. LMK1C110x Reference Phase Noise 24.8-fs (12 kHz to 20 MHz)



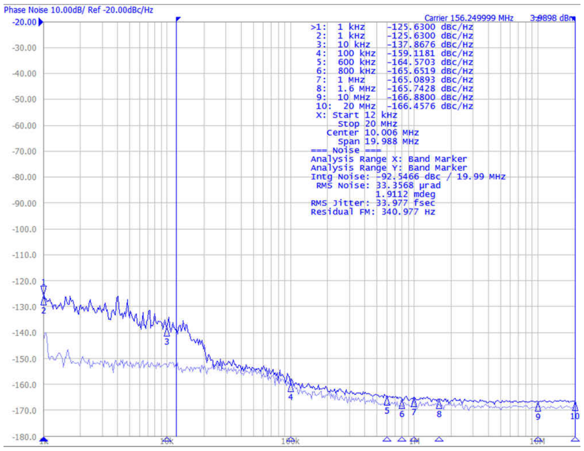
```
>1:  1 kHz    -143.8959 dBc/Hz
 2:  1 kHz    -143.8959 dBc/Hz
 3:  10 kHz   -151.6579 dBc/Hz
 4:  100 kHz  -160.4958 dBc/Hz
 5:  600 kHz  -166.0275 dBc/Hz
 6:  800 kHz  -166.8098 dBc/Hz
 7:  1 MHz    -167.2271 dBc/Hz
 8:  1.6 MHz  -167.3802 dBc/Hz
 9:  10 MHz   -167.6291 dBc/Hz
 10:  20 MHz  -167.9080 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -94.4517 dBc / 19.99 MHz
 RMS Noise: 26.7873 µrad
            1.5348 mdeg
RMS Jitter: 27.285 fsec
Residual FM: 293.695 Hz
```

图 9-3. LMK1C110x 3.3-V Output Phase Noise 27.3-fs (12 kHz to 20 MHz)



```
>1:  1 kHz    -134.8697 dBc/Hz
 2:  1 kHz    -134.8697 dBc/Hz
 3:  10 kHz   -148.2642 dBc/Hz
 4:  100 kHz  -162.2418 dBc/Hz
 5:  600 kHz  -166.2977 dBc/Hz
 6:  800 kHz  -166.6589 dBc/Hz
 7:  1 MHz    -165.0501 dBc/Hz
 8:  1.6 MHz  -166.8789 dBc/Hz
 9:  10 MHz   -166.8313 dBc/Hz
 10:  20 MHz  -167.8703 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -93.9281 dBc / 19.99 MHz
 RMS Noise: 28.4517 µrad
            1.63016 mdeg
RMS Jitter: 28.981 fsec
Residual FM: 310.312 Hz
```

图 9-4. LMK1C110x 2.5-V Output Phase Noise 29-fs (12 kHz to 20 MHz)



```
>1:  1 kHz    -125.6300 dBc/Hz
 2:  1 kHz    -125.6300 dBc/Hz
 3:  10 kHz   -137.8676 dBc/Hz
 4:  100 kHz  -159.1181 dBc/Hz
 5:  600 kHz  -164.5703 dBc/Hz
 6:  800 kHz  -165.6519 dBc/Hz
 7:  1 MHz    -165.0893 dBc/Hz
 8:  1.6 MHz  -165.7428 dBc/Hz
 9:  10 MHz   -166.8800 dBc/Hz
 10:  20 MHz  -166.4576 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -92.5466 dBc / 19.99 MHz
 RMS Noise: 33.3568 µrad
            1.9112 mdeg
RMS Jitter: 33.977 fsec
Residual FM: 340.977 Hz
```

图 9-5. LMK1C110x 1.8-V Output Phase Noise 34-fs (12 kHz to 20 MHz)

10 Power Supply Recommendations

High-performance clock buffers can be sensitive to noise on the power supply, which may dramatically increase the additive jitter of the buffer. Thus, it is essential to manage any excessive noise from the system power supply, especially for applications where the jitter and phase noise performance is critical.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly bypass the supply, the decoupling capacitors must be placed very close to the power-supply terminals, be connected directly to the ground plane, and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

图 10-1 shows this recommended power supply decoupling method.

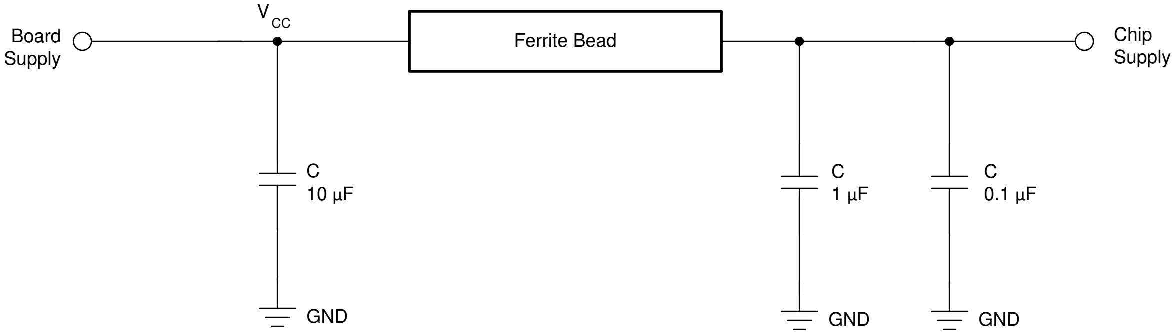


图 **10-1. Power Supply Decoupling**

11 Layout

11.1 Layout Guidelines

图 11-1 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

11.2 Layout Example

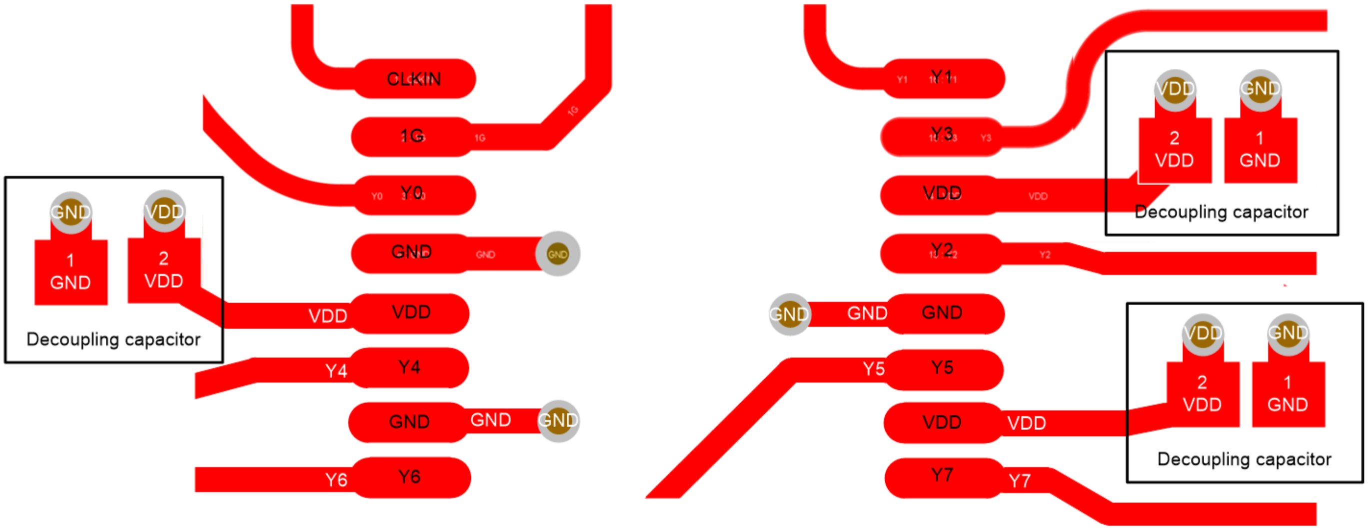


图 11-1. PCB Conceptual Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

LMK1C1108EVM User Guide

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK1C1106PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMK1C6
LMK1C1106PWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C6
LMK1C1108PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMK1C8
LMK1C1108PWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C8
LMK1C1108PWRG4	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C8
LMK1C1108PWRG4.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMK1C8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

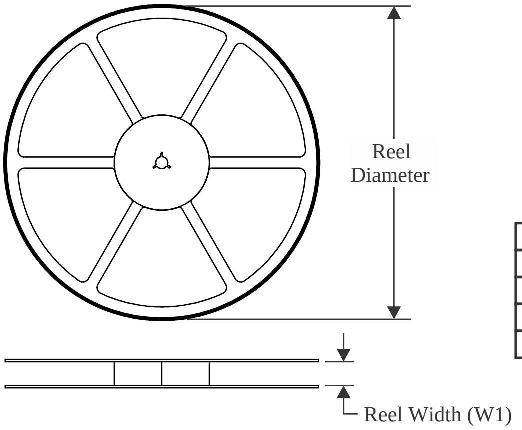
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

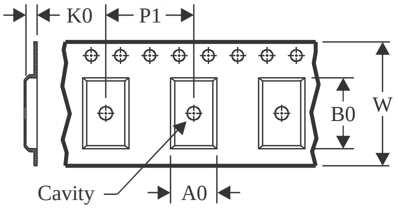
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

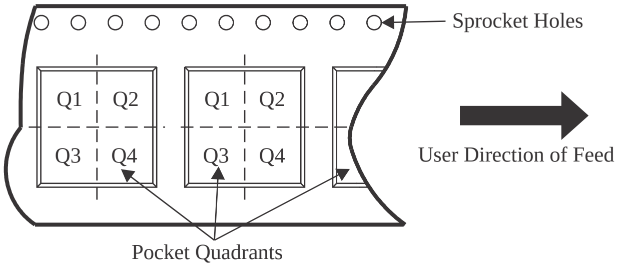


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

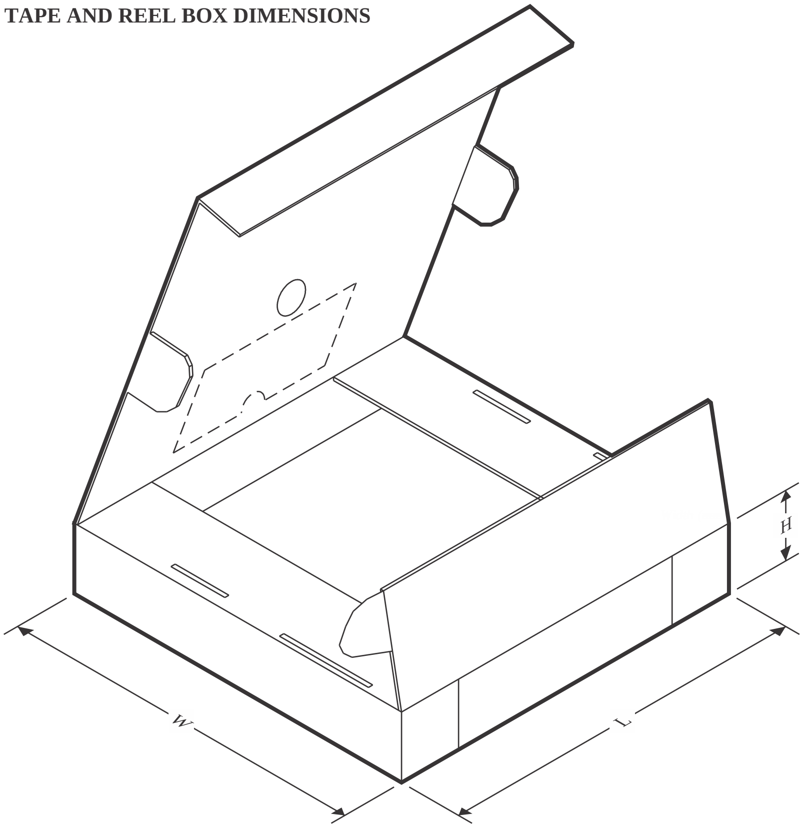
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1C1106PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMK1C1108PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMK1C1108PWRG4	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

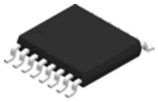
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1C1106PWR	TSSOP	PW	14	3000	356.0	356.0	35.0
LMK1C1108PWR	TSSOP	PW	16	3000	356.0	356.0	35.0
LMK1C1108PWRG4	TSSOP	PW	16	3000	353.0	353.0	32.0

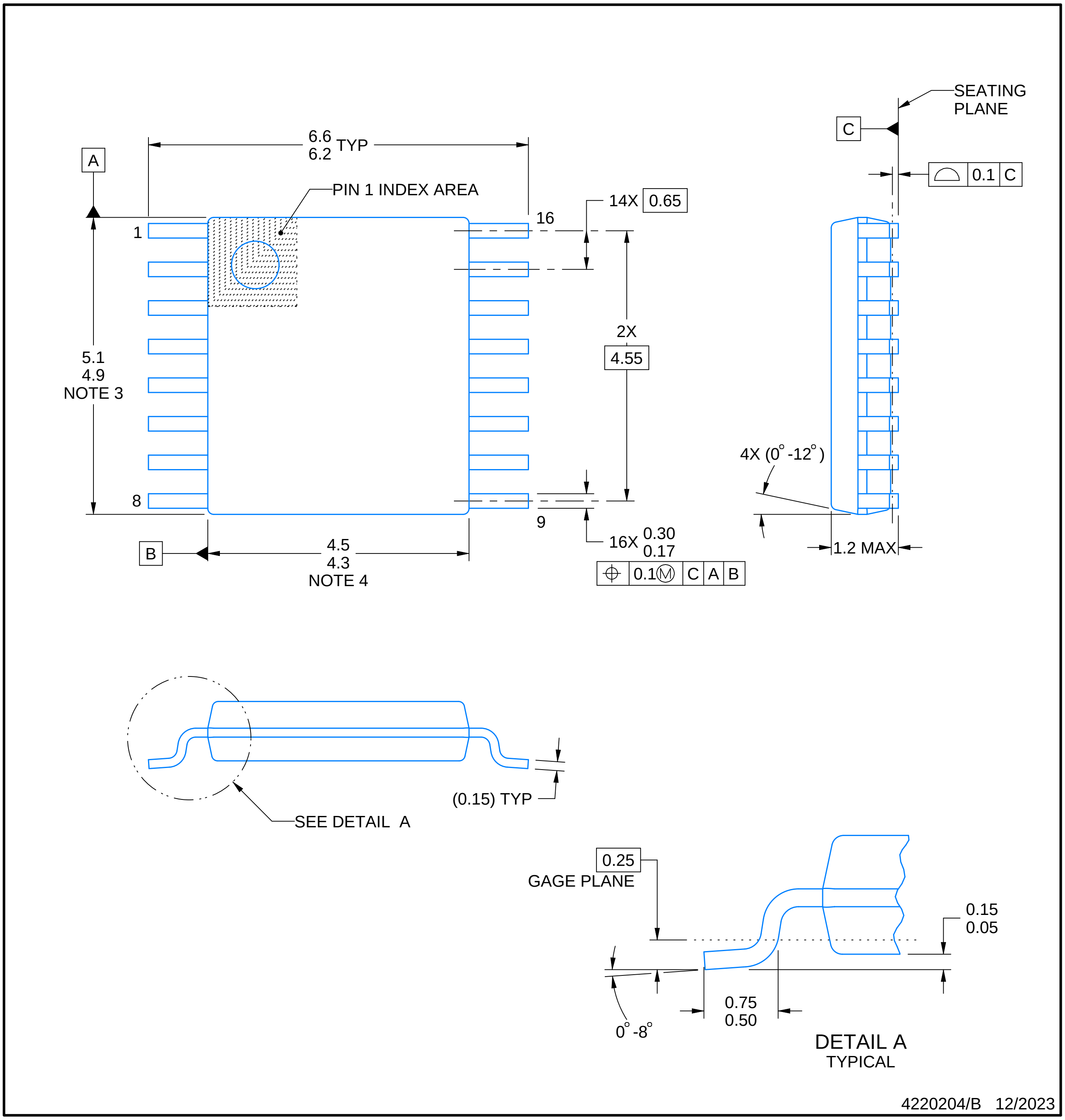
PACKAGE OUTLINE



PW0016A

TSSOP - 1.2 mm max height

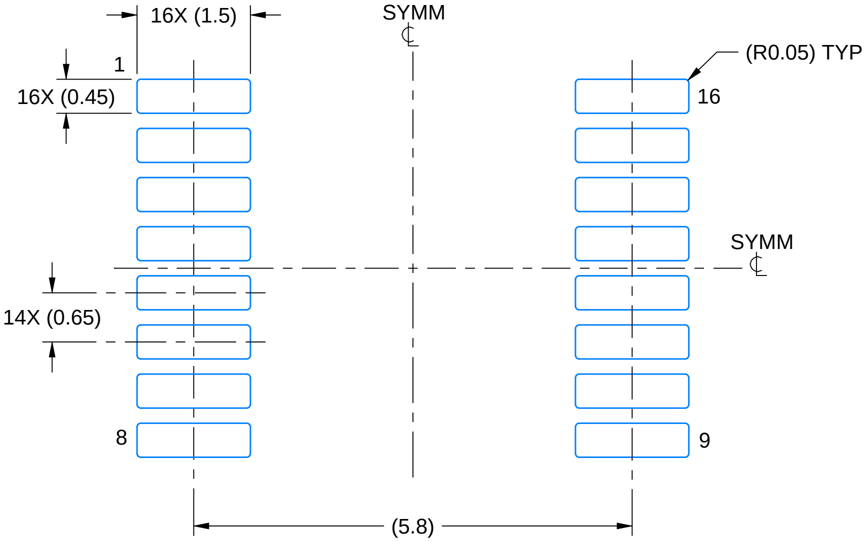
SMALL OUTLINE PACKAGE



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

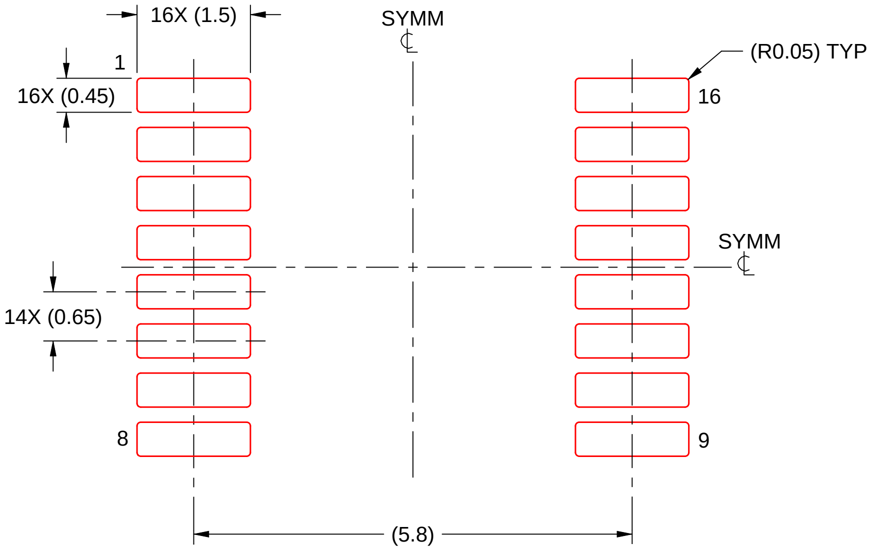
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

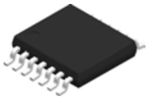
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

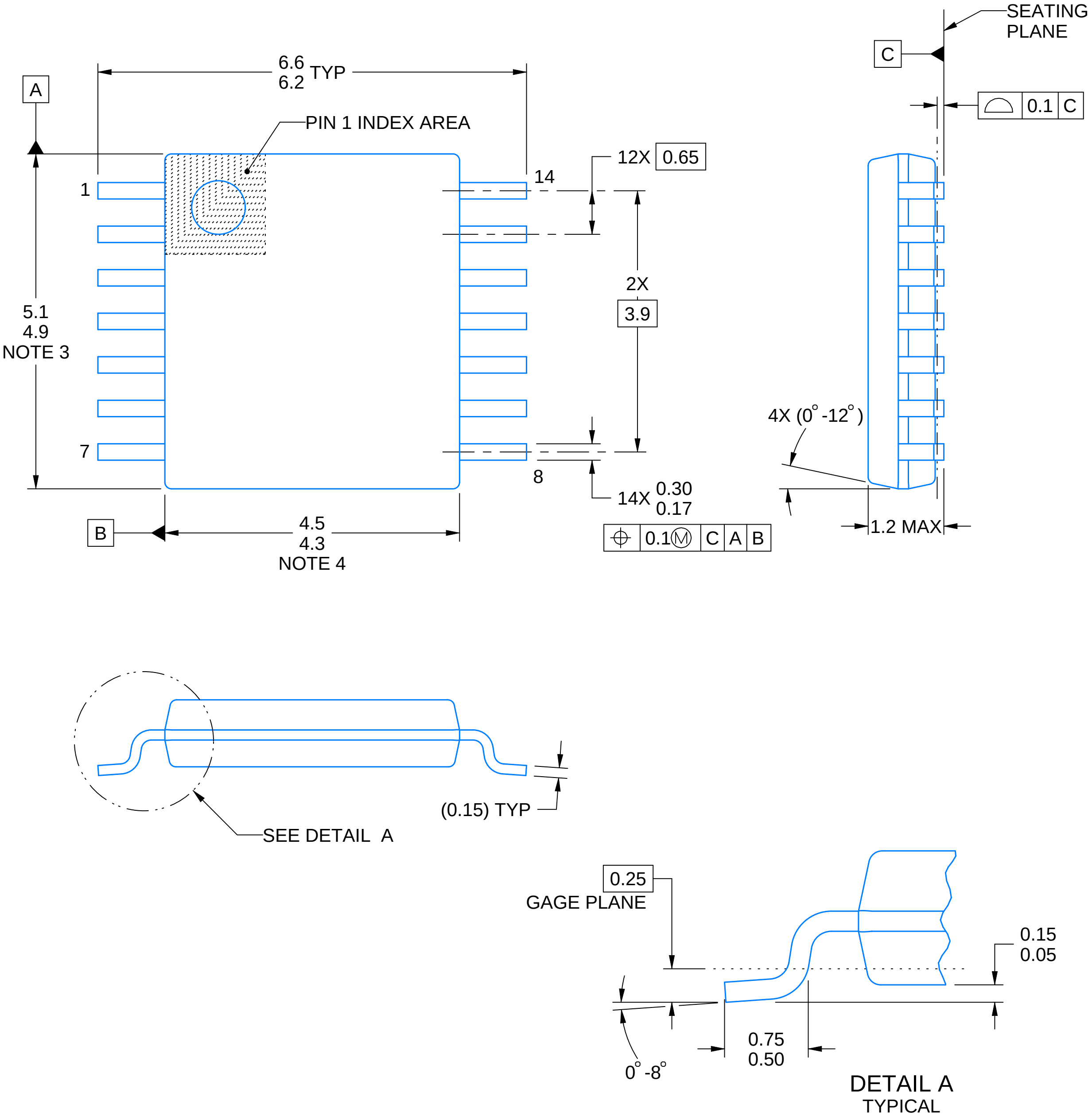
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

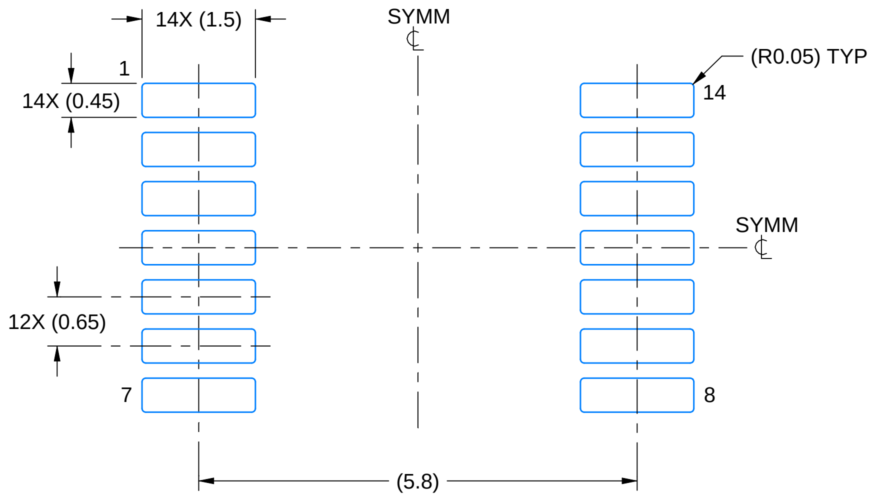
SMALL OUTLINE PACKAGE



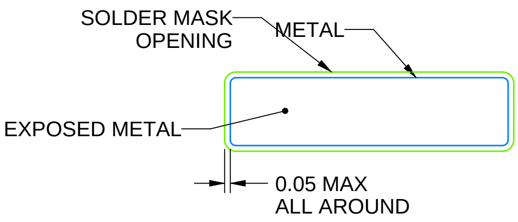
4220202/B 12/2023

NOTES:

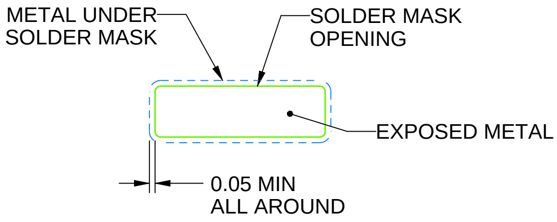
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)



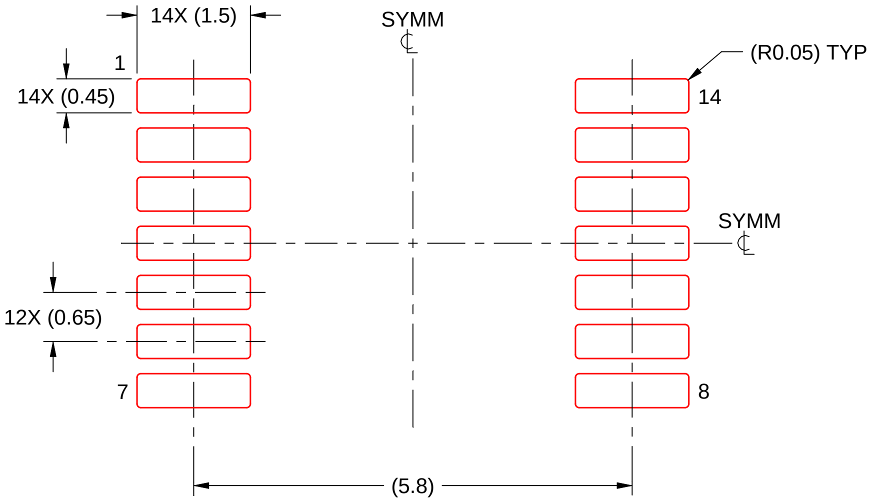
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

最后更新日期：2025 年 10 月