









development

LMK03806 ZHCSHU9K - SEPTEMBER 2011 - REVISED DECEMBER 2023

# 具有 14 个可编程输出的 LMK03806 超低抖动时钟发生器

# 1 特性

- 高性能、超低抖动时钟发生器
- 低抖动:
  - 输出频率为 312.5MHz 时抖动小于 50fs (1.875MHz - 20MHz)
  - 输出频率为 312.5MHz 时抖动小于 150fs (12kHz - 20MHz)
- 从低成本晶体或外部时钟生成多个时钟
- 14 路可编程输出格式 (LVDS、LVPECL、 CMOS)的输出
- 多达8个独特输出频率。
- 工业温度范围: -40°C 至 85°C
- 可调 VCO 频率: 2.37 GHz 2.6 GHz
- 可编程分频器从低成本晶体生成多个时钟。
- 工作电压范围为 3.15V 至 3.45V

## 2 应用

- SONET/SDH 中的超高速串行接口
- 千兆位级以太网和光纤通道线卡
- 用于 RAN 应用的基带单元 (BBU)
- GPON OLT/ONU、高速串行接口(如 PCle、 XAUI、SATA、SAS)
- 时钟 ADC 和 DAC
- 时钟 DSP、微处理器和 FPGA

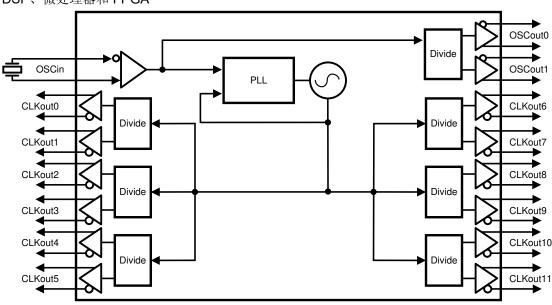
# 3 描述

LMK03806 器件是一款高性能、超低抖动、多速率时 钟发生器,能够在频率高达 2.6GHz 的条件下针对 14 路输出合成8个不同的频率。每个输出时钟可设定为 LVDS、LVPECL 或 LVCMOS 格式。LMK03806 集成 了高性能的整数 N PLL、低噪声 VCO 和可编程输出分 频器,能够以低成本的晶体为 SONET、以太网、光纤 通道、XAUI、背板、PCIe、SATA 和网络处理器生成 多个参考时钟。

### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
LMK03806	WQFN (64)	9.00mm x 9.00mm

- (1) 有关所有可用封装,请参阅节 12。
- (2) 封装尺寸(长×宽)为标称值,并包括引脚(如适用)。



功能方框图



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# 4 Pin Configuration and Functions

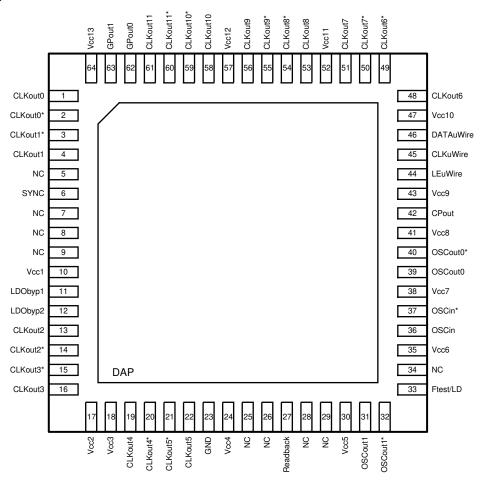


图 4-1. NKD Package 64-Pin WQFN Top View

表 4-1. Pin Functions

PIN		I/O TYPE		DESCRIPTION	
NAME	NO.	] "	1112	DESCRIPTION	
CLKout0, CLKout0*	1, 2	0	Programmable	Clock output 0 (clock group 0).	
CLKout1*, CLKout1	3, 4	0	Programmable	Clock output 1 (clock group 0).	
CLKout2, CLKout2*	13, 14	0	Programmable	Clock output 2 (clock group 1).	
CLKout3*, CLKout3	15, 16	0	Programmable	Clock output 3 (clock group 1).	
CLKout4, CLKout4*	19, 20	0	Programmable	Clock output 4 (clock group 2).	
CLKout5*, CLKout5	21, 22	0	Programmable	Clock output 5 (clock group 2).	
CLKout6, CLKout6*	48, 49	0	Programmable	Clock output 6 (clock group 3).	
CLKout7*, CLKout7	50, 51	0	Programmable	Clock output 7 (clock group 3).	
CLKout8, CLKout8*	53, 54	0	Programmable	Clock output 8 (clock group 4).	
CLKout9*, CLKout9	55, 56	0	Programmable	Clock output 9 (clock group 4).	
CLKout10, CLKout10*	58, 59	0	Programmable	Clock output 10 (clock group 5).	
CLKout11*, CLKout11	60, 61	0	Programmable	Clock output 11 (clock group 5).	
CLKuWire	45	I	CMOS	MICROWIRE Clock Input.	

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# 表 4-1. Pin Functions (续)

PIN					
NAME	NO.	I/O	TYPE	DESCRIPTION	
CPout	42	0	ANLG	Charge pump output.	
DAP	DAP	_	GND	DIE ATTACH PAD, connect to GND.	
DATAuWire	46	I	CMOS	MICROWIRE Data Input.	
Ftest/LD	33	0	Programmable	Multiplexed Lock Detect and Test output pin.	
GND	23	_	PWR	Ground	
GPout0, GPout1	62, 63	0	CMOS	These pins can be programmed for general purpose output.	
LDObyp1	11	_	ANLG	LDO Bypass, bypassed to ground with 10 µF capacitor.	
LDObyp2	12	_	ANLG	LDO Bypass, bypassed to ground with a 0.1 μF capacitor.	
LEuWire	44	I	CMOS	MICROWIRE Latch Enable Input.	
NC	5, 7, 8, 9, 25, 26, 28,29, 34	_	Do Not Connect	These pins must be left floating. Do NOT ground.	
OSCout1, OSCout1*	31, 32	0	LVPECL	Buffered output 1 of OSCin port.	
OSCin, OSCin*	36, 37	I	ANLG	Reference input to PLL. Reference input may be:  A Crystal for use with the internal crystal oscillator circuit.  A XO, TCXO, or other external clock. Must be AC Coupled.	
OSCout0, OSCout0*	39, 40	0	Programmable	Buffered output 0 of OSCin port.	
Readback	27	0	CMOS	Pin that can be used to readback register information.	
SYNC	6	I	CMOS	Clock synchronization input.	
Vcc1	10	_	PWR	Power supply for VCO LDO.	
Vcc2	17	_	PWR	Power supply for clock group 1: CLKout2 and CLKout3.	
Vcc3	18	_	PWR	Power supply for clock group 2: CLKout4 and CLKout5.	
Vcc4	24	_	PWR	Power supply for digital.	
Vcc5	30	_	PWR	Power supply for clock inputs.	
Vcc6	35	_	PWR	Power supply. No bypassing required on this pin.	
Vcc7	38	_	PWR	Power supply for OSCin port.	
Vcc8	41	_	PWR	Power supply for PLL charge pump.	
Vcc9	43	_	PWR	Power supply for PLL.	
Vcc10	47	_	PWR	Power supply for clock group 3: CLKout6 and CLKout7.	
Vcc11	52	_	PWR	Power supply for clock group 4: CLKout8 and CLKout9.	
Vcc12	57	_	PWR	Power supply for clock group 5: CLKout10 and CLKout11.	
Vcc13	64	_	PWR	Power supply for clock group 0: CLKout0 and CLKout1.	

# **5 Specifications**

# 5.1 Absolute Maximum Ratings

See (1) (3).

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage (2)	- 0.3	3.6	V
V <sub>IN</sub>	Input voltage	- 0.3	V <sub>CC</sub> + 0.3	V
T <sub>L</sub>	Lead temperature (solder 4 seconds)		260	°C
T <sub>J</sub>	Junction temperature		150	°C
I <sub>IN</sub>	Differential input current (OSCin/OSCin*)	- 5	5	mA
MSL	Moisture sensitivity level		3	
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Never to exceed 3.6 V.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

# 5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	V
		Machine model (MM)	±150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
T <sub>A</sub>	Ambient temperature	V <sub>CC</sub> = 3.3 V	- 40	25	85	°C
TJ	Junction temperature	V <sub>CC</sub> = 3.3 V			125	°C
V <sub>CC</sub>	Supply voltage		3.15	3.3	3.45	V

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### **5.4 Thermal Information**

		LMK03806	
	THERMAL METRIC <sup>(1)</sup>	NKD (WQFN)	UNIT
		64 PINS	
R <sub>0</sub> JA	Junction-to-ambient thermal resistance on 4-layer JEDEC PCB <sup>(2)</sup>	25.2	°C/W
R <sub>θ JC(top)</sub>	Junction-to-case (top) thermal resistance <sup>(3)</sup>	6.9	°C/W
R <sub>0</sub> JB	Junction-to-board thermal resistance	4.0	°C/W
ψJT	Junction-to-top characterization parameter	0.1	°C/W
ψ ЈВ	Junction-to-board characterization parameter	4.0	°C/W
R <sub>θ JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	0.8	°C/W

- For more information about traditional and new thermal metrics, see the Semiconductors and IC Package Thermal Metrics application report (SPRA953).
- Specification assumes 32 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC PCB. These vias play a key role in improving the thermal performance of the WQFN. Note that the JEDEC PCB is a standard thermal measurement PCB and does not represent best performance a PCB can achieve. TI recommends that the maximum number of vias be used in the board layout. R  $_{\theta}$  JA is unique for each PCB.
- Case is defined as the DAP (die attach pad)

# 5.5 Electrical Characteristics

 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  =  $3.3~V,~T_{A}$  =  $25^{\circ}C,$  at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CO	NSUMPTION				<u> </u>	
I <sub>CC_PD</sub>	Powerdown supply current	No DC path to ground on OSCout1/1*(1)		1		mA
I <sub>CC_CLKS</sub>	Supply current with all clocks enabled <sup>(2)</sup>	CLKoutX_Y_DIV = 16, CLKoutX_TYPE = 1 (LVDS), PLL locked		445		mA
EXTERNAL C	LOCK (OSCin) SPECIFICATIONS	1	,		J.	
f <sub>OSCin</sub>	PLL reference Input <sup>(4)</sup>		1		500	MHz
SLEW <sub>OSCin</sub>	PLL reference clock minimum slew rate on OSCin <sup>(9)</sup>	20% to 80%	0.15	0.5		V/ns
V <sub>OSCin</sub>	Input voltage for OSCin or OSCin*(9)	AC coupled; Single-ended (Unused pin AC coupled to GND)	0.2		2.4	Vpp
V <sub>ID</sub> OSCin	Differential voltage ewing	AC coupled see Ø 6.4	0.2		1.55	V
V <sub>SS</sub> OSCin		AC coupled, see   6-1	0.4		3.1	Vpp
V <sub>OSCin-offset</sub>	DC offset voltage between OSCin/ OSCin* OSCinX* - OSCinX	Each pin AC coupled		20		mV
f <sub>doubler_max</sub>	Doubler input frequency <sup>(9)</sup>	EN_PLL_REF_2X = 1; OSCin Duty Cycle 40% to 60%			155	MHz
CRYSTAL OS	CILLATOR MODE SPECIFICATIONS				'	
f <sub>XTAL</sub>	Crystal frequency range <sup>(9)</sup>	$R_{ESR} \leqslant 40 \Omega$ $C_L \leqslant 20 pF$	16		20.5	MHz
IXTAL	Crystal frequency range.	$R_{ESR} \le 80 \Omega$ $C_L \le 22 pF$	6		16	MHz
P <sub>XTAL</sub>	Crystal power dissipation	Vectron VXB1 crystal, 20.48 MHz, $ \begin{array}{l} {\sf R_{ESR}} \leqslant 40~\Omega \\ {\sf C_L} \leqslant 20~{\sf pF} \end{array} $		120		μW
C <sub>IN</sub>	Input capacitance of the OSCin port	- 40°C to +85°C		6		pF
RMS JITTER	PERFORMANCE					

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 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  =  $3.3~V,~T_{A}$  =  $25^{\circ}C,$  at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
	Integration bandwidth	156.25 MHz, LVDS/LVPECL	81	fs
	10 kHz to 1 MHz	312.5 MHz, LVDS/LVPECL	85	fs
		100 MHz, LVDS	139	fs
		100 MHz, LVPECL	117	fs
		106.25 MHz, LVDS	145	fs
		106.25 MHz, LVPECL	126	fs
	Integration bandwidth 12 kHz to 20 MHz	156.25 MHz, LVDS	111	fs
. (44) (45)	TE KI IE to EO WII IE	156.25 MHz, LVPECL	100	fs
XO mode <sup>(14)</sup> (15) (16)		312.5 MHz, LVDS	108	fs
(10)		312.5 MHz, LVPECL	95	fs
		622.08 MHz, LVDS/LVPECL	141	fs
	Integration bandwidth	106.25 MHz, LVDS	78	fs
	637 kHz to 10 MHz	106.25 MHz, LVPECL	60	fs
	Integration bandwidth 1.875 MHz to 20 MHz	156.25 MHz, LVDS	70	fs
		156.25 MHz, LVPECL	57	fs
		312.5 MHz, LVDS	57	fs
		312.5 MHz, LVPECL	43	fs
	Integration bandwidth 10 kHz to 1 MHz	156.25 MHz, LVDS/LVPECL	190	fs
		312.5 MHz, LVDS/LVPECL	200	fs
		100 MHz, LVDS	235	fs
		100 MHz, LVPECL	210	fs
		106.25 MHz, LVDS	280	fs
		106.25 MHz, LVPECL	250	fs
	Integration bandwidth 12 kHz to 20 MHz	156.25 MHz, LVDS	200	fs
		156.25 MHz, LVPECL	195	fs
Crystal mode jitter <sup>(10)</sup> (11) (12)		312.5 MHz, LVDS	220	fs
,		312.5 MHz, LVPECL	190	fs
		622.08 MHz, LVDS/LVPECL	255	fs
	Integration bandwidth	106.25 MHz, LVDS	90	fs
	637 kHz to 10 MHz	106.25 MHz, LVPECL	65	fs
		156.25 MHz, LVDS	75	fs
	Integration bandwidth	156.25 MHz, LVPECL	65	fs
	1.875 MHz to 20 MHz	312.5 MHz, LVDS	60	fs
		312.5 MHz, LVPECL	45	fs

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 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  = 3.3 V,  $T_{A}$  = 25°C, at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

	luct characterization and are not e PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PHASE NOISE F	PERFORMANCE					
		10 kHz		- 142		dBc/Hz
PHASE NOISE P		100 kHz		- 143		dBc/Hz
		1 MHz		- 157		dBc/Hz
	100 MHz (LVDS/LVPECL)(14)	10 MHz (LVDS)		- 159		dBc/Hz
		20 MHz (LVDS)		- 160		dBc/Hz
		10 MHz (LVPECL)		- 160		dBc/Hz
		20 MHz (LVPECL)		- 161		dBc/Hz
		10 kHz		- 141		dBc/Hz
		100 kHz		- 140		dBc/Hz
		1 MHz		- 156		dBc/Hz
	106.25 MHz (LVDS/LVPECL) <sup>(15)</sup>	10 MHz (LVDS)		- 159		dBc/Hz
		20 MHz (LVDS)		- 160		dBc/Hz
		10 MHz (LVPECL)		- 162		dBc/Hz
		20 MHz (LVPECL)		- 163		dBc/Hz
		10 kHz		- 139		dBc/Hz
		100 kHz		- 140		dBc/Hz
		1 MHz		- 153		dBc/Hz
XO mode phase noise	156.25 MHz (LVDS/LVPECL) <sup>(14)</sup>	10 MHz (LVDS)		- 159		dBc/Hz
		20 MHz (LVDS)		- 159		dBc/Hz
		10 MHz (LVPECL)		- 160		dBc/Hz
		20 MHz (LVPECL)		- 160		dBc/Hz
		10 kHz		- 132		dBc/Hz
		100 kHz		- 133		dBc/Hz
		1 MHz		- 148		dBc/Hz
	312.5 MHz (LVDS/LVPECL) <sup>(14)</sup>	10 MHz (LVDS)		- 154		dBc/Hz
		20 MHz (LVDS)		- 155		dBc/Hz
		10 MHz (LVPECL)		- 157		dBc/Hz
		20 MHz (LVPECL)		- 158		dBc/Hz
		10 kHz		- 123		dBc/Hz
		100 kHz		- 121		dBc/Hz
		1 MHz		- 143		dBc/Hz
	622.08 MHz (LVDS/LVPECL) <sup>(16)</sup>	10 MHz (LVDS)		- 154		dBc/Hz
		20 MHz (LVDS)		- 154		dBc/Hz
		10 MHz (LVPECL)		- 157		dBc/Hz
ı		20 MHz (LVPECL)		- 158		dBc/Hz

 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  = 3.3~V,  $T_{A}$  =  $25^{\circ}C,$  at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

	PARAMETER	TEST CONDITIONS	MIN TYP N	IAX UNIT
	100 MHz (LVDS/LVPECL) <sup>(10)</sup>	10 kHz	- 129	dBc/Hz
		100 kHz	- 137	dBc/Hz
		1 MHz	- 156	dBc/Hz
	100 MHz (LVDS/LVPECL) <sup>(10)</sup>	10 MHz (LVDS)	- 158	dBc/Hz
		20 MHz (LVDS)	- 159	dBc/Hz
		10 MHz (LVPECL)	- 160	dBc/Hz
		20 MHz (LVPECL)	- 161	dBc/Hz
		10 kHz	- 124	dBc/Hz
		100 kHz	- 137	dBc/Hz
		1 MHz	- 156	dBc/Hz
	106.25 MHz (LVDS/LVPECL) <sup>(11)</sup>	10 MHz (LVDS)	- 158	dBc/Hz
		20 MHz (LVDS)	- 159	dBc/Hz
		10 MHz (LVPECL)	- 160	dBc/Hz
		20 MHz (LVPECL)	- 161	dBc/Hz
	156.25 MHz (LVDS/LVPECL) <sup>(10)</sup>	10 kHz	- 125	dBc/Hz
		100 kHz	- 132	dBc/Hz
		1 MHz	- 153	dBc/Hz
Crystal mode phase noise		10 MHz (LVDS)	- 158	dBc/Hz
p.1.0.00		20 MHz (LVDS)	- 159	dBc/Hz
		10 MHz (LVPECL)	- 160	dBc/Hz
		20 MHz (LVPECL)	- 160	dBc/Hz
		10 kHz	- 119	dBc/Hz
		100 kHz	- 126	dBc/Hz
		1 MHz	- 147	dBc/Hz
	312.5 MHz (LVDS/LVPECL) <sup>(10)</sup>	10 MHz (LVDS)	- 153	dBc/Hz
		20 MHz (LVDS)	- 154	dBc/Hz
		10 MHz (LVPECL)	- 156	dBc/Hz
		20 MHz (LVPECL)	- 157	dBc/Hz
		10 kHz	- 110	dBc/Hz
		100 kHz	- 120	dBc/Hz
		1 MHz	- 140	dBc/Hz
	622.08 MHz (LVDS/LVPECL) <sup>(12)</sup>	10 MHz (LVDS)	- 153	dBc/Hz
		20 MHz (LVDS)	- 153	dBc/Hz
		10 MHz (LVPECL)	- 154	dBc/Hz
		20 MHz (LVPECL)	- 154	dBc/Hz

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 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  = 3.3 V,  $T_{A}$  = 25°C, at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
PLL PHASE DE	TECTOR AND CHARGE PUMP SPECIFI	CATIONS			
f <sub>PD</sub>	Phase detector frequency			155	MHz
		V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 0	100		μA
	DI Laboratoria de la companya de la	V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 1	400		μA
I <sub>CPout</sub> SOURCE	PLL charge pump source current	V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 2	1600		μA
		V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 3	3200		μA
		V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 0	- 100		μA
I CINIZ	Did sharms mayon sink summer	V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 1	- 400		μA
I <sub>CPout</sub> SINK	PLL charge pump sink current	V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 2	- 1600		μA
		V <sub>CPout</sub> =V <sub>CC</sub> /2, PLL_CP_GAIN = 3	- 3200		μA
I <sub>CPout</sub> %MIS	Charge pump sink/source mismatch	V <sub>CPout</sub> =V <sub>CC</sub> /2, T <sub>A</sub> = 25°C	3%	10%	
$I_{CPout}V_{TUNE}$	Magnitude of charge pump current vs. charge pump voltage variation	0.5 V < V <sub>CPout</sub> < V <sub>CC</sub> - 0.5 V T <sub>A</sub> = 25°C	4%		
I <sub>CPout</sub> %TEMP	Charge pump current vs. temperature variation		4%		
I <sub>CPout</sub> TRI	Charge pump leakage	0.5 V < V <sub>CPout</sub> < V <sub>CC</sub> - 0.5 V		10	nA
PN10kHz	PLL 1/f noise at 10 kHz offset <sup>(5)</sup> .  Normalized to  1-GHz output frequency	PLL_CP_GAIN = 400 µA	- 118		dBc/Hz
		PLL_CP_GAIN = 3200 µA	- 121		dBc/Hz
DNI411-	Normalized phase noise contribution <sup>(6)</sup>	PLL_CP_GAIN = 400 μA	- 222.5		dBc/Hz
PN1Hz		PLL_CP_GAIN = 3200 μA	- 227		dBc/Hz
	PLL phase noise (Assumes a very wide bandwidth, noiseless crystal, 2500-MHz output frequency, and 25-MHz phase detector	1-kHz Offset	- 93		dBc/Hz
1 (5)		10 kHz	- 103		dBc/Hz
L(f)		100-kHz Offset	- 116		dBc/Hz
	frequency)	1-MHz Offset	- 116		dBc/Hz
INTERNAL VCC	SPECIFICATIONS				
f <sub>VCO</sub>	VCO tuning range		2370	2600	MHz
	Fine tuning sensitivity	f <sub>VCO</sub> at low end	16		
K <sub>vco</sub>	(The range displayed in the typical column indicates the lower sensitivity is typical at the lower end of the tuning range, and the higher tuning sensitivity is typical at the higher end of the tuning range).	$f_{VCO}$ at high end	21		MHz/V
∆T <sub>CL</sub>	Allowable temperature drift for continuous lock <sup>(7)</sup> (9)  After programming R30 for lock, no changes to output configuration are permitted to guarantee continuous lock			125	°C
	Phase noise	10-kHz Offset	- 87		dBc/Hz
L(f)	(Assumes a very narrow loop	100-kHz Offset	- 112		dBc/Hz
	bandwidth)	1-MHz Offset	- 133		dBc/Hz

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 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  =  $3.3~V,~T_{A}$  =  $25^{\circ}C,$  at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		LVDS-to-LVDS, T = 25°C, $f_{CLK}$ = 800 MHz, $R_L$ = 100 $\Omega$ AC coupled		30		ps
T <sub>SKEW</sub>	Maximum CLKoutX to CLKoutY <sup>(8)</sup> (9)	LVPECL-to-LVPECL, T = 25°C, $f_{CLK}$ = 800 MHz, $R_L$ = 100 $\Omega$ emitter resistors = 240 $\Omega$ to GND AC coupled		30		ps
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout <sup>(8)</sup> (9)	$R_L = 50 \Omega$ , $C_L = 5 pF$ , $T = 25^{\circ}C$ , $F_{CLK} = 100 MHz$ . <sup>(8)</sup>		100		ps
Mixed <sub>SKEW</sub>	ed <sub>SKEW</sub> LVDS or LVPECL to LVCMOS Same device, T = 25°C, 250 MHz			750		ps
LVDS CLOCK	OUTPUTS (CLKoutX), CLKoutX_TYPE =	1			1	
f <sub>CLKout</sub>	Operating frequency <sup>(9)</sup> (13)	R <sub>L</sub> = 100 Ω			1300	MHz
V <sub>OD</sub>	Differential automotive to the market of		250	400	450	mV
V <sub>SS</sub>	Differential output voltage 图 6-2		500	800	900	mVpp
ΔV <sub>OD</sub>	Change in magnitude of V <sub>OD</sub> for complementary output states	T = 25°C, DC measurement AC-coupled to receiver input	- 50		50	mV
Vos	Output offset voltage $R = 100-\Omega$ differential termination		1.125	1.25	1.375	V
ΔV <sub>OS</sub>	Change in V <sub>OS</sub> for complementary output states				35	mV
т /т	Output rise time	20% to 80%, R <sub>L</sub> = 100 Ω		200		ps
$T_R/T_F$	Output fall time	80% to 20%, $R_L$ = 100 $\Omega$		200		ps
I <sub>SA</sub> I <sub>SB</sub>	Output short circuit current - single- ended	Single-ended output shorted to GND, T = 25°C	- 24		24	mA
I <sub>SAB</sub>	Output short circuit current - differential	Complimentary outputs tied together, T = 25°C	- 12		12	mA
LVPECL CLO	CK OUTPUTS (CLKoutX)					
f <sub>CLKout</sub>	Operating frequency <sup>(9)</sup> (13)				1300	MHz
	20% to 80% output rise	$R_L = 100 \Omega$ , emitter resistors =				
T <sub>R</sub> / T <sub>F</sub>	80% to 20% output fall time	240 Ω to GND CLKoutX_TYPE = 4 or 5 (1600 or 2000 mVpp)		150		ps

Product Folder Links: LMK03806

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 $3.15~V \leqslant V_{CC} \leqslant 3.45~V,~-40^{\circ}C \leqslant T_{A} \leqslant 85^{\circ}C,$  Junction Temperature  $T_{J} \leqslant 125^{\circ}C.$  Typical values represent most likely parametric norms at  $V_{CC}$  = 3.3~V,  $T_{A}$  =  $25^{\circ}C,$  at *Recommended Operating Conditions* at the time of product characterization and are not ensured. (3)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
700-mVpp L\	PECL CLOCK OUTPUTS (CLKoutX),	CLKoutX_TYPE = 2				
V <sub>OH</sub>	Output high voltage		V <sub>C</sub>	<sub>C</sub> - 1.03		V
V <sub>OL</sub>	Output low voltage	T = 25°C, DC measurement Termination = 50 $\Omega$ to	V <sub>C</sub>	<sub>C</sub> - 1.41		V
V <sub>OD</sub>	Output wells as 图 C O	V <sub>CC</sub> = 1.4 V	305	380	440	mV
V <sub>SS</sub>	Output voltage 图 6-2		610	760	880	mVpp
1200-mVpp L	VPECL CLOCK OUTPUTS (CLKoutX	), CLKoutX_TYPE = 3				
V <sub>OH</sub>	Output high voltage		V <sub>CC</sub> - 1.07			V
V <sub>OL</sub>	Output low voltage	T = 25°C, DC measurement  Termination = 50 $\Omega$ to	V <sub>CC</sub> - 1.69			V
V <sub>OD</sub>	Output voltage Ø 6 2	V <sub>CC</sub> - 1.7 V	545	625	705	mV
V <sub>SS</sub>	Output voltage 图 6-2		1090	1250	1410	mVpp
1600-mVpp l	VPECL CLOCK OUTPUTS (CLKoutX	), CLKoutX_TYPE = 4				
V <sub>OH</sub>	Output high voltage		V <sub>C</sub>	<sub>C</sub> - 1.10		V
V <sub>OL</sub>	Output low voltage	T = 25°C, DC Measurement  Termination = 50 $\Omega$ to	V <sub>CC</sub> - 1.97			V
V <sub>OD</sub>	Output wells as 图 C O	V <sub>CC</sub> - 2 V	660	870	965	mV
V <sub>SS</sub>	Output voltage 图 6-2		1320	1740	1930	mVpp
2000-mVpp l	VPECL (2VPECL) CLOCK OUTPUTS	(CLKoutX), CLKoutX_TYPE = 5				
V <sub>OH</sub>	Output high voltage		V <sub>CC</sub> - 1.13			V
V <sub>OL</sub>	Output low voltage	T = 25°C, DC Measurement Termination = 50 $\Omega$ to	V <sub>C</sub>	<sub>C</sub> - 2.20		V
V <sub>OD</sub>	Output wells as 图 C O	V <sub>CC</sub> - 2.3 V	800	1070	1200	mV
V <sub>SS</sub>	Output voltage 图 6-2		1600	2140	2400	mVpp
LVCMOS CL	OCK OUTPUTS (CLKoutX)	·				
f <sub>CLKout</sub>	Operating frequency <sup>(9)</sup>	5-pF Load			250	MHz
V <sub>OH</sub>	Output high voltage	1-mA Load	V <sub>CC</sub> - 0.1			V
V <sub>OL</sub>	Output low voltage	1-mA Load			0.1	V
I <sub>OH</sub>	Output high current (Source)	V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		28		mA
I <sub>OL</sub>	Output low current (Sink)	V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		28		mA
DUTY <sub>CLK</sub>	Output duty cycle <sup>(9)</sup>	$V_{CC}/2$ to $V_{CC}/2$ , $F_{CLK}$ = 100 MHz, $T$ = 25°C	45	50	55	%
T <sub>R</sub>	Output rise time	20% to 80%, R <sub>L</sub> = 50 $\Omega$ , CL = 5 pF	400			ps
T <sub>F</sub>	Output fall time	80% to 20%, R <sub>L</sub> = 50 $\Omega$ , CL = 5 pF	400			ps
DIGITAL OU	TPUTS (Ftest/LD, Readback, GPoutX)	)	1		Į.	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -500 μA	V <sub>CC</sub> - 0.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 500 μA			0.4	V

3.15 V  $\leq$  V<sub>CC</sub>  $\leq$  3.45 V,  $^-$  40°C  $\leq$  T<sub>A</sub>  $\leq$  85°C, Junction Temperature T<sub>J</sub>  $\leq$  125°C.

Typical values represent most likely parametric norms at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C, at Recommended Operating Conditions at the time of product characterization and are not ensured. (3)

PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
UTS (SYNC)				
High-level input voltage		1.6	V <sub>CC</sub>	V
Low-level input voltage			0.4	V
UTS (CLKuWire, DATAuWire, LEuWire)		•		
High-level input voltage		1.6	V <sub>CC</sub>	V
Low-level input voltage			0.4	V
High-level input current	V <sub>IH</sub> = V <sub>CC</sub>	5	25	μA
Low-level input current	V <sub>IL</sub> = 0	- 5	5	μA
	High-level input voltage Low-level input voltage  JTS (CLKuWire, DATAuWire, LEuWire)  High-level input voltage  Low-level input voltage  High-level input current	High-level input voltage  Low-level input voltage  JTS (CLKuWire, DATAuWire, LEuWire)  High-level input voltage  Low-level input voltage  High-level input current  V <sub>IH</sub> = V <sub>CC</sub>	High-level input voltage Low-level input voltage  JTS (CLKuWire, DATAuWire, LEuWire)  High-level input voltage  Low-level input voltage  1.6  Low-level input voltage  High-level input current  V <sub>IH</sub> = V <sub>CC</sub> 5	High-level input voltage 1.6 $V_{CC}$ Low-level input voltage 0.4  JTS (CLKuWire, DATAuWire, LEuWire)  High-level input voltage 1.6 $V_{CC}$ Low-level input voltage 0.4  High-level input voltage 5.25

- If emitter resistors are placed on the OSCout1/1\* pins, there will be a DC current to ground which will cause powerdown lcc to (1)
- Load conditions for output clocks: LVDS: 100 Ω differential. See Current Consumption and Power Dissipation Calculations for Icc for (2) specific part configuration and how to calculate lcc for a specific design.
- In order to meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device will function at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.
- F<sub>OSCin</sub> maximum frequency guaranteed by characterization. Production tested at 200 MHz.
- A specification in modeling PLL in-band phase noise is the 1/f flicker noise, L<sub>PLL flicker</sub>(f), which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10kHz = L<sub>PL1 flicker</sub>(10 kHz) - 20log(Fout / 1 GHz), where L<sub>PLL flicker</sub>(f) is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure L<sub>PLL</sub> flicker(f) it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). LPLL flicker(f) can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of L<sub>PLL flicker</sub>(f) and L<sub>PLL flat</sub>(f).
- A specification modeling PLL in-band phase noise. The normalized phase noise contribution of the PLL, L<sub>PLL</sub> flat(f), is defined as:  $PN1HZ = L_{PLL\_flat}(f) - 20log(N) - 10log(f_{PD}). \ L_{PLL\_flat}(f) \ is \ the \ single \ side \ band \ phase \ noise \ measured \ at \ an \ offset \ frequency, f, in \ a \ 1 \ Hz$ bandwidth and  $f_{PD}$  is the phase detector frequency of the synthesizer.  $L_{PLL\_flat}(f)$  contributes to the total noise, L(f).
- Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R30 register was last programmed, and still have the part stay in lock. The action of programming the R30 register, even to the same value, activates a frequency calibration routine. This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R30 register to ensure it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of -40°C to 85°C without violating specifications.
- Equal loading and identical clock output configuration on each clock output is required for specification to be valid.
- (9) Guaranteed by characterization.

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- (10) Jitter and phase noise data for 100 MHz, 156.25, and 312.5 MHz collected using an ECS crystal, part number ECS-200-20-30B-DU. Loop filter values are C1 = 220 pF, C2 = 18 nF, R2 = 820  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, R4 = 200  $\Omega$ . Charge pump current = 3.2 mA. LVPECL emitter resistors,  $R_e$  = 240  $\Omega$ . Reference doubler disabled. VCO frequency = 2500 MHz using a phase detector frequency = 20 MHz the loop bandwidth = 62 kHz and phase margin = 76°.
- (11) Jitter and phase noise data for 106.25 MHz collected using an ECS crystal, part number ECS-200-20-30B-DU. Loop filter values are C1 = 220 pF, C2 = 18 nF, R2 = 820  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, R4 = 200  $\Omega$ . Charge pump current = 3.2 mA. LVPECL emitter resistors,  $R_e = 240 \Omega$ . Reference doubler disabled. VCO frequency = 2550 MHz using a phase detector frequency = 10 MHz the loop bandwidth = 32 kHz and phase margin = 69°.
- Jitter and phase noise data for 622.08 MHz collected using a Vectron crystal, part number VXB1-1137-15M360. Loop filter values are C1 = 100 pF, C2 = 120 nF, R2 = 470 \( \Omega\), C3 = 10 pF, R3 = 200 \( \Omega\), C4 = 10 pF, R4 = 200 \( \Omega\), Charge pump current = 3.2 mA, LVPECL emitter resistors, R<sub>e</sub> = 240 Ω. Reference doubler enabled. VCO frequency = 2488.32 MHz using a phase detector frequency = 30.72 MHz the loop bandwidth = 54 kHz and phase margin = 86°.
- (13) Refer to typical performance charts for output operation performance at higher frequencies than the minimum maximum output frequency.
- (14) Jitter and phase noise data for 100 MHz, 156.25, and 312.5 MHz collected using a Wenzel crystal oscillator, part number 501 -04623G. Loop filter values are C1 = 39 pF, C2 = 3.3 nF, R2 = 680  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, R4 = 200  $\Omega$ . Charge pump current = 3.2 mA. LVPECL emitter resistors, R<sub>e</sub> = 240 Ω. Reference doubler disabled. VCO frequency = 2500 MHz using a phase detector frequency = 100 MHz the loop bandwidth = 80 kHz and phase margin = 60°.
- (15) Jitter and phase noise data for 106.25 MHz collected using a Wenzel crystal oscillator, part number 501 04623G. Loop filter values are C1 = 39pF, C2 = 3.3 nF, R2 = 820  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, R4 = 200  $\Omega$ . Charge pump current = 3.2 mA. LVPECL



- emitter resistors,  $R_e$  = 240  $\Omega$ . Reference doubler disabled. VCO frequency = 2550 MHz using a phase detector frequency = 10 MHz the loop bandwidth = 80 kHz and phase margin = 60°.
- (16) Jitter and phase noise data for 622.08 MHz collected using a Crystec oscillator, part number CVHD-950. Loop filter values are C1 = 39 pF, C2 = 3.3 nF, R2 = 680  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, R4 = 200  $\Omega$ . Charge pump current = 3.2 mA. LVPECL emitter resistors,  $R_e$  = 240  $\Omega$ . Reference doubler enabled. VCO frequency = 2488.32 MHz using a phase detector frequency = 30.72 MHz the loop bandwidth = 80 kHz and phase margin = 60°.

# 5.6 Timing Requirements

See *Programming* for additional information

			MIN	NOM	MAX	UNIT
T <sub>ECS</sub>	LE to clock set-up time	See 图 5-1	25			ns
T <sub>DCS</sub>	Data to clock set-up time	See 图 5-1	25			ns
T <sub>CDH</sub>	Clock to data hold time	See 图 5-1	8			ns
T <sub>CWH</sub>	Clock pulse width high	See 图 5-1	25			ns
T <sub>CWL</sub>	Clock pulse width low	See 图 5-1	25			ns
T <sub>CES</sub>	Clock to LE set-up time	See 图 5-1	25			ns
T <sub>EWH</sub>	LE pulse width	See 图 5-1	25			ns
T <sub>CR</sub>	Falling clock to readback time	See READBACK	25			ns

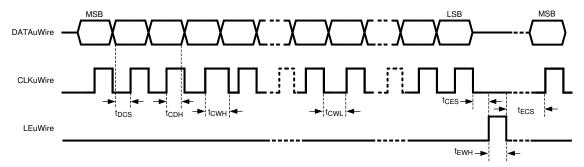


图 5-1. MICROWIRE Timing Diagram

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# **5.7 Typical Characteristics**

# **Clock Output AC Characteristics**

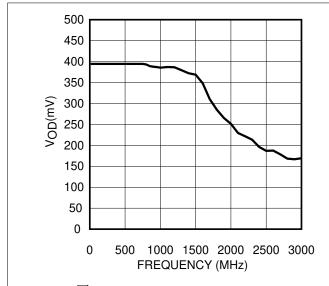


图 5-2. LVDS V<sub>OD</sub> vs Frequency

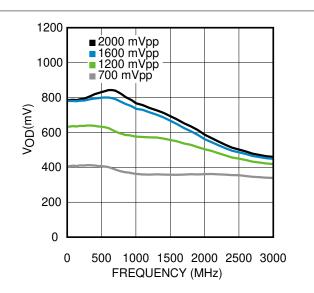


图 5-3. LVPECL With 240-Ω Emitter Resistors V<sub>OD</sub> vs Frequency

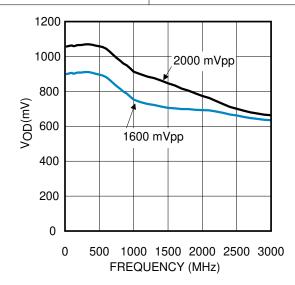


图 5-4. LVPECL With 120- $\Omega$  Emitter Resistors V<sub>OD</sub> vs Frequency

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# **6 Parameter Measurement Information**

# 6.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically  $V_{ID}$  or  $V_{OD}$  depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is  $V_{SS}$  and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair.  $V_{SS}$  can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of  $V_{CD}$  as described in the first description.

 $V_{ID}$  and  $V_{OD}$  are often defined as volts (V) and  $V_{SS}$  is often defined as volts peak-to-peak ( $V_{PP}$ ).

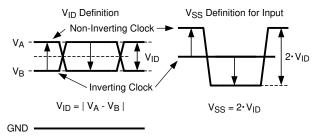


图 6-1. Two Different Definitions for Differential Input Signals

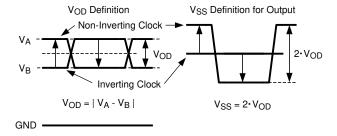


图 6-2. Two Different Definitions for Differential Output Signals

Refer to application note AN-912, Common Data Transmission Parameters and their Definitions (SNLA036) for more information.

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# 7 Detailed Description

## 7.1 Overview

The LMK03806 is an ultra-low-noise clock generator that integrates a high-performance integer-N PLL, lownoise VCO, and flexible output clock division/fan-out with 14 programmable drivers. It operates with a standard off-the-shelf crystal or low noise external clock as the reference oscillator input (OSCin).

The integrated VCO tuning range is from 2370 to 2600 MHz. The VCO clock drives 6 output dividers that support a divide range of 1 to 1045 (even and odd) with 50% output duty cycle. Each output divider feeds 2 output drivers for a total of 12 CLKoutX outputs. Each CLKoutX driver is programmable to LVDS, LVPECL, or 2x LVCMOS 3.3-V output levels and synchronized by means of the SYNC input pin.

The device provides 2 additional outputs (OSCout0 and OSCout1) that are buffered or divided-down copies of the OSCin input. The divide value for the OSCoutX outputs can be set independently by programming the OSC divider. The OSC divider value range is 1 to 8. The OSCout0 driver is programmable to LVDS, LVPECL or 2x LVCMOS 3.3-V output levels. The OSCout1 driver supports LVPECL output levels only.

The LMK03806 has programmable 3rd and 4th order loop filter resistors and capacitors for the internal PLL. The integrated programmable resistors and capacitors compliment external loop filter components mounted near the chip. These integrated components can be disabled through register programming. The device registers are programmable through serial Microwire interface.

# 7.2 Functional Block Diagrams

▼ 7-1 shows the complete LMK03806 block diagram.

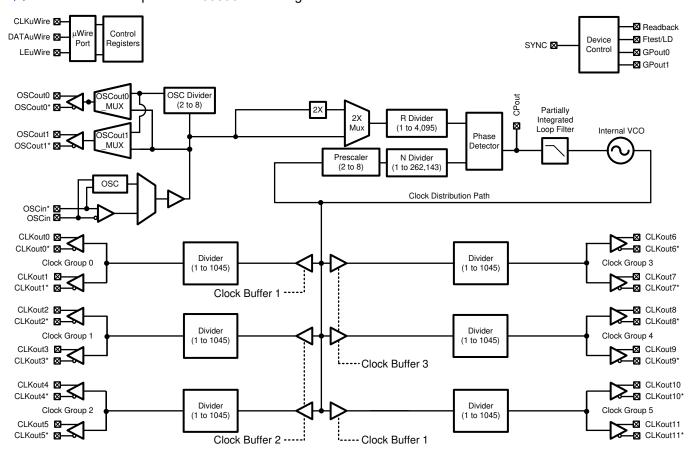


图 7-1. Detailed LMK03806 Block Diagram

Product Folder Links: LMK03806

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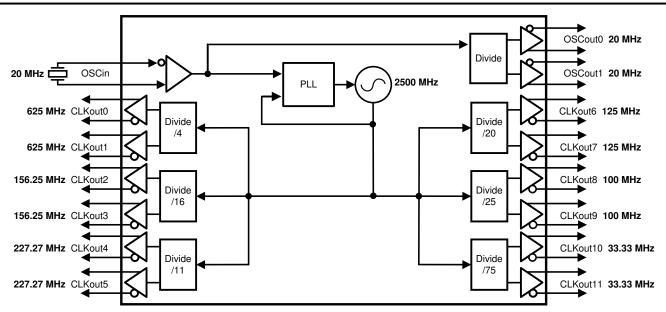


图 7-2. 10-Gigabit Ethernet Reference Clocks

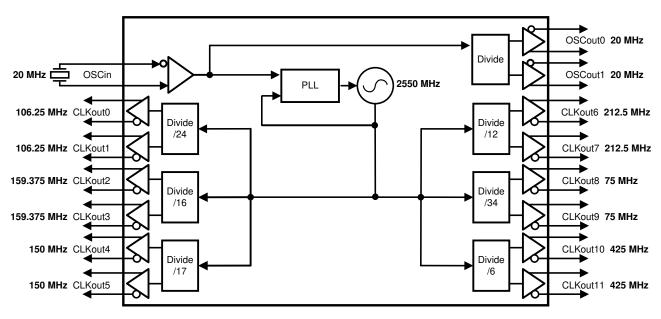


图 7-3. Fiber Channel Reference Clocks

Product Folder Links: LMK03806

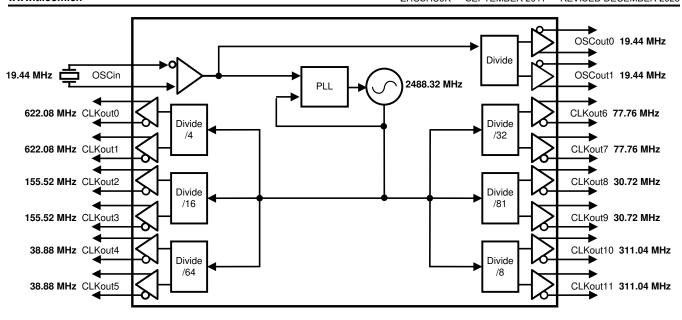


图 7-4. SONET/SDH Reference Clocks

# 7.3 Features Description

### 7.3.1 Serial MICROWIRE Timing Diagram and Terminology

Register programming information on the DATAuWire pin is clocked into a shift register on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the register is sent from the shift register to the register addressed. A few programming considerations are listed below:

- A slew rate of at least 30 V/us is recommended for the programming signals
- After the programming is complete, the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state
- If the CLKuWire or DATAuWire lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

#### 7.3.2 Crystal Support With Buffered Outputs

The LMK03806 provides 2 dedicated outputs which are a buffered copy of the PLL reference input. This reference input is typically a low noise external clock or Crystal.

The OSCout0 buffer output type is programmable to LVDS, LVPECL, or LVCMOS. The OSCout1 buffer is fixed to LVPECL.

The dedicated output buffers OSCout0 and OSCout1 can output frequency lower than the Input frequency by programming the OSC Divider. The OSC Divider value range is 1 to 8. Each OSCoutX can individually choose to use the OSC Divider output or to bypass the OSC Divider.

Crystal buffered outputs cannot be synchronized to the VCO clock distribution outputs. The assertion of SYNC will still cause these outputs to become low. Since these outputs will turn off and on asynchronously with respect to the VCO sourced clock outputs during a SYNC, it is possible for glitches to occur on the buffered clock outputs when SYNC is asserted and unasserted. If the NO\_SYNC\_CLKoutX\_Y bits are set these outputs will not be affected by the SYNC event except that the phase relationship will change with the other synchronized clocks unless a buffered clock output is used as a qualification clock during SYNC.

#### 7.3.3 Integrated Loop Filter Poles

The LMK03806 features programmable 3rd and 4th order loop filter poles for PLL. These internal resistors and capacitor values may be selected from a fixed range of values to achieve either a 3rd or 4th order loop filter

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response. The integrated programmable resistors and capacitors compliment external components mounted near the chip.

These integrated components can be effectively disabled by programming the integrated resistors and capacitors to their minimum values.

## 7.3.4 Integrated VCO

The output of the internal VCO is routed to the Clock Distribution Path and also fed back to the PLL phase detector through a prescaler and N-divider.

#### 7.3.5 Clock Distribution

The LMK03806 features a total of 12 outputs driven from the internal VCO.

All VCO driven outputs have programmable output types. They can be programmed to LVPECL, LVDS, or LVCMOS. When all distribution outputs are configured for LVCMOS or single-ended LVPECL a total of 24 outputs are available.

### 7.3.5.1 CLKout DIvider

Each clock group, which is a pair of outputs such as CLKout0 and CLKout1, has a single clock output divider. The divider supports a divide range of 1 to 1045 (even and odd) with 50% output duty cycle. When divides of 26 or greater are used, the divider block uses extended mode.

## 7.3.5.2 Programmable Output Type

For increased flexibility all LMK03806 clock outputs (CLKoutX) and OSCout0 can be programmed to an LVDS, LVPECL, or LVCMOS output type. OSCout1 is fixed as LVPECL.

Any LVPECL output type can be programmed to 700-, 1200-, 1600-, or 2000-mVpp amplitude levels. The 2000-mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000-mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

### 7.3.5.3 Clock Output Synchronization

Using the SYNC input causes all active clock outputs to share a rising edge.

By toggling the SYNC\_POL\_INV bit, it is possible to generate a SYNC through uWire eliminating the need for connecting the external SYNC pin to external circuitry.

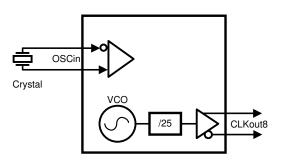
### 7.3.6 Default Start-Up Clocks

Before the LMK03806 is programmed some clocks will operate at default frequencies upon power up. The active output clocks depend upon the reference input type. If a crystal reference is used with OSCin, only CLKout8 will operate at a nominal VCO frequency /25. When an XO or other external reference is used as a reference with OSCin, OSCout0 will buffer the OSCin frequency in addition to CLKout8 operating at a nominal VCO frequency /25. These clocks can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, and so forth, before the LMK03806 is programmed. Refer to \$\mathbb{Z}\$ 7-5 or \$\mathbb{Z}\$ 7-6 for illustration of start-up clocks.

The nominal VCO frequency of CLKout8 on power up will typically be 98 MHz.

Note during programming CLKout8 may momentarily stop or glitch during the VCO calibration routine.

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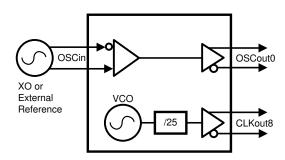


图 7-5. Start-Up Clock Using Crystal Reference

图 7-6. Start-Up Clock Using XO or Other External Reference

## 7.4 Device Functional Modes

By using the tunable range of the VCO followed by a programmable divider, the LMK03806 can achieve any of the frequencies in  $\frac{1}{2}$  7-1.

表 7-1. Achievable Frequencies

ACHIEVED FREQUENCY (MHZ)
0070 0000
2370 - 2600
1185 - 1300
790 - 866.7
592.5 - 650
474 - 520
395.7 - 433
338.6 - 371.4
296.25 - 325
263.3 - 288.9
237 - 260
Any frequency in the range of 2.27 - 236.36

表 7-2. Common Frequency Plans

STANDARD/APPLICATION	OUTPUT FREQUENCIES (MHZ)	VCO FREQUENCY	RECOMMENDED CRYSTAL VALUE
Infiniband	100, 200		
SATA	75, 150, 300, 600	2400 MHz	
SAS	37.5, 75, 120, 150		
Fast Ethernet	25		
1 GbE	125		20 MHz
10 GbE	156.25, 312.5, 625	2500 MHz	20 MH2
XAUI	78.125, 156.25, 312.5		
Backplane	227.27		
2G/4G/16G Fiber Channel	106.25, 212.5	2550 MHz	
10G Fiber Channel	159.375	2000 IVITZ	
40/100 GbE	644.53125, 322.265625, 161.1328125	2578.125 MHz	12.5 MHz
SONET	19.44, 38.88, 77.76, 155.52, 311.04, 622.08	2488.32 MHz	19.44 MHz
A/D Clocking	30.72, 61.44, 122.88, 153.6, 245.76, 491.52, 983.04	2457.6 MHz	19.2 MHz or 12.288 MHz

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# 7.5 Programming

### 7.5.1 General Information

LMK03806 devices are programmed using 32-bit registers. Each register consists of a 5-bit address field and 27-bit data field. The address field is formed by bits 0 through 4 (LSBs) and the data field is formed by bits 5 through 31 (MSBs). The contents of each register is clocked in MSB first (bit 31), and the LSB (bit 0) last. During programming, the LEuWire signal should be held *low*. The serial data is clocked in on the rising edge of the CLKuWire signal. After the LSB (bit 0) is clocked in the LEuWire signal should be toggled *low-to-high-to-low* to latch the contents into the register selected in the address field. TI recommends to program registers in numeric order, for example R0 to R14, R16, R24, R26, and R28 to R31 to achieve proper device operation. Refer to the *Timing Requirements* for the timing for the programming.

To achieve proper frequency calibration, the OSCin port must be driven with a valid signal before programming register R30. Changes to PLL R divider or the OSCin port frequency require register R30 to be reloaded in order to activate the frequency calibration process.

# 7.5.1.1 Special Programming Case for R0 to R5 for CLKoutX\_Y\_DIV > 25

When programming register R0 to R5 to change the CLKoutX\_Y\_DIV divide value, the register must be programmed twice if the CLKoutX\_Y\_DIV value is greater than 25.

# 7.5.1.2 Recommended Initial Programming Sequence

The registers are to be programmed in numeric order with R0 being the first and R31 being the last register programmed as shown below:

- 1. Program R0 with RESET bit = 1. This ensures that the device is configured with default settings. When RESET = 1, all other R0 bits are ignored.
  - If R0 is programmed again during the initial configuration of the device, the RESET bit must be cleared.
- 2. R0 through R5: CLKouts.
  - It is required to program R3 after power up.
  - Program as necessary to configure the clock outputs, CLKout0 to CLKout11 as desired. These registers configure clock output controls such as powerdown, divider value, and clock source select.
- 3. R6 through R8: CLKouts.
  - Program as necessary to configure the clock outputs, CLKout0 to CLKout11 as desired. These registers configure the output format for each clock output.
- 4. R9: Undisclosed bits.
  - Program this register as shown in the register map for proper operation.
- 5. R10: OSCouts.
- 6. R11: SYNC, and XTAL.
- 7. R12: LD pin and SYNC.
- 8. R13: Readback pin & GPout0.
- 9. R14: GPout1.
- 10. R16: Undisclosed bits.
  - · Program this register as shown in the register map for proper operation.
- 11. R24: Partially integrated PLL filter values.
- 12. R26, R28, R29, and R30: PLL.
- 13. R31: uWire readback and uWire lock.

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#### **7.5.1.3 READBACK**

At no time should the MICROWIRE registers be programmed to any value other than what is specified in the datasheet.

For debug of the MICROWIRE interface or programming, TI recommends to simply program an LD\_MUX to active low and then toggle the output type register between output and inverting output while observing the output pin for a low to high transition. For example, to verify MICROWIRE programming, set the LD\_MUX = 0 (Low) and then toggle the LD\_TYPE register between 3 (Output, push-pull) and 4 (Output inverted, pushpull). The result will be that the Ftest/LD pin will toggle from low to high.

Readback from the MICROWIRE programming registers is available. The MICROWIRE readback function can be accessed on the Readback pin. The READBACK\_TYPE register can be programmed to *Output (push-pull)* for active output, or for communication with FPGAs/microcontrollers with lower voltage rails than 3.3 V the READBACK\_TYPE register can be programmed to *Output (Open-Drain)* while connecting an external pull-up resistor to the voltage rail needed.

To perform a readback operation:

- 1. Write the register address to be read back by programming the READBACK ADDR register in R31.
- 2. With the LEuWire pin held low continue to clock the CLKuWire pin. On every falling edge of the CLKuWire pin a new data bit is clocked onto the Readback pin.
- 3. Data is clocked out MSB first. After 32 clocks all the data values will have been read and the read operation is complete. The 5 LSB bits which are the address will be undefined during readback.

#### 7.5.1.3.1 Readback Example

To readback register R3 perform the following steps:

- 1. Write R31 with READBACK\_ADDR = 3. DATAuWire and CLKuWire are toggled as shown in ☒ 5-1 with new data being clocked in on rising edges of CLKuWire
- 2. Toggle LEuWire high and low as shown in \bigsup 5-1.
- 3. Toggle CLKuWire high and then low 32 times to read back all 32 bits of register R3. Data is read MSB first. Data is valid on falling edge of CLKuWire.

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# 8 Application and Implementation

# 备注

以下应用部分中的信息不属于 TI 器件规格的范围,TI 不担保其准确性和完整性。TI 的客 户应负责确定 器件是否适用于其应用。客户应验证并测试其设计,以确保系统功能。

# 8.1 Application Information

# 8.1.1 Crystal Interface

The LMK03806 has an integrated crystal oscillator circuit on that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in 图 8-1.

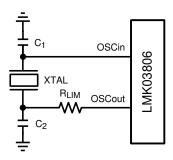


图 8-1. Crystal Interface

The load capacitance ( $C_L$ ) is specific to the crystal, but usually on the order of 18 - 20 pF. While  $C_L$  is specified for the crystal, the OSCin input capacitance (CIN = 6 pF typical) of the device and PCB stray capacitance (CSTRAY approximately 1 pF to 3 pF) can affect the discrete load capacitor values, C1 and C2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_{L} = (C_{1} \times C_{2}) / (C_{1} + C_{2}) + C_{IN} + C_{STRAY}$$
(1)

Typically,  $C_1 = C_2$  for optimum symmetry, so 方程式 1 can be rewritten in terms of  $C_1$  only:

$$C_L = C_1^2 / (2 \times C_1) + C_{IN} + C_{STRAY}$$
 (2)

Finally, solve for C<sub>1</sub>:

$$C_1 = (C_1 - C_{IN} - C_{STRAY}) \times 2$$
 (3)

Electrical Characteristics provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P<sub>XTAL</sub>, can be computed by:

$$P_{XTAL} = I_{RMS}^{2} \times R_{ESR} \times (1 + C_0/C_L)^2$$
(4)

where

- I<sub>RMS</sub> is the RMS current through the crystal.
- R<sub>ESR</sub> is the maximum equivalent series resistance specified for the crystal
- C<sub>L</sub> is the load capacitance specified for the crystal
- C<sub>0</sub> is the minimum shunt capacitance specified for the crystal

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I<sub>RMS</sub> can be measured using a current probe (for example, Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCin\* with the oscillation circuit active.

As shown in 🛚 8-1, an external resistor, R<sub>LIM</sub>, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R<sub>LIM</sub> shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R<sub>LIM</sub> shorted, then a zero value for R<sub>LIM</sub> can be used. As a starting point, a suggested value for  $R_{LIM}$  is 1.5 k $\Omega$ .

## 8.1.2 Driving OSCin Pins With a Single-Ended Source

The LMK03806 has an the ability to be driven by an external reference. Typical external reference interfaces are shown in 图 8-2 and 图 8-3.

In applications where the external reference amplitude is less than the  $V_{OSCin}$  specification of 2.4  $V_{pp}$   $\boxtimes$  8-2 is an appropriate method of interfacing the reference to the LMK03806.

In applications where the external reference amplitude is greater than the  $V_{OSCin}$  specification of 2.4  $V_{pp} \boxtimes 8-3$  is an appropriate method of interfacing the reference to the LMK03806.

In both cases C1 and C2 should be present a low impedance at the reference frequency. A typical value for C1 and C2 is 0.1 µF.

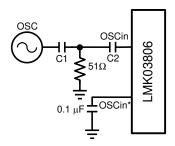


图 8-2. LVCMOS External Reference Interface

图 8-3. 3.3 V<sub>pp</sub> External Reference Interface

Using an external reference, such as a crystal oscillator (XO), may provide better phase noise than a crystal at offsets below the loop bandwidth. If the jitter integration bandwidth for the application of interest is above the loop filter bandwidth, the added phase noise of a crystal will not be a significant jitter contributor and may be a more cost effective solution than an XO. Also, operating at higher reference frequencies allows higher phase detector frequencies, which also improves in band PLL phase noise performance.

### 8.1.3 Driving OSCin Pins With a Differential Source

The OSCin port can be driven by differential signals. The LMK03806 internally biases the input pins so the differential interface should be AC coupled. The recommended circuits for driving the OSCin pins with either LVDS or LVPECL are shown below.

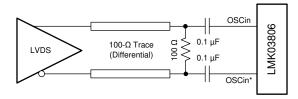


图 8-4. OSCin/OSCin\* Termination for an LVDS Reference Clock Source

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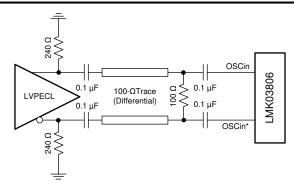


图 8-5. OSCin/OSCin\* Termination for an LVPECL Reference Clock Source

# 8.1.4 Frequency Planning With the LMK03806

Calculating the value of the output dividers is simple due to the architecture of the LMK03806. That is, the clock output dividers allow for even and odd output divide values from 2 to 1045. The procedure for determining the PLL and clock output divider values for a set of clock output frequencies is straightforward.

- 1. Calculate the least common multiple (LCM) of the clock output frequencies.
- 2. Determine which VCO frequency will support the target clock output frequencies given the LCM.
- 3. Determine the clock output divide values based on VCO frequency.
- 4. Determine the PLL divider values VCO DIV, PLL P, PLL N, and PLL R to allow the VCO frequency to lock to the OSCin frequency. For best in-band PLL noise, try to maximize the PLL phase detector frequency by using the smallest PLL divider values and enabling the PLL doubler.

For example, given the following target output frequencies: 156.25 MHz, 125 MHz, 100 MHz, and 25 MHz with a OSCin frequency of 20 MHz:

- 1. Determine the LCM of the three frequencies. LCM(156.25, 125, 100, 25) = 2500 MHz. The LCM frequency is the lowest frequency for which all of the target output frequencies are integer divisors of the LCM. Note: if there is one frequency which causes the LCM to be very large, greater than 2.6 GHz for example, determine if there is a single frequency requirement which causes this. It may be possible to select the crystal frequency to satisfy this frequency requirement through OSCout or CLKout6/7/8/9 driven by OSCin. In this way it is possible to get non-integer related frequencies at the outputs.
- 2. Multiply the LCM frequency by an integer value that causes the product (LCM × X) to fall into the valid VCO frequency range from 2370 to 2600 MHz. In this case, the LCM frequency of 2500 MHz is already within the VCO frequency.
- 3. Continuing the example by using a VCO frequency of 2500 MHz, the CLKout dividers can be calculated by simply dividing the VCO frequency by the output frequency. To output 156.25 MHz, 125 MHz, 100 MHz, and 25 MHz, the output dividers will be 16, 20, 25, and 100, respectively.
  - a. 2500 MHz / 156.25 MHz = 16
  - b. 2500 MHz / 125 MHz = 20
  - c. 2500 MHz / 100 MHz = 25
  - d. 2500 MHz / 25 MHz = 100
- 4. The PLL must be locked to its input reference. Refer to Configuring the PLL for more information on this topic. By programming the clock output dividers and the PLL dividers, the VCO can be locked to 2500 MHz and the clock outputs dividers can each divide-down the VCO frequency to the achieve the target output frequencies.

Refer to Application Note AN-1865, Frequency Synthesis and Planning for PLL Architectures (SNAA061) for more information on this topic and LCM calculations.

#### 8.1.5 Configuring the PLL

For the PLL to operate in closed-loop mode, the following relationships in Equations 5 and 6 must be satisfied to ensure the PLL phase detector input frequencies for the reference and feedback paths are equal.

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$$F_{pd} = F_{osc} \times PLL_D / PLL_R$$
 (PLL reference path)

$$F_{pd} = F_{vco} / (PLL_P \times PLL_N) (PLL feedback path)$$

#### (6)

#### where

- F<sub>pd</sub> = PLL phase detector frequency (F<sub>pd</sub> ≤ 155 MHz)
- F<sub>OSCin</sub> = OSCin reference frequency (F<sub>osc</sub> ≤ 500 MHz)
- $F_{vco}$  = VCO frequency (VCO tuning range = 2370 to 2600 MHz)
- PLL D = PLL reference doubler mode (Disabled = 1, Enabled = 2)
- PLL R = PLL reference divider (values = 1 to 4095)
- PLL P = PLL N prescaler divider (values = 2 to 8)
- PLL N = PLL N divider (values = 1 to 262143)

### 备注

When  $F_{OSCin}$  and  $F_{pd}$  are equal, the best PLL in-band noise can be achieved with the PLL reference doubler enabled (EN PLL REF 2X=1) and the PLL reference divider is 2 (PLL R =2), rather than with the doubler disabled (EN\_PLL\_REF\_2X=0) and PLL reference divider of 1 (PLL\_R=1).

The output frequency is related to  $F_{vco}$  as follows.

$$F_{CLKout} = F_{vco} / OUT_DIV$$
 (7)

## where

OUT DIV: Output channel divider (value = 1 to 1045)

### 8.1.5.1 Example PLL Configuration

Continuing the example above, we are given the target output frequencies of 156.25 MHz, 125 MHz, 100 MHz, and 25 MHz with an OSCin frequency of 20 MHz. As previously calculated, the LCM and F<sub>vco</sub> is 2500 MHz.

First, we will consider the PLL reference path. For lowest possible in-band PLL flat noise, we will try to maximize phase detector frequency. In this case, the highest F<sub>pd</sub> possible from the reference path is 40 MHz (with the reference doubler enabled, doubling the 20 MHz OSCin). However, since 40 MHz does not divide into 2500 MHz by an integer value (and thus is unable to be reproduced by the PLL feedback path), we are required to use an F<sub>nd</sub> of 20 MHz instead, which does divide into 2500 by an integer value of 125. As noted above, when F<sub>OSCin</sub> and F<sub>pd</sub> are equal, the best PLL in-band noise can be achieved with the PLL reference doubler enabled (EN\_PLL\_REF\_2X=1) and the PLL reference divider is 2 (PLL\_R =2).

Next, we will consider the PLL feedback path. As determined earlier, F<sub>vco</sub> is 2500 MHz and F<sub>pd</sub> is 20 MHz, which is 2500 MHz divided by 125. The prescaler and N divider settings together must divide  $F_{vco}$  by 125. Given that the prescaler can be set between 2 to 8 and the N divider can be set between 1 to 262,143, the only setting that would work in this case is a prescaler value of 5 and an N divider value of 25. Note that in a case where multiple configurations are possible, increasing the N divider value will reduce loop filter component sizes.

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### 8.1.6 Digital Lock Detect

The digital lock detect circuit is used to determine the lock status of the PLL. The flowchart in 🖺 8-6 shows the general way this circuit works.

EV	ENT	PLL	WINDOW SIZE (ε)	LOCK COUNT
Р	PLL Locked	PLL	3.7 ns	PLL_DLD_CNT

For a digital lock detect event to occur there must be a number of PLL phase detector cycles during which the time/phase error of the PLL\_R reference and PLL\_N feedback signal edges are within the 3.7 ns window size of the LMK03806. *Lock count* is the term which is used to specify how many PLL phase detector cycles have been within the window size of 3.7 ns at any given time. Since there must be a specified number phase detector events before a lock event occurs, a minimum digital lock event time can be calculated as *lock count* / F<sub>pd</sub>.

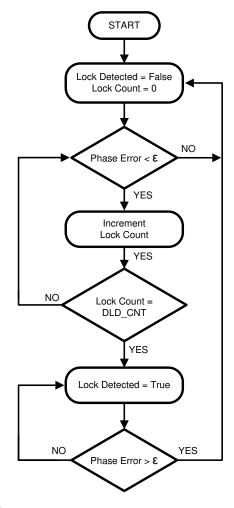


图 8-6. Digital Lock Detect Flow Diagram

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A user specified ppm accuracy for lock detect is programmable using a lock count register. By using 方程式 8, values for a lock count and window size can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs. Units of F<sub>pd</sub> are Hertz:

$$ppm = \frac{2e6 \times 3.7 \text{ ns} \times f_{PD}}{PLL\_DLD\_CNT}$$
(8)

The effect of the lock count value is that it shortens the effective lock window size by dividing the window size by lock count.

If at any time the PLL\_R reference and PLL\_N feedback signals are outside the time window set by window size, then the lock count value is reset to 0.

For example, we will calculate the minimum PLL digital lock time given a PLL F<sub>pd</sub> of 40 MHz and PLL\_DLD\_CNT = 10,000. The minimum lock time of PLL will be  $10,000 / 40 \text{ MHz} = 250 \mu \text{s}$ .

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# 8.2 Typical Application

Normal use case of the LMK03806 device is as a clock generator. This section will discuss a design example to show the various functional aspects of the LMK03806 device.

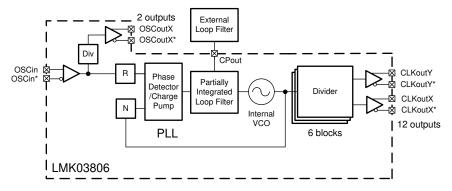


图 8-7. Simplified Functional Block Diagram

## 8.2.1 Design Requirements

A networking line card type application needs a clocking solution for an ASIC, FPGA, CPU, PCIe 3.0 interface, and a 10G PHY. The input clock will be a crystal oscillator. A summary of clock input and output requirements are as follows:

### Clock Input:

20 MHz oscillator

#### **Clock Outputs:**

- 2x 156.25-MHz LVPECL clock for ASIC
- 2x 156.25-MHz LVPECL clock for 10G PHY
- 4x 100-MHz HCSL for PCIe 3.0
- 2x 100-MHz LVDS for FPGA
- 2x 50-MHz LVCMOS for CPU

The following information reviews the steps to produce this design.

# 8.2.2 Detailed Design Procedure

Design of all aspects of the LMK03806 is quite involved and software has been written to assist in part selection, part programming, loop filter design, and simulation. This design procedure will give a quick outline of the process.

### 备注

This information is current as of the date of the release of this data sheet. Design tools receive continuous enhancements to add features and improve model accuracy. Refer to software instructions or training for latest features.

# 1. Device Selection

- The key to device selection is the required  $F_{vco}$  given the required output frequencies. The device must be able to produce a F<sub>vco</sub> that can be divided down to required output frequencies.
- The software design tools will take into account the  $F_{vco}$  range for specific devices based on the application's required output frequencies.

### 2. Device Configuration

There are many possible permutations of dividers and other registers to get same output frequencies from a device. However there are some optimizations and trade-offs to be considered.

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- If more than one divider is in series, for instance PLL prescaler followed by PLL N divider, it is possible although not assured that some crosstalk/mixing could be created when using some divides.
- The design software normally attempts to maximize F<sub>pd</sub>, use smallest dividers, and maximize PLL charge pump current.
- Refer to *Configuring the PLL* for divider equations to ensure the PLL is locked. The design software is able to configure the device for most cases.
- These guidelines may be followed when configuring PLL related dividers or other related registers:
  - For lowest possible in-band PLL flat noise, maximize F<sub>pd</sub> to minimize N divide value.
  - For lowest possible in-band PLL flat noise, maximize charge pump current. Higher value charge pump currents often yield similar performance.
  - To reduce loop filter component sizes, increase the total feedback divide value (PLL\_P × PLL\_N)
    and/or reduce charge pump current.
  - As rule of thumb, keep  $F_{pd}$  approximately between 10 × PLL loop bandwidth and 100 × PLL loop bandwidth. An  $F_{pd}$  value less than 5 × PLL bandwidth may be unstable and a  $F_{pd}$  > 100 × loop bandwidth may experience increased lock time due to cycle slipping.

#### 3. PLL Loop Filter Design

- TI recommends to use Clock Design Tool or Clock Architect to design your loop filter.
- The Clock Design Tool will return solutions with high reference/phase detector frequencies by default. In the Clock Design Tool the user may choose to increase the reference divider to reduce the F<sub>pd</sub> to achieve a narrow loop bandwidth, so it is possible to reduce loop filter capacitor to a practical value.
- While designing the loop filter, adjusting the charge pump current and/or the total feedback divide value (PLL\_P × PLL\_N) can help with loop filter component selection. Lower charge pump currents and larger N values result in smaller loop filter capacitor values but at the expense of increased in-band PLL phase noise.
- More detailed understanding of PLL loop filter design can found in PLL Performance, Simulation, and Design (www.ti.com/tool/pll\_book).

### 4. Clock Output Assignment

- At this point of time, the design software does not take into account frequency assignment to specific
  outputs except to ensure that the output frequencies can be achieved. It is best to consider proximity of
  each clock output to each other and other PLL circuitry when choosing final clock output locations. Here
  are some guidelines to help achieve best performance when assigning outputs to specific CLKout/
  OSCout pins.
  - Group common frequencies together.
  - PLL charge pump circuitry can cause crosstalk at charge pump frequency. Place outputs sharing charge pump frequency or lower priority outputs that are not sensitive to charge pump frequency spurs together.
- 5. Other device specific configuration. For LMK03806 consider the following:
  - · PLL digital lock detect based on programming:
    - There is a digital lock detect circuit which is used to determine the lock status of the PLL. It can also be used to ensure a specific frequency accuracy. A user specified frequency accuracy required to trigger a lock detect event is programmable using a lock count register. Refer to *Digital Lock Detect* for more information.

#### 6. Device Programming

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 The software tool CodeLoader for EVM programming can be used to set up the device in the desired configuration, then export a hex register map suitable for use in application. Some additional information on each part of the design procedure for the example is outlined below.

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#### 8.2.2.1 Device Selection

WEBENCH Clock Architect Tool or Clock Design Tool can be used as aids in device selection. Enter the required frequencies and formats into the tools. To find this device, select a solution based on LMK03806B (referring to the evaluation board).

#### 8.2.2.1.1 Clock Architect

When generating solutions, it is possible to narrow the parts used in the solution by setting the appropriate part filter.

### 8.2.2.1.2 Clock Design Tool

In wizard-mode, select Single PLL and fill in the input frequency and desired output frequencies to generate a list of solutions. If the example values are used, the LMK03806 should be listed as the first result.

### 8.2.2.1.3 Calculation Using LCM

In this example, the LCM of 156.25 MHz, 100 MHz, and 50 MHz = 2500 MHz. This value is a valid  $F_{vco}$  for the LMK03806. Therefore, it may be used to produce these output frequencies.

### 8.2.2.2 Device Configuration

The tools listed above automatically configure the clock solution to meet the input and output frequency requirements given and make assumptions about certain parameters to give default simulation results. The assumptions made are to maximize input frequencies,  $F_{pd}$ , and charge pump currents while minimizing  $F_{vco}$  and divider values. We will also outline the steps for manually configuring the device below for greater flexibility. Note that this procedure is the same as the one outlined in the *Frequency Planning With the LMK03806* and *Configuring the PLL* sections, which can be referenced for a more detailed explanation.

We are given the target output frequencies of 156.25 MHz, 125 MHz, 100 MHz, and 25 MHz with an  $F_{OSCin}$  of 20 MHz. As previously calculated, the LCM and  $F_{vco}$  is 2500 MHz.

First, we will consider the PLL reference path. For lowest possible in-band PLL flat noise, we will try to maximize  $F_{pd}$ . 20 MHz is the highest frequency which divides into 2500 MHz by an integer value and which can also be synthesized from  $F_{OSCin}$ . As noted earlier, when  $F_{OSCin}$  and  $f_{pd}$  are equal, the best PLL in-band noise can be achieved with the PLL reference doubler enabled (EN\_PLL\_REF\_2X=1) and the PLL reference divider is 2 (PLL\_R=2).

Next, we will consider the PLL feedback path. As determined earlier,  $F_{vco}$  is 2500 MHz and the  $F_{pd}$  is 20 MHz, which is 2500 MHz divided by 125. The prescaler and N divider settings together must divide  $F_{vco}$  by 125. The only setting that works in this case is a prescaler value of 5 and an N divider value of 25.

At this point the design meets all input and output frequency requirements and it is possible to design a loop filter for the application and simulate phase noise of the output clocks.

### 8.2.2.3 PLL Loop Filter Design

At this time, the user may choose to use the simulation tools for more accurate simulations. For example:

- Clock Design Tool allows loading a custom phase noise profile for various blocks. Typically, a custom phase
  noise plot is entered for OSCin to match the reference phase noise to the device. For improved accuracy in
  simulation and optimum loop filter design, be sure to load these custom noise profiles for use in application.
  After loading a phase noise plot, user should recalculate the recommended loop filter design.
- The Clock Design Tool will return solutions with high reference/phase detector frequencies by default. In the
  Clock Design Tool the user may increase the reference divider to reduce the frequency if desired. For
  example, if a narrow loop bandwidth is desired, it is possible to reduce F<sub>pd</sub> by increasing the PLL R divider.

Note: Clock Design Tool provides some recommended loop filters upon first loading the simulation. These values are not re-calculated any time PLL related values are changed (for example, input phase noise, charge pump current, divider values, etc.), so it is recommended to re-design the PLL loop filter, either by manually entering desired values, or by using the 'Design a Loop Filter' button in the LOOPFILTER box.

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#### 8.2.2.3.1 Example Loop Filter Design

In the LOOPFILTER box, there are options for displaying a bode plot, simulating phase noise, and re-calculating loop filter values. Selecting the 'Design a Loop Filter' button brings up a window where a target bandwidth and phase margin can be entered and the tool will re-design the loop filter component values to converge to the specified targets. Component values can also be manually entered and the tool will calculate the resulting loop filter parameters.

For this example, a custom phase noise plot was uploaded based on measured data for the reference oscillator input.  $F_{pd}$  was set to 20 MHz and loop filter was optimized to achieve a loop bandwidth of 62 kHz and phase margin of 76°. The loop filter values used were C1 = 220 pF, C2 = 18 nF, R2 = 820  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, and R4 = 200  $\Omega$ . The charge pump current was set to 3.2 mA.

## 8.2.2.4 Other Device Specific Configuration

### 8.2.2.4.1 Digital Lock Detect

Digital lock time for the PLL will ultimately depend upon the programming of the PLL\_DLD\_CNT register as discussed in *Digital Lock Detect*. Since the PLL  $F_{pd}$  in this example is 20 MHz, the lock time will = PLL\_DLD\_CNT / 20 MHz. If PLL\_DLD\_CNT is set to 10,000, the lock time will be 0.5 ms. The ppm accuracy required to indicate lock will be (2e6 × 3.7 ns ×  $f_{pd}$ ) / PLL\_DLD\_CNT, or 14.8 ppm. Refer to *Digital Lock Detect* for more detail on calculating lock times.

# 8.2.2.5 Device Programming

The CodeLoader software is used to program the LMK03806B evaluation board using the LMK03806B profile. It also allows the exporting of a register map which can be used to program the device to the user's desired configuration. Once a configuration of dividers has been achieved using the Clock Design Tool to meet the requested input/output frequencies with the desired performance, the CodeLoader software needs to be manually updated with this configuration to meet the required application. At this time no automatic import between the two tools exists.

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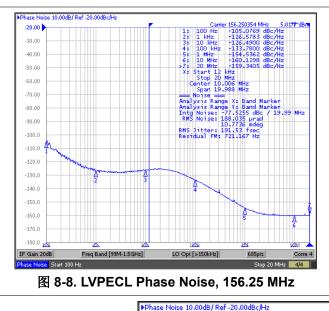
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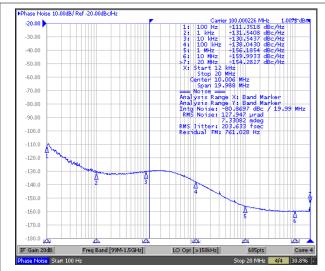
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### 8.2.3 Application Curves

The following jitter and phase noise data was captured from an LMK03806 evaluation board.  $F_{vco}$  was set to 2500 MHz and  $F_{pd}$  was set to 20 MHz. In order to obtain a loop bandwidth of 62 kHz and a phase margin of 76°, the loop filter values used were C1 = 220 pF, C2 = 18 nF, R2 = 820  $\Omega$ , C3 = 10 pF, R3 = 200  $\Omega$ , C4 = 10 pF, and R4 = 200  $\Omega$ . The charge pump current was set to 3.2 mA.







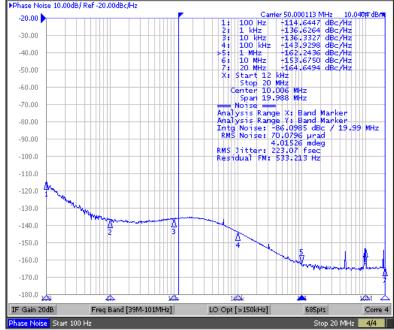
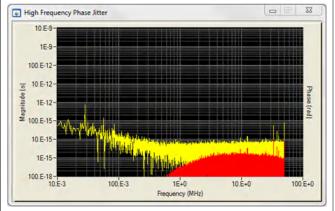


图 8-10. LVCMOS Phase Noise, 50 MHz

The following PCIe 3.0 phase jitter results were obtained using the Intel Clock Jitter Tool using waveform data captured with an Agilent DSA90804A. The RMS jitter result of 0.107 ps easily meets the PCIe 3.0 jitter requirement of 1ps with significant margin.



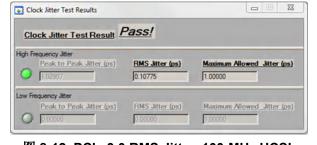


图 8-12. PCIe 3.0 RMS Jitter, 100-MHz HCSL

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# 8.3 System Examples

## 8.3.1 System Level Diagram

⊗ 8-13 shows a detailed system level diagram of the example above to serve as a guideline for good practices when designing with the LMK03806.

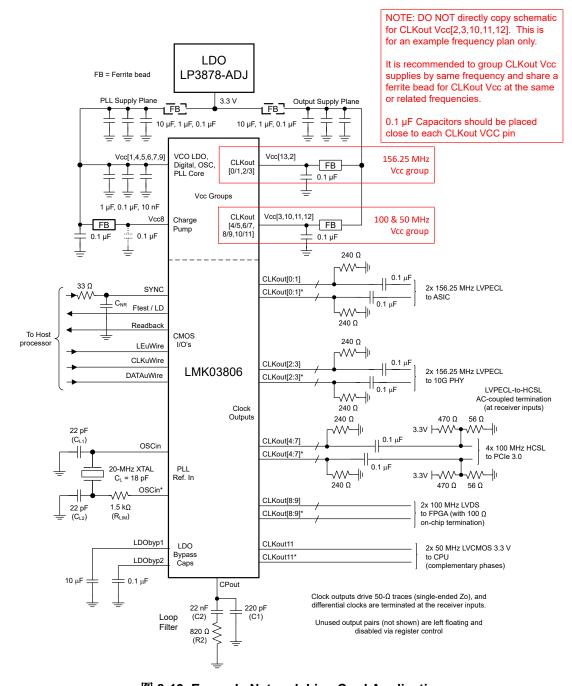


图 8-13. Example Network Line Card Application

## 8.4 Best Design Practices

#### 8.4.1 LVCMOS Complementary vs. Non-Complementary Operation

- TI recommends to use a complementary LVCMOS output format such as LVCMOS (Norm/Inv) to reduce switching noise and crosstalk when using LVCMOS.
- If only a single LVCMOS output is required, the complementary LVCMOS output format can still be used by leaving the unused LVCMOS output floating.
- A non-complimentary format such as LVCMOS (Norm/Norm) is not recommended as increased switching noise is present.

#### 8.4.2 LVPECL Outputs

When using an LVPECL output it is not recommended to place a capacitor to ground on the output as might be done when using a capacitor input LC lowpass filter. The capacitor will appear as a short to the LVPECL output drivers which are able to supply large amounts of switching current. The effect of the LVPECL sourcing large switching currents can result in the following:

- 1. Large switching currents through the Vcc pin of the LVPECL power supply resulting in more Vcc noise and possible Vcc spikes.
- 2. Large switching currents injected into the ground plane through the capacitor which could couple onto other Vcc pins with bypass capacitors to ground resulting in more Vcc noise and possible Vcc spikes.

#### 8.4.3 Sharing MICROWIRE (SPI) Lines

When CLKuWire and DATAuWire toggle and an internal VCO mode is used, there may some spurious content on the phase noise plot related to the frequency of the CLKuWire and DATAuWire pins.

#### 8.4.4 SYNC Pin

If the SYNC pin is connected to a host device (for example, FPGA, CPLD, CPU) with noisy I/O power rails, use small series resistor and shunt capacitor ( $C_{NR}$ ) as shown in  $\boxed{8}$  8-13. An external low-pass filter can prevent noise on the SYNC input from coupling unwanted spurious content to nearby internal analog circuitry.

#### 8.4.5 CLKout Vcc Pins

Place  $0.1-\mu$  F capacitors after the ferrite beads and as close as possible to each CLKout Vcc pin (Vcc2, Vcc3, Vcc10, Vcc11, Vcc12, Vcc13) for optimal output performance.

#### 8.5 Power Supply Recommendations

#### 8.5.1 Current Consumption and Power Dissipation Calculations

From  $\frac{1}{8}$  8-1 the current consumption can be calculated for any configuration.

For example, the current for the entire device with 1 LVDS (CLKout0) and 1 LVPECL 1.6 Vpp with 240- $\Omega$  emitter resistors (CLKout1) output active with a clock output divide = 1, and no other features enabled can be calculated by adding up the following blocks: core current, base clock distribution, clock output group, clock divider, one LVDS output buffer current, and one LVPECL output buffer current. There will also be one LVPECL output drawing emitter current, which means some of the power from the current draw of the device is dissipated in the external emitter resistors which doesn't add to the thermal power dissipation budget for the device. In addition to emitter resistor power, power dissipated in the load for LVDS/LVPECL do not contribute to the thermal power dissipation budget for the device.

For total current consumption of the device, add up the significant functional blocks. In this example, 212.9 mA =

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- 122 mA (core current)
- 17.3 mA (base clock distribution)
- 2.8 mA (CLKout group for two outputs)
- 25.5 mA (CLKout0 ans CLKout1 divider)
- 14.3 mA (LVDS buffer)
- 31 mA (LVPECL 1.6 Vpp buffer with a 240- Ω emitter resistors)

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Once total current consumption has been calculated, power dissipated by the device can be calculated. The power dissipation of the device is equation to the total current entering the device multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of the LVPECL outputs or any other external load power dissipation. Continuing the above example which has 212.9 mA total Icc and one output with 240- $\Omega$  emitter resistors and one LVDS output. Total IC power = 666 mW = 3.3 V × 212.9 mA  $^-$  35 mW  $^-$  1.5 mW.

表 8-1. Typical Current Consumption for Selected Functional Blocks  $(T_A = 25^{\circ}\text{C}, V_{CC} = 3.3 \text{ V})$ 

BLOCK		DITION	TYPICAL I <sub>CC</sub> (mA)	POWER DISSIPATED IN DEVICE (mW)(2)	POWER DISSIPATED EXTERNALLY (mW) <sup>(3)</sup>
	COR	E AND FUNCTIONAL BLOCKS			
Core	Internal VCO Locked		122	403	-
Base Clock Distribution	At least 1 CLKoutX_Y_PD = 0		17.3	57.1	-
CLKout Group	Each CLKout group (CLKout0/1 and CLKout10/11, CLKou CLKout8/9)	t2/3 and CLKout4/5, CLKout6/7 and	2.8	9.2	-
Clock Divider	Divide < 25		25.5	84.1	-
Clock Divide	Divide >= 25		29.6	97.7	-
SYNC Asserted	While SYNC is asserted, this extra cu	rrent is drawn	1.7	5.6	-
Crystal Mode	Crystal Oscillator Buffer		1.8	5.9	-
OSCin Doubler	EN_OSCin_2X = 1		2.8	9.2	-
	(	CLOCK OUTPUT BUFFERS			
LVDS	100- $\Omega$ differential termination		14.3	45.7	1.5
	LVPECL 2.0 Vpp, AC coupled using 2	40- Ω emitter resistors	32	70.6	35
	LVPECL 1.6 Vpp, AC coupled using 2	40-Ω emitter resistors	31	67.3	35
LVPECL (1)	LVPECL 1.6 Vpp, AC coupled using 1	20-Ω emitter resistors	46	91.8	60
	LVPECL 1.2 Vpp, AC coupled using 2	40-Ω emitter resistors	30	59	40
	LVPECL 0.7 Vpp, AC coupled using 2	40-Ω emitter resistors	29	55.7	40
	LVCMOS Pair (CLKoutX Y TYPE	3 MHz	24	79.2	-
	= 6 to 10)	30 MHz	26.5	87.5	-
LVCMOS	C <sub>L</sub> = 5 pF	150 MHz	36.5	120.5	-
LVCMOS	= 11 to 13) 3	3 MHz	15	49.5	-
		30 MHz	16	52.8	-
	$C_L = 5 pF$	150 MHz	21.5	71	-

<sup>(1)</sup> Power is dissipated externally in LVPECL emitter resistors. The externally dissipated power is calculated as twice the DC voltage level of one LVPECL clock output pin squared over the emitter resistance. That is to say power dissipated in emitter resistors = 2 × Vem<sup>2</sup> / Rem

#### 8.6 Layout

### 8.6.1 Layout Guidelines

Power consumption of the LMK03806 can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate,  $T_A$  (ambient temperature) plus device power consumption times  $\theta_{JA}$  should not exceed 125°C.

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<sup>(2)</sup> Assuming  $\theta_{JA} = 15^{\circ}\text{C/W}$ , the total power dissipated on chip must be less than (125°C - 85°C) / 16°C/W = 2.5 W to guarantee a junction temperature is less than 125°C.

<sup>(3)</sup> Worst case power dissipation can be estimated by multiplying typical power dissipation with a factor of 1.15.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed-circuit-board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in 🛭 8-14. More information on soldering WQFN packages and gerber footprints can be obtained: http://www.ti.com/packaging.

A recommended footprint including recommended solder mask and solder paste layers can be found at: http:// www.ti.com/packaging for the NKD0064A package.

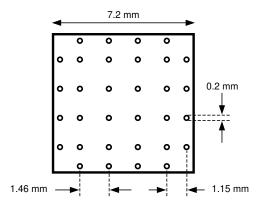


图 8-14. Recommended Land and Via Pattern

To minimize junction temperature, TI recommends that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in [8] 8-14 should connect these top and bottom copper layers and to the ground layer. These vias act as heat pipes to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

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English Data Sheet: SNAS522



### 8.6.2 Layout Example

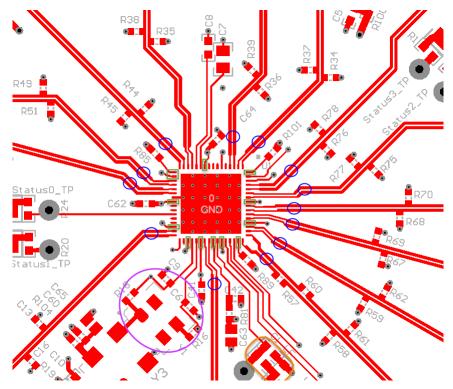


图 8-15. LMK03806 Layout Example

### Crystal input to OSCin pins (purple circle):

- Place crystal with associated load capacitors (C6 and C9) as close as possible to the chip, and use short/ direct routing to the OSCin pins.
- If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, avoid using vias in the crystal signal path and routing other signals below the crystal paths, as these could be potential areas for noise coupling.

### Clock outputs (blue circles):

- Differential signals should be routed tightly coupled to minimize PCB crosstalk. Trace impedance and loading/ terminations should be designed according to output type being used (that is, LVDS, LVPECL...).
- Unused output pins should be left open without connection to a trace. Unused outputs should be powered down through registers to reduce power and switching noise.

### Power pins (green rectangles):

Place ferrite beads and bypass caps as close as possible to the Vcc pins as possible. Design a low
impedance power distribution network over a wide frequency range using multiple decoupling and bypass
caps with different values/sizes. Use ferrite beads to isolate the device supply pins from board noise sources.

#### Loop filter (orange oval):

Place loop filter resistor and capacitors nearby the chip, and route loop filter nodes from digital traces or noisy
power traces/planes to avoid noise coupling.

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## 9 Device and Documentation Support

### 9.1 Device Support

### 9.1.1 Development Support

For additional support, see the following:

- Clock Design Tool: http://www.ti.com/tool/clockdesigntool
- Clock Architect: http://www.ti.com/lsds/ti/analog/webench/clock-architect.page
- Loop Filter Design: PLL Performance, Simulation, and Design (www.ti.com/tool/pll\_book)

### 9.2 Documentation Support

#### 9.2.1 Related Documentation

For additional information, see the following:

- Texas Instruments, Common Data Transmission Parameters and their Definitions application note
- Texas Instruments, Crystal Based Oscillator Design with the LMK04000 Family application note
- Texas Instruments, Frequency Synthesis and Planning for PLL Architectures application note

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#### 9.7 术语表

TI术语表 本术语表列出并解释了术语、首字母缩略词和定义。

Product Folder Links: LMK03806

English Data Sheet: SNAS522



# 10 Register Maps

表 10-1 Provides the register map for device programming. At no time should registers be programmed to undefined values. Only valid register values should be written.

表 10-1. Register Map

																_		IVIA	_													
REGIST ER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	01.16							Π				I	DA	TA [2	6:0]														ADDI	RESS	[4:0]	
R0	out 0_1 _PD	0	0	0	0	0	0	0	0	0	0	0	0	0	RE SE T	0				CL	Kout0	_1_0	)IV [1	5:5]				0	0	0	0	0
R1	CLK out 2_3 _PD	0	0	0	0	0	0	0	0	0	0	0	0	0	PO WE RD O WN	0				CL	Kout2	!_3_C	)IV [1	5:5]				0	0	0	0	1
R2	CLK out 4_5 _PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				CL	Kout4	_5_0	)IV [1ŧ	5:5]				0	0	0	1	0
R3	CLK out 6_7 _PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				CL	Kout6	5_7_C	)IV [1ŧ	5:5]				0	0	0	1	1
R4	CLK out 8_9 _PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				CL	Kout8	3_9_C	)IV [1ŧ	5:5]				0	0	1	0	0
R5	CLK out 10_ 11_ PD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				CLK	Cout10	)_11_	DIV [1	15:5]				0	0	1	0	1
R6	CL	Kout3	 3_TYI	PE	CL	_Kout	2_TYI :24]	PE	CL	Kout:	1_TYI	PE	CL		 0_TYI :16]	PE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R7	CL	Kout7 [31:	_TYI	PE	CL	Kout		PE	CL		5_TYI	PE	CL	.Kout	4_TYI :16]	PE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R8	CLŁ	Cout1 [31:		PE	CL	Kout1 [27	10_TY :24]	PE	CL	Kout!	9_TYI :20]	PE	CL		8_TYI :16]	PE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R9	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	0	1
R10	OSC _TY [31:	PΕ	0	1	OS	SCout [27	:0_TY :24]	PE	EN O SC out 1	EN O SC out 0	OS Co ut1 _M UX	OS Co ut0 _M UX	0		Cout_ 18:16		0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R11	0	0	1	1	0	1	NO S YN C_ CL Ko ut1 0_1	NO S YN C CL Ko ut8 9	NO S N C C K o ut 7	NO S YN C_ CL Ko ut4 _5	NO S YN C CL Ko ut2 3	NO S YN C CL Ko ut0 _1	0	0	0	SY NC P OL IN	0	0	YF	IC_T PE :12]	0	0	0	0	0	0	EN P LL XT AL	0	1	0	1	1
R12	L	_D_M	UX [	31:27]	]	_	test/L _TYPI [26:24	E	SY NC P LL D LD	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0
R13	0	0	1	1	1		ADB <i>A</i> _TYPI [26:24	E	0	0	0	0	0		Pout 18:16		1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R14	0	0	0	0	0		3Pout [26:24		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
R16	1	1	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
R24	P	LL_C [31:		=		PLL_0 [27	C3_LF :24]	F	0		R4 22:20		0		L_R3 18:16		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

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表 10-1. Register Map (续)

														,	J - 1			r 1		,												
REGIST	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ER		DATA [26:0]												ADDRESS [4:0]																		
R26	1	0	EN _P LL _ RE F_ 2X	0	_G.	_CP AIN :26]	1	1	1	0	1	0						PI	LL_DI [1!	LD_C 9:6]	NT						0	1	1	0	1	0
R28						PLL	_R						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
R29	0	0	0	0	0		Cin_FF 26:24		1								PLI	_N_C	CAL [2	22:5]								1	1	1	0	1
R30	0	0	0	0	0	F	PLL_F	)	0								ı	PLL_N	N [22:	5]								1	1	1	1	0
R31	0	0	0	0	0	0	0	0	0	0	0	R		3ACK [20:16		DDR	0	0	0	0	0	0	0	0	0	0	uW ire_ LO CK	1	1	1	1	1

# 10.1 Default Device Register Settings After Power On Reset

表 10-2 shows the default register settings programmed in silicon for the LMK03806 after power on or asserting the reset bit. Capital X and Y represent numeric values.

表 10-2. Default Device Register Settings After Power On/Reset

GROUP	FIELD NAME	DEFAULT VALUE (DECIMAL)	DEFAULT STATE	FIELD DESCRIPTION	REGISTER	BIT LOCATION (MSB:LSB)			
	CLKout0_1_PD	1	PD		R0				
	CLKout2_3_PD	1	PD		R1				
	CLKout4_5_PD	1	PD	Powerdown control for divider,	R2	31			
	CLKout6_7_PD	0	Normal	and both output buffers	R3	31			
	CLKout8_9_PD	0	Normal		R4				
	CLKout10_11_PD	1	PD		R5				
	RESET	0	Not in reset	Performs power on reset for device	R0	17			
	POWERDOWN	0	Disabled (device is active)	Device power down control	R1	17			
	CLKout0_1_DIV	25	Divide-by-25		R0				
	CLKout2_3_DIV	25	Divide-by-25		R1				
	CLKout4_5_DIV	25	Divide-by-25	Divide for electronic	R2	45.5 (44)			
	CLKout6_7_DIV <sup>(1)</sup>	1	Divide-by-1	Divide for clock outputs	R3	15:5 [11]			
Clock Output	CLKout8_9_DIV	25	Divide-by-25		R4				
Control	CLKout10_11_DIV	25	Divide-by-25		R5				
	CLKout3_TYPE	0	Powerdown		R6				
	CLKout7_TYPE	0	Powerdown		R7	31:28 [4]			
	CLKout11_TYPE	0	Powerdown		R8				
	CLKout2_TYPE	0	Powerdown		R6				
	CLKout6_TYPE <sup>(1)</sup>	8	LVCMOS (Norm/Norm)	Individual clock output format.	R7	27:24 [4]			
	CLKout10_TYPE	0	Powerdown	Select from LVDS/LVPECL/	R8				
	CLKout1_TYPE	0	Powerdown	LVCMOS.	R6				
	CLKout5_TYPE	0	Powerdown		R7	23:20 [4]			
	CLKout9_TYPE	0	Powerdown		R8				
	CLKout0_TYPE	0	Powerdown		R6				
(	CLKout4_TYPE	0	Powerdown		R7	19:16 [4]			
	CLKout8_TYPE	1	LVDS		R8				

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表 10-2. Default Device Register Settings After Power On/Reset (续)

GROUP	FIELD NAME	DEFAULT VALUE (DECIMAL)	DEFAULT STATE	FIELD DESCRIPTION	REGISTER	BIT LOCATION (MSB:LSB)
	OSCout1_TYPE	2	1600 mVpp LVPECL	Set LVPECL amplitude	R10	31:30 [2]
	OSCout0_TYPE	1	LVDS	OSCout0 default clock output	R10	27:24 [4]
	EN_OSCout1	0	Disabled	Disable OSCout1 output buffer	R10	23
Osc Buffer Control	EN_OSCout0	1	Enabled	Enable OSCout0 output buffer	R10	22
Mode	OSCout1_MUX	0	Bypass Divider	Select OSCout divider for OSCout1 or bypass	R10	21
	OSCout0_MUX	0	Bypass Divider	Select OSCout divider for OSCout0 or bypass	R10	20
	OSCout_DIV	0	Divide-by-8	OSCout divider value	R10	18:16 [3]
	NO_SYNC_CLKout10_11	0	Will sync		R11	25
	NO_SYNC_CLKout8_9	1	Will not sync		R11	24
	NO_SYNC_CLKout6_7	1	Will not sync	Disable individual clock groups	R11	23
	NO_SYNC_CLKout4_5	0	Will sync	from becoming synchronized.	R11	22
SVNC Control	NO_SYNC_CLKout2_3	0	Will sync		R11	21
SYNC Control	NO_SYNC_CLKout0_1	0	Will sync		R11	20
	SYNC_POL_INV	1	Logic Low	Sets the polarity of the SYNC pin when input. (Use for software SYNC)	R11	16
	SYNC_TYPE	1	Input /w Pull-up	SYNC IO pin type	R11	13:12 [2]
	EN_PLL_XTAL	0	Disabled	Enable Crystal oscillator for OSCin	R11	5
	LD_MUX	3	Reserved	Ftest/LD pin selection when output	R12	31:27 [5]
Other Mode Control	LD_TYPE	3	Output (Push-Pull)	LD IO pin type	R12	26:24 [3]
	SYNC_PLL_DLD	0	No effect	When set, force SYNC until PLL locks	R12	23
	READBACK_TYPE	3	Output (Push-Pull)	Readback Pin Type	R13	26:24 [3]
GPout	GPout0	2	Weak pull-down	GPout0 output state	R13	18:16 [3]
Grout	GPout1	2	Weak pull-down	GPout1 output state	R14	28:26 [3]
	PLL_C4_LF	0	10 pF	PLL integrated capacitor C4 value	R24	31:28 [4]
	PLL_C3_LF	0	10 pF	PLL integrated capacitor C3 value	R24	27:24 [4]
	PLL_R4_LF	0	200 Ω	PLL integrated resistor R4 value	R24	22:20 [3]
	PLL_R3_LF	0	200 Ω	PLL integrated resistor R3 value	R24	18:16 [3]
	EN_PLL_REF_2X	0	Disabled, 1x	Doubles reference frequency of PLL.	R26	29
	PLL_CP_GAIN	3	3.2 mA	PLL Charge Pump Gain	R26	27:26 [2]
PLL Control	PLL_DLD_CNT	8192	8192 Counts	Number of PDF cycles which phase error must be within DLD window before LD state is asserted.	R26	19:6 [14]
	PLL_R	4	Divide-by-4	PLL R Divider (1 to 4095)	R28	31:20 [12]
	OSCin_FREQ	7	448 to 500 MHz	OSCin frequency range	R29	26:24 [3]
	PLL_N_CAL	48	Divide-by-48	Must be programmed to PLL_N value.	R29	22:5 [18]
PLL	PLL_P	2	Divide-by-2	PLL N Divider Prescaler (2 to 8)	R30	26:24 [3]
<u> </u>	PLL_N	48	Divide-by-48	PLL N Divider (1 to 262143)	R30	22:5 [18]

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# 表 10-2. Default Device Register Settings After Power On/Reset (续)

GROUP	FIELD NAME	DEFAULT VALUE (DECIMAL)	DEFAULT STATE	FIELD DESCRIPTION	REGISTER	BIT LOCATION (MSB:LSB)
uWire	uWire_LOCK	0	Writable	The values of registers R0 to R30 are lockable	R31	5

On POR, any output from CLKout6 cannot be used. R3 must be programmed per data sheet specifications before CLKout6 can be

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### 10.2 Register R0 TO R5

Registers R0 through R5 control the 12 clock outputs CLKout0 to CLKout11. Register R0 controls CLKout0 and CLKout1, Register R1 controls CLKout2 and CLKout3, and so on. The X and Y in CLKoutX\_Y\_PD, CLKoutX\_Y\_DIV denote the actual clock output which may be from 0 to 11 where X is even and Y is odd. Two clock outputs CLKoutX and CLKoutY form a clock output group and are often run together in bit names as CLKoutX Y.

Two additional bits within the R0 to R5 register range are:

- The RESET bit, which is only in register R0.
- The POWERDOWN bit, which is only in register R1.

备注

R3 must be programmed after POR.

### 10.2.1 CLKoutX\_Y\_PD, Powerdown CLKoutX\_Y Output Path

This bit powers down the clock group as specified by CLKoutX and CLKoutY. This includes the divider and output buffers.

### 表 10-3. CLKoutX\_Y\_PD

R0-R5[31]	STATE
0	Power up clock group
1	Power down clock group

#### 10.2.2 RESET

The RESET bit is located in register R0 only. Setting this bit will cause the silicon default values to be loaded. When programming register R0 with the RESET bit set, all other programmed values are ignored. After resetting the device, the register R0 must be programmed again (with RESET = 0) to set non-default values in register R0.

The reset occurs on the falling edge of the LEuWire pin which loaded R0 with RESET = 1.

The RESET bit is automatically cleared upon writing any other register. For instance, when R0 is written to again with default values.

### 表 10-4. RESET

R0[17]	STATE
0	Normal operation
1	Reset (automatically cleared)

#### 10.2.3 POWERDOWN

The POWERDOWN bit is located in register R1 only. Setting the bit causes the device to enter powerdown mode. Normal operation is resumed by clearing this bit with MICROWIRE.

#### 表 10-5. POWERDOWN

R1[17]	STATE
0	Normal operation
1	Powerdown

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### 10.2.4 CLKoutX\_Y\_DIV, Clock Output Divide

CLKoutX\_Y\_DIV sets the divide value for the clock group. The divide may be even or odd. Both even and odd divides output a 50% duty cycle clock.

Using a divide value of 26 or greater will cause the clock group to operate in extended mode.

Programming CLKoutX\_Y\_DIV can require special attention.

表 10-6. CLKoutX\_Y\_DIV, 11 bits

R0-R5[15:5]	DIVIDE VALUE	POWER MODE
0 (0x00)	Reserved	
1 (0x01)	1	
2 (0x02)	2 (1)	
3 (0x03)	3	
4 (0x04)	4 (1)	Normal Mode
5 (0x05)	5 (1)	Normal Mode
6 (0x06)	6	
24 (0x18)	24	
25 (0x19)	25	
26 (0x1A)	26	
27 (0x1B)	27	
		Extended Mode
1044 (0x414)	1044	
1045 (0x415)	1045	

After programming PLL\_N value, a SYNC must occur on channels using this divide value. Programming PLL\_N does generate a SYNC event automatically which satisfies this requirement, but NO\_SYNC\_CLKoutX\_Y must be set to 0 for these clock groups.

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# 10.3 Registers R6 TO R8

## 10.3.1 CLKoutX\_TYPE

The clock output types of the LMK03806 are individually programmable. The CLKoutX\_TYPE registers set the output type of an individual clock output to LVDS, LVPECL, LVCMOS, or powers down the output buffer. Note that LVPECL supports four different amplitude levels and LVCMOS supports single LVCMOS outputs, inverted, and normal polarity of each output pin for maximum flexibility.

The programming addresses table shows at what register and address the specified clock output CLKoutX\_TYPE register is located.

The CLKoutX\_TYPE table shows the programming definition for these registers.

表 10-7. CLKoutX TYPE Programming Addresses

CLKoutX	PROGRAMMING ADDRESS
CLKout0	R6[19:16]
CLKout1	R6[23:20]
CLKout2	R6[27:24]
CLKout3	R6[31:28]
CLKout4	R7[19:16]
CLKout5	R7[23:20]
CLKout6	R7[27:24]
CLKout7	R7[31:28]
CLKout8	R8[19:16]
CLKout9	R8[23:20]
CLKout10	R8[27:24]
CLKout11	R8[31:28]

表 10-8. CLKoutX\_TYPE, 4 Bits

R6-R8[31:28, 27:24, 23:20]	DEFINITION
0 (0x00)	Powerdown
1 (0x01)	LVDS
2 (0x02)	LVPECL (700 mVpp)
3 (0x03)	LVPECL (1200 mVpp)
4 (0x04)	LVPECL (1600 mVpp)
5 (0x05)	LVPECL (2000 mVpp)
6 (0x06)	LVCMOS (Norm/Inv)
7 (0x07)	LVCMOS (Inv/Norm)
8 (0x08) <sup>(1)</sup>	LVCMOS (Norm/Norm)
9 (0x09) <sup>(1)</sup>	LVCMOS (Inv/Inv)
10 (0x0A) <sup>(1)</sup>	LVCMOS (Low/Norm)
11 (0x0A) <sup>(1)</sup>	LVCMOS (Low/Inv)
12 (0x0C) <sup>(1)</sup>	LVCMOS (Norm/Low)
13 (0x0D) <sup>(1)</sup>	LVCMOS (Inv/Low)
14 (0x0E) <sup>(1)</sup>	LVCMOS (Low/Low)

<sup>(1)</sup> TI recommends to use one of the complementary LVCMOS modes. Best noise performance is achieved using LVCMOS (Norm/Inv) or LVCMOS (Inv/Norm) due to the differential switching of the outputs. The next best performance is achieved using an LVCMOS mode with only one output on. Finally, LVCMOS (Norm/Norm) or LVCMOS (Inv/Inv) have the create the most switching noise.

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#### 10.4 REGISTER R9

Register 9 contains no user programmable bits, but must be programmed as described in the register map.

#### **10.5 REGISTER R10**

### 10.5.1 OSCout1\_TYPE, LVPECL Output Amplitude Control

The OSCout1 clock output can only be used as an LVPECL output type. OSCout1 TYPE sets the LVPECL output amplitude of the OSCout1 clock output.

表 10-9. OSCout1 TYPE, 2 Bits

R10[31:30]	OUTPUT FORMAT
0 (0x00)	LVPECL (700 mVpp)
1 (0x01)	LVPECL (1200 mVpp)
2 (0x02)	LVPECL (1600 mVpp)
3 (0x03)	LVPECL (2000 mVpp)

### 10.5.2 OSCout0 TYPE

The OSCout0 clock output has a programmable output type. The OSCout0\_TYPE register sets the output type to LVDS, LVPECL, LVCMOS, or powers down the output buffer. Note that LVPECL supports four different amplitude levels and LVCMOS supports dual and single LVCMOS outputs with inverted, and normal polarity of each output pin for maximum flexibility.

To turn on the output, the OSCout0 TYPE must be set to a non-power down setting and enabled with EN\_OSCoutX, OSCout Output Enable.

表 10-10. OSCout0\_TYPE, 4 Bits

R10[27:24]	DEFINITION
0 (0x00)	Powerdown
1 (0x01)	LVDS
2 (0x02)	LVPECL (700 mVpp)
3 (0x03)	LVPECL (1200 mVpp)
4 (0x04)	LVPECL (1600 mVpp)
5 (0x05)	LVPECL (2000 mVpp)
6 (0x06)	LVCMOS (Norm/Inv)
7 (0x07)	LVCMOS (Inv/Norm)
8 (0x08) <sup>(1)</sup>	LVCMOS (Norm/Norm)
9 (0x09) <sup>(1)</sup>	LVCMOS (Inv/Inv)
10 (0x0A) <sup>(1)</sup>	LVCMOS (Low/Norm)
11 (0x0B) <sup>(1)</sup>	LVCMOS (Low/Inv)
12 (0x0C) <sup>(1)</sup>	LVCMOS (Norm/Low)
13 (0x0D) <sup>(1)</sup>	LVCMOS (Inv/Low)
14 (0x0E) <sup>(1)</sup>	LVCMOS (Low/Low)

<sup>(1)</sup> TI recommends to use one of the complementary LVCMOS modes. Best noise performance is achieved using LVCMOS (Norm/Inv) or LVCMOS (Inv/Norm) due to the differential switching of the outputs. The next best performance is achieved using an LVCMOS mode with only one output on. Finally, LVCMOS (Norm/Norm) or LVCMOS (Inv/Inv) have the create the most switching noise.

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### 10.5.3 EN\_OSCoutX, OSCout Output Enable

EN\_OSCoutX is used to enable an oscillator buffered output.

### 表 10-11. EN\_OSCout1

R10[23]	OUTPUT STATE
0	OSCout1 Disabled
1	OSCout1 Enabled

### 表 10-12. EN\_OSCout0

R10[22]	OUTPUT STATE
0	OSCout0 Disabled
1	OSCout0 Enabled

OSCout0 note: In addition to enabling the output with EN\_OSCout0. The OSCout0\_TYPE must be programmed to a non-power down value for the output buffer to power up.

### 10.5.4 OSCoutX\_MUX, Clock Output Mux

Sets OSCoutX buffer to output a divided or bypassed OSCin signal.

### 表 10-13. OSCout1\_MUX

R10[21]	MUX OUTPUT
0	Bypass divider
1	Divided

### 表 10-14. OSCout0\_MUX

R10[20]	Mux Output
0	Bypass divider
1	Divided

### 10.5.5 OSCout\_DIV, Oscillator Output Divide

The OSCout divider can be programmed from 2 to 8. Divide by 1 is achieved by bypassing the divider with OSCoutX\_MUX, Clock Output Mux.

表 10-15. OSCout\_DIV, 3 Bits

R10[18:16]	DIVIDE
0 (0x00)	8
1 (0x01)	2
2 (0x02)	2
3 (0x03)	3
4 (0x04)	4
5 (0x05)	5
6 (0x06)	6
7 (0x07)	7

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### **10.6 REGISTER R11**

### 10.6.1 NO\_SYNC\_CLKoutX\_Y

The NO\_SYNC\_CLKoutX\_Y bits prevent individual clock groups from becoming synchronized during a SYNC event. A reason to prevent individual clock groups from becoming synchronized is that during synchronization, the clock output is in a fixed low state or can have a glitch pulse.

By disabling SYNC on a clock group, it will continue to operate normally during a SYNC event.

Setting the NO\_SYNC\_CLKoutX\_Y bit has no effect on clocks already synchronized together.

表 10-16. NO\_SYNC\_CLKoutX\_Y Programming Addresses

NO_SYNC_CLKoutX_Y	PROGRAMMING ADDRESS
CLKout0 and 1	R11:20
CLKout2 and 3	R11:21
CLKout4 and 5	R11:22
CLKout6 and 7	R11:23
CLKout8 and 9	R11:24
CLKout10 and 11	R11:25

### 表 10-17. NO\_SYNC\_CLKoutX\_Y

R11[25, 24, 23, 22, 21, 20]	DEFINITION
0	CLKoutX_Y will synchronize
1	CLKoutX_Y will not synchronize

### 10.6.2 SYNC\_POL\_INV

Sets the polarity of the SYNC pin when input. When SYNC is asserted the clock outputs will transition to a low state.

### 表 10-18. SYNC\_POL\_INV

R11[16]	POLARITY
0	SYNC is active high
1	SYNC is active low

### 10.6.3 SYNC\_TYPE

Sets the IO type of the SYNC pin.

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#### 表 10-19. SYNC\_TYPE, 2 Bits

R11[13:12]	POLARITY
0 (0x00)	Input
1 (0x01)	Input /w pull-up resistor
2 (0x02)	Input /w pull-down resistor

### 10.6.4 EN\_PLL\_XTAL

If an external crystal is being used to implement a discrete VCXO, the internal feedback amplifier must be enabled with this bit in order to complete the oscillator circuit.

### 表 10-20. EN\_PLL\_XTAL

R11[5]	OSCILLATOR AMPLIFIER STATE
0	Disabled
1	Enabled

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## **10.7 REGISTER R12**

### 10.7.1 LD\_MUX

LD\_MUX sets the output value of the Ftest/LD pin.

All the outputs logic is active high when LD\_TYPE = 3 (Output). All the outputs logic is active low when LD\_TYPE = 4 (Output Inverted). For example, when LD\_MUX = 0 (Logic Low) and LD\_TYPE = 3 (Output) then Ftest/LD pin outputs a logic low. When LD\_MUX = 0 (Logic Low) and LD\_TYPE = 4 (Output Inverted) then Ftest/LD pin outputs a logic high.

表 10-21. LD\_MUX, 5 Bits

R12[31:27]	DIVIDE
0 (0x00)	Logic Low
1 (0x01)	Reserved
2 (0x02)	PLL DLD
3 (0x03)	Reserved
12 (0x0C)	Reserved
13 (0x0D)	PLL N
14 (0x0E)	PLL N/2
15 (0x0F)	Reserved
16 (0x10)	Reserved
17 (0x11)	PLL R (1)
18 (0x12)	PLL R/2 <sup>(1)</sup>

<sup>(1)</sup> Only valid when LD\_MUX is not set to 2 (PLL\_DLD).

### 10.7.2 LD\_TYPE

Sets the IO type of the LD pin.

表 10-22. LD\_TYPE, 3 Bits

R12[26:24]	POLARITY
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Reserved
3 (0x03)	Output (push-pull)
4 (0x04)	Output inverted (push-pull)
5 (0x05)	Output (NMOS open source)
6 (0x06)	Output (PMOS open drain)

## 10.7.3 SYNC\_PLL\_DLD

By setting SYNC\_PLL\_DLD a SYNC mode will be engaged (asserted SYNC) until the PLL locks.

表 10-23. SYNC\_PLL\_DLD

R12[23]	SYNC MODE FORCED
0	No
1	Yes

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# 10.8 REGISTER R13

### 10.8.1 READBACK\_TYPE

Sets the IO format of the readback pin. The open drain output type can be used to interface the LMK03806 with low voltage IO rails.

表 10-24. READBACK\_TYPE, 3 Bits

R13[26:24]	POLARITY
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Reserved
3 (0x03)	Output (push-pull)
4 (0x04)	Output inverted (push-pull)
5 (0x05)	Output (NMOS open source)
6 (0x06)	Output (PMOS open drain)

### 10.8.2 GPout0

Sets the output state of the GPout0 pin.

表 10-25. GPout0, 3 Bits

R13[18:16]	OUTPUT STATE
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Weak pull-down
3 (0x03)	Low (0 V)
4 (0x04)	High (3.3 V)

### **10.9 REGISTER 14**

### 10.9.1 GPout1

Sets the output state of the GPout1 pin.

表 10-26. GPout1, 3 Bits

· · · · · · · · · · · · · · · · · · ·	
R14[26:24]	OUTPUT STATE
0 (0x00)	Reserved
1 (0x01)	Reserved
2 (0x02)	Weak pull-down
3 (0x03)	Low (0 V)
4 (0x04)	High (3.3 V)

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### **10.10 REGISTER 16**

Register 16 contains no user programmable bits, but must be programmed as described in the register map.

### **10.11 REGISTER 24**

## 10.11.1 PLL\_C4\_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter capacitor C4 can be set according to the values listed in 表 10-27.

表 10-27. PLL\_C4\_LF, 4 Bits

R24[31:28]	LOOP FILTER CAPACITANCE (pF)
0 (0x00)	10 pF
1 (0x01)	15 pF
2 (0x02)	29 pF
3 (0x03)	34 pF
4 (0x04)	47 pF
5 (0x05)	52 pF
6 (0x06)	66 pF
7 (0x07)	71 pF
8 (0x08)	103 pF
9 (0x09)	108 pF
10 (0x0A)	122 pF
11 (0x0B)	126 pF
12 (0x0C)	141 pF
13 (0x0D)	146 pF
14 (0x0E)	Reserved
15 (0x0F)	Reserved

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### 10.11.2 PLL\_C3\_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter capacitor C3 can be set according to the values listed in 表 10-28.

表 10-28. PLL\_C3\_LF, 4 Bits

R24[27:24]	LOOP FILTER CAPACITANCE (pF)
0 (0x00)	10 pF
1 (0x01)	11 pF
2 (0x02)	15 pF
3 (0x03)	16 pF
4 (0x04)	19 pF
5 (0x05)	20 pF
6 (0x06)	24 pF
7 (0x07)	25 pF
8 (0x08)	29 pF
9 (0x09)	30 pF
10 (0x0A)	33 pF
11 (0x0B)	34 pF
12 (0x0C)	38 pF
13 (0x0D)	39 pF
14 (0x0E)	Reserved
15 (0x0F)	Reserved

## 10.11.3 PLL\_R4\_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter resistor R4 can be set according to the values listed in 表 10-29.

表 10-29. PLL\_R4\_LF, 3 Bits

R24[22:20]	RESISTANCE
0 (0x00)	200 Ω
1 (0x01)	1 kΩ
2 (0x02)	2 kΩ
3 (0x03)	4 kΩ
4 (0x04)	16 kΩ
5 (0x05)	Reserved
6 (0x06)	Reserved
7 (0x07)	Reserved

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### 10.11.4 PLL\_R3\_LF, PLL Integrated Loop Filter Component

Internal loop filter components are available for the PLL, enabling either 3rd or 4th order loop filters without requiring external components.

Internal loop filter resistor R3 can be set according to the values listed in 表 10-30.

表 10-30. PLL\_R3\_LF, 3 Bits

R24[18:16]	RESISTANCE
0 (0x00)	200 Ω
1 (0x01)	1 kΩ
2 (0x02)	2 k Ω
3 (0x03)	<b>4 k</b> Ω
4 (0x04)	16 kΩ
5 (0x05)	Reserved
6 (0x06)	Reserved
7 (0x07)	Reserved

#### **10.12 REGISTER 26**

### 10.12.1 EN\_PLL\_REF\_2X, PLL Reference Frequency Doubler

Enabling the PLL reference frequency doubler allows for higher phase detector frequencies on the PLL than would normally be allowed with the given VCXO or Crystal frequency.

Higher phase detector frequencies reduces the PLL N values which makes the design of wider loop bandwidth filters possible.

表 10-31. EN\_PLL\_REF\_2X

R26[29]	DESCRIPTION
0	Reference frequency normal
1	Reference frequency doubled (2x)

### 10.12.2 PLL\_CP\_GAIN, PLL Charge Pump Current

This bit programs the PLL charge pump output current level.

表 10-32. PLL CP GAIN, 2 Bits

R26[27:26]	CHARGE PUMP CURRENT (μA)
0 (0x00)	100
1 (0x01)	400
2 (0x02)	1600
3 (0x03)	3200

### 10.12.3 PLL\_DLD\_CNT

The reference and feedback of the PLL must be within the window of acceptable phase error for **PLL\_DLD\_CNT** cycles before PLL digital lock detect is asserted.

表 10-33. PLL\_DLD\_CNT, 14 Bits

R26[19:6]	DIVIDE					
0 (0x00)	Reserved					
1 (0x01)	1					
2 (0x02)	2					
3 (0x03)	3					
16,382 (0x3FFE)	16,382					
16,383 (0x3FFF)	16,383					

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#### **10.13 REGISTER 28**

### 10.13.1 PLL\_R, PLL R Divider

The reference path into the PLL phase detector includes the PLL R divider.

表 10-34 lists the valid values for PLL\_R.

表 10-34. PLL\_R, 12 Bits

R28[31:20]	DIVIDE					
0 (0x00)	Not Valid					
1 (0x01)	1					
2 (0x02)	2					
3 (0x03)	3					
4,094 (0xFFE)	4,094					
4,095 (0xFFF)	4,095					

#### **10.14 REGISTER 29**

### 10.14.1 OSCin\_FREQ, PLL Oscillator Input Frequency Register

The frequency of the PLL reference input to the PLL Phase Detector (OSCin/OSCin\* port) must be programmed in order to support proper operation of the frequency calibration routine which locks the internal VCO to the target frequency.

表 10-35. OSCin\_FREQ, 3 Bits

R29[26:24]	OSCin FREQUENCY					
0 (0x00)	0 to 63 MHz					
1 (0x01)	>63 MHz to 127 MHz					
2 (0x02)	>127 MHz to 255 MHz					
3 (0x03)	Reserved					
4 (0x04)	>255 MHz to 500 MHz					

### 10.14.2 PLL\_N\_CAL, PLL N Calibration Divider

During the frequency calibration routine, the PLL uses the divide value of the PLL\_N\_CAL register instead of the divide value of the PLL\_N register to lock the VCO to the target frequency.

表 10-36. PLL\_N\_CAL, 18 Bits

R29[22:5]	DIVIDE
0 (0x00)	Not Valid
1 (0x01)	1
2 (0x02)	2
262,143 (0x3FFFF)	262,143

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#### **10.15 REGISTER 30**

Programming Register 30 triggers the frequency calibration routine. This calibration routine will also generate a SYNC event.

### 10.15.1 PLL\_P, PLL N Prescaler Divider

The PLL N Prescaler divides the output of the VCO and is connected to the PLL N divider.

表 10-37. PLL\_P, 3 Bits

R30[26:24]	DIVIDE VALUE
0 (0x00)	8
1 (0x01)	2
2 (0x02)	2
3 (0x03)	3
4 (0x04)	4
5 (0x05)	5
6 (0x06)	6
7 (0x07)	7

### 10.15.2 PLL\_N, PLL N Divider

The feedback path into the PLL phase detector includes the PLL N divider.

Each time register 30 is updated through the MICROWIRE interface, a frequency calibration routine runs to lock the VCO to the target frequency. During this calibration PLL\_N is substituted with PLL\_N\_CAL.

表 10-38 lists the valid values for PLL\_N.

表 10-38. PLL\_N, 18 Bits

R30[22:5]	DIVIDE
0 (0x00)	Not Valid
1 (0x01)	1
2 (0x02)	2
262,143 (0x3FFFF)	262,143

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English Data Sheet: SNAS522



# 10.16 REGISTER 31 10.16.1 READBACK\_ADDR

### 表 10-39. READBACK\_ADDR

R0 R1 R2 R3 R4 R5 R6 R7 R8
R2 R3 R4 R5 R6 R7
R3 R4 R5 R6 R7
R4 R5 R6 R7
R5 R6 R7
R6 R7
R7
R8
1.0
R9
R10
R11
R12
R13
R14
Reserved
R16
Reserved
Reserved
R24
Reserved
R26
Reserved
R28
R29
R30

### 10.16.2 uWire\_LOCK

Setting uWire\_LOCK will prevent any changes to uWire registers R0 to R30. Only by clearing the uWire\_LOCK bit in R31 can the uWire registers be unlocked and written to once more.

It is not necessary to lock the registers to perform a readback operation.

## 表 10-40. uWire\_LOCK

R31[5]	STATE				
0	Registers unlocked				
1	Registers locked, Write-protect				



# 11 Revision History

注:以前版本的页码可能与当前版本的页码不同

・ 更新了整个文档中的表格、图和交叉参考的编号格式	Changes from Revision J (March 2018) to Revision K (December 2023)	Page
・ 将 <i>器件信息</i> 表更改为 <i>封装信息</i>	• 更新了整个文档中的表格、图和交叉参考的编号格式	1
Removed the external VCO text from the Clock Distribution section		
* Added CLKout Vcc Pins section	Removed the external VCO text from the Clock Distribution section	20
* Added CLKout Vcc Pins section	• Changed 图 8-13	36
・Removed unresolvable cross-references		
<ul> <li>Added initial programming requirement of R3</li></ul>	Changes from Revision I (November 2015) to Revision J (March 2018)	Page
<ul> <li>Changed readback text from "rising" to "falling"</li></ul>	Removed unresolvable cross-references	6
<ul> <li>Bolded pin 30 of register R3 for emphasis</li></ul>	Added initial programming requirement of R3	22
<ul> <li>Added table note to Default Device Register Settings After Power On Reset to clarify proper use of CLKout6</li></ul>	Changed readback text from "rising" to "falling"	23
CLKout6	Bolded pin 30 of register R3 for emphasis	42
<ul> <li>Added note to Register R0 TO R5 regarding programming R3</li></ul>	· Added table note to Default Device Register Settings After Power On Reset to clarify prop	er use of
Changes from Revision H (August 2012) to Revision I (November 2015)  • 添加了器件信息表、ESD 等级表、热性能信息表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	CLKout6	43
<ul> <li>添加了器件信息表、ESD 等级表、热性能信息表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分</li></ul>	Added note to Register R0 TO R5 regarding programming R3	46
相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	Changes from Revision H (August 2012) to Revision I (November 2015)	Page
<ul> <li>Separated Timing Requirements into its own section</li></ul>	• 添加了 <i>器件信息</i> 表、ESD 等级表、热性能信息表、特性说明部分、器件功能模式、应用。	<i>和实施</i> 部分、 <i>电源</i>
<ul> <li>Moved Serial MICROWIRE Timing Diagram and Terminology section.</li> <li>Moved Achievable Frequencies table and Common Frequency Plans table to Device Functional Modes section.</li> <li>Added Driving OSCin Pins with a Differential Source section.</li> <li>Added Frequency Planning with the LMK03806 and Configuring the PLL sections.</li> </ul>	相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
<ul> <li>Moved Achievable Frequencies table and Common Frequency Plans table to Device Functional Modes section</li></ul>	Separated Timing Requirements into its own section	14
section	Moved Serial MICROWIRE Timing Diagram and Terminology section	19
<ul> <li>Added Driving OSCin Pins with a Differential Source section.</li> <li>Added Frequency Planning with the LMK03806 and Configuring the PLL sections.</li> </ul>	• Moved Achievable Frequencies table and Common Frequency Plans table to Device Fund	ctional Modes
Added Frequency Planning with the LMK03806 and Configuring the PLL sections	section	21
· · · · · · · · · · · · · · · · · · ·	Added Driving OSCin Pins with a Differential Source section	25
Moved Thermal Management section and renamed it to Layout Guidelines	Added Frequency Planning with the LMK03806 and Configuring the PLL sections	26
	Moved Thermal Management section and renamed it to Layout Guidelines	38

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	( )	( )			(-)	(4)	(5)		(-,
LMK03806BISQ/NOPB	Active	Production	WQFN (NKD)   64	1000   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ
LMK03806BISQ/NOPB.A	Active	Production	WQFN (NKD)   64	1000   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ
LMK03806BISQE/NOPB	Active	Production	WQFN (NKD)   64	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ
LMK03806BISQE/NOPB.A	Active	Production	WQFN (NKD)   64	250   SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ
LMK03806BISQX/NOPB	Active	Production	WQFN (NKD)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ
LMK03806BISQX/NOPB.A	Active	Production	WQFN (NKD)   64	2000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	K03806BISQ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



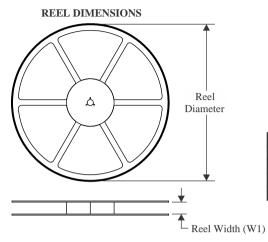
# **PACKAGE OPTION ADDENDUM**

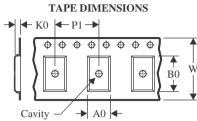
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# **PACKAGE MATERIALS INFORMATION**

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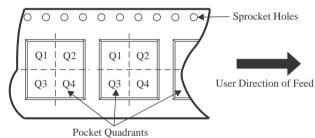
### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

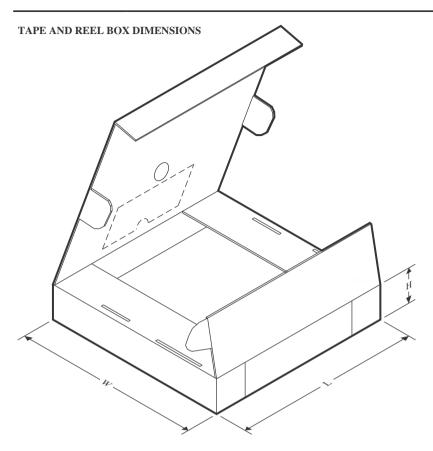
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK03806BISQ/NOPB	WQFN	NKD	64	1000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
LMK03806BISQE/NOPB	WQFN	NKD	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
LMK03806BISQX/NOPB	WQFN	NKD	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

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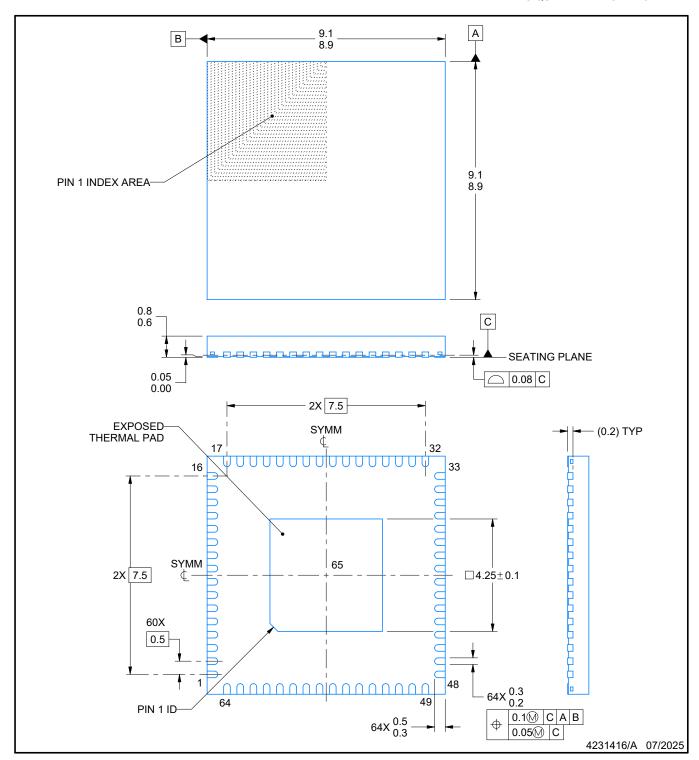


### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK03806BISQ/NOPB	WQFN	NKD	64	1000	356.0	356.0	36.0
LMK03806BISQE/NOPB	WQFN	NKD	64	250	208.0	191.0	35.0
LMK03806BISQX/NOPB	WQFN	NKD	64	2000	356.0	356.0	36.0



PLASTIC QUAD FLATPACK - NO LEAD

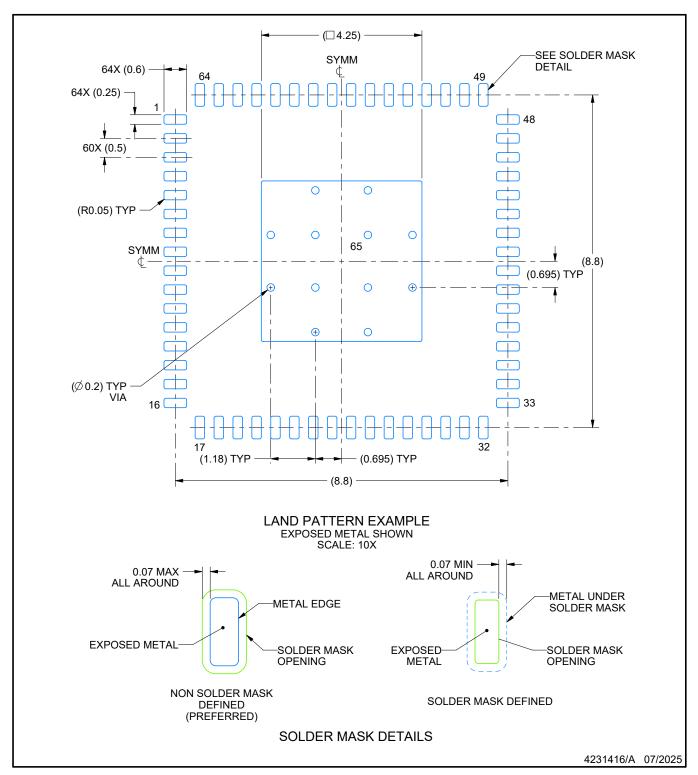


#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

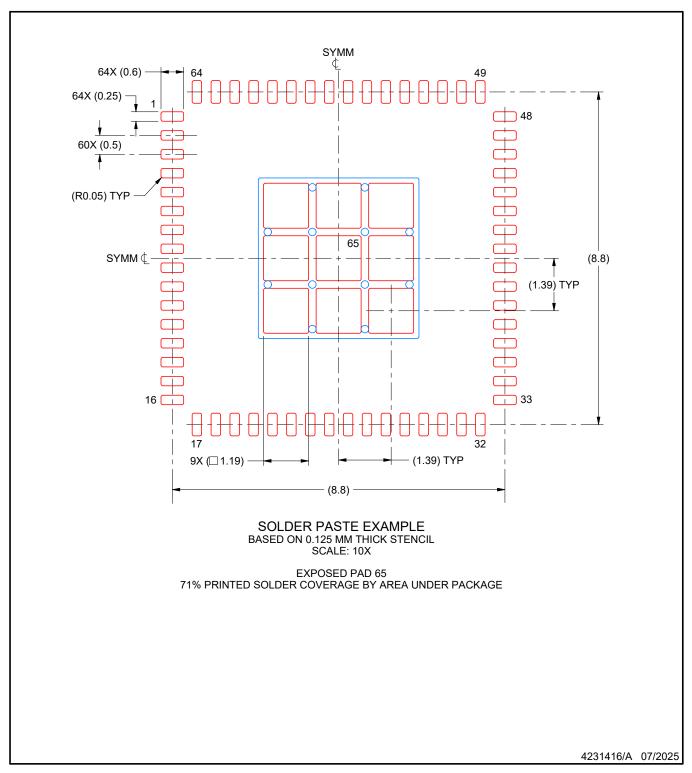


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





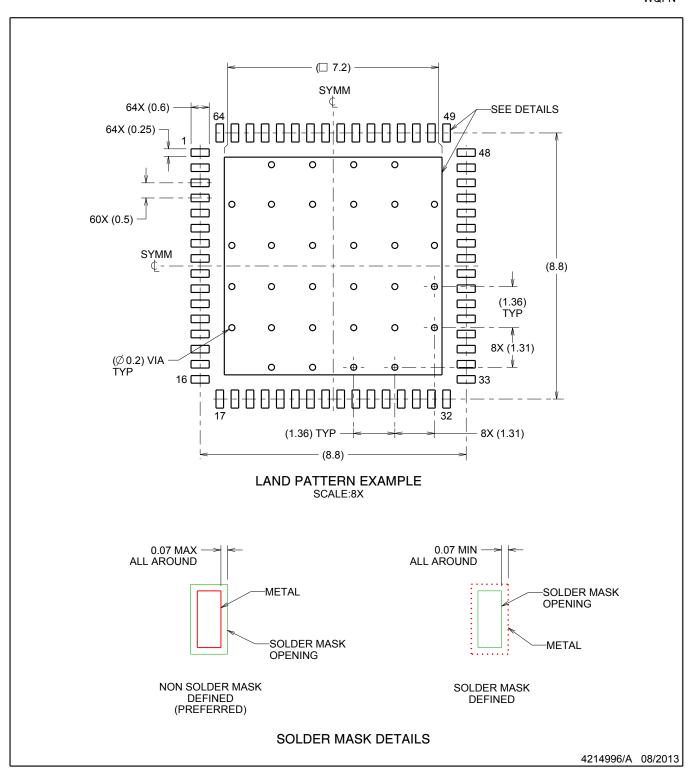
WQFN Α 8.9 PIN 1 INDEX AREA 9.1 0.3 0.2 **DETAIL** OPTIONAL TERMINAL TYPICAL 0.8 MAX С SEATING PLANE (0.1) TYP  $\square$  7.2  $\pm$  0.1 SEE TERMINAL 17 32 60X 0.5 **DETAIL** 4X חחחחח 7.5  $\vdash$ Þ PIN 1 ID 49 (OPTIONAL) 0.1M C AS BS 64X  $^{0.5}_{0.3}$  -0.05M C 4214996/A 08/2013

#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



WQFN

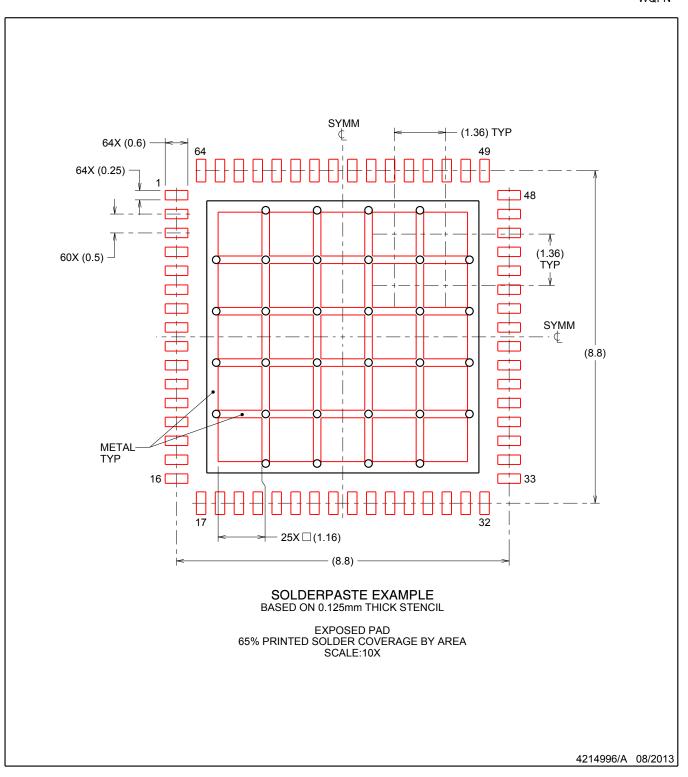


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



WQFN



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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