LMK00105 具有通用输入的超低抖动 LVCMOS 扇出缓冲器和电平转换器

1 特性

- 5 个低电压互补金属氧化物半导体 (LVCMOS) 输出，频率范围为直流至 200MHz
- 通用输入
  - 低电压正射极耦合逻辑 (LVPECL)
  - 低压差分信令 (LVDS)
  - 主机时钟信号电平 (HCSL)
  - 短截线串联端接逻辑 (SSTL)
  - LVCMOS 和低电压晶体管-晶体管逻辑电路 (LVTTL)
- 晶体振荡器接口
  - 晶振输入频率：10 至 40MHz
- 输出偏斜：6ps
- 附加相位抖动
  - 156.25MHz（12kHz 至 20MHz）时为 30fs
- 低传播延迟
- 由 3.3V 或 2.5V 内核电源电压供电运行
- 可调输出电源
  - 每组均可选择 1.5V、1.8V、2.5V 和 3.3V
- 24 引脚超薄型四方扁平无引线 (WQFN) 封装封装 (4.0mm × 4.0mm × 0.8mm)

2 应用

- 针对射频拉远单元 (RRU) 应用的 LO 基准分布
- 同步光网络 (SONET)，以太网，光纤信道线路接口卡
- 光传输网络
- 千兆无源光网络 (GPON) 光线路终端 (OLT) / 光网络单元 (ONU)
- 服务器和存储局域网络互连
- 医疗成像
- 便携式测试和测量
- 高端 A/V

3 说明

LMK00105 是一款高性能、低噪声 LVCMOS 扇出缓冲器，可通过差分、单端或晶振输入实现五路超低抖动时钟。 LMK00105 支持同步输出使能功能，可确保无毛刺脉冲运行。 这款缓冲器具有超低偏斜、低抖动和高电源抑制比 (PSRR) 等诸多优势，因此非常适合各类网络互连、电信、服务器和存储局域网络互连、RRU LO 基准分布、医疗和测试设备应用。

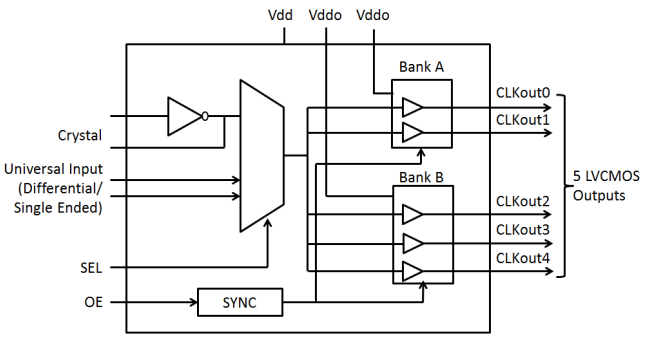
内核电压可设置为 2.5V 或 3.3V，而输出电压可设置为 1.5V、1.8V、2.5V 或 3.3V。通过引脚编程功能可轻松配置 LMK00105。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMK00105	WQFN (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

功能方框图



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史 ... 2
5 **Pin Configuration and Diagrams** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 7
7 **Detailed Description** ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 10
8 **Application and Implementation** ... 11
8.1 Application Information ... 11
8.2 Typical Applications ... 13
9 **Power Supply Recommendations** ... 19
9.1 Power Supply Filtering ... 19
9.2 Power Supply Ripple Rejection ... 19
9.3 Power Supply Bypassing ... 20
10 **Layout** ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 21
10.3 Thermal Management ... 21
11 器件和文档支持 ... 22
11.1 文档支持 ... 22
11.2 商标 ... 22
11.3 静电放电警告 ... 22
11.4 术语表 ... 22
12 机械、封装和可订购信息 ... 23

4 修订历史

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2013) to Revision G **Page**

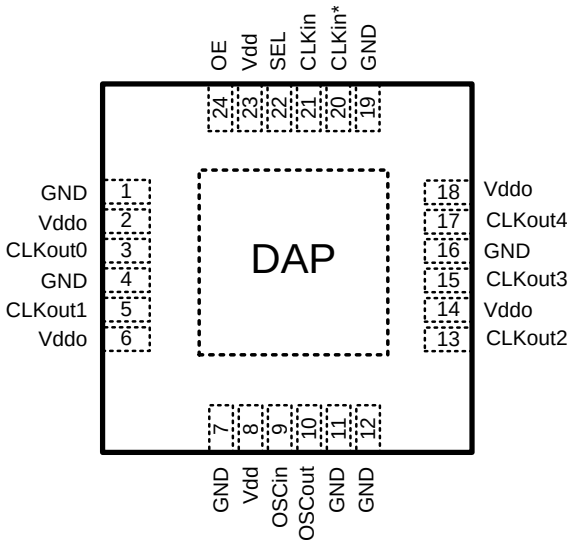
- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision E (February 2013) to Revision F **Page**

- 已添加 器件名称至文档标题。 ... 1
- 已更改 所有 LLP 和 QFN 封装至 WQFN 封装（通篇）。 ... 1
- Deleted optional from CLKin* pin description. And changed complimentary to complementary. ... 3
- Added max limit to Output Skew parameter and added tablenote to parameter in Electrical Characteristics Table. ... 5
- Changed typical value for both conditions of Propagation Delay in the Electrical Characteristics Table. ... 5
- Added Min/Max limits to both conditions of Propagation Delay parameter in Electrical Characteristics Table. ... 5
- Changed unit value for the first condition of Part-to-part Skew from ps to ns in the Electrical Characteristics Table. ... 5
- Changed both Max values of each Part-to-part Skew condition in Electrical Characteristics Table. ... 5
- Changed the Typ value of each Rise/Fall Time condition in the Electrical Characteristics Table. ... 5
- Deleted V_{IL} table note. ... 6
- Added V_{I_SE} parameter and spec limits with corresponding table note to Electrical Characteristics Table. ... 6
- Added CLKin* column to *CLKin Input vs. Output States* table. Also added fourth row starting with Logic Low under CLKin column. ... 9
- Changed table title from *CLKin input vs. Output States* to *OSCin Input vs. Output States* ... 9
- Changed third paragraph in *Driving the Clock Inputs* section to include CLKin* and LVCMOS text. Removed extra references to other figures. Revised to better correspond with information in Electrical Characteristics Table. ... 11
- Deleted Figure 10 (*Near End termination*) and Figure 11 (*Far End termination*) from *Driving the Clock Inputs* section ... 11
- Changed bypass cap text to signal attenuation text of the fourth paragraph in *Driving the Clock Inputs* section. ... 11
- Changed *Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing* image with revised graphic. ... 12
- Deleted sentence in reference to two deleted images. ... 12
- Changed link from National packaging site to TI packaging site. ... 21

5 Pin Configuration and Diagrams

24-Pin
WQFN Package
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO		
DAP	DAP	—	The DAP should be grounded
Vddo	2, 6	Power	Power Supply for Bank A (CLKout0 and CLKout 1) CLKout pins.
CLKout0	3	Output	LVCMOS Output
GND	1,4,7,11, 12, 16,19	GND	Ground
CLKout1	5	Output	LVCMOS Output
Vdd	8,23	Power	Supply for operating core and input buffer
OSCin	9	Input	Input for Crystal
OSCout	10	Output	Output for Crystal
CLKout2	13	Output	LVCMOS Output
Vddo	14,18	Power	Power Supply for Bank B (CLKout2 to CLKout 4) CLKout pins
CLKout3	15	Output	LVCMOS Output
CLKout4	17	Output	LVCMOS Output
CLKin*	20	Input	Complementary input pin
CLKin	21	Input	Input Pin
SEL	22	Input	Input Clock Selection. This pin has an internal pulldown resistor.(1)
OE	24	Input	Output Enable. This pin has an internal pulldown resistor.(1)

(1) CMOS control input with internal pulldown resistor.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Vdd	Core Supply Voltage	–0.3	3.6	V
Vddo	Output Supply Voltage	–0.3	3.6	V
V_{IN}	Input Voltage	–0.3	Vdd + 0.3	V
T_L	Lead Temperature (solder 4 s)		260	°C
T_J	Junction Temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
T_A	Ambient Temperature	–40	25	85	°C
Vdd	Core Supply Voltage	2.375	3.3	3.45	V
Vddo	Output Supply Voltage (1)	1.425	3.3	Vdd	V

(1) V_{ddo} should be less than or equal to V_{dd} ($V_{ddo} \leq V_{dd}$)

6.4 Thermal Information

THERMAL METRIC(1)		LMK00105 RTW 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	
ψ_{JT}	Junction-to-top characterization parameter	1.9	
ψ_{JB}	Junction-to-board characterization parameter	25.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

(2.375 V ≤ V_{dd} ≤ 3.45 V, 1.425 ≤ V_{ddo} ≤ V_{dd}, -40 °C ≤ T_A ≤ 85 °C, Differential inputs. Typical values represent most likely parametric norms at V_{dd} = V_{ddo} = 3.3 V, T_A = 25 °C, at the Recommended Operation Conditions at the time of product characterization and are **not** ensured). Test conditions are: F_{test} = 100 MHz, Load = 5 pF in parallel with 50 Ω unless otherwise stated.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TOTAL DEVICE CHARACTERISTICS						
Vdd	Core Supply Voltage		2.375	2.5 or 3.3	3.45	V
Vddo	Output Supply Voltage		1.425	1.5, 1.8, 2.5, or 3.3	Vdd	V
I_{Vdd}	Core Current	No CLKin		16	25	mA
		V_{ddo} = 3.3 V, F_{test} = 100 MHz		24		
		V_{ddo} = 2.5 V, F_{test} = 100 MHz		20		
$I_{Vddo[n]}$	Current for Each Output	V_{ddo} = 2.5 V, OE = High, F_{test} = 100 MHz		5		mA
		V_{ddo}= 3.3 V, OE = High, F_{test} = 100 MHz		7		
		OE = Low		0.1		
I_{Vdd} + I_{Vddo}	Total Device Current with Loads on all outputs	OE = High @ 100 MHz		48		mA
		OE = Low		16		
POWER SUPPLY RIPPLE REJECTION (PSRR)						
PSRR	Ripple Induced Phase Spur Level	100 kHz, 100 mVpp Ripple Injected on V_{dd}, V_{ddo} = 2.5 V		-44		dBc
OUTPUTS (1)						
Skew	Output Skew (2)	Measured between outputs, referenced to CLKout0		6	25	ps
t_{PD}	Propagation Delay CLKin to CLKout (2)	C_L = 5 pF, R_L = 50 Ω V_{dd} = 3.3 V; V_{ddo} = 3.3 V	0.85	1.4	2.2	ns
		C_L = 5 pF, R_L = 50 Ω V_{dd} = 2.5 V; V_{ddo} = 1.5 V	1.1	1.8	2.8	ns
$t_{PD, PP}$	Part-to-part Skew (2) (3)	C_L = 5 pF, R_L = 50 Ω V_{dd} = 3.3 V; V_{ddo} = 3.3 V			0.35	ns
		C_L = 5 pF, R_L = 50 Ω V_{dd} = 2.5 V; V_{ddo} = 1.5 V			0.6	ns
f_{CLKout}	Output Frequency (4)		DC		200	MHz
t_{Rise}	Rise/Fall Time	V_{dd} = 3.3 V, V_{ddo} = 1.8 V, C_L = 10 pF		250		ps
		V_{dd} = 2.5 V, V_{ddo} = 2.5 V, C_L = 10 pF		275		
		V_{dd} = 3.3 V, V_{ddo} = 3.3 V, C_L = 10 pF		315		
V_{CLKout}Low	Output Low Voltage				0.1	V
V_{CLKout}High	Output High Voltage		V_{ddo}-0.1			
R_{CLKout}	Output Resistance			50		ohm
t_j	RMS Additive Jitter	f_{CLKout} = 156.25 MHz, CMOS input slew rate ≥ 2 V/ns C_L = 5 pF, BW = 12 kHz to 20 MHz		30		fs

(1) AC Parameters for CMOS are dependent upon output capacitive loading
(2) Parameter is specified by design, not tested in production.
(3) Part-to-part skew is calculated as the difference between the fastest and slowest tPD across multiple devices.
(4) Specified by characterization.

Electrical Characteristics (continued)

(2.375 V ≤ V_{dd} ≤ 3.45 V, 1.425 ≤ V_{ddo} ≤ V_{dd}, -40 °C ≤ T_A ≤ 85 °C, Differential inputs. Typical values represent most likely parametric norms at V_{dd} = V_{ddo} = 3.3 V, T_A = 25 °C, at the Recommended Operation Conditions at the time of product characterization and are **not** ensured). Test conditions are: F_{test} = 100 MHz, Load = 5 pF in parallel with 50 Ω unless otherwise stated.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (OE, SEL0, SEL1)						
V_{Low}	Input Low Voltage	V_{dd} = 2.5 V			0.4	V
V_{High}	Input High Voltage	V_{dd} = 2.5 V	1.3			V
		V_{dd} = 3.3 V	1.6			
I_{IH}	High Level Input Current				50	uA
I_{IL}	Low Level Input Current		-5		5	uA
CLKin/CLKin* INPUT CLOCK SPECIFICATIONS (5) (6)						
I_{IH}	High Level Input Current	V_{CLKin} = V_{dd}			20	uA
I_{IL}	Low Level Input Current	V_{CLKin} = 0 V	–20			uA
V_{IH}	Input High Voltage				Vdd	V
V_{IL}	Input Low Voltage		GND			V
V_{CM}	Differential Input Common Mode Input Voltage (7)	V_{ID} = 150 mV	0.5		Vdd-1.2	V
		V_{ID} = 350 mV	0.5		Vdd-1.1	
		V_{ID} = 800 mV	0.5		Vdd-0.9	
V_{I_SE}	Single-Ended Input Voltage Swing (2)	CLKinX driven single-ended (AC or DC coupled), CLKinX* AC coupled to GND or externally biased within V_{CM} range	0.3		2	Vpp
V_{ID}	Differential Input Voltage Swing	CLKin driven differentially	0.15		1.5	V
OSCin/OSCout PINS						
f_{OSCin}	Input Frequency (4)	Single-Ended Input, OSCout floating	DC		200	MHz
f_{XTAL}	Crystal Frequency Input Range	Fundamental Mode Crystal ESR < 200 Ω (f_{Xtal} ≤ 30 MHz) ESR < 120 Ω (f_{Xtal} > 30 MHz) (4) (8)	10		40	MHz
C_{OSCin}	Shunt Capacitance			1		pF
V_{IH}	Input High Voltage	Single-Ended Input, OSCout floating			2.5	V

(5) See *差分电压测量术语* for definition of V_{OD} and V_{ID}.
(6) Refer to application note AN-912 Common Data Transmission Parameters and their Definitions for more information.
(7) When using differential signals with V_{CM} outside of the acceptable range for the specified V_{ID}, the clock must be AC coupled.
(8) The ESR requirements stated are what is necessary in order to ensure that the Oscillator circuitry has no start up issues. However, lower ESR values for the crystal might be necessary in order to stay below the maximum power dissipation requirements for that crystal.

6.6 Typical Characteristics

Unless otherwise specified: V_{dd} = V_{ddo} = 3.3 V, T_A = 20 °C, C_L = 5 pF, CLKin driven differentially, input slew rate ≥ 2 V/ns.

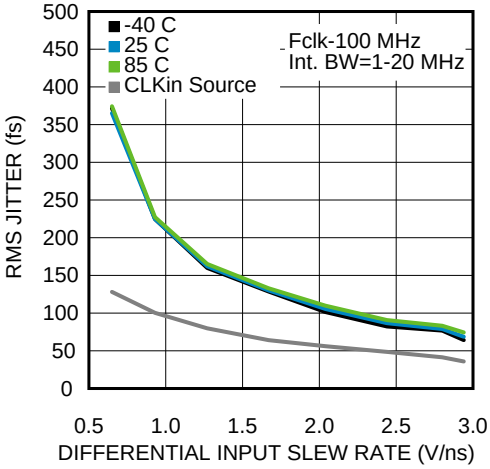


Figure 1. RMS Jitter vs. CLKin Slew Rate @ 100 MHz

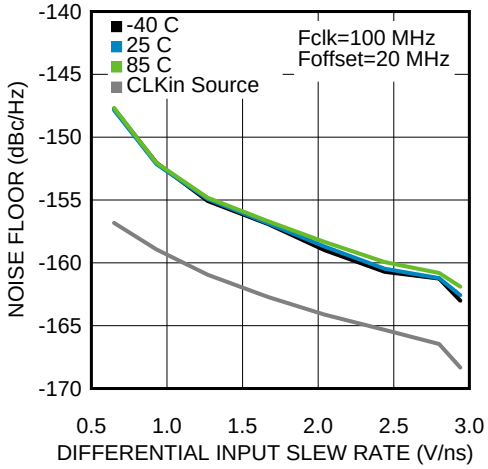
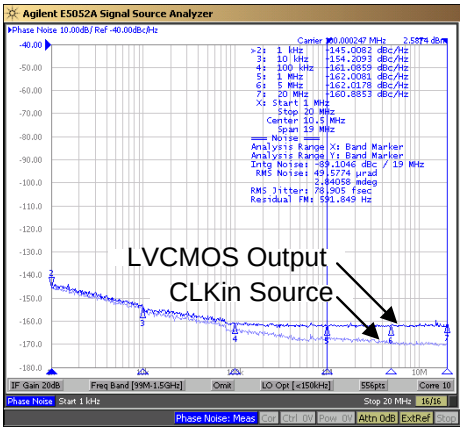


Figure 2. Noise Floor vs. CLKin Slew Rate @ 100 MHz



Test conditions: LVCMOS Input, slew rate ≥ 2 V/ns, C_L = 5 pF in parallel with 50 Ω, BW = 1 MHz to 20 MHz

Figure 3. LVCMOS Phase Noise @ 100 MHz

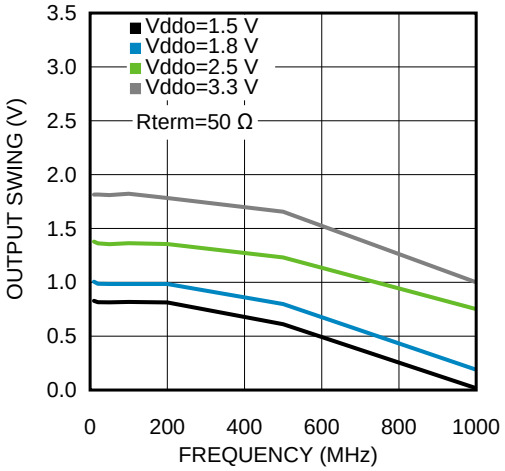


Figure 4. LVCMOS Output Swing vs. Frequency

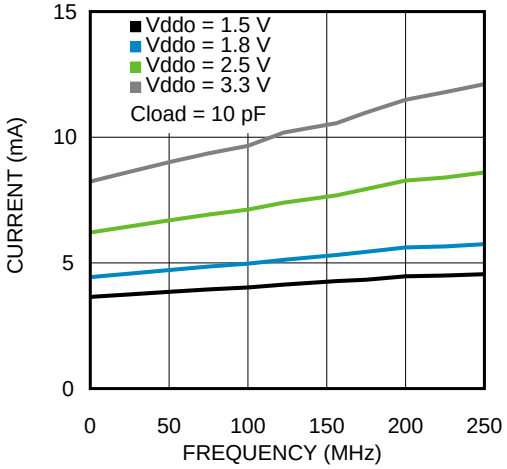


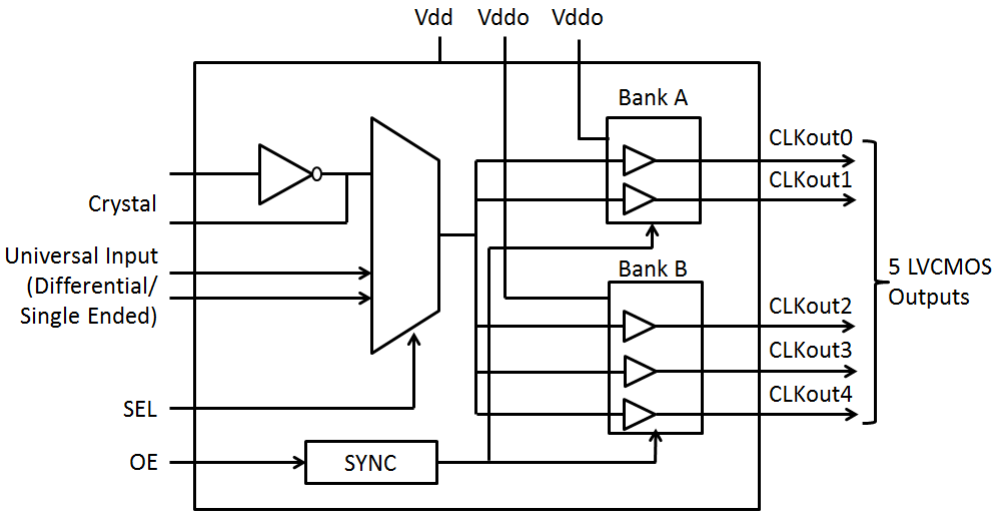
Figure 5. Iddo per Output vs Frequency

7 Detailed Description

7.1 Overview

The LMK00105 is a 5 output LVCMOS clock fanout buffer with low additive jitter that can operate up to 200 MHz. It features a 2:1 input multiplexer with a crystal oscillator input, single supply or dual supply (lower power) operation, and pin-programmable device configuration. The device is offered in a 24-pin WQFN package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 V_{dd} and V_{ddo} Power Supplies

Separate core and output supplies allow the output buffers to operate at the same supply as the Vdd core supply (3.3 V or 2.5 V) or from a lower supply voltage (3.3 V, 2.5 V, 1.8 V, or 1.5 V). Compared to single-supply operation, dual supply operation enables lower power consumption and output-level compatibility.

Bank A (CLKout0 and CLKout1) and Bank B (CLKout2 to CLKout4) may also be operated at different V_{ddo} voltages, provided neither V_{ddo} voltage exceeds V_{dd}.

NOTE

Care should be taken to ensure the V_{ddo} voltage does not exceed the V_{dd} voltage to prevent turning-on the internal ESD protection circuitry.

DO NOT DISCONNECT OR GROUND ANY OF THE V_{ddo} PINS because the V_{ddo} pins are internally connected within an output bank.

7.3.2 Clock Input

The LMK00105 has one differential input, CLKin/CLKin* and OSCin, that can be driven in different manners that are described in the following sections.

7.3.2.1 Selection of Clock Input

Clock input selection is controlled using the SEL pin as shown in Table 1. Refer to *Clock Inputs* for clock input requirements. When CLKin is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator will start-up and its clock will be distributed to all outputs. Refer to *Crystal Interface* for more information. Alternatively, OSCin may be driven by a single ended clock, up to 200 MHz, instead of a crystal.

Table 1. Input Selection

SEL	Input
0	CLKin, CLKin*
1	OSCin (Crystal Mode)

7.3.2.1.1 CLKin/CLKin* Pins

The LMK00105 has a differential input (CKLin/CLKin*) which can be driven single-ended or differentially. It can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, or other differential and single ended signals that meet the input requirements in *Electrical Characteristics* and when using differential signals with V_{CM} outside of the acceptable range for the specified V_{ID}, the clock must be AC coupled. Refer to *Clock Inputs* for more details on driving the LMK00105 inputs.

In the event that a Crystal mode is not selected and the CLKin pins do not have an AC signal applied to them, Table 2 following will be the state of the outputs.

Table 2. CLKin Input vs. Output States

CLKin	CLKin*	Output State
Open	Open	Logic Low
Logic Low	Logic Low	Logic Low
Logic High	Logic Low	Logic High
Logic Low	Logic High	Logic Low

7.3.2.1.2 OSCin/OSCout Pins

The LMK00105 has a crystal oscillator which will be powered up when OSCin is selected. Alternatively, OSCin may be driven by a single ended clock, up to 200 MHz, instead of a crystal. Refer to *Crystal Interface* for more information. If Crystal mode is selected and the pins do not have an AC signal applied to them, Table 3 will be the state of the outputs. If Crystal mode is selected an open state is not allowed on OSCin, as the outputs may oscillate due to the crystal oscillator circuitry.

Table 3. OSCin Input vs. Output States

OSCin	Output State
Open	Not Allowed
Logic Low	Logic High
Logic High	Logic Low

7.3.3 Clock Outputs

The LMK00105 has 5 LVCMOS outputs.

7.3.3.1 Output Enable Pin

When the output enable pin is held High, the outputs are enabled. When it is held Low, the outputs are held in a Low state as shown in Table 4.

Table 4. Output Enable Pin States

OE	Outputs
Low	Disabled (Hi-Z)
High	Enabled

The OE pin is synchronized to the input clock to ensure that there are no runt pulses. When OE is changed from Low to High, the outputs will initially have an impedance of about 400 Ω to ground until the second falling edge of the input clock and starting with the second falling edge of the input clock, the outputs will buffer the input. If the OE pin is taken from Low to High when there is no input clock present, the outputs will either go high or low and stay a that state; they will not oscillate. When the OE pin is taken from High to Low the outputs will be Low after the second falling edge of the clock input and then will go to a Disabled (Hi-Z) state starting after the next rising edge.

7.3.3.2 Using Less than Five Outputs

Although the LMK00105 has 5 outputs, not all applications will require all of these. In this case, the unused outputs should be left floating with a minimum copper length to minimize capacitance. In this way, this output will consume minimal output current because it has no load.

NOTE

For best soldering practices, the minimum trace length should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

7.4 Device Functional Modes

LMK00105 can be driven by a clock input or a crystal according to SEL pin. Refer to *Selection of Clock Input* for more information.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Clock Inputs

The LMK00105 has a differential input (CLKin/CLKin*) that can accept AC or DC coupled 3.3V/2.5V LVPECL, LVDS, and other differential and single ended signals that meet the input requirements specified in *Electrical Characteristics*. The device can accept a wide range of signals due to its wide input common mode voltage range (V_{CM}) and input voltage swing (V_{ID})/dynamic range. AC coupling may also be employed to shift the input signal to within the V_{CM} range.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have a high slew rate of 2 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential input signal is recommended over single-ended because it typically provides higher slew rate and common-mode noise rejection.

While it is recommended to drive the CLKin/CLKin* pair with a differential signal input, it is possible to drive it with a single-ended clock provided it conforms to the Single-Ended Input specifications for CLKin pins listed in the *Electrical Characteristics*. For large single-ended input signals, such as 3.3 V or 2.5 V LVCMOS, a 50 Ω load resistor should be placed near the input for signal attenuation to prevent input overdrive as well as for line termination to minimize reflections. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in Figure 6. The output impedance of the LVCMOS driver plus Rs should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.

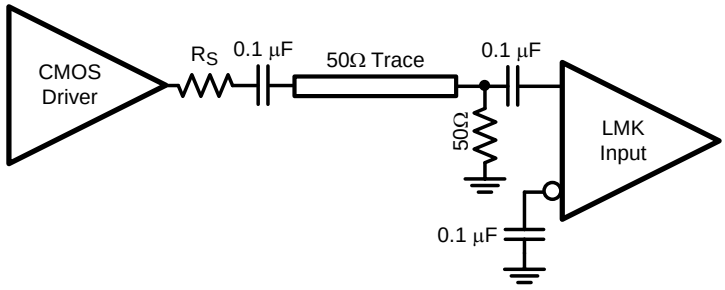


Figure 6. Preferred Configuration: Single-Ended LVCMOS Input, AC Coupling

A single-ended clock may also be DC coupled to CLKin as shown in Figure 7. A 50-Ω load resistor should be placed near the CLKin input for signal attenuation and line termination. Because half of the single-ended swing of the driver ($V_{O,PP}$ / 2) drives CLKin, CLKin* should be externally biased to the midpoint voltage of the attenuated input swing (($V_{O,PP}$ / 2) × 0.5). The external bias voltage should be within the specified input common voltage (V_{CM}) range. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

Application Information (continued)

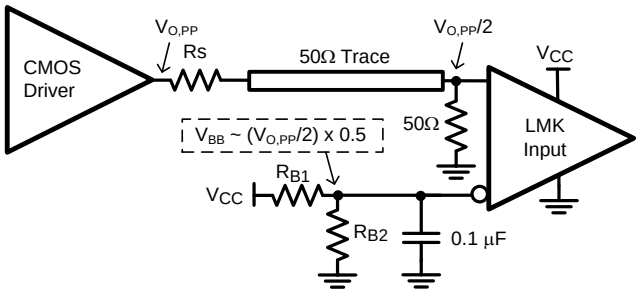


Figure 7. Single-Ended LVCMOS Input, DC Coupling With Common Mode Biasing

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with an single-ended external clock as shown in Figure 8. The input clock should be AC coupled to the OSCin pin, which has an internally generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either differential input (CLKin) since it offers higher operating frequency, better common mode, improved power supply noise rejection, and greater performance over supply voltage and temperature variations.

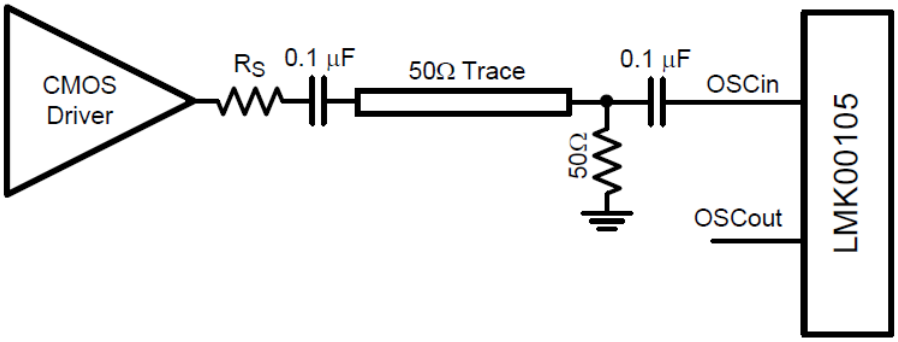


Figure 8. Driving OSCin With a Single-Ended External Clock

8.1.2 Clock Outputs

The LMK00105 LVCMOS driver output impedance (Ro) is nominally 50 ohms and well-matched to drive a 50 ohm transmission line (Zo), as shown as below. If driving a transmission line with higher characteristic impedance than 50 ohms, a series resistor (Rs) should be placed near the driver to provide source termination, where Rs = Zo – Ro.

The LMK00105 has two output banks, Bank A and Bank B, which are separately powered by independent Vddo supply pins. The Vddo supply pins for Bank A and Bank B are not connected together internally, and may be supplied with different voltages. This allows the LMK00105 outputs to easily interface to multiple receivers with different input threshold or input supply voltage (Vddi) requirements without the need for additional voltage divider networks.

Application Information (continued)

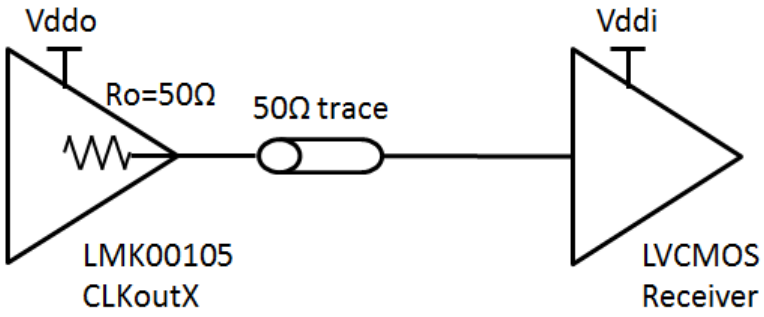


Figure 9. LMK00105 Output Termination

8.2 Typical Applications

8.2.1 Typical Application Block Diagram

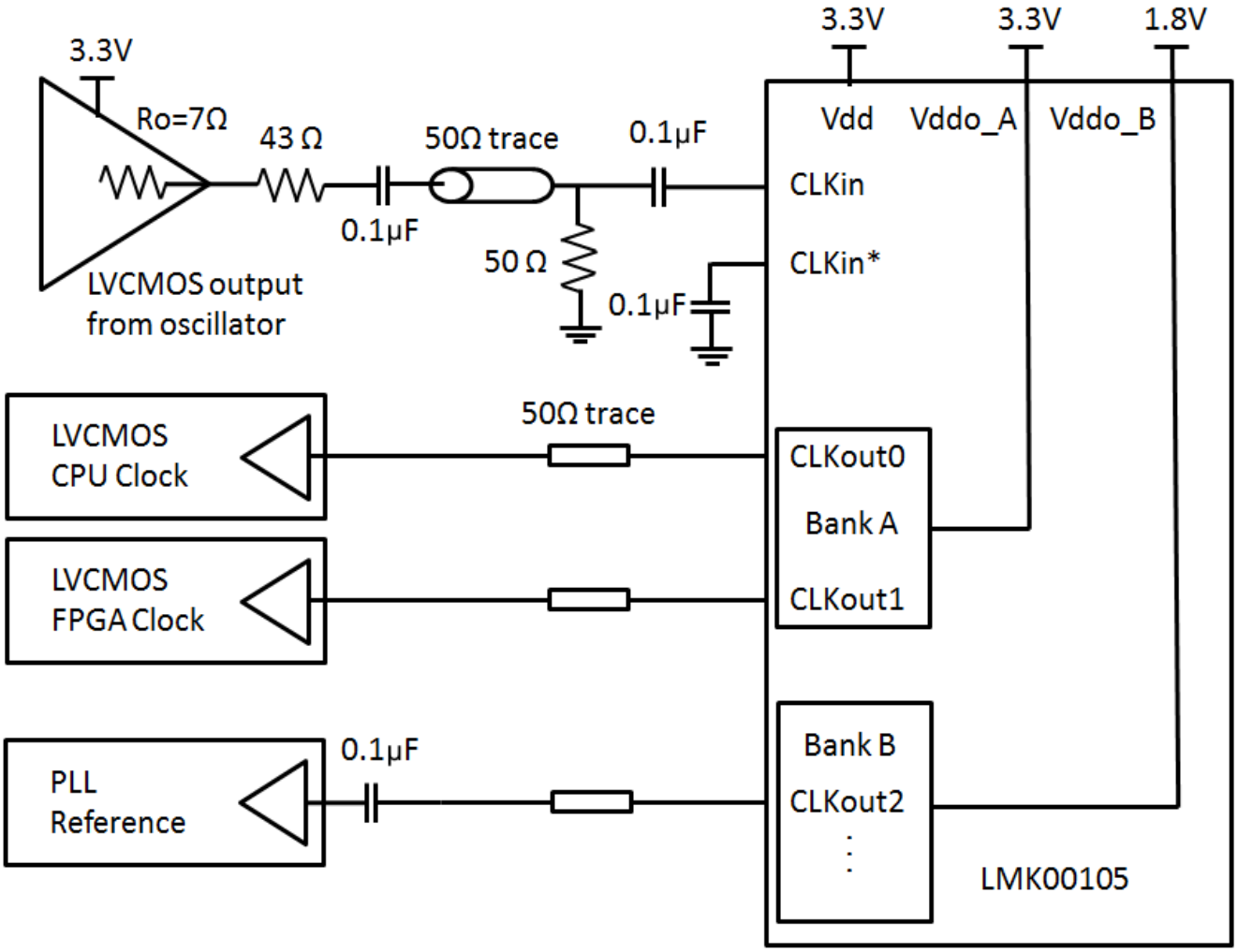


Figure 10. Typical Application Block Diagram

Typical Applications (continued)

8.2.1.1 Design Requirements

In the example application shown in Figure 10, the LMK00105 is used to fan-out a 3.3-V LVCMOS oscillator to three receiver devices with the following characteristics:

- The CPU input accepts a DC-coupled 3.3-V LVCMOS input clock. The LMK00105 has an internal 50-Ω series termination, thus the receiver is connected directly to the output.
- The FPGA input also requires a 3.3-V LVCMOS input clock, like the CPU.
- The PLL input requires a single-ended voltage swing less than 2 Vpp, so 1.8-V LVCMOS input signaling is needed. The PLL receiver requires AC coupling since it has internal input biasing to set its own common mode voltage level.

8.2.1.2 Detailed Design Procedure

Refer to *Clock Inputs* to properly interface the 3.3-V LVCMOS oscillator output to the CLKin input buffer of the LMK00105.

See *Figure 9* for output termination schemes depending on the receiver application. Since the CPU/FPGA inputs and PLL input require different input voltage levels, the LMK00105 output banks are supplied from separate Vddo rails of 3.3 V and 1.8 V for CLKout0/1 (Bank A) and CLKout2 (Bank B), respectively.

Unused outputs can be left floating.

See *Power Supply Recommendations* for recommended power supply filtering and decoupling/bypass techniques.

8.2.1.3 Application Curves

The LMK00105 was tested using multiple low-jitter XO clock sources to evaluate the impact of the buffer's additive phase noise/jitter. The plots on the left show the phase noise of the clock source, while the plots on the right show the total output phase noise from LMK00105 contributed by both the clock source noise and buffer additive noise. Note that the phase noise "hump" around 80 kHz offset on the phase noise plots is correlated to the XO source, which is attributed to power supply noise at this frequency.

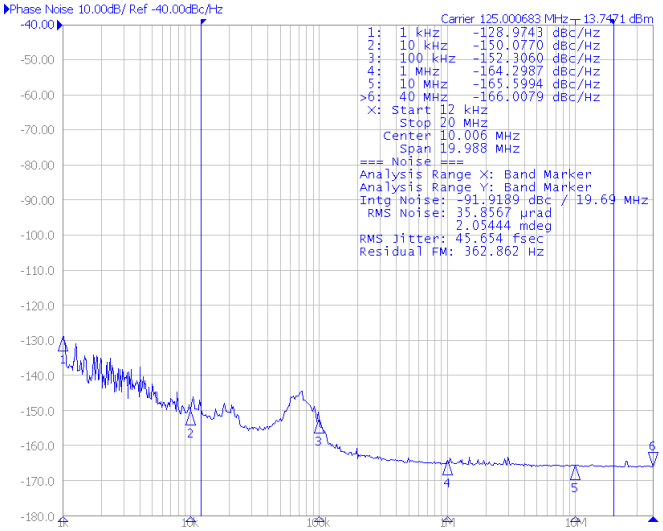


Figure 11. Phase Noise of 125-MHz Clock Source

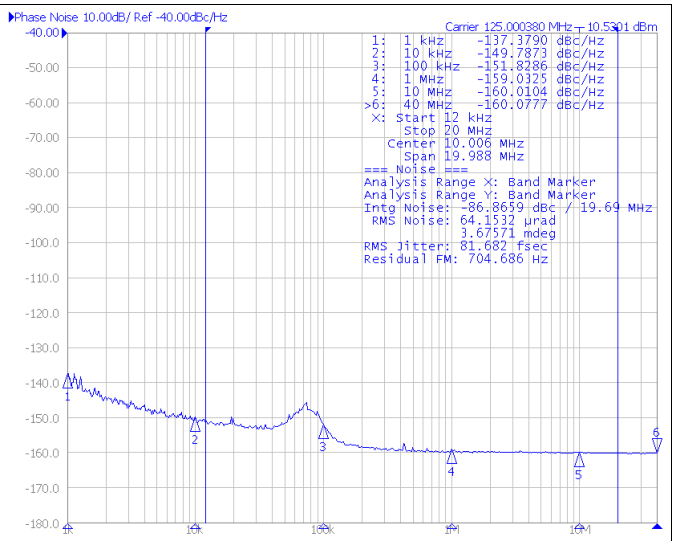


Figure 12. LMK00105 Clock Output

A low-noise 125 MHz XO clock source with 45.6 fs RMS jitter (Figure 11) was used to drive the LMK00105, resulting in in a total output phase jitter of 81.6 fs RMS (Figure 12) integrated from 12 kHz to 20 MHz. The resultant additive jitter of the buffer is 67.7 fs RMS computed using the "Square-Root of the Difference of Squares" method.

Typical Applications (continued)

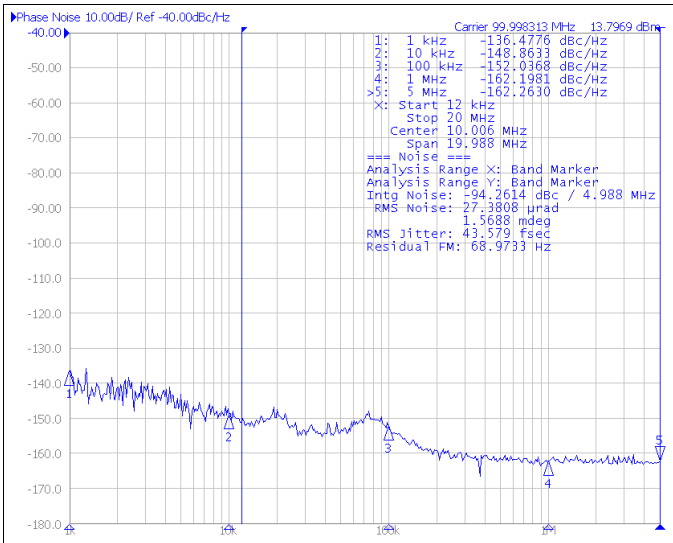


Figure 13. Phase Noise of 100-MHz Clock Source

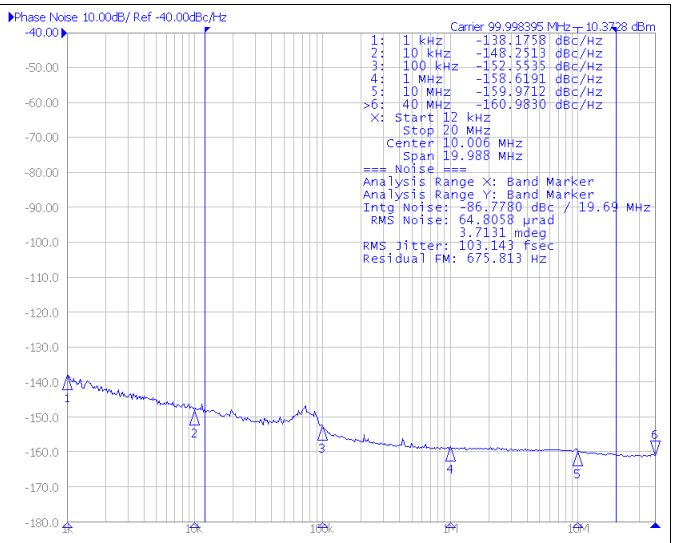


Figure 14. LMK00105 Clock Output

A low-noise 100 MHz XO clock source with 43.5 fs RMS jitter (Figure 13) was used to drive the LMK00105, resulting in a total output phase jitter of 103.1 fs RMS (Figure 14) integrated from 12 kHz to 20 MHz. The resultant additive jitter of the buffer is 93.4 fs RMS computed using the "Square-Root of the Difference of Squares" method.

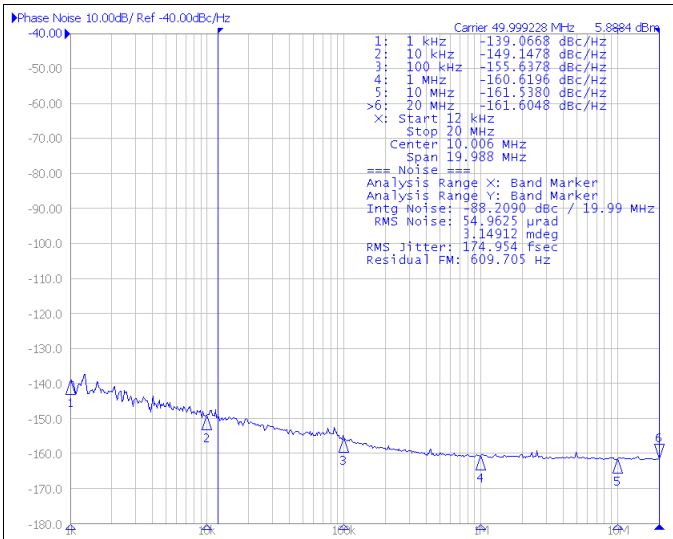


Figure 15. Phase Noise of 50-MHz Clock Source

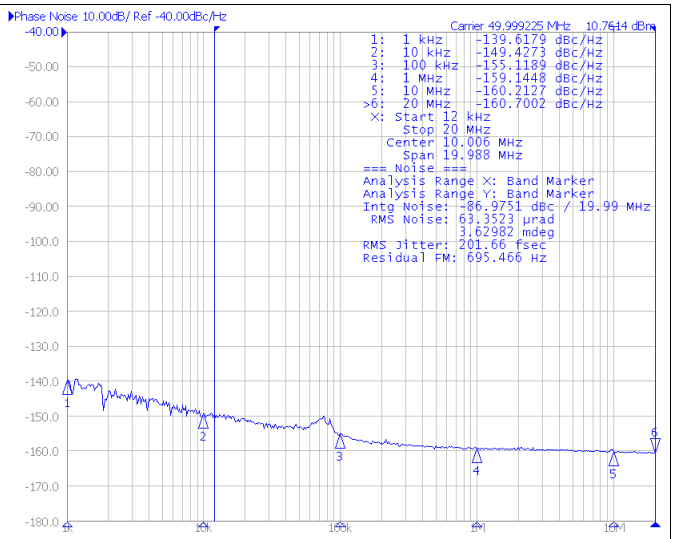


Figure 16. LMK00105 Clock Output

A divide-by-2 circuit was used with the low-noise 100-MHz XO to generate a 50-MHz clock source with 174.9fs RMS jitter (Figure 15), resulting in a total output phase jitter of 201.6 fs RMS (Figure 16) integrated from 12 kHz to 20 MHz.

In this case, the total output phase noise/jitter is highly correlated to the clock source phase noise and jitter, which prevents us from computing the true additive jitter of the buffer using the "Square-Root of the Difference of Squares" method. To accurately specify the additive jitter of the buffer at this frequency, a clock source with lower noise (compared to the DUT) would be needed for this measurement.

Typical Applications (continued)

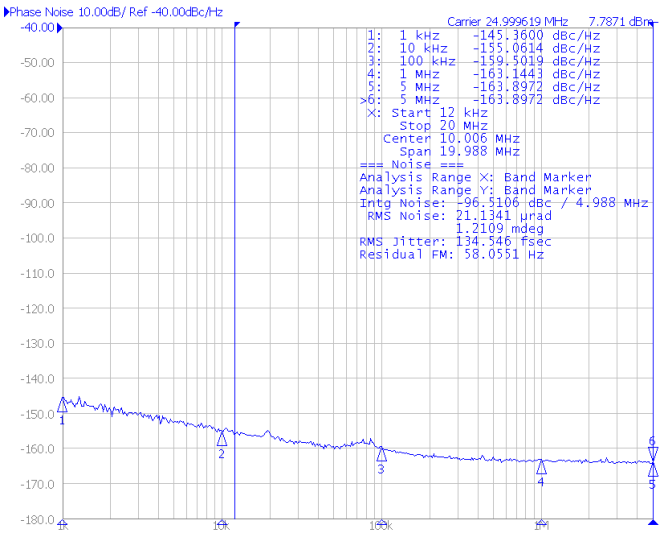


Figure 17. Phase Noise of 25-MHz Clock Source

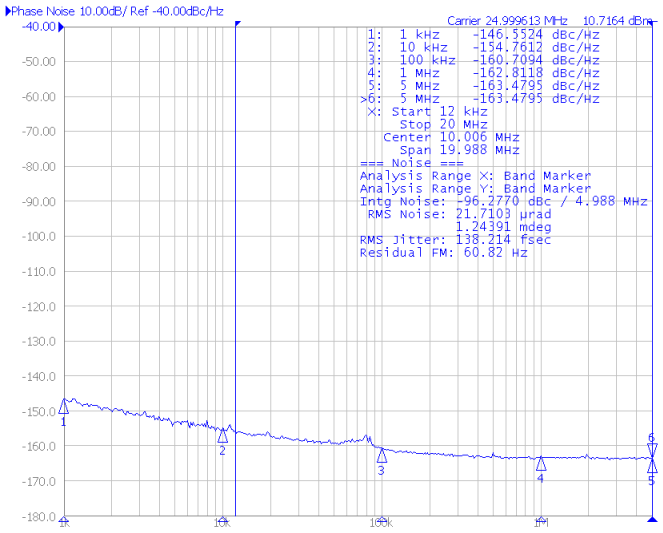


Figure 18. LMK00105 Clock Output

A divide-by-4 circuit was used with the low-noise 100 MHz XO to generate a 25-MHz clock source with 134.5 fs RMS (Figure 17), resulting in a total output phase jitter of 138.2 fs RMS (Figure 18) integrated from 12 kHz to 5 MHz.

In this case, the total output phase noise and jitter is highly correlated to the clock source phase noise and jitter, which prevents us from computing the true additive jitter of the buffer using the “Square-Root of the Difference of Squares” method. To accurately specify the additive jitter of the buffer at this frequency, a clock source with lower noise (compared to the DUT) would be needed for this measurement.

Typical Applications (continued)

8.2.2 Crystal Interface

The LMK00105 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in Figure 19.

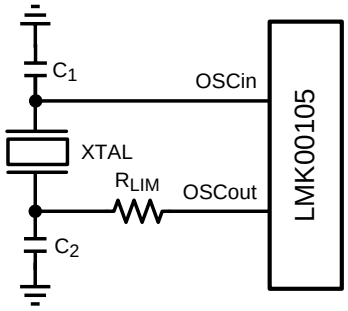


Figure 19. Crystal Interface

8.2.2.1 Design Requirements

The value of capacitor and resistor depend on the crystal. Each crystal is specified with a load capacitance and resistor is used to avoid over driving the crystal.

The example crystal specifications are given in Table 5.

Table 5. Example 25-MHz Crystal Electrical Specifications

NO.	ITEM	SYMBOL	ELECTRICAL SPECIFICATION			
			MIN	TYP	MAX	UNIT
1	Nominal Frequency	F0		25		MHz
2	Mode of Vibration			Fundamental		
3	Frequency Tolerance	ΔF/F0	–15		15	ppm
4	Load Capacitance	CL		9		pF
5	Drive Level	DL		100	300	µW
6	Equivalent Series Resistance	R1		9	50	Ω
7	Shunt Capacitance	C0		2.1 ± 15%		pF
8	Motional Capacitance	C1		9.0 ± 15%		fF
9	Motional Inductance	L		4.6 ± 15%		mH
10	Frequency Stability	TC	–20		20	ppm
11	C0/C1 Rate				250	

Based on the OSCin shunt capacitance and stray capacitance, C1 and C2 are chosen as 6.8 pF to make the load capacitance (CL) to be 9 pF. Suggested value of RLIM is 1.5 kΩ. Refer to *Detailed Design Procedure* for the derivation.

8.2.2.2 Detailed Design Procedure

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 to 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 1 pF typical) of the device and PCB stray capacitance (C_{STRAY} ~ 1 to 3 pF) can affect the discrete load capacitor values, C_1 and C_2. For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so Equation 1 can be rewritten in terms of C_1only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY}) * 2 \quad (3)$$

Electrical Characteristics provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR} * (1 + C_0 / C_L)^2 \quad (4)$$

Where:

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the maximum equivalent series resistance specified for the crystal.
- C_L is the load capacitance specified for the crystal.
- C_0 is the minimum shunt capacitance specified for the crystal.

I_{RMS} can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in Figure 19, an external resistor, R_{LIM}, can be used to limit the crystal drive level if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ.

Figure 20 shows the LMK00105 output phase noise performance in crystal mode with the 25-MHz crystal specified in Table 5.

8.2.2.3 Application Curves

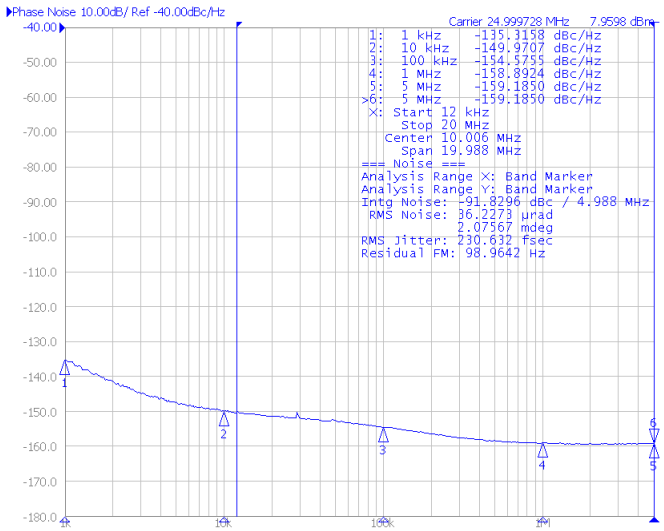


Figure 20. Output Phase Noise in Crystal Mode with 25-MHz Crystal (230.6 fs RMS jitter, 12 kHz to 5 MHz)

9 Power Supply Recommendations

9.1 Power Supply Filtering

It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

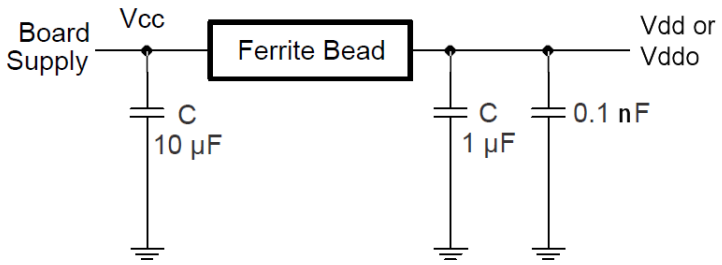


Figure 21. Power-Supply Decoupling

9.2 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, etc. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00105, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the singleside band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00105, power supply ripple rejection (PSRR), was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the V_{ddo} supply. The PSRR test setup is shown in Figure 22.

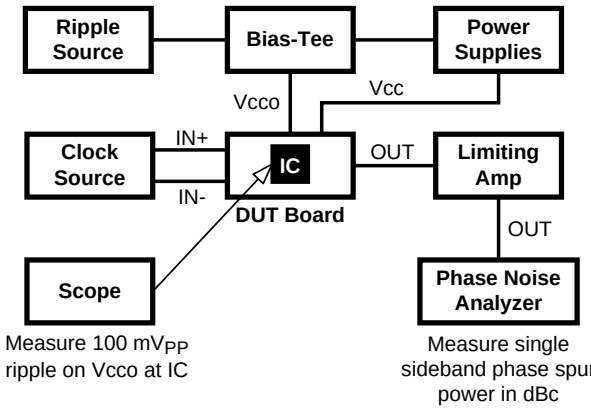


Figure 22. PSRR Test Setup

A signal generator was used to inject a sinusoidal signal onto the V_{ddo} supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the V_{ddo} pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 100 MHz under the following power supply ripple conditions:

Power Supply Ripple Rejection (continued)

- Ripple amplitude: 100 mVpp on V_{ddo} = 2.5 V
- Ripple frequency: 100 kHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ\ (ps\ pk\text{-}pk) = [(2 * 10^{(PSRR/20)}) / (\pi * f_{clk})] * 10^{12} \quad (5)$$

9.3 Power Supply Bypassing

The V_{dd} and V_{ddo} power supplies should have a high frequency bypass capacitor, such as 100 pF, placed very close to each supply pin. Placing the bypass capacitors on the same layer as the LMK00105 improves input sensitivity and performance. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

10 Layout

10.1 Layout Guidelines

10.1.1 Ground Planes

Solid ground planes are recommended as they provide a low-impedance return paths between the device and its bypass capacitors and its clock source and destination devices. Avoid return paths of other system circuitry (for example, high-speed/digital logic) from passing through the local ground of the device to minimize noise coupling, which could induce added jitter and spurious noise.

10.1.2 Power Supply Pins

Follow the power supply schematic and layout example described in *Power Supply Bypassing*.

10.1.3 Differential Input Termination

- Place input termination resistors as close as possible to the CLKin/CLKin* pins.
- Avoid or minimize vias in the 50-Ω input traces to minimize impedance discontinuities. Intra-pair skew should be also be minimized on the differential input traces.
- If not used, CLKin/CLKin* inputs may be left floating.

10.1.4 Output Termination

- Place series termination resistors as close as possible to the CLKoutX outputs at the launch of the controlled impedance traces.
- Avoid or minimize vias in the 50-Ω traces to minimize impedance discontinuities.
- Any unused CLKoutX output should be left floating and not routed.

10.2 Layout Example

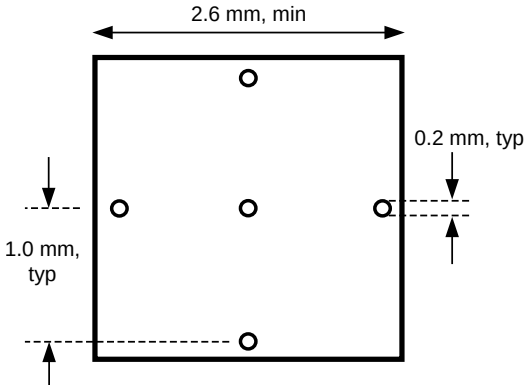


Figure 23. Recommended Land and Via Pattern

10.3 Thermal Management

For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, TA (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in Figure 23. More information on soldering WQFN packages and gerber footprints can be obtained: www.ti.com/packaging.

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 23 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

11 器件和文档支持

11.1 文档支持

11.1.1 差分电压测量术语

差分信号的差分电压存在两种不同的定义，这会导致读者在阅读数据表或与其他工程师交流时产生混淆。 本部分将介绍差分信号的测量和说明，以便读者在使用时能够理解并区分这两种不同的定义。

差分信号的第一种定义是反相和同相信号之间电势差的绝对值。 这种测量的符号通常为 V_{ID} 或 V_{OD}，具体取决于说明对象是输入电压还是输出电压。

差分信号的第二种定义测量的是同相信号相对于反相信号的电势。 这种测量的符号为 V_{SS}，该参数通过计算得出。在集成电路 (IC) 中，该信号相对于接地是不存在的，它仅相对于其差分对存在。 V_{SS} 值既可以借助浮动基准电压直接通过示波器测得，也可以通过将第一部分所述的 V_{OD} 值乘以 2 计算得出。

图 24 并排显示了针对输入的两种不同定义，而 图 25 并排显示了针对输出的两种不同定义。 V_{ID} 和 V_{OD} 定义中给出了 V_{IH} 和 V_{IL} 两个直流电平，同相信号和反相信号均在这两种电平之间切换（相对于接地）。 在 V_{SS} 输入和输出定义中，如果将反相信号视为基准电势，则此时同相信号的电势将超出以接地为基准时的同相电势范围。 因此，可以测量差分信号的峰峰值电压。

V_{ID} 和 V_{OD} 通常定义为电压 (V)，V_{SS} 通常定义为电压峰峰值 (V_{PP})。

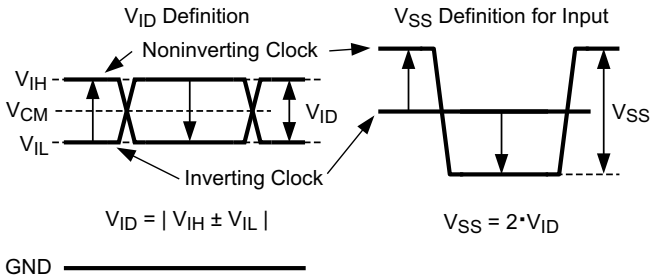


图 **24.** 差分输入信号的两种不同定义

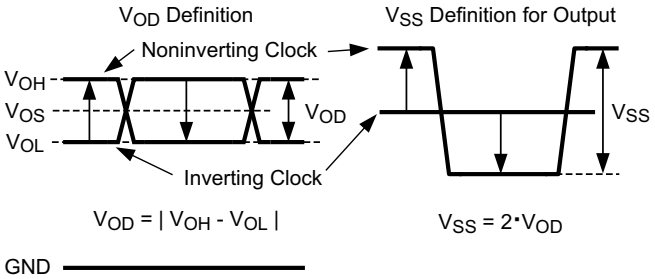


图 **25.** 差分输出信号的两种不同定义

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK00105SQ/NOPB	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00105
LMK00105SQ/NOPB.A	Active	Production	WQFN (RTW) | 24	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00105
LMK00105SQE/NOPB	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00105
LMK00105SQE/NOPB.A	Active	Production	WQFN (RTW) | 24	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00105
LMK00105SQX/NOPB	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00105
LMK00105SQX/NOPB.A	Active	Production	WQFN (RTW) | 24	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	K00105

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

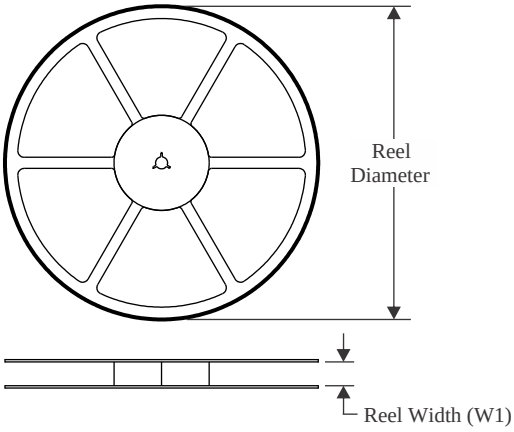
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

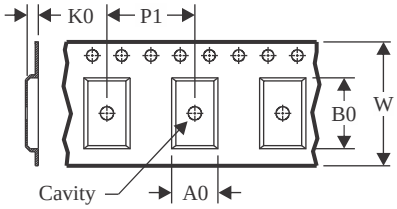
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

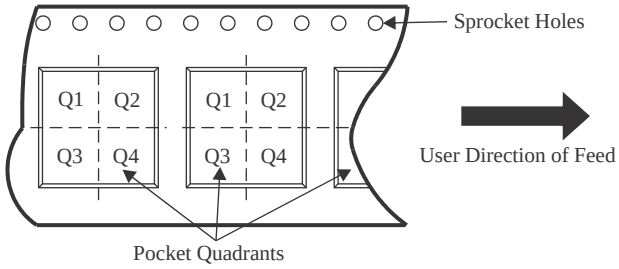


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

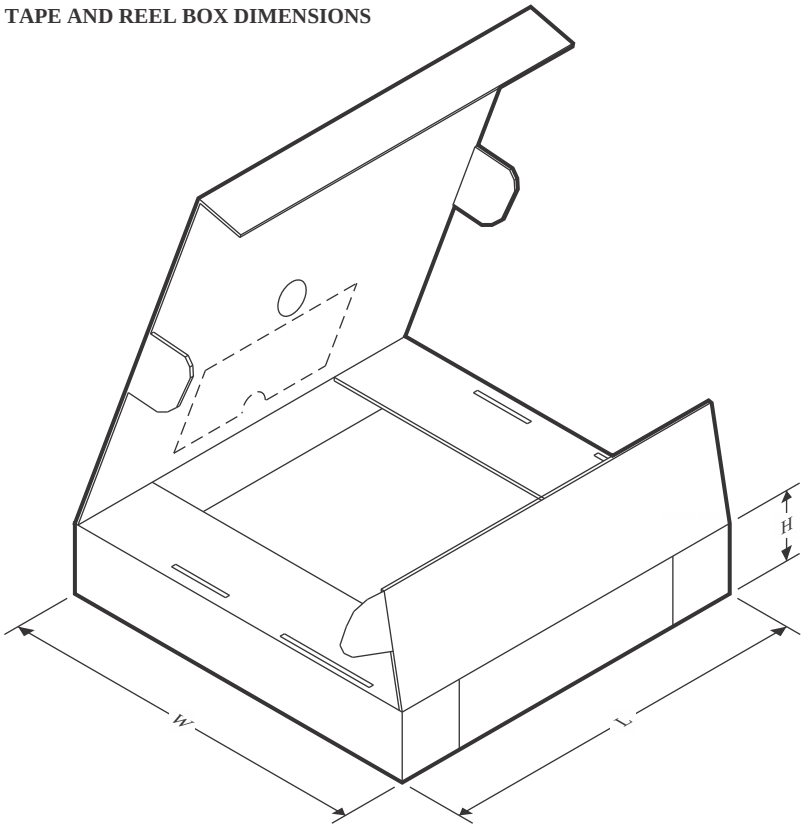
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00105SQ/NOPB	WQFN	RTW	24	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMK00105SQE/NOPB	WQFN	RTW	24	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMK00105SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

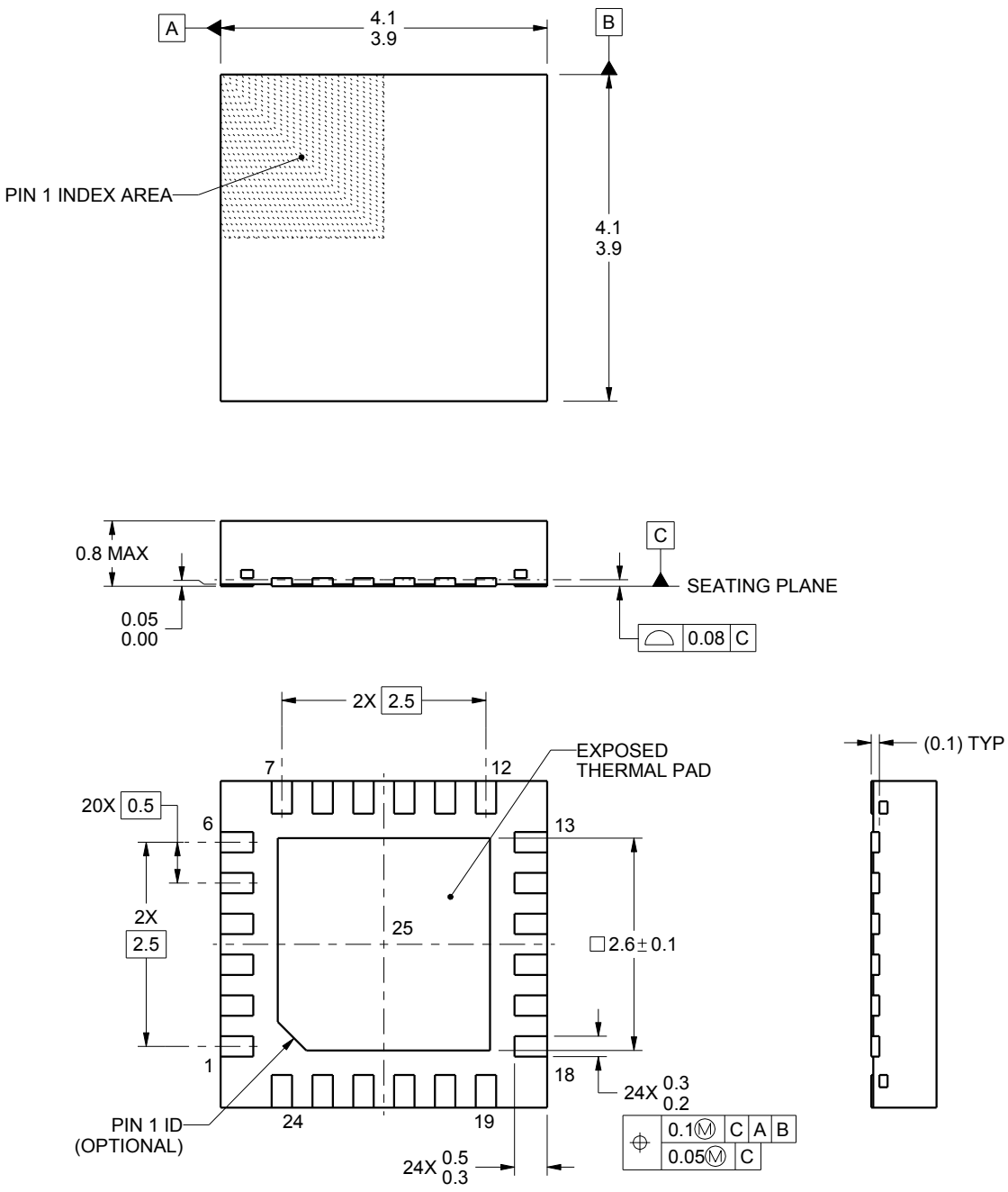
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00105SQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LMK00105SQE/NOPB	WQFN	RTW	24	250	208.0	191.0	35.0
LMK00105SQX/NOPB	WQFN	RTW	24	4500	356.0	356.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

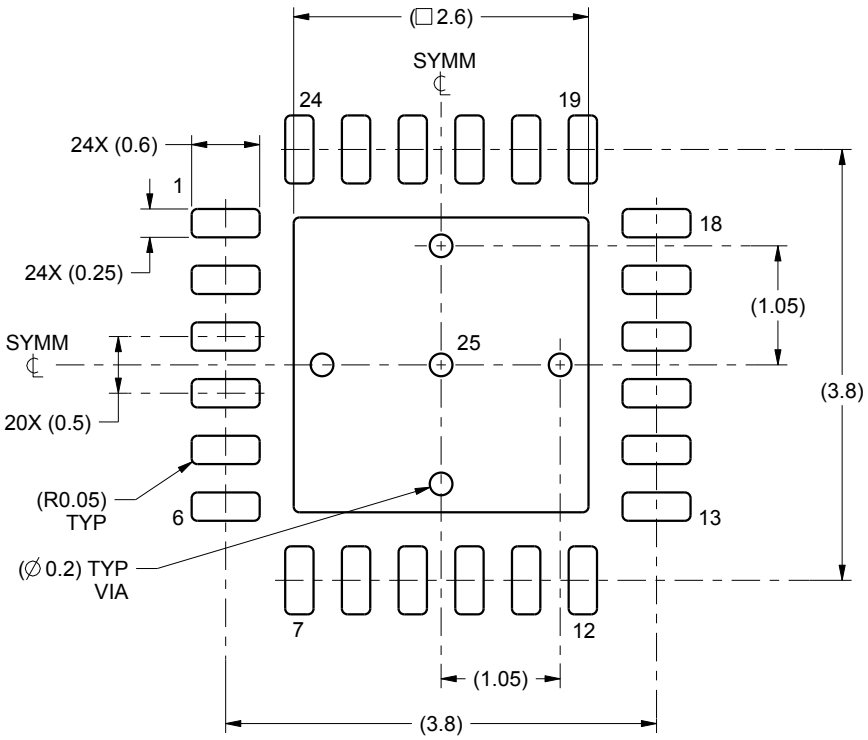
PLASTIC QUAD FLATPACK - NO LEAD



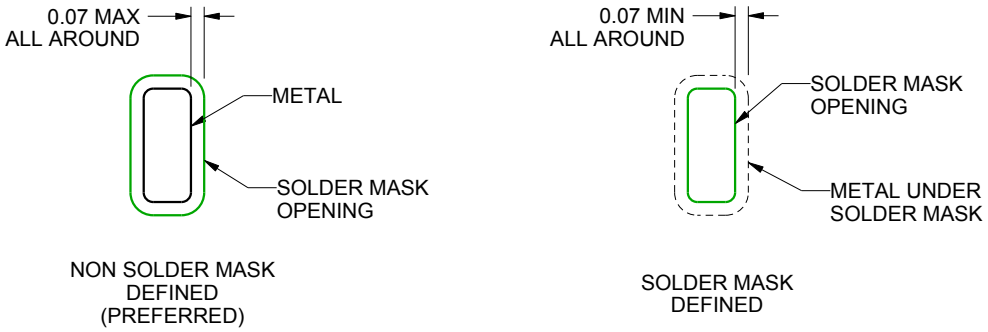
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

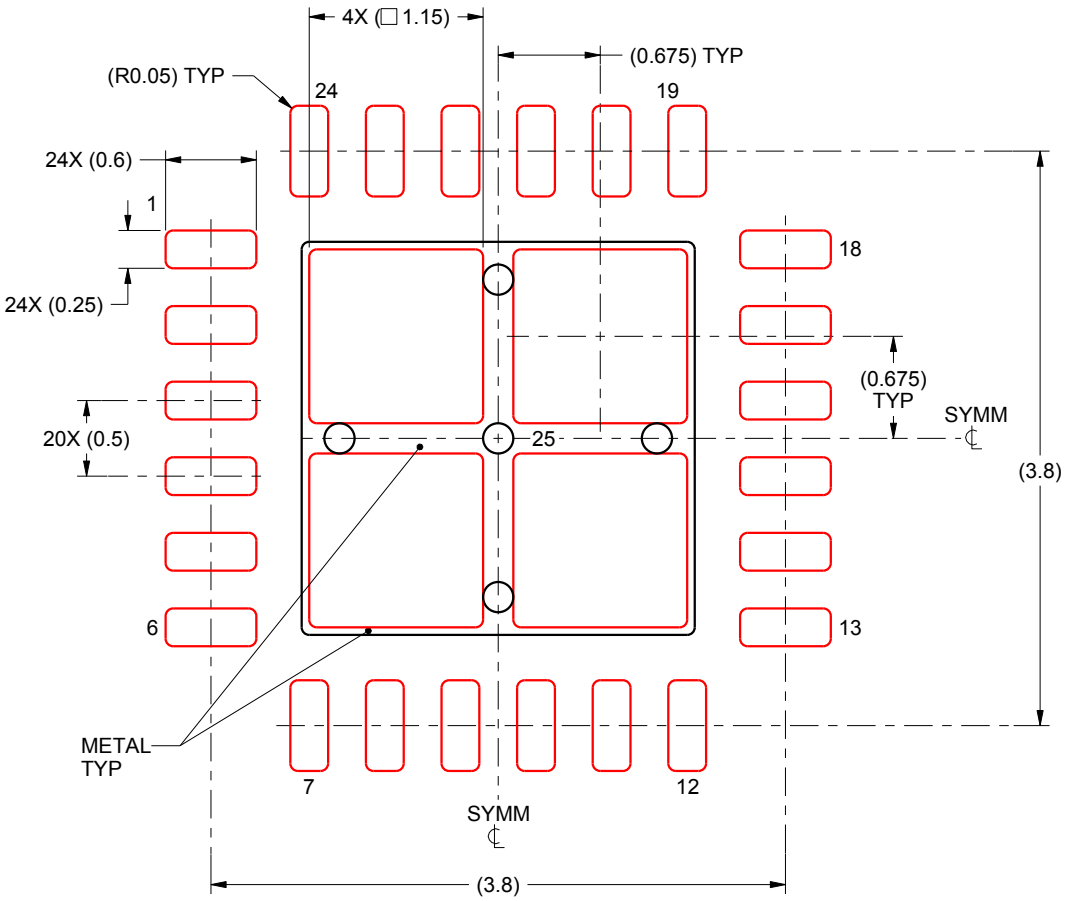


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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最后更新日期：2025 年 10 月