LMG210xR0xx 100V GaN Half-Bridge Power Stage With Integrated Protection and Smart-Switching Features

ADVANCE INFORMATION

1 Features

- GaN half bridge power stage with integrated driver: 100V (GaN FET options: 2.2mΩ, 4.4mΩ)
- Efficient and high-density power conversion with
  - Ultra-low propagation delay (20ns) and matching (2ns)
  - Independent turn-on and turn-off slew-rate control for both the GaN FETs
  - Zero-voltage detection (ZVD) reporting for dead-time optimization
  - Ideal diode mode (IDM) to reduce third quadrant losses in soft switching application
- Input control flexibility
  - Independent input mode (IIM) control
  - Single PWM input with resistor programmable dead time option for IO-limited controllers
- Robust protection
  - Interlock protection in IIM mode (LMG2104)
  - Internal bootstrap supply voltage regulation to prevent GaN FET overdrive
  - V_{DS} monitoring based cycle-by-cycle short-circuit protection
  - Fault indication for over-temperature, supply under-voltage and short-circuit events
- External bias power supply: 5V
  - Supports 3.3V and 5V input logic levels
- Parasitic optimized QFN package with exposed top pad to support top-side cooling

2 Applications

- Server PSU and BBU
- Telecom power
- Energy infrastructure
- Motor drives
- Class-D audio amplifiers

3 Description

The LMG210xR0xx device is a family of 100V half-bridge power stages, with integrated gate-driver and enhancement-mode gallium nitride (GaN) FETs. The devices consist of a high-frequency GaN FET driver in a half-bridge configuration, that drives two 100V GaN FETs.

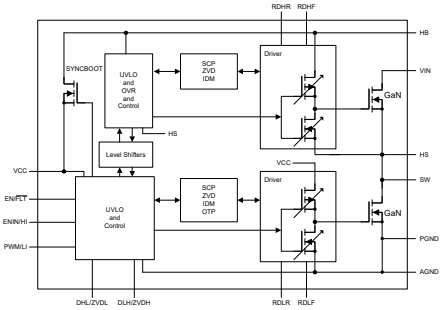
GaN FETs provide significant advantages for power conversion as GaN FETs have zero reverse recovery and very small input capacitance (C_{ISS}) and output capacitance (C_{OSS}). All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements, which can be easily mounted on PCBs.

The TTL logic compatible inputs support 3.3V and 5V logic levels, regardless of the VCC voltage. A proprietary bootstrap voltage control technique regulates the gate voltages of the enhancement mode GaN FETs within the safe operating range. The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. The device is an excellent option for applications requiring high-frequency, high-efficiency operation in a small form factor.

Device Information

PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
LMG210xR022	VBN (VQFN-FCRLF, 18)	7mm × 4.5mm
LMG210xR044	RAR (VQFN-FCRLF, 17)	5.5mm × 4.5mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Tables*.



Simplified Block Diagram

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ADVANCE INFORMATION

4 Device Comparison

Table 4-1. Device Comparison

DEVICE		$R_{DS\ (ON)}$(mΩ)	PACKAGE SIZE[2]
LMG2105R022VBNR	LMG2104R022VBNR	2.2	7.00mm × 4.50mm
LMG2105R044RARR	LMG2104R044RARR	4.4	5.50mm × 4.50mm

Table 4-2. Feature Comparison

PART NUMBER	INTERLOCK IN IIM MODE
LMG2104Rxxx	Enabled
LMG2105Rxxx	Disabled

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5 Device and Documentation Support

5.1 Documentation Support

5.1.1 Related Documentation

- Texas Instruments, *Layout Considerations for LMG5200 GaN Power Stage* application note
- Texas Instruments, *Using the LMG5200: GaN Half-Bridge Power Stage EVM* user's guide

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Trademarks

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

DATE	REVISION	NOTES
May 2026	*	Initial Release

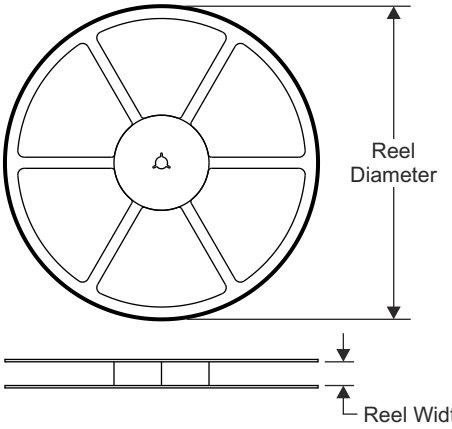
ADVANCE INFORMATION

7 Mechanical, Packaging, and Orderable Information

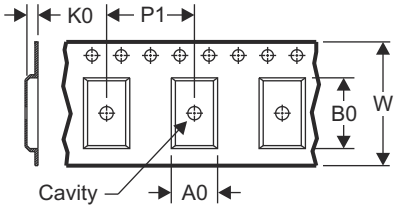
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

REEL DIMENSIONS

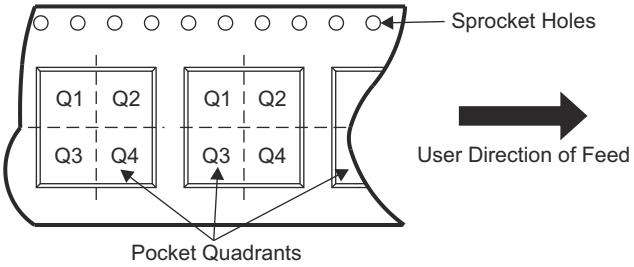


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG2104R022VBNR	VQFN-FCRLF	VBN	18	2000	330	16.4	5.3	7.8	1.2	8	16.0	Q1
LMG2104R044RARR	VQFN-FCRLF	RAR	17	2000	330	16.4	4.8	5.8	1.15	8	16.0	Q1
LMG2105R022VBNR	VQFN-FCRLF	VBN	18	2000	330	16.4	5.3	7.8	1.2	8	16.0	Q1
LMG2105R044RARR	VQFN-FCRLF	RAR	17	2000	330	16.4	4.8	5.8	1.15	8	16.0	Q1

ADVANCE INFORMATION

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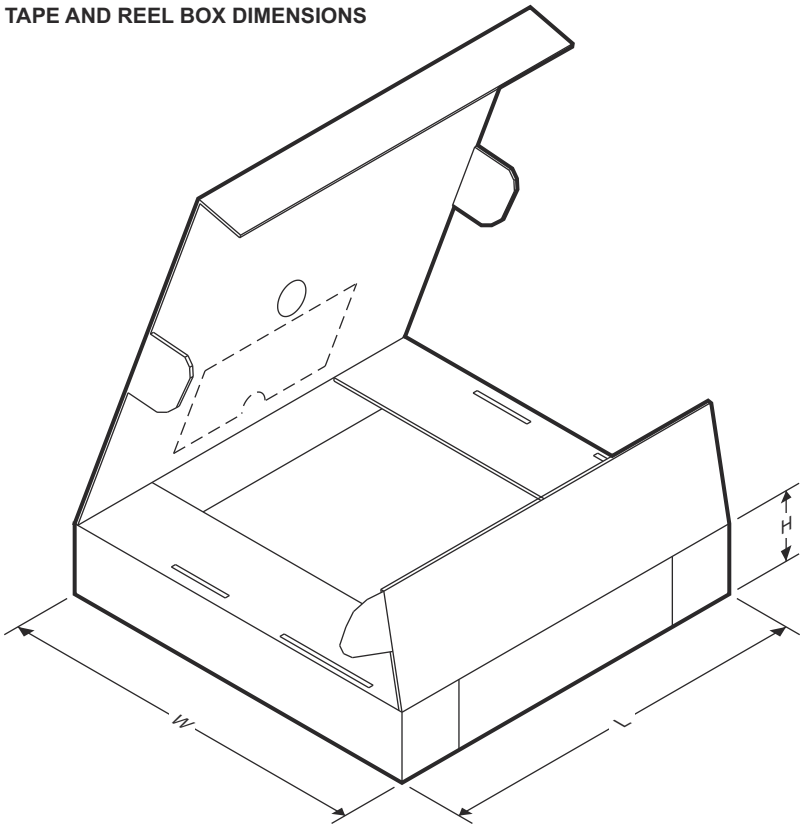
TAPE AND REEL BOX DIMENSIONS



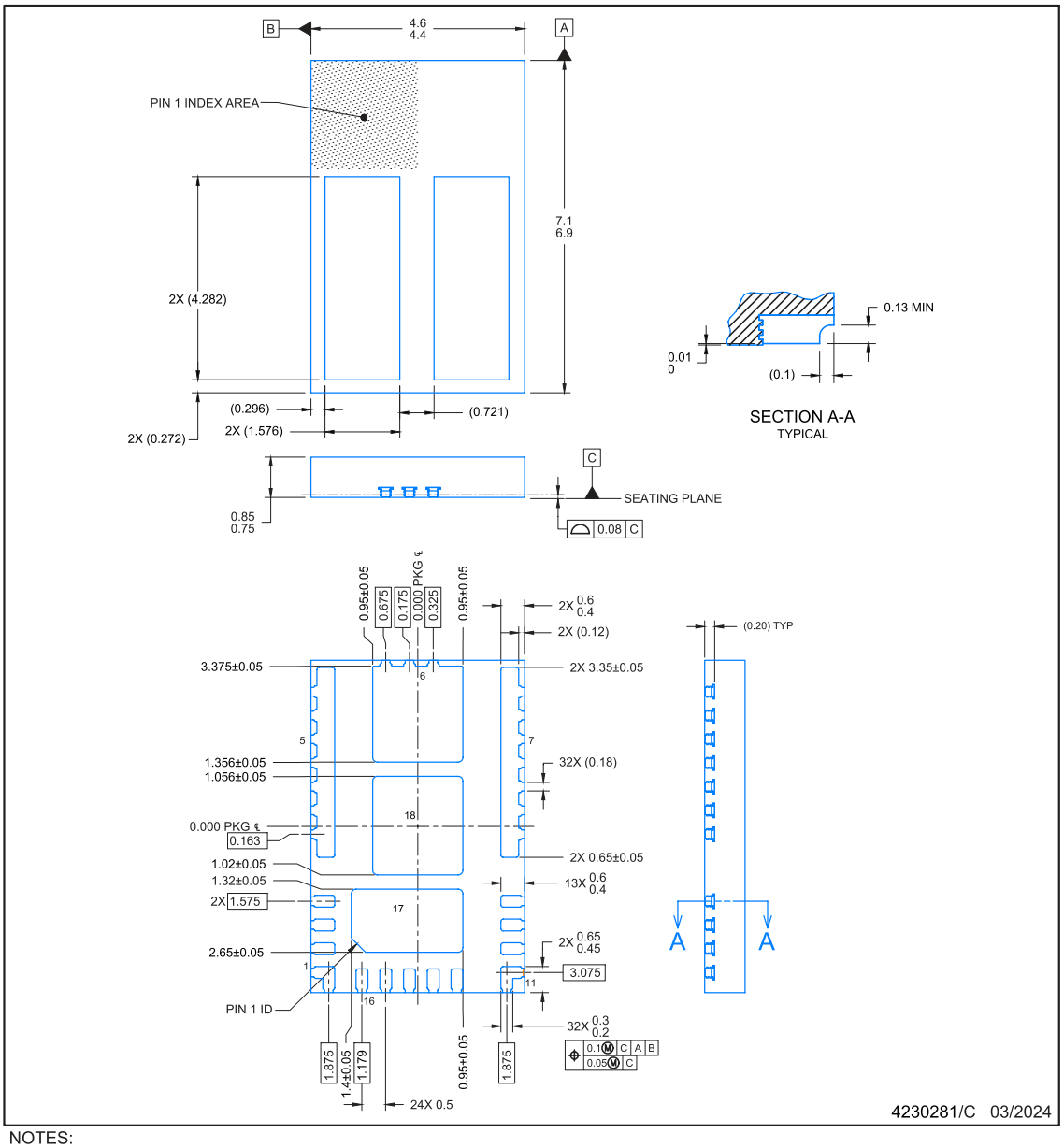
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG2104R022VBNR	VQFN-FCRLF	VBN	18	2000	336.6	336.6	28.6
LMG2104R044RARR	VQFN-FCRLF	RAR	17	2000	336.6	336.6	28.6
LMG2105R022VBNR	VQFN-FCRLF	VBN	18	2000	336.6	336.6	28.6
LMG2105R044RARR	VQFN-FCRLF	RAR	17	2000	336.6	336.6	28.6

7.2 Mechanical Data

PACKAGE OUTLINE

VBN0018A — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

ADVANCE INFORMATION

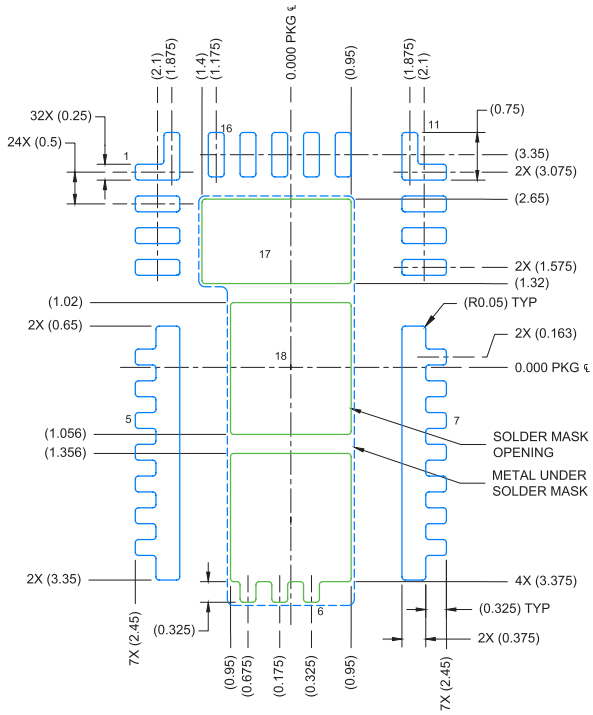
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

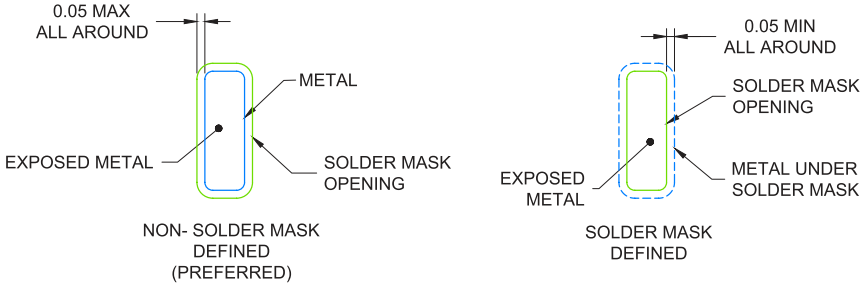
VBN0018A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

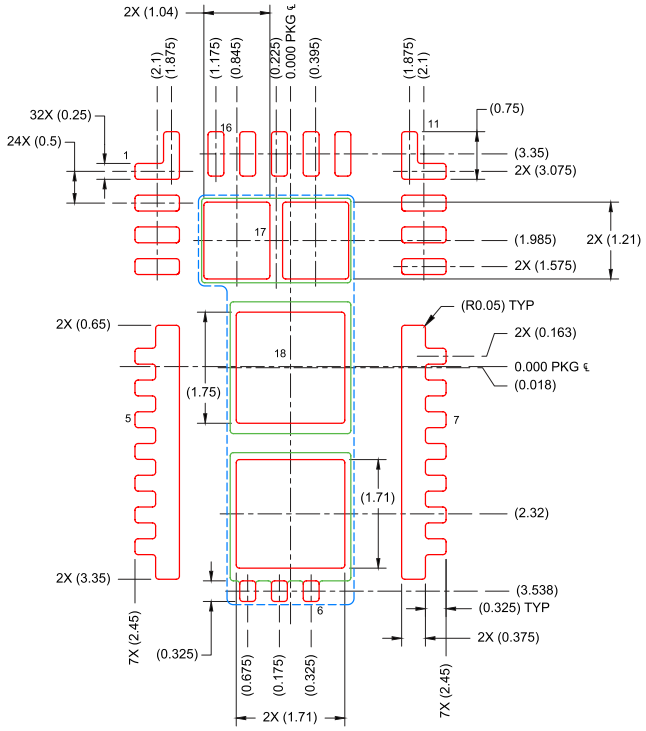
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VBN0018A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 6: 78%
PAD 17: 81%
PAD 18: 76%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

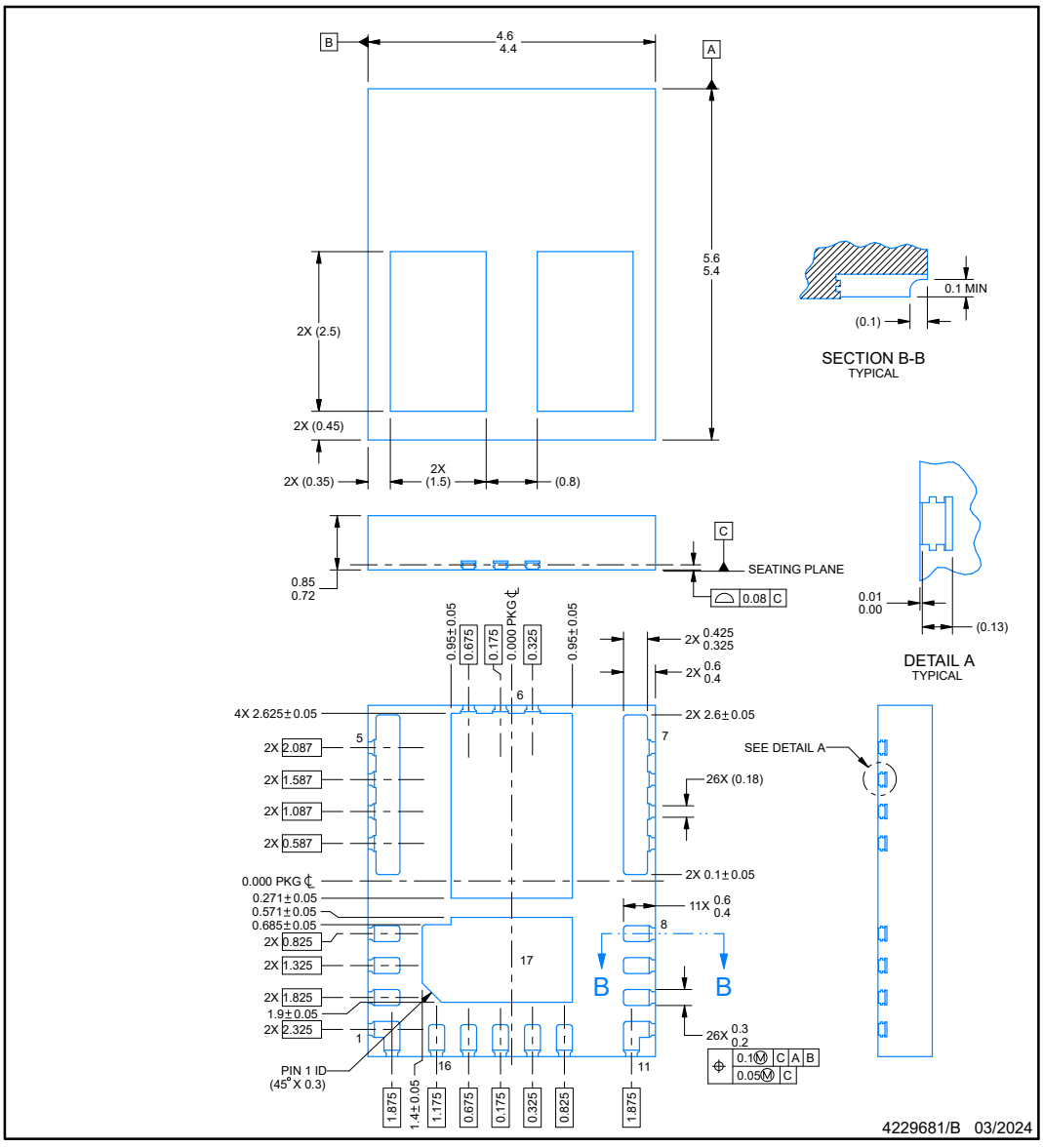
ADVANCE INFORMATION

PACKAGE OUTLINE

RAR0017B

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



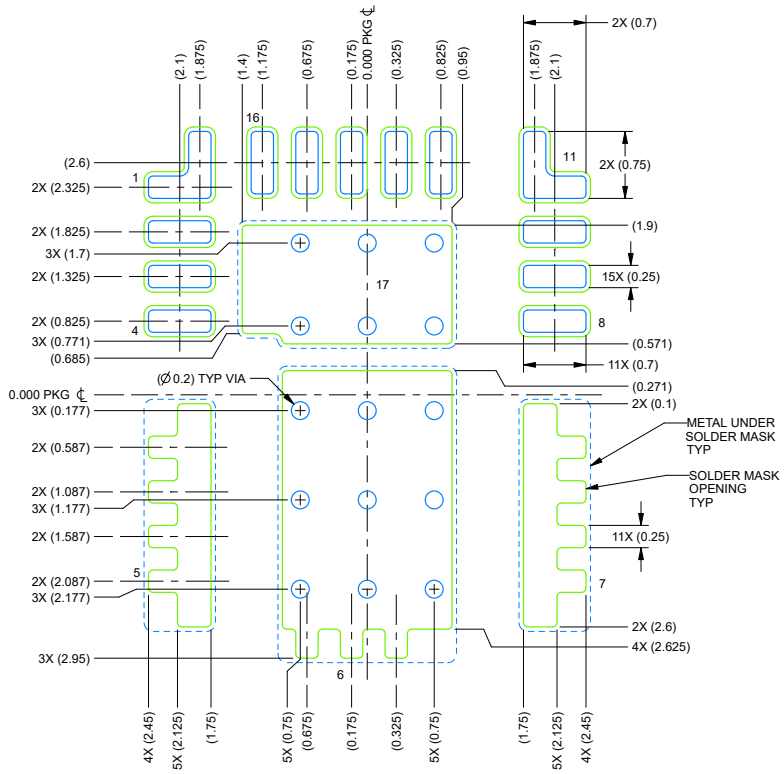
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

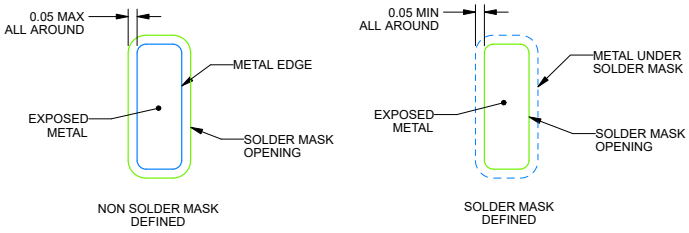
EXAMPLE BOARD LAYOUT

RAR0017B — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

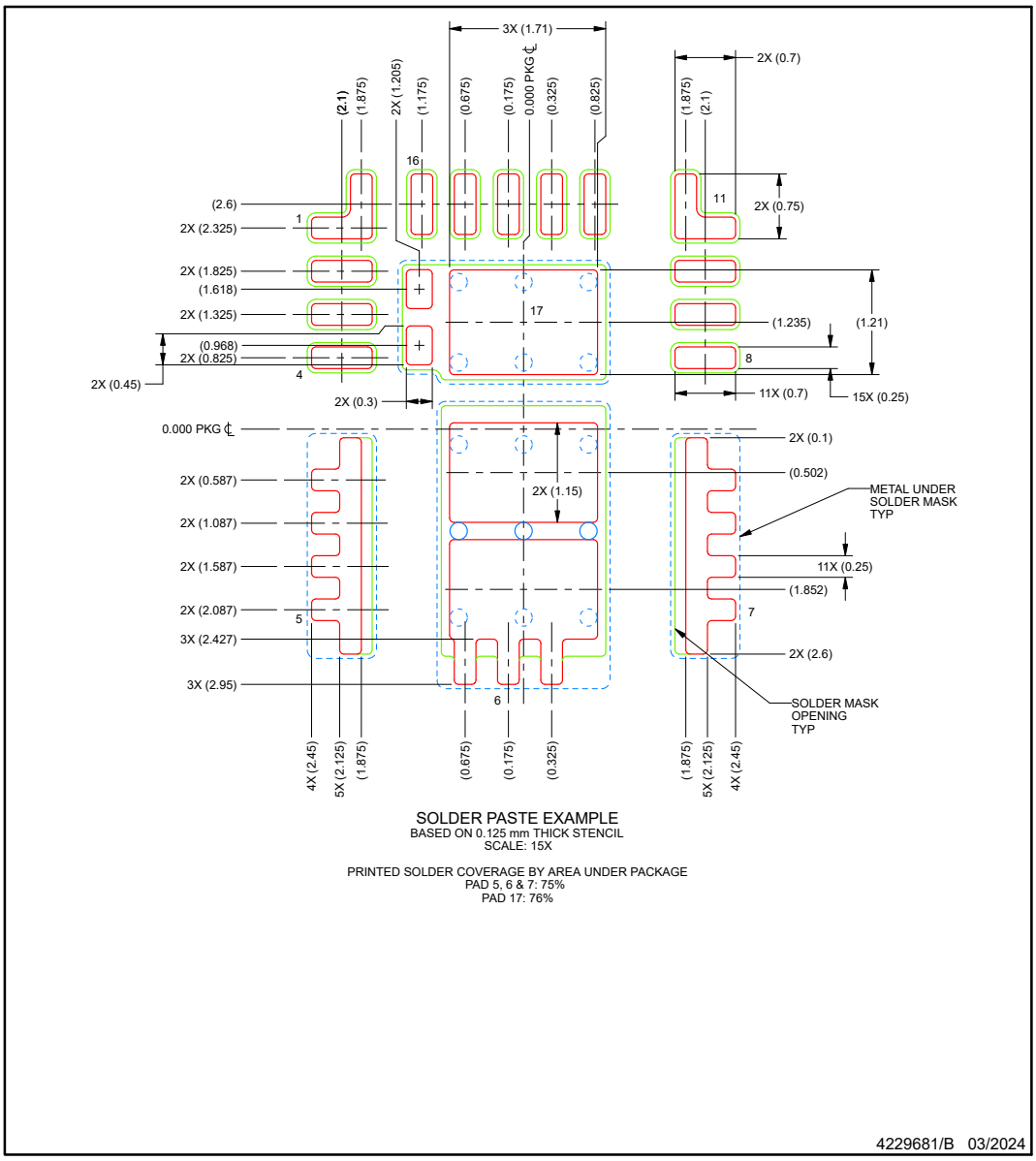
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RAR0017B — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 5, 6 & 7: 75%
PAD 17: 76%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025