LMC649x 双路和四路 CMOS 轨到轨输入/输出运算放大器

1 特性

- 额定温度范围的轨到轨输入共模电压范围
- 轨到轨输出摆幅（在 100mV 电源轨以内、负载为 2kΩ）
- 在 5V 至 15V 电源下工作
- 出色的 CMRR 和 PSRR：82dB
- 超低输入电流：150fA
- 低电源电流（V_S = 5V）：500μA/放大器
- 低失调电压漂移：1.0μV/°C

2 应用

- 汽车传感器放大器
- 压力传感器
- 氧传感器
- 温度传感器
- 速度传感器

3 说明

LMC6492 和 LMC6494 (LMC649x) 放大器专为工作温度范围为 −40°C 至 +125°C 的单电源应用而开发。由于温度范围较宽，此功能是汽车系统的理想选择。独特的设计拓扑使 LMC649x 共模电压范围能够适应超出电源轨的输入信号。这消除了由于输入信号超出传统限制的共模电压范围而导致的非线性输出误差。LMC649x 信号范围具有 82dB 的高 CMRR，可在同相电路配置中实现出色的精度。

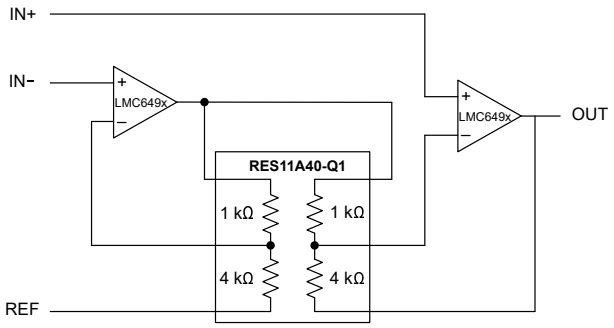
LMC649x 采用轨到轨输入，并具有轨到轨输出摆幅。此配置可提供最大动态信号范围，在 5V 系统中尤为重要。

150fA 超低输入电流和 120dB 开环增益可提供高精度，并可与高阻抗源直接连接。

器件信息

器件型号	通道数	封装(1)
LMC6492	双通道	D（SOIC，8）
LMC6494	四通道	D（SOIC，14）

(1) 有关详细信息，请参阅 节 9。



使用 RES11A-Q1 的两级运算放大器仪表放大器

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Pin Configuration and Functions 2
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 ESD Ratings 4
5.3 Recommended Operating Conditions 4
5.4 Thermal Information 4
5.5 Electrical Characteristics 5
5.6 Typical Characteristics 8
6 Application and Implementation 14
6.1 Application Information 14
6.2 Typical Application 17
6.3 Layout 19
7 Device and Documentation Support 21
7.1 器件支持 21
7.2 接收文档更新通知 22
7.3 支持资源 22
7.4 静电放电警告 22
7.5 术语表 22
8 Revision History 23
9 Mechanical, Packaging, and Orderable Information 23

4 Pin Configuration and Functions

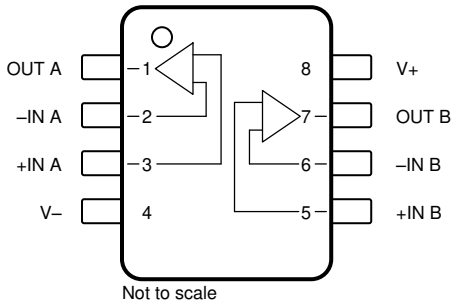


图 4-1. LMC6492: D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions: LMC6492

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for amplifier A
2	−IN A	Input	Inverting input for amplifier A
3	+IN A	Input	Noninverting input for amplifier A
4	V −	Power	Negative supply voltage input
5	+IN B	Input	Noninverting input for amplifier B
6	−IN B	Input	Inverting input for amplifier B
7	OUT B	Output	Output for amplifier B
8	V+	Power	Positive supply voltage input

Copyright © 2023 Texas Instruments Incorporated

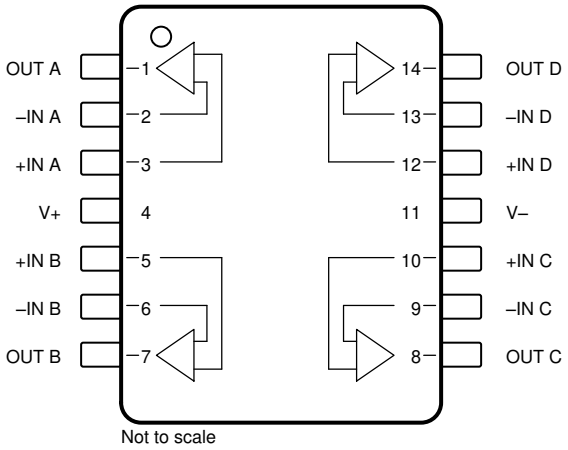


图 4-2. LMC6494: D Package, 14-Pin SOIC (Top View)

表 4-2. Pin Functions: LMC6494

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for amplifier A
2	−IN A	Input	Inverting input for amplifier A
3	+IN A	Input	Noninverting input for amplifier A
4	V+	Power	Positive supply voltage input
5	+IN B	Input	Noninverting input for amplifier B
6	−IN B	Input	Inverting input for amplifier B
7	OUT B	Output	Output for amplifier B
8	OUT C	Output	Output for amplifier C
9	−IN C	Input	Inverting input for amplifier C
10	+IN C	Input	Noninverting input for amplifier C
11	V –	Power	Negative supply voltage input
12	+IN C	Input	Inverting input for amplifier D
13	+IN C	Input	Noninverting input for amplifier D
14	OUT C	Output	Output for amplifier D

Copyright © 2023 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
	Differential input voltage		±Supply Voltage	
	Voltage at input/output pin	(V–) – 0.3	(V+) + 0.3	V
V_S	Supply voltage, V_S = (V+) – (V–)		16	V
	Current at input pin	–5	5	mA
	Current at output pin (3)	–30	30	mA
	Current at power supply pin		40	mA
	Lead temperature (soldering, 10 sec)		260	°C
T_{STG}	Storage temperature	–65	150	°C
T_J	Junction temperature (4)		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If military- or aerospace-specified devices are required, please contact the TI Sales Office or Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over a long term can adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a printed circuit board (PCB).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.5		15.5	V
T_J	Junction temperature	–40		125	℃

5.4 Thermal Information

THERMAL METRIC(1)		LMC6492	LMC6494	UNIT
		D (SOIC)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171	118	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2023 Texas Instruments Incorporated

5.5 Electrical Characteristics

at T_J = +25°C, V+ = 5 V, V– = 0 V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{OS}	Input offset voltage	LMC649xAE			±0.11	±3	mV
			T_A = –40°C to +125°C			±3.8	
		LMC649xBE			±0.11	±6	
			T_A = –40°C to +125°C			±6.8	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±1		µV/°C
I_B	Input bias current				±0.15		pA
		T_A = –40°C to +125°C				±200	
I_{OS}	Input offset current				±0.075		pA
		T_A = –40°C to +125°C				±100	
C_{IN}	Common-mode input capacitance				3		pF
R_{IN}	Input resistance				>10		TΩ
CMRR	Common-mode rejection ratio	LMC649xAE 0 V < V_{CM} < 15 V, V+ = 15 V		65	82		dB
			T_A = –40°C to +125°C	60			
		LMC649xBE 0 V < V_{CM} < 15 V, V+ = 15 V		63	82		
			T_A = –40°C to +125°C	58			
		LMC649xAE 0 V < V_{CM} < 5 V, V+ = 5 V		65	82		
			T_A = –40°C to +125°C	60			
		LMC649xBE 0 V < V_{CM} < 5 V, V+ = 5 V		63	82		
			T_A = –40°C to +125°C	58			
+PSRR	Positive power-supply rejection ratio	LMC649xAE 5 V < V+ < 15 V, V– = 0 V, V_O = 2.5 V		65	82		dB
			T_A = –40°C to +125°C	60			
		LMC649xBE 5 V < V+ < 15 V, V– = 0 V, V_O = 2.5 V		63	82		
			T_A = –40°C to +125°C	58			
–PSRR	Negative power-supply rejection ratio	LMC649xAE –5 V < V– < –15 V, V+ = 0 V, V_O = –2.5 V		65	82		dB
			T_A = –40°C to +125°C	60			
		LMC649xBE –5 V < V– < –15 V, V+ = 0 V, V_O = –2.5 V		63	82		
			T_A = –40°C to +125°C	58			
V_{CM}	Input common-mode voltage	V+ = 5 V and 15 V, for CMRR ≥ 50 dB	Low		(V–) – 0.3	–0.25	V
			Low, T_A = –40°C to +125°C			0	
			High	(V+) + 0.25	(V+) + 0.3		
			High, T_A = –40°C to +125°C	V+			
A_V	Large-signal voltage gain	Sourcing, R_L = 2 kΩ to 7.5 V, V+ = 15 V, 7.5 V ≤ V_O ≤ 11.5 V			300		V/mV
		Sinking, R_L = 2 kΩ to 7.5 V, V+ = 15 V, 3.5 V ≤ V_O ≤ 7.5 V			40		

Copyright © 2023 Texas Instruments Incorporated

5.5 Electrical Characteristics（续）

at T_J = +25°C, V+ = 5 V, V– = 0 V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output swing	V+ = 5 V, R_L = 2 kΩ to V+ / 2	Swing high	4.8	4.9		V
			Swing high, T_A = –40°C to +125°C	4.7			
			Swing low		0.1	0.18	
			Swing low, T_A = –40°C to +125°C			0.24	
		V+ = 5 V, R_L = 600 Ω to V+ / 2	Swing high	4.5	4.7		
			Swing high, T_A = –40°C to +125°C	4.24			
			Swing low		0.3	0.5	
			Swing low, T_A = –40°C to +125°C			0.65	
		V+ = 15 V, R_L = 2 kΩ to V+ / 2	Swing high	14.4	14.7		
			Swing high, T_A = –40°C to +125°C	14.0			
			Swing low		0.16	0.35	
			Swing low, T_A = –40°C to +125°C			0.5	
		V+ = 15 V, R_L = 600 Ω to V+ / 2	Swing high	13.4	14.1		
			Swing high, T_A = –40°C to +125°C	13			
			Swing low		0.5	1.0	
			Swing low, T_A = –40°C to +125°C			1.5	
I_{SC}	Output short-circuit current	V+ = 5 V, sourcing, V_O = 0 V		16	25		mA
			T_A = –40°C to +125°C	10			
		V+ = 5 V, sinking, V_O = 5 V		11	22		
			T_A = –40°C to +125°C	8			
		V+ = 15 V, sourcing, V_O = 0 V		28	30		
			T_A = –40°C to +125°C	20			
		V+ = 15 V, sinking, V_O = 5 V[1]		30	30		
			T_A = –40°C to +125°C	22			
I_S	Supply current	Per amplifier, V+ = 5 V, V_O = V+ / 2			0.5	0.875	mA
			T_A = –40°C to +125°C			1.05	
		Per amplifier, V+ = 15 V, V_O = V+ / 2			0.65	0.975	
			T_A = –40°C to +125°C			1.15	

Copyright © 2023 Texas Instruments Incorporated

5.5 Electrical Characteristics（续）

at T_J = +25°C, V+ = 5 V, V– = 0 V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC SPECS							
SR	Slew rate(2)	V+ = 15 V, connected as voltage follower with 10-V step		0.7	1.3		V/μs
			T_A = –40°C to +125°C	0.5			
GBW	Gain bandwidth	V+ = 15 V			1.5		MHz
Θ_m	Phase margin				50		Deg
G_m	Gain margin				15		dB
	Amp-to-amp isolation	Input referred V+ = 15 V, R_L = 100 kΩ to 7.5 V, V_O = 12 V_{PP}, f = 1 kHz			150		dB
e_n	Input-referred voltage noise	f = 1 kHz, V_{CM} = 1 V			37		nV/$\sqrt{\text{Hz}}$
i_n	Input current noise density	f = 1 kHz			0.06		pA/$\sqrt{\text{Hz}}$
THD	Total harmonic distortion	f = 1 kHz, A_V = –2, R_L = 10 kΩ, V_O = –4.1 V_{PP}			0.01		%
		f = 10 kHz, A_V = –2, R_L = 10 kΩ, V_O = 8.5 V_{PP}, V+ = 10 V			0.01		

(1) Do not short circuit output to V+ when V+ is greater than 13 V or reliability is adversely affected.
(2) Number specified is the slower of either the positive or negative slew rates.

Copyright © 2023 Texas Instruments Incorporated

5.6 Typical Characteristics

at V_S = +15 V, single supply, and T_A = 25°C (unless otherwise specified)

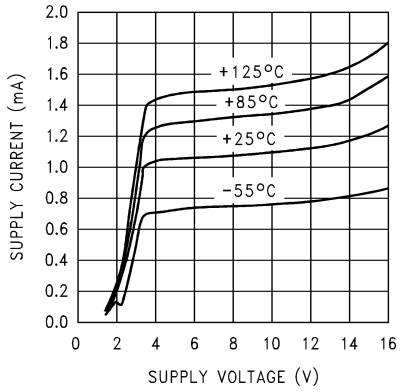


图 5-1. Supply Current vs Supply Voltage

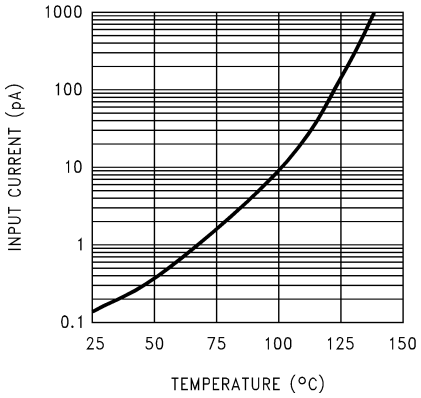


图 5-2. Input Current vs Temperature

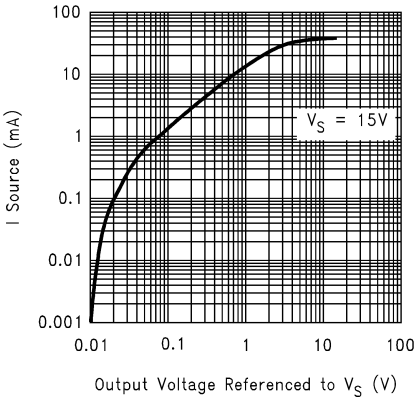


图 5-3. Sourcing Current vs Output Voltage

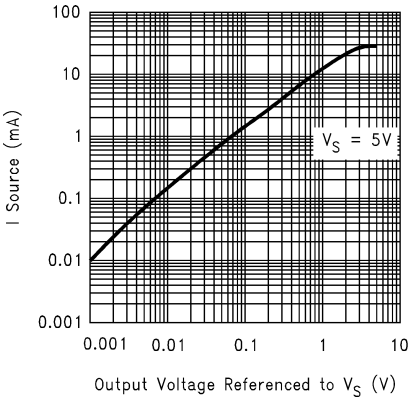


图 5-4. Sourcing Current vs Output Voltage

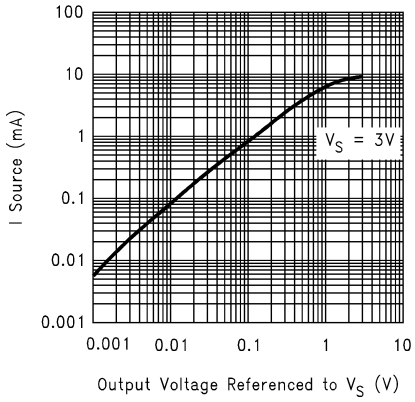


图 5-5. Sourcing Current vs Output Voltage

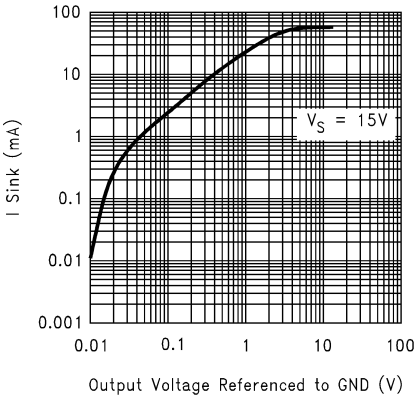


图 5-6. Sinking Current vs Output Voltage

Copyright © 2023 Texas Instruments Incorporated

5.6 Typical Characteristics (continued)

at V_S = +15 V, single supply, and T_A = 25°C (unless otherwise specified)

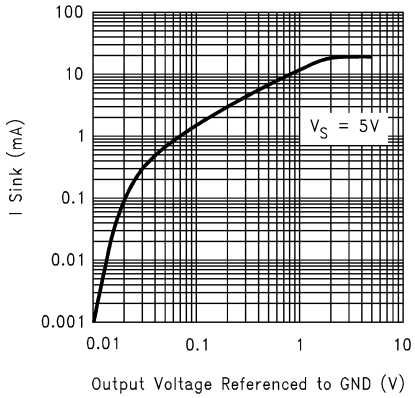


图 5-7. Sinking Current vs Output Voltage

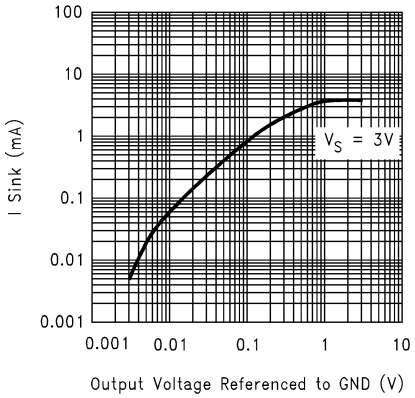


图 5-8. Sinking Current vs Output Voltage

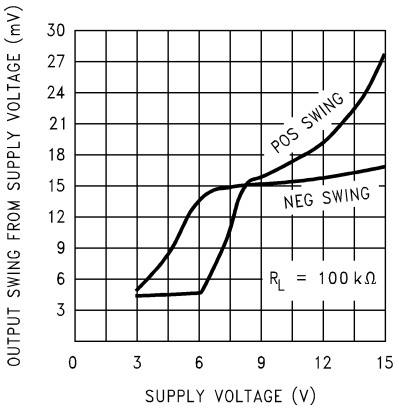


图 5-9. Output Voltage Swing vs Supply Voltage

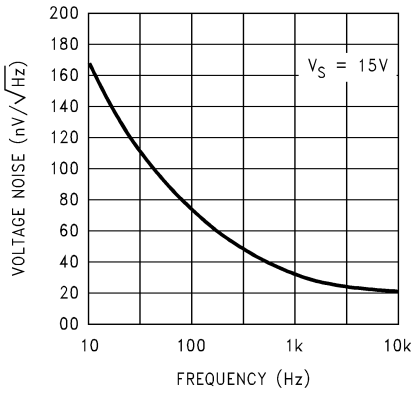


图 5-10. Input Voltage Noise vs Frequency

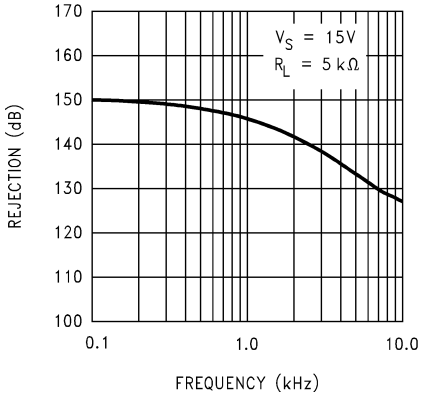


图 5-11. Crosstalk Rejection vs Frequency

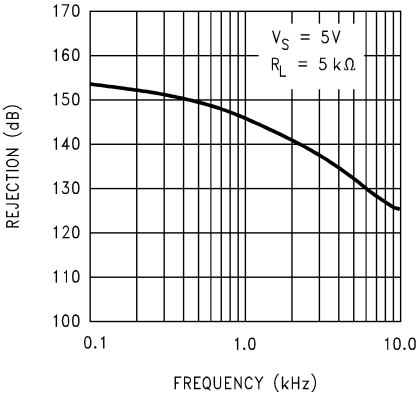


图 5-12. Crosstalk Rejection vs Frequency

Copyright © 2023 Texas Instruments Incorporated

5.6 Typical Characteristics (continued)

at V_S = +15 V, single supply, and T_A = 25°C (unless otherwise specified)

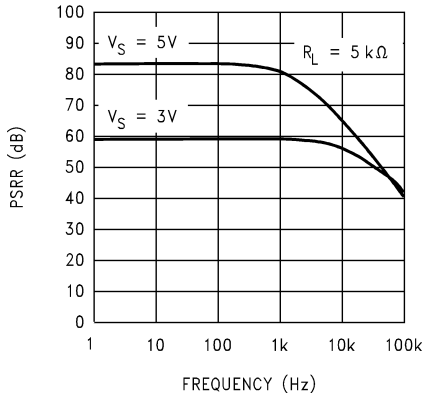


图 5-13. Positive PSRR vs Frequency

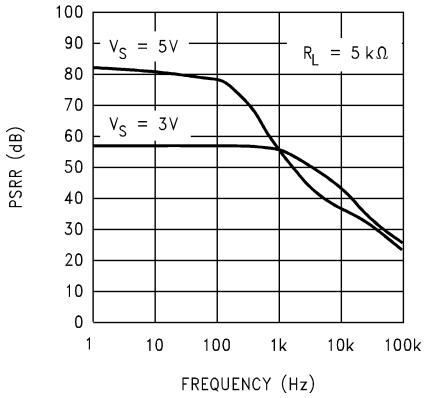


图 5-14. Negative PSRR vs Frequency

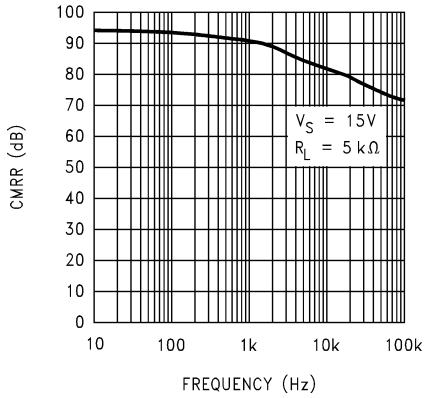


图 5-15. CMRR vs Frequency

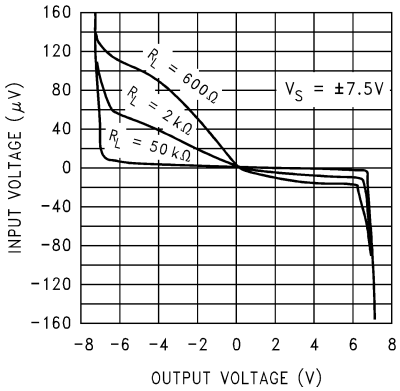


图 5-16. Input Voltage vs Output Voltage

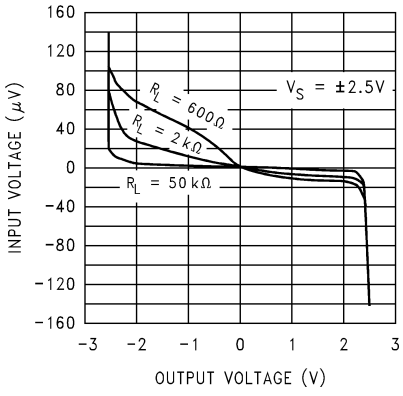


图 5-17. Input Voltage vs Output Voltage

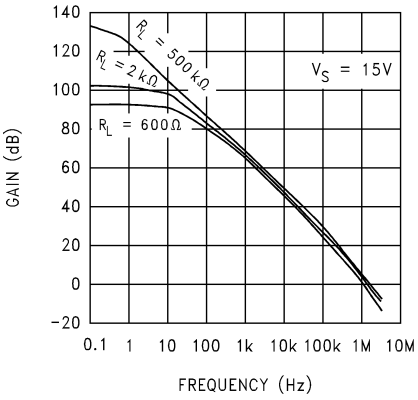


图 5-18. Open Loop Frequency Response

Copyright © 2023 Texas Instruments Incorporated

5.6 Typical Characteristics (continued)

at V_S = +15 V, single supply, and T_A = 25°C (unless otherwise specified)

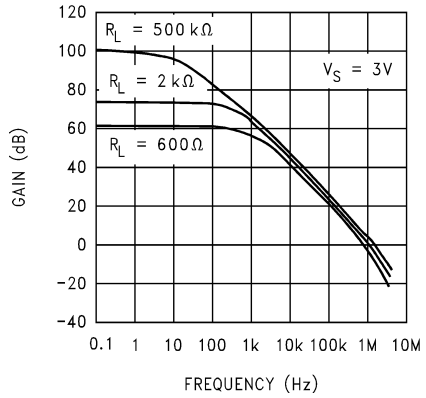


图 5-19. Open Loop Frequency Response

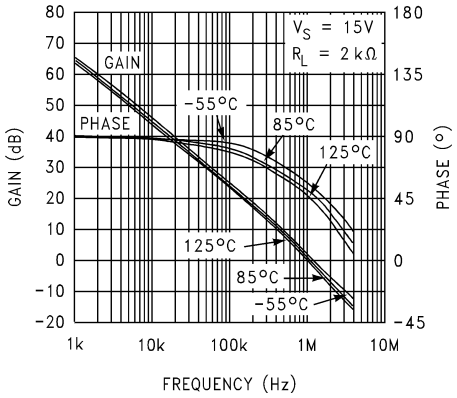


图 5-20. Open Loop Frequency Response vs Temperature

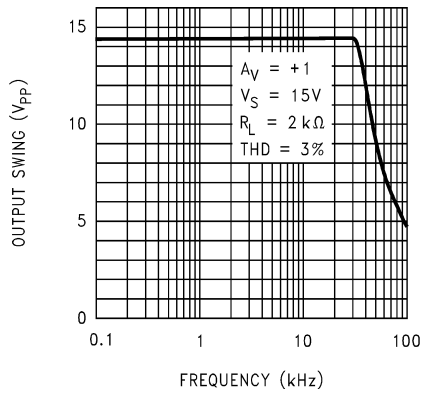


图 5-21. Maximum Output Swing vs Frequency

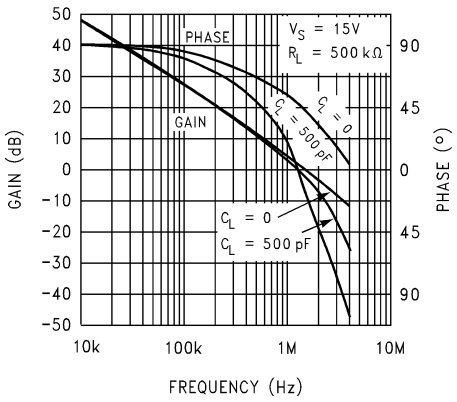


图 5-22. Gain and Phase vs Capacitive Load

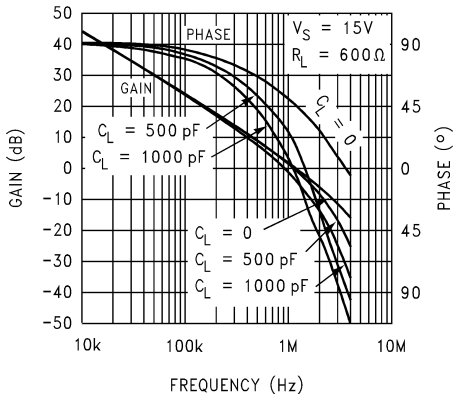


图 5-23. Gain and Phase vs Capacitive Load

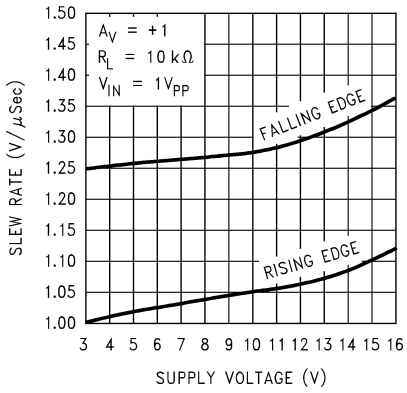


图 5-24. Slew Rate vs Supply Voltage

Copyright © 2023 Texas Instruments Incorporated

5.6 Typical Characteristics (continued)

at V_S = +15 V, single supply, and T_A = 25°C (unless otherwise specified)

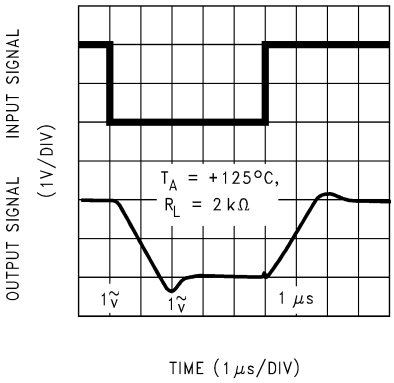


图 5-25. Non-Inverting Large Signal Pulse Response

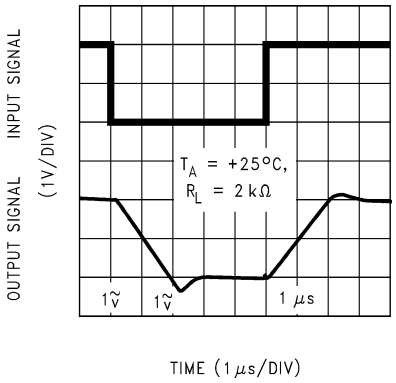


图 5-26. Non-Inverting Large Signal Pulse Response

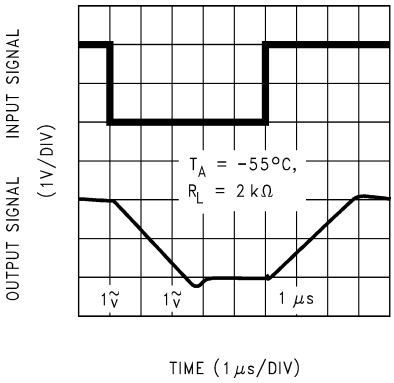


图 5-27. Non-Inverting Large Signal Pulse Response

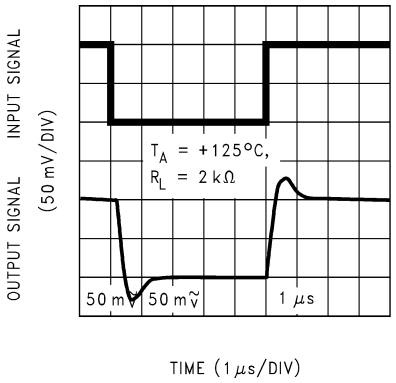


图 5-28. Non-Inverting Small Signal Pulse Response

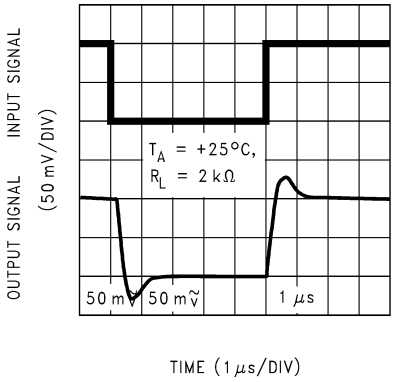


图 5-29. Non-Inverting Small Signal Pulse Response

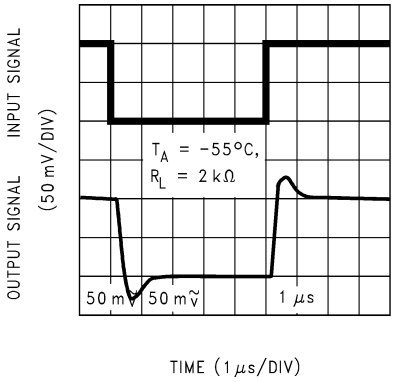


图 5-30. Non-Inverting Small Signal Pulse Response

Copyright © 2023 Texas Instruments Incorporated

5.6 Typical Characteristics (continued)

at V_S = +15 V, single supply, and T_A = 25°C (unless otherwise specified)

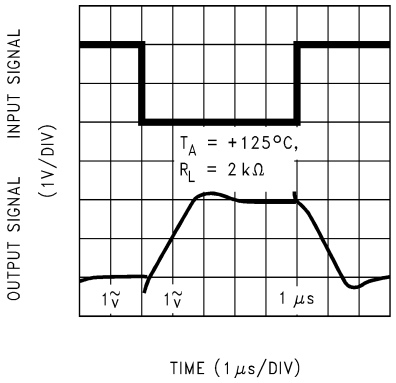


图 5-31. Inverting Large Signal Pulse Response

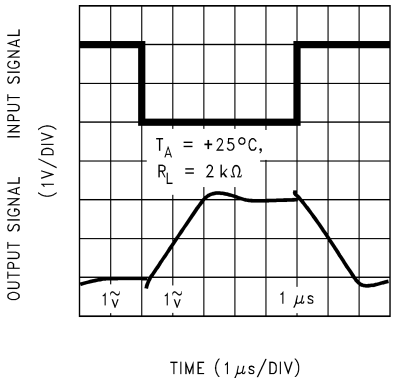


图 5-32. Inverting Large Signal Pulse Response

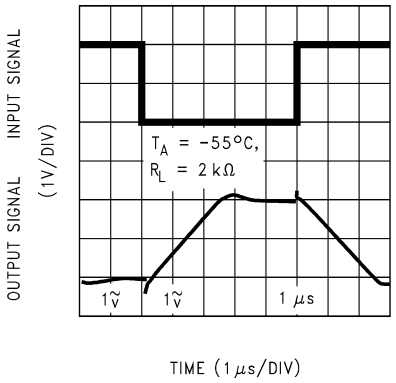


图 5-33. Inverting Large Signal Pulse Response

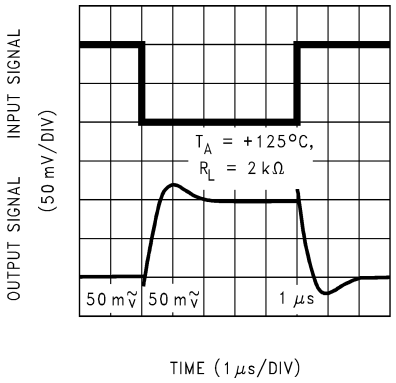


图 5-34. Inverting Small Signal Pulse Response

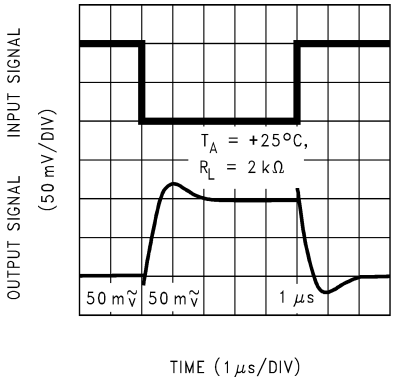


图 5-35. Inverting Small Signal Pulse Response

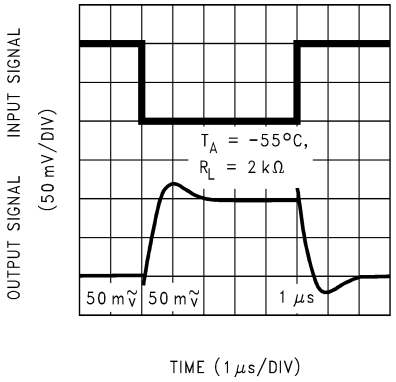


图 5-36. Inverting Small Signal Pulse Response

Copyright © 2023 Texas Instruments Incorporated

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Application Information

6.1.1 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC649x does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. 图 6-1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

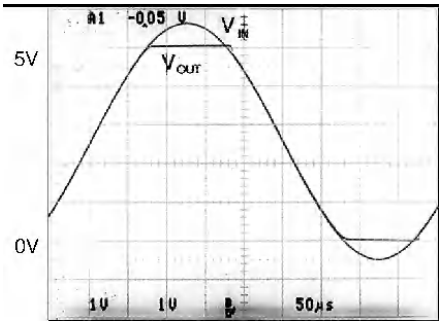


图 6-1. Input Voltage Signal Exceeds the LMC649x Power Supply Voltages With No Output Phase Inversion

The LMC649x is a true rail-to-rail input operational amplifier with an input common-mode range that extends beyond either supply rail. When the input common-mode voltage swings to about 3 V from the positive rail, some dc specifications, namely offset voltage, can be slightly degraded. 图 6-2 illustrates the input offset behavior across the entire common-mode range.

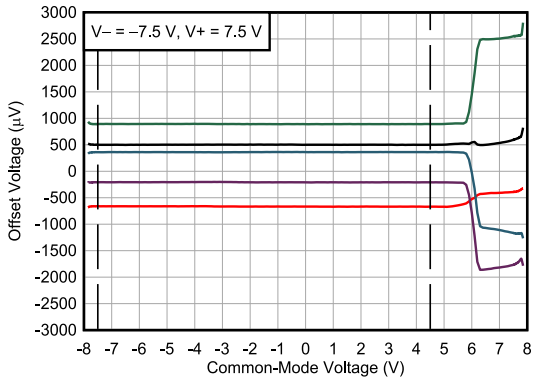


图 6-2. Input Offset Voltage vs Common-Mode Voltage

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in 图 6-3, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

Copyright © 2023 Texas Instruments Incorporated

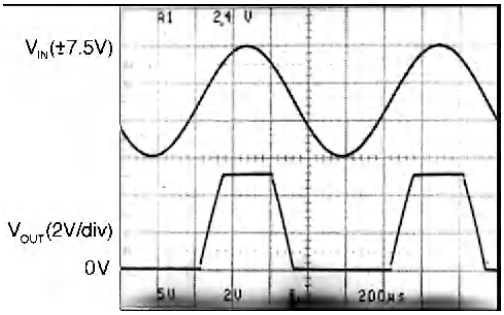


图 6-3. A ±7.5-V Input Signal Greatly Exceeds the 5-V Supply in Figure 6-3, Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in 图 6-4.

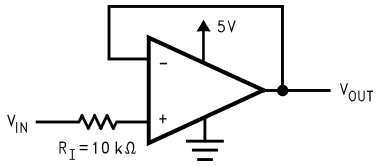


图 6-4. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

6.1.2 Rail-to-Rail Output

The LMC649x output can swing to within a few hundred millivolts of either supply voltage. Using the specified output swing specifications, an approximate output resistance can be calculated for different sourcing and sinking conditions. Using the calculated output resistance, the maximum output voltage swing can be estimated as a function of load.

6.1.3 Compensating for Input Capacitance

Large values of feedback resistance are commonly used for amplifiers with ultra-low input current, such as the LMC649x.

Although the LMC649x is highly stable over a wide range of operating conditions, make sure that certain precautions are met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance (due to transducers, photodiodes, and circuit board parasitics) reduce phase margins.

When high input impedances are demanded, guarding of the LMC649x is suggested. Guarding input lines not only reduces leakage, but also lowers stray input capacitance. See Printed-Circuit-Board Layout for High Impedance Work.

The effect of input capacitance can be compensated by adding a capacitor, C_f, around the feedback resistors (as in 图 6-1) so that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leqslant R_2 C_f \quad (2)$$

Copyright © 2023 Texas Instruments Incorporated

The exact value of C_{IN} is difficult to know; therefore, C_f can be experimentally adjusted so that the desired pulse response is achieved. See the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

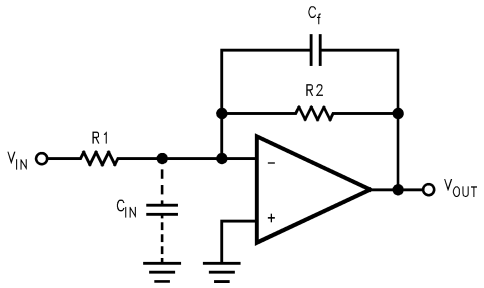


图 6-5. Canceling the Effect of Input Capacitance

6.1.4 Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Curves).

Direct capacitive loading reduces the phase margin of many op amps. A pole in the feedback loop is created by the combination of the op-amp output impedance and the capacitive load. The open-loop output impedance of the LMC649x is shown in 图 6-6. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in 图 6-7.

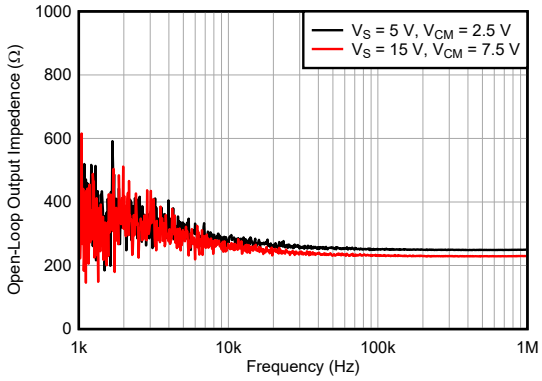


图 6-6. LMC649x Open-Loop Ouput Impedance

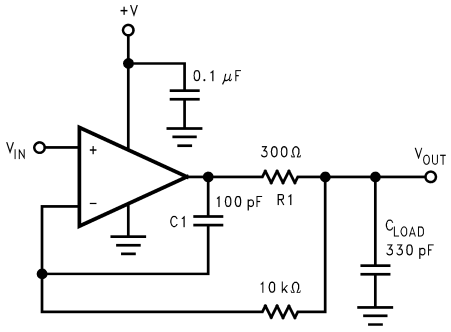
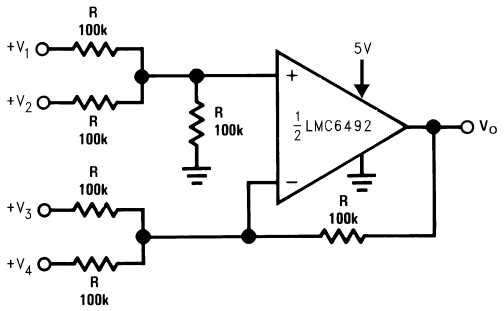


图 6-7. LMC649x Noninverting Amplifier, Compensated to Handle Capacitive Loads

Copyright © 2023 Texas Instruments Incorporated

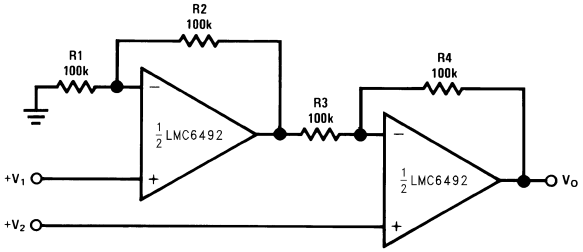
6.2 Typical Application

6.2.1 Application Circuits



Where: $V_0 = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_0 > 0\ V_{DC}$

图 6-8. DC Summing Amplifier ($V_{IN} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$



For

$$\frac{R1}{R2} = \frac{R4}{R3}$$

(CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

As shown: $V_O = 2(V_2 - V_1)$

图 6-9. High Input Z, DC Differential Amplifier

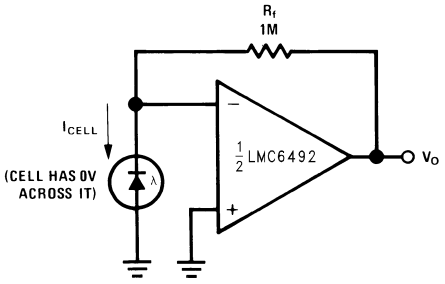
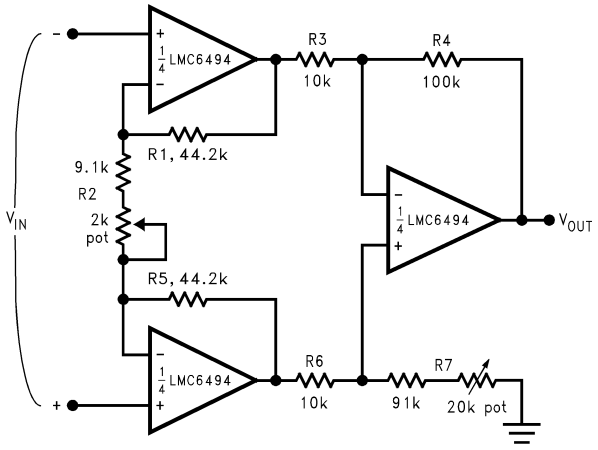


图 6-10. Photo Voltaic-Cell Amplifier

Copyright © 2023 Texas Instruments Incorporated



If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.3k).

图 6-11. Instrumentation Amplifier

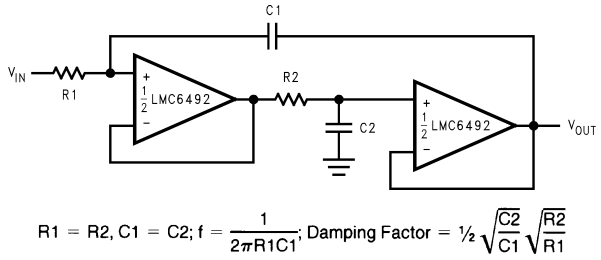


图 6-12. Rail-to-Rail Single Supply Low Pass Filter

This low-pass filter circuit can be used as an antialiasing filter with the same supply as the ADC. Filter designs can also take advantage of the LMC649x ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This configuration in turn allows the use of smaller-valued capacitors that take up less board space and cost less.

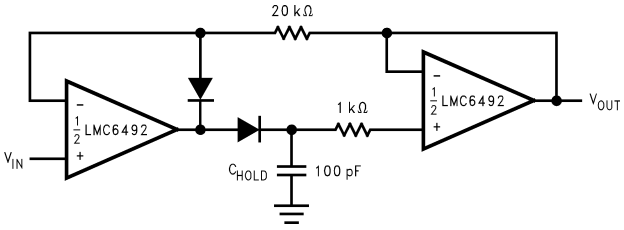
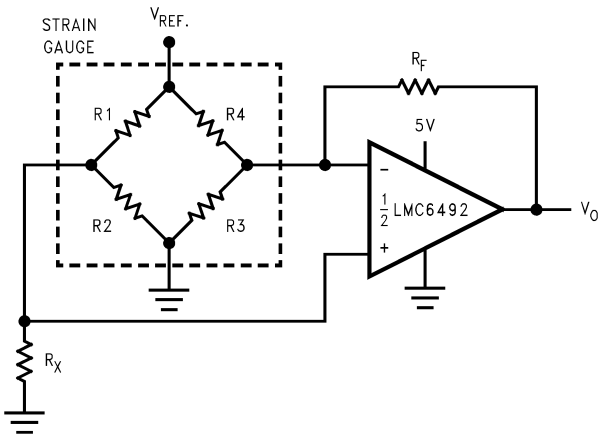


图 6-13. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

Dielectric absorption and leakage is minimized by using a polystyrene or polypropylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. Select low-leakage current diodes to minimize drooping.

Copyright © 2023 Texas Instruments Incorporated



$R_f = Rx$

$R_f >> R1, R2, R3, \text{ and } R4$

$$V_O = \left(\frac{R2}{R1 + R2} - \frac{R3}{R4 + R3}\right)\frac{R_f\,(R3 + R4)}{R3\,R4}V_{REF}$$

图 6-14. Pressure Sensor

In a manifold absolute pressure sensor application, a strain gauge is mounted on the intake manifold in the engine unit. Manifold pressure causes the sensing resistors, R1, R2, R3 and R4 to change. The resistors change in a way such that R2 and R4 increase by the same amount R1 and R3 decrease. This causes a differential voltage between the input of the amplifier. The gain of the amplifier is adjusted by R_f.

6.3 Layout

6.3.1 Layout Guidelines

6.3.1.1 Printed-Circuit-Board Layout For High-Impedance Work

Any circuit that operates with less than 1000 pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC649x, typically 150 fA, an excellent layout is required. Fortunately, the techniques to obtain low leakages are quite simple. First, do not ignore the surface leakage of the PCB. Even though this leakage can sometimes appear acceptably low, under conditions of high humidity or dust or contamination, the surface leakage is appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6492x inputs and the terminals of components connected to the op-amp inputs, as in 图 6-15. To have a significant effect, place guard rings on both the top and bottom of the PCB. This printed circuit foil must then be connected to a voltage that is at the same voltage as the amplifier inputs because no leakage current can flow between two points at the same potential.

For example, a PCB trace-to-pad resistance of 10^{12} Ω, which is normally considered a very large resistance, can leak 5 pA if the trace is a 5-V bus adjacent to the pad of the input. This causes a 33 times degradation from the LMC649x actual performance. If a guard ring is used and held within 5 mV of the inputs, then the same resistance of 10^{11} Ω only causes 0.05 pA of leakage current. 图 6-15 to 图 6-17 show typical connections of guard rings for standard op-amp configurations.

Copyright © 2023 Texas Instruments Incorporated

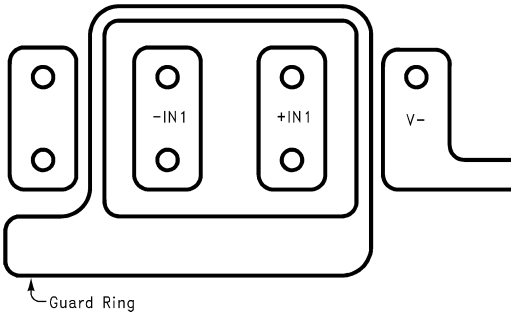


图 6-15. Examples of Guard Ring in PCB Layout

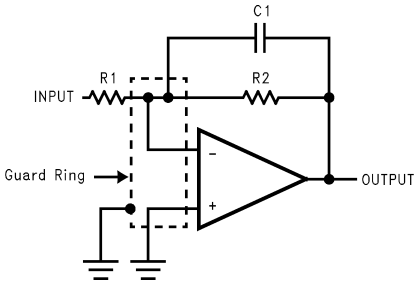


图 6-16. Inverting Amplifier

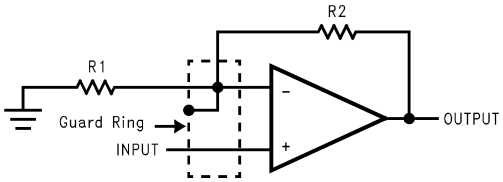


图 6-17. Noninverting Amplifier

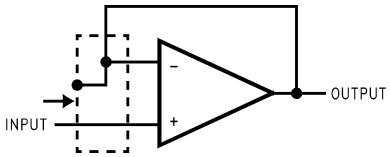
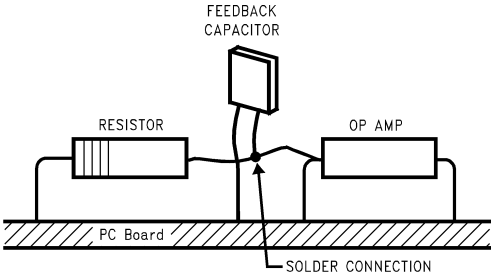


图 6-18. Follower

Be aware that when laying out a PCB for the sake of just a few circuits is inappropriate, the following technique is even better than a guard ring on a PCB. Do not insert the amplifier input pin into the board at all; instead, bend the input pin up in the air and use only air as an insulator because air is an excellent insulator. In this case, some of the advantages of PCB construction are lost, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. 图 6-19 shows an example of air wiring.



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to the PCB).

图 6-19. Air Wiring

Copyright © 2023 Texas Instruments Incorporated

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 器件支持

7.1.1 开发支持

7.1.1.1 Spice Macromodel

A spice macromodel is available for the LMC649x. This model includes accurate simulation of:

- Input common-model voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many other characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

7.1.1.2 PSpice® for TI

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

7.1.1.3 TINA-TI™ 仿真软件（免费下载）

TINA-TI™ 仿真软件是一款简单易用、功能强大且基于 SPICE 引擎的电路仿真程序。TINA-TI 仿真软件是 TINA™ 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 仿真软件提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 仿真软件提供全面的后处理能力，便于用户以多种方式获得结果，用户可从设计工具和仿真网页免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的能力，从而构建一个动态的快速启动工具。

备注

必须安装 TINA 软件或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI™ 软件文件夹中下载免费的 TINA-TI 仿真软件。

7.1.1.4 DIP-Adapter-EVM

借助 DIP-Adapter-EVM 加快运算放大器的原型设计和测试，该 EVM 有助于快速轻松地连接小型表面贴装器件并且价格低廉。使用随附的 Samtec 端子板连接任何受支持的运算放大器，或者将这些端子板直接连接至现有电路。DIP-Adapter-EVM 套件支持以下业界通用封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV（SOT-23-6、SOT-23-5 和 SOT-23-3）、DCK（SC70-6 和 SC70-5）和 DRL (SOT563-6)。

7.1.1.5 DIYAMP-EVM

DIYAMP-EVM 是一款独特的评估模块 (EVM)，可提供真实的放大器电路，使用户能够快速评估设计概念并验证仿真。此 EVM 采用 3 种业界通用封装选项（SC70、SOT23 和 SOIC）并提供 12 种流行的放大器配置，包括放大器、滤波器、稳定性补偿以及同时适用于单电源和双电源的比较器配置。

7.1.1.6 TI 参考设计

TI 参考设计是由 TI 的精密模拟应用专家创建的模拟解决方案。TI 参考设计提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 参考设计可在线获取，网址为 https://www.ti.com/reference-designs。

Copyright © 2023 Texas Instruments Incorporated

7.1.1.7 滤波器设计工具

滤波器设计工具是一款简单、功能强大且便于使用的有源滤波器设计程序。利用滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源器件来打造理想滤波器设计方案。

设计工具和仿真网页以基于网络的工具形式提供滤波设计工具。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

7.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
所有商标均为其各自所有者的财产。

7.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

Copyright © 2023 Texas Instruments Incorporated

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (March 2013) to Revision E (November 2023)	Page
• 更新了 *特性*	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了 *引脚配置和功能*、*规格*、*ESD 等级*、*热性能信息*、*应用和实现*、*应用信息*、*典型应用*、*布局*、*布局指南*、*器件和文档支持*，以及 *机械、封装和可订购信息* 部分	1
• 删除了数据表中的 P (PDIP) 封装	1
• 更改了 *描述* 中的应用电路	1
• Moved ESD tolerance value from *Absolute Maximum Ratings* to *ESD Ratings*	4
• Updated note 1 of *Absolute Maximum Ratings*	4
• Changed *Operating Conditions* to *Recommended Operating Conditions* and deleted redundant table note	4
• Moved thermal information values from *Operating Conditions* to *Thermal Information*	4
• Updated format of *Electrical Characteristics*	5
• Deleted table notes 1, 2, and 3 from *Electrical Characteristics* to be consistent with standard TI data sheets	5
• Added ± to input offset voltage, input offset voltage drift, input bias current, and input offset current in *Electrical Characteristics*	5
• Updated parameter names to be consistent with modern data sheets	5
• Moved the *AC Electrical Characteristics* and *DC Electrical Characteristics* to *Electrical Characteristics*	5
• Changed supply current specification from total to per amplifier in *Electrical Characteristics*	5
• Deleted Figures 13 to 15, Figures 21 to 25, Figures 34 to 35, and Figures 51 to 54	8
• Added Input Offset Voltage vs Common-Mode Voltage plot in *Amplifier Topology* and related description	14
• Updated description of *Rail-to-Rail Output*	15

Changes from Revision C (March 2013) to Revision D (March 2013)	Page
• Changed layout of National Data Sheet to TI format	21

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6492AEM	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 125	LMC64 92AEM	
LMC6492AEM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMC64 92AEM	
LMC6492AEMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMC64 92AEM	Samples
LMC6492BEM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMC64 92BEM	
LMC6492BEMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMC64 92BEM	Samples
LMC6494AEMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMC6494 AEM	Samples
LMC6494BEMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMC6494 BEM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

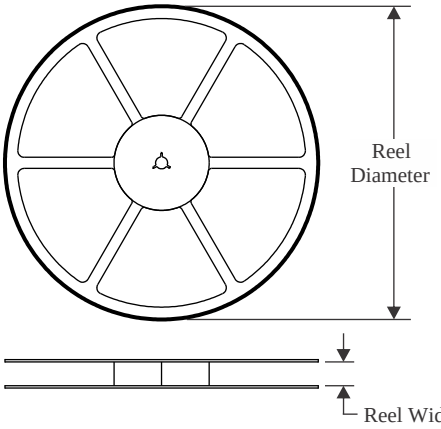
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

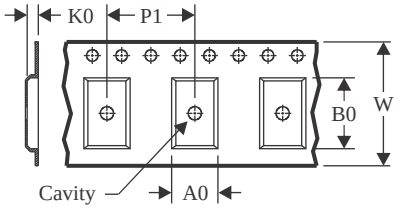
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

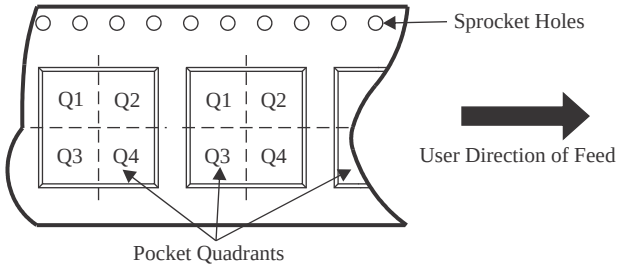


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

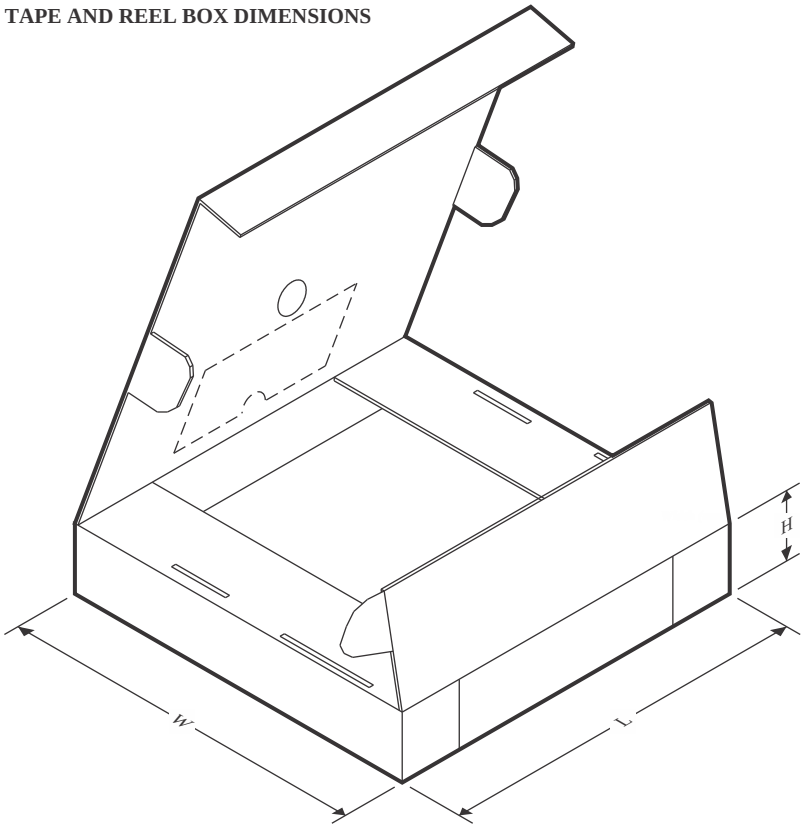
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6492AEMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6492BEMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6494AEMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6494BEMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

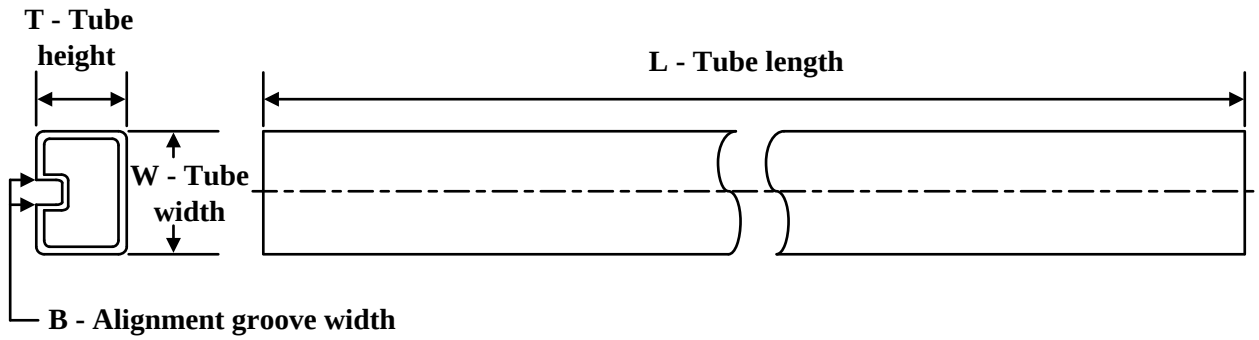
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6492AEMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6492BEMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6494AEMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMC6494BEMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

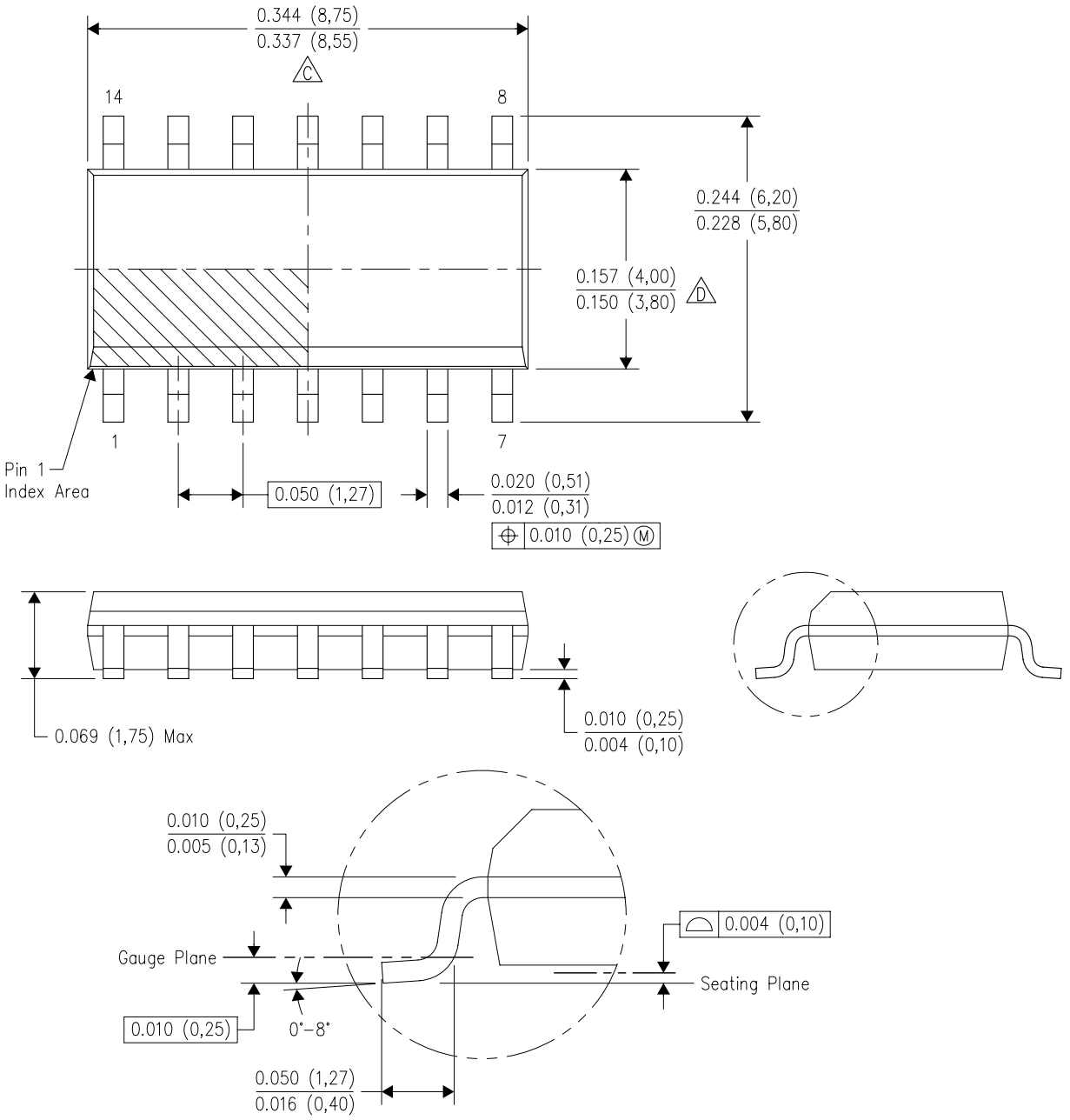
TUBE



*All dimensions are nominal

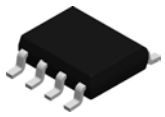
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6492AEM	D	SOIC	8	95	495	8	4064	3.05
LMC6492AEM	D	SOIC	8	95	495	8	4064	3.05
LMC6492AEM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6492BEM/NOPB	D	SOIC	8	95	495	8	4064	3.05

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

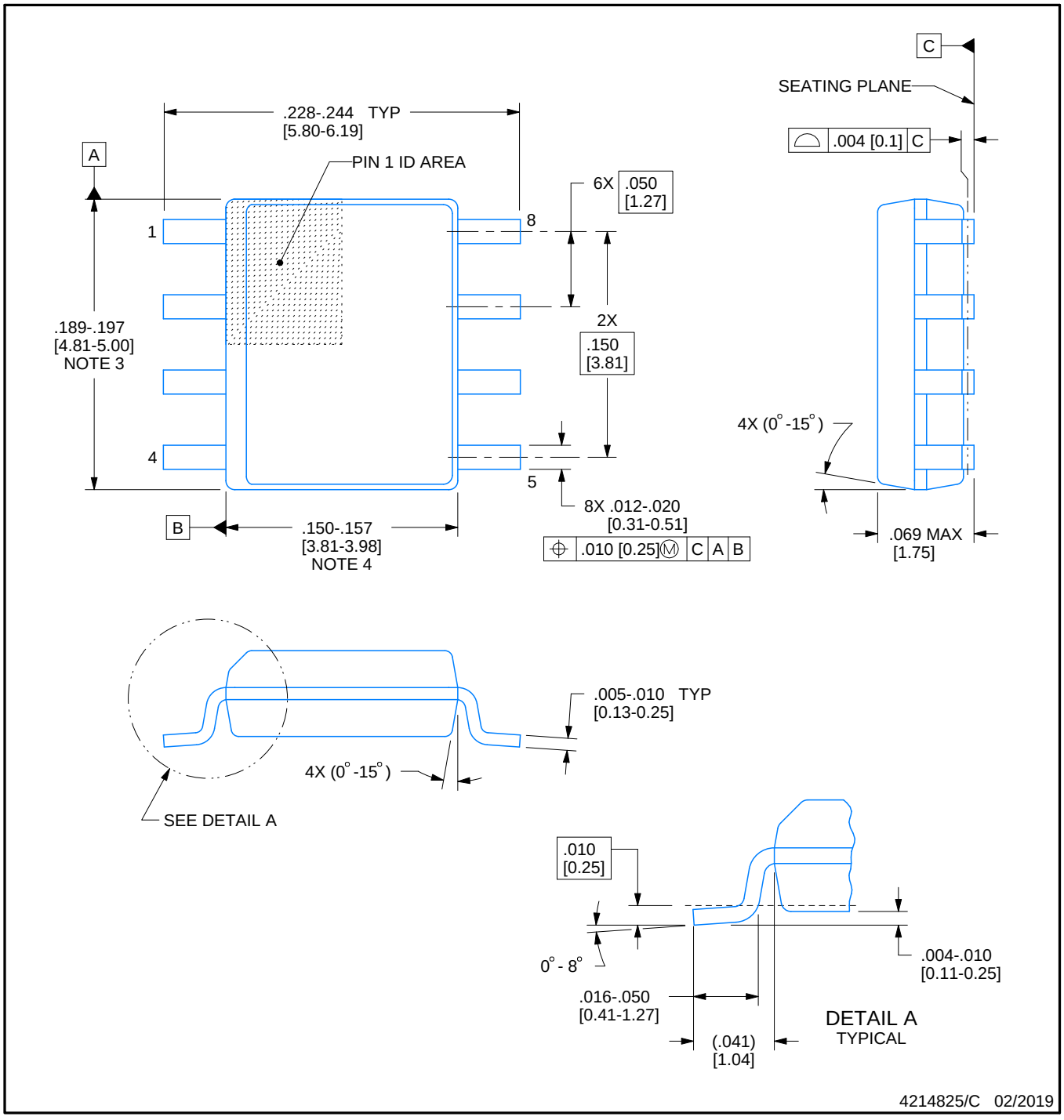


PACKAGE OUTLINE

D0008A

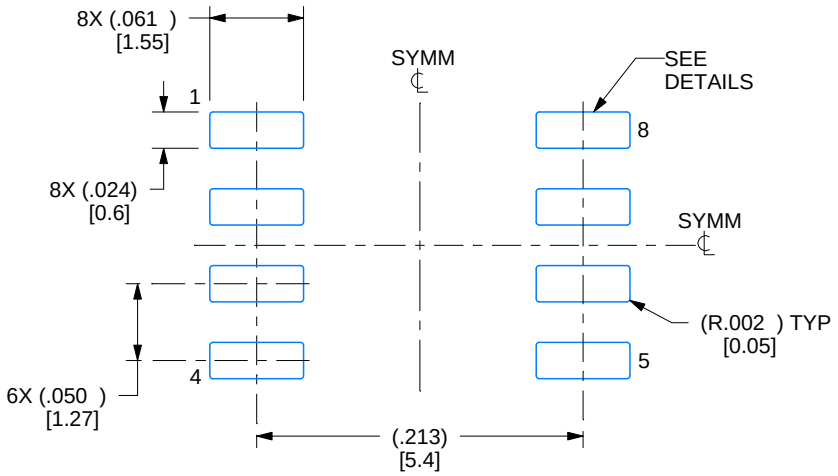
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

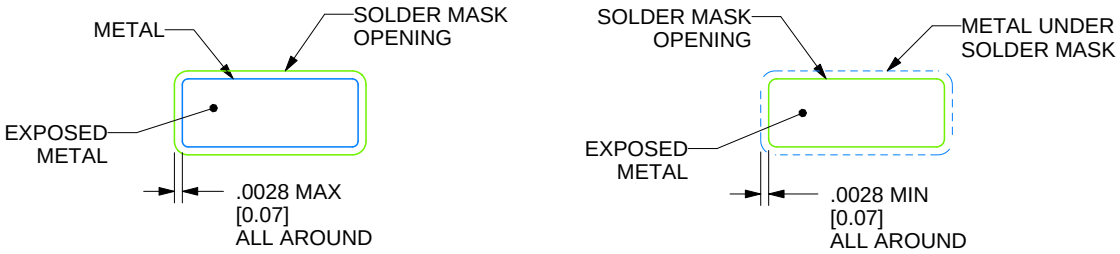


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

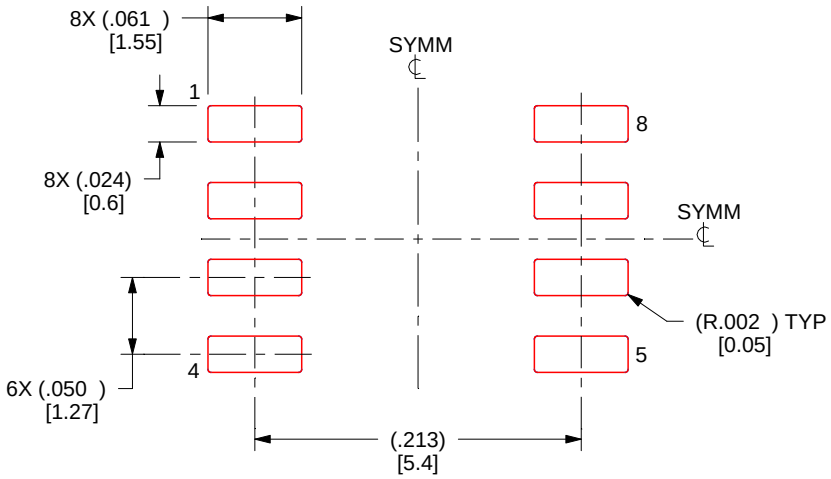
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司