

## LM654B0-Q1 引脚兼容 20A (25A 峰值) ZEN 1 可堆叠 汽车级 降压

### 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C 至 +125°C，T<sub>A</sub>
- 内置时钟同步功能，支持转换器堆叠
- 内部或外部补偿
- 引脚可选输出电压：3.3V 和 5V 固定输出，或 0.8V 至  $0.9 \times V_{IN}$  可调输出
- 宽输入电压范围：3V 至 36V
- ZEN 1 开关技术
  - 针对低 EMI 要求进行了优化
  - 有助于符合 CISPR 25 5 级 CISPR 11 B 级标准
  - 具有对称引脚排列的增强型 HotRod™ QFN 封装
- 开关频率范围为 300kHz 至 2.2MHz
  - 引脚可配置自动或 FPWM 运行
  - 可与外部时钟同步
- 短最小导通时间：40ns (最大值)
  - 在 2.2MHz 下实现 36V 至 3.3V 的转换
- 高效率和高功率密度

### 2 应用

- 高级驾驶辅助系统 (ADAS)
- 汽车信息娱乐系统与仪表组
- 混合动力、电动和动力总成系统
- 医疗成像系统
- 测试和测量系统
- 无线基础设施系统

### 3 说明

LM654B0-Q1 是降压转换器，专为汽车应用而设计，采用 ZEN 开关技术，可实现高效率、高功率密度和低 EMI 性能。这些转换器可在 3V 至 36V 的宽输入电压范围内工作，提供可通过引脚选择的 3.3V、5V 固定输出电压或可调输出配置。

通过最大限度减小环路电感、优化 SW 节点压摆率和双随机展频 (DRSS)，实现低 EMI 运行。DRSS 可通过三角调制与假随机调制的组合显著降低峰值发射，同时保持超低的输出电压纹波。

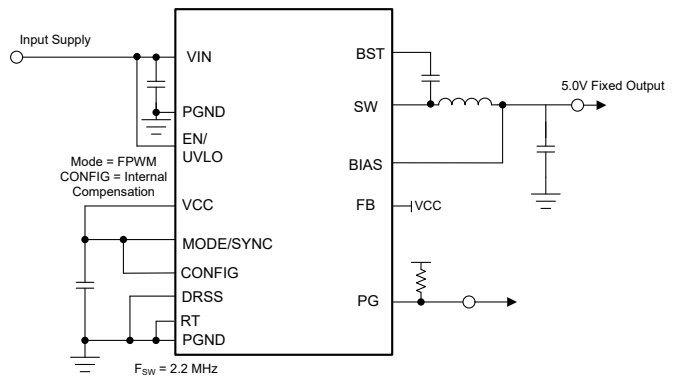
电流模式控制架构，搭配 32ns 典型最短导通时间，可在高频下实现高转换比，提供快速瞬态响应以及出色的负载和线路调整。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
LM654B0-Q1	VDA (WQFN-FCRLF, 26)	4.5mm × 4.5mm

(1) 有关更多信息，请参阅节 7。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



简化版原理图



## 内容

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#### 4 器件比较表

器件	可订购器件型号	工程器件型号	额定输出电 流	顶部外露散热焊 盘	底部外露散 热焊盘	封装	结温范围
LM654B0-Q1	LM654B0VDARQ1	PLM654B0VDARQ1	20	是	是	VDA (26)	-40°C 至 150°C

## 5 器件和文档支持

### 5.1 器件支持

#### 5.1.1 第三方产品免责声明

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### 5.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 5.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 5.4 商标

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### 5.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 5.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

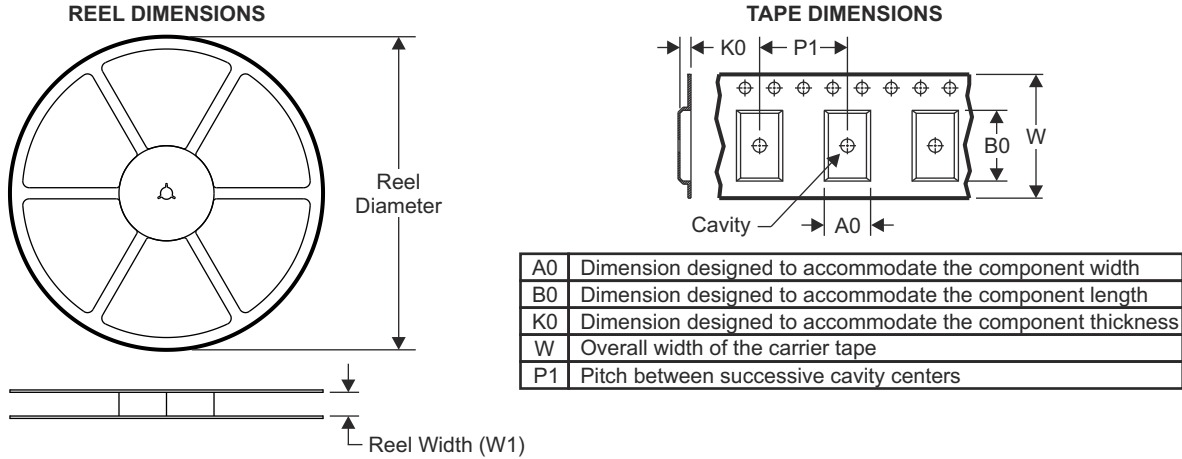
## 6 修订历史记录

日期	修订版本	注释
November 2025	*	初始发行版

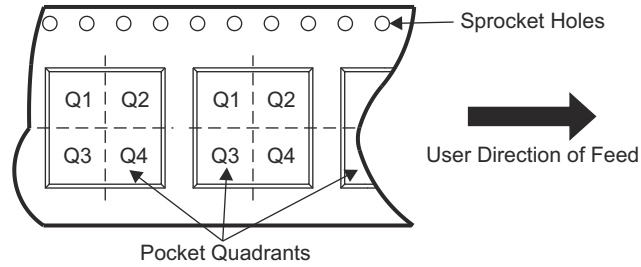
## 7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

### 7.1 卷带包装信息

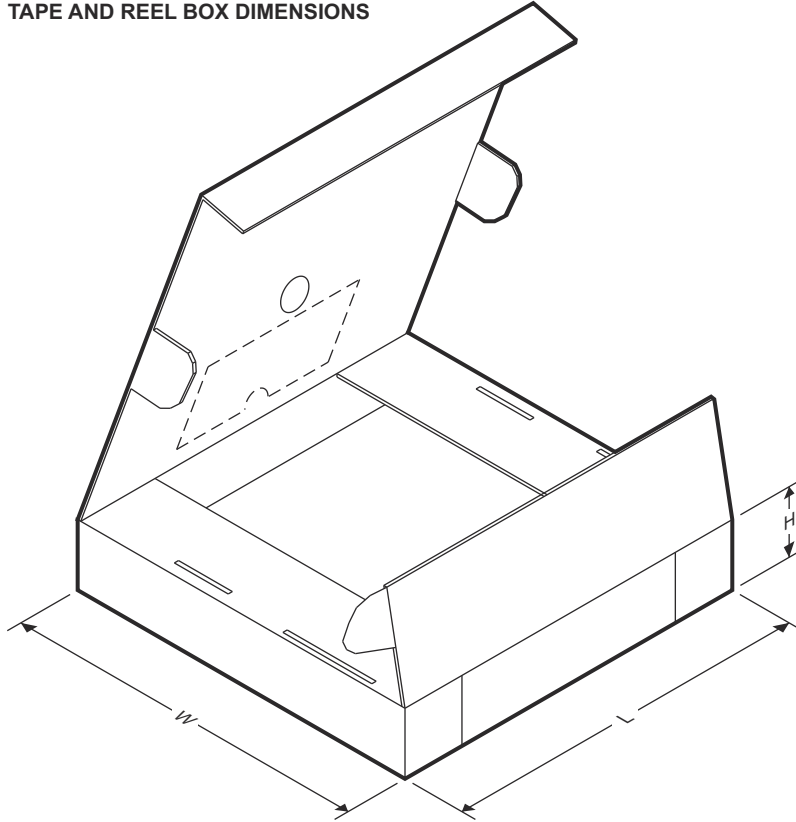


#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



器件	封装类型	封装图	引脚	SPQ	卷带直径 (mm)	卷带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限
PLM654B0VDARQ1	WQFN-FCRLF	VDA	26	3000	330	12.4	4.8	4.8	1.4	8.0	12	Q2

## TAPE AND REEL BOX DIMENSIONS



器件	封装类型	封装图	引脚	SPQ	长度 (mm)	宽度 (mm)	高度 (mm)
PLM654B0VDARQ1	WQFN-FCRLF	VDA0026A	26	3000	346	346	33

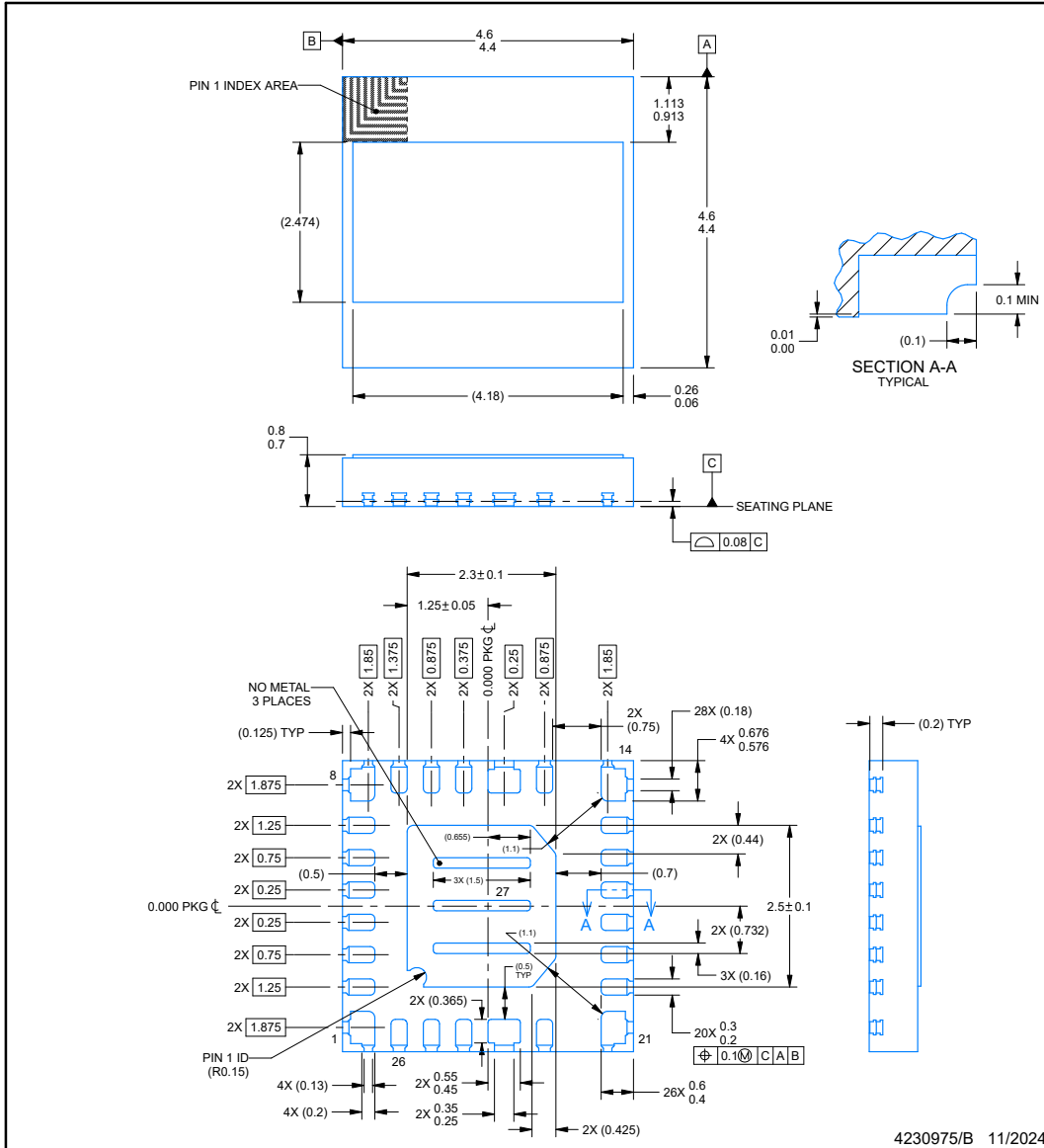


PACKAGE OUTLINE

VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

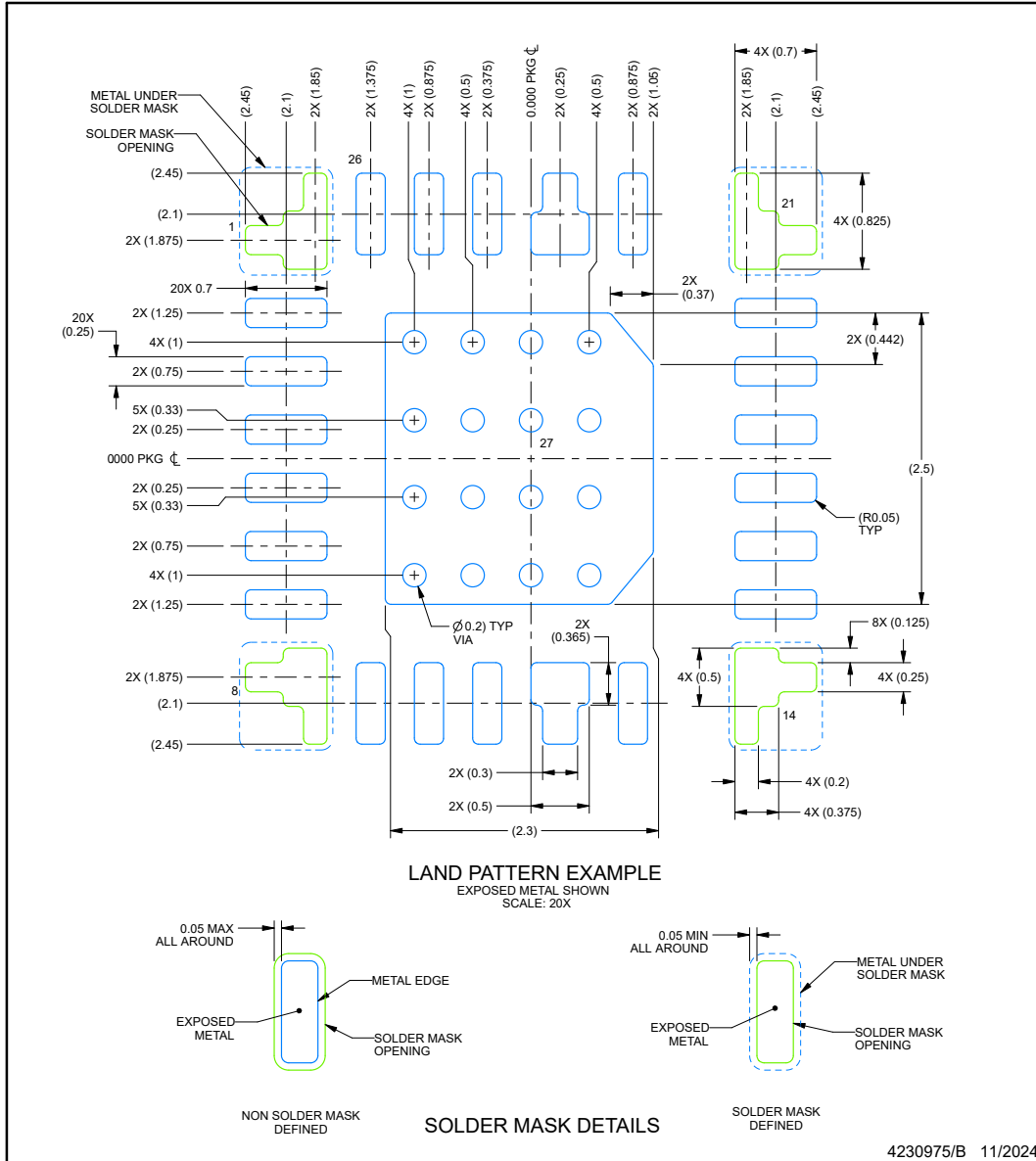
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT**

**VDA0026A**

**WQFN-FCRLF - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

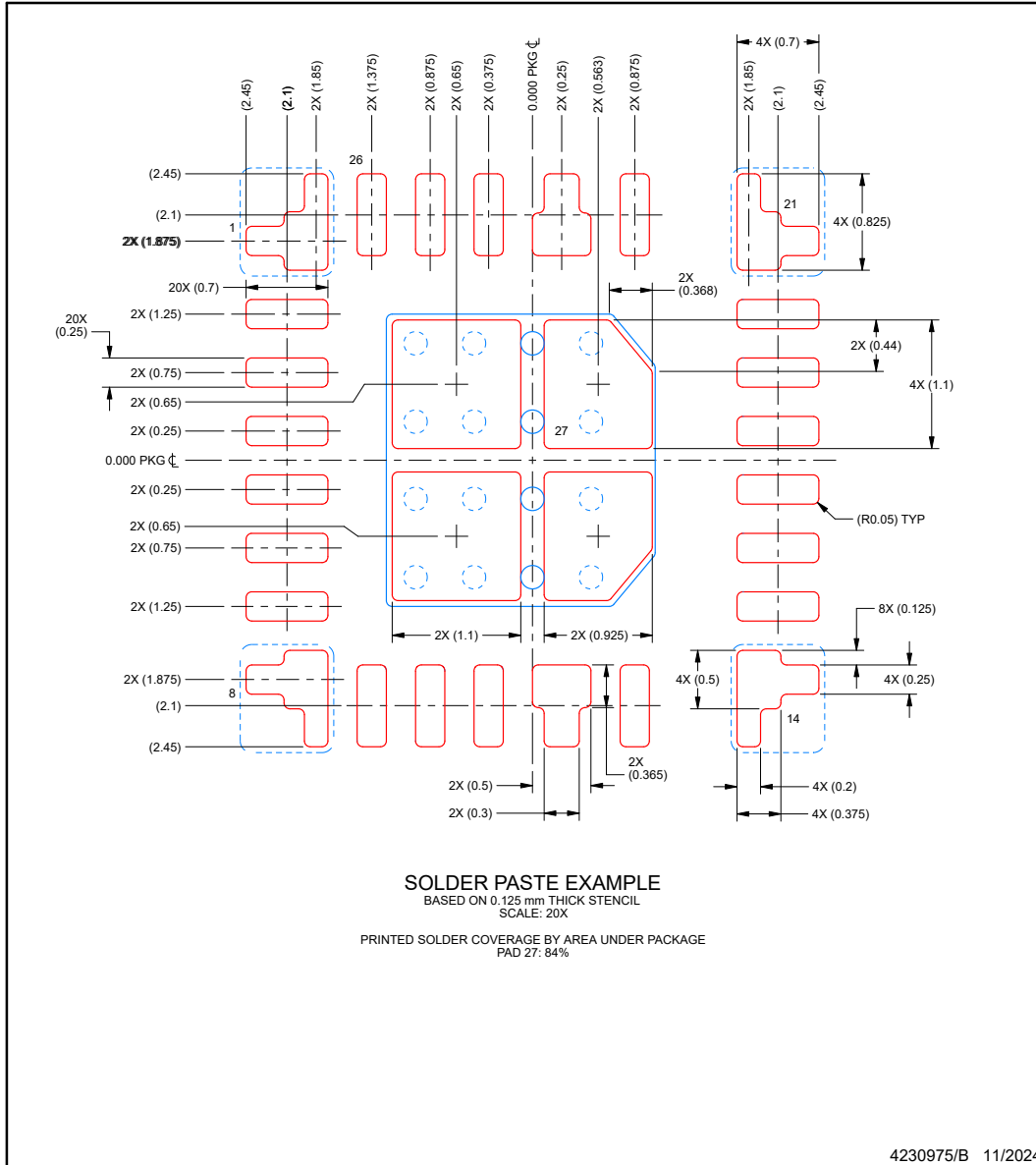
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLM654B0VDARQ1	Active	Preproduction	WQFN-FCRLF (VDA)   26	3000   LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

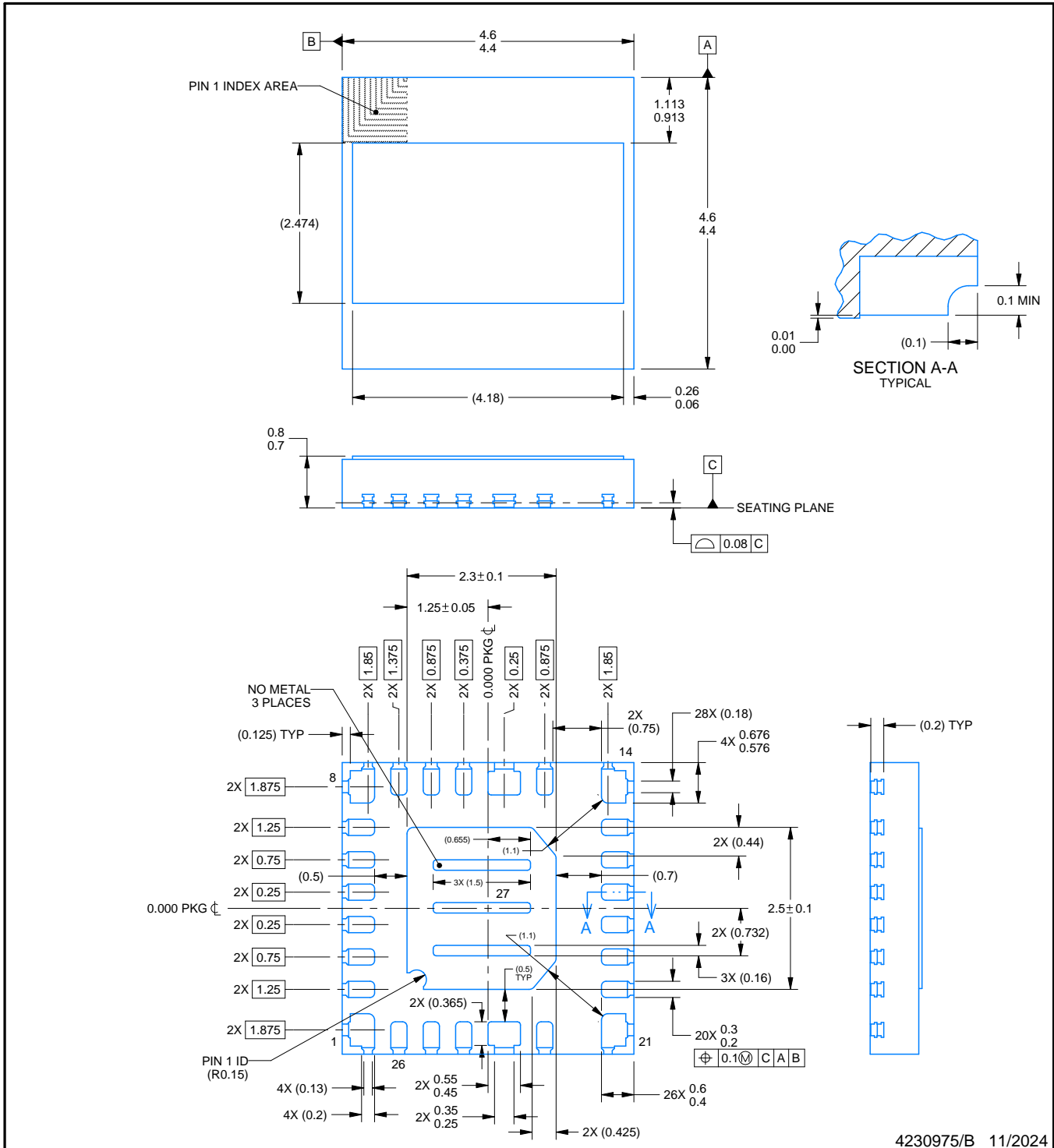
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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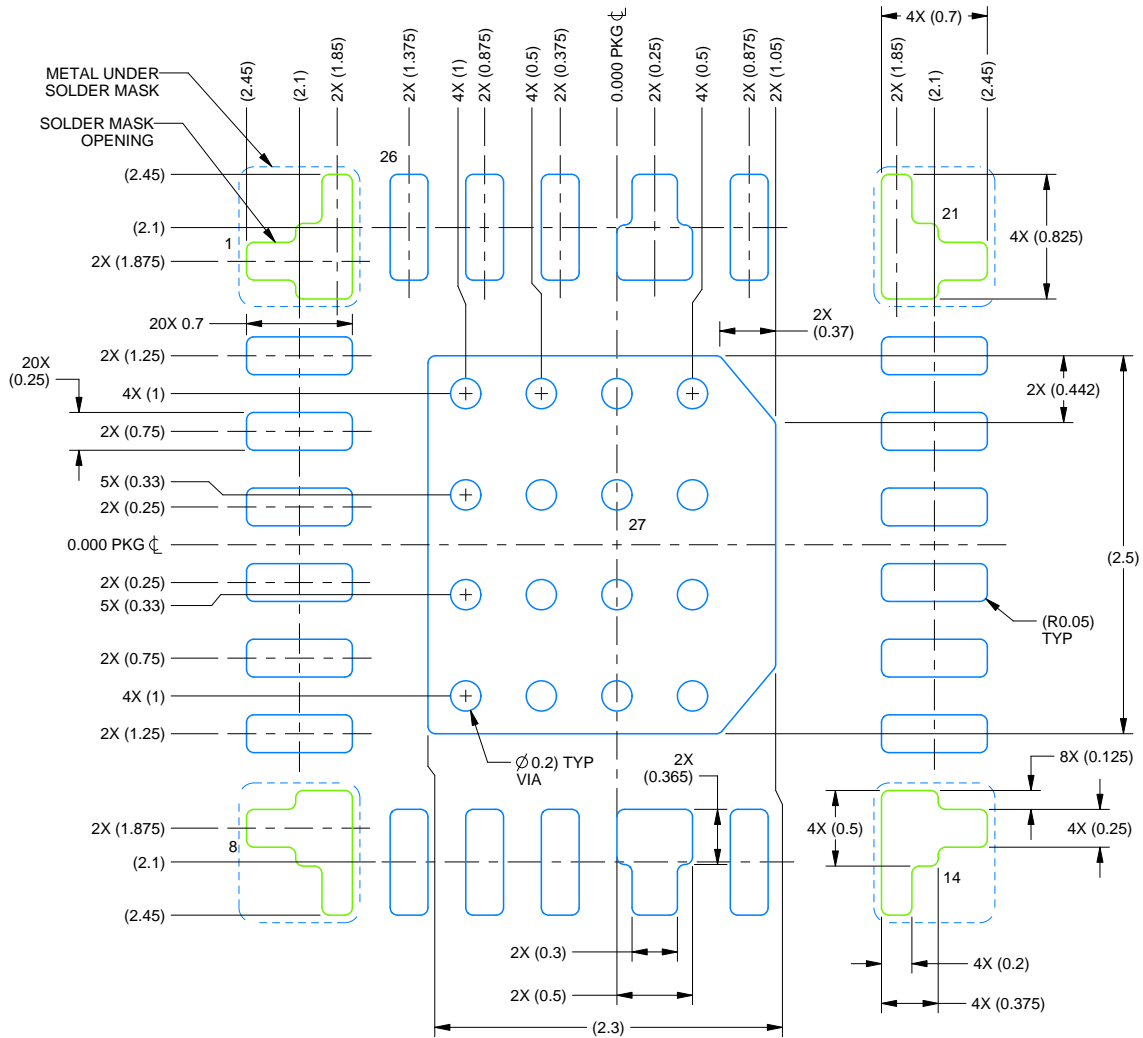
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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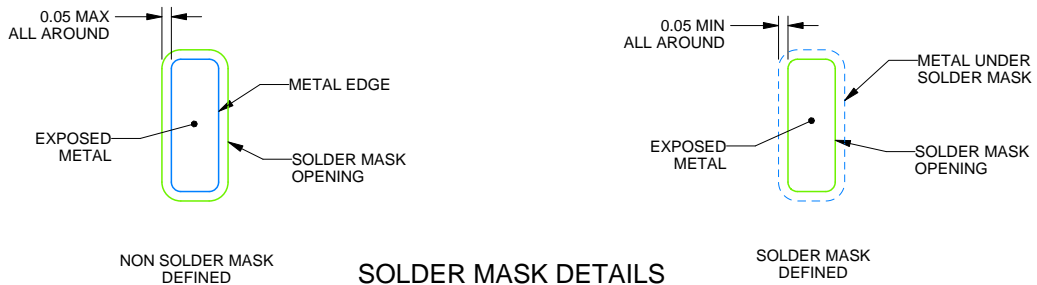
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

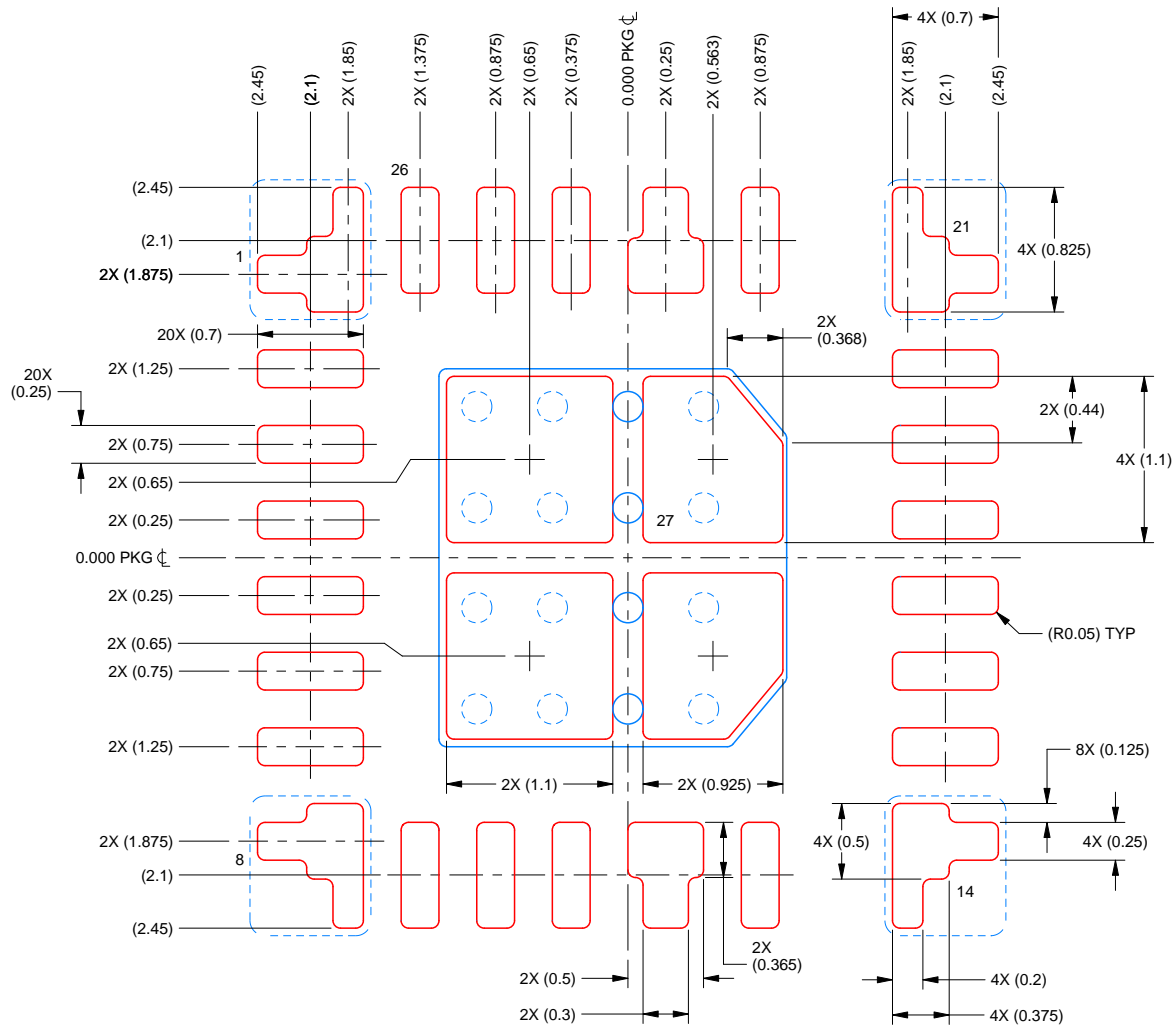
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VDA0026A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL  
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PAD 27: 84%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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