LM4752 Stereo 11W Audio Power Amplifier

Check for Samples: LM4752

FEATURES

- **Drives 4Ω and 8Ω Loads**
- **Internal Gain Resistors (A_V = 34 dB)**
- **Minimum External Component Requirement**
- **Single Supply Operation**
- **Internal Current Limiting**
- **Internal Thermal Protection**
- **Compact 7-lead TO-220 Package**
- **Low Cost-Per-Watt**
- **Wide Supply Range 9V - 40V**

APPLICATIONS

- **Compact Stereos**
- **Stereo TVs**
- **Mini Component Stereos**
- **Multimedia Speakers**

KEY SPECIFICATIONS

- **Output Power at 10% THD+N with 1kHz into 4Ω V_{CC} = 24V 11 W (typ)**
- **Output Power at 10% THD+N with 1kHz into 8Ω V_{CC} = 24V 7 W (typ)**
- **Closed Loop Gain 34 dB (typ)**
- **P_O at 10% THD+N @ 1 kHz into 4Ω Single-Ended DDPAK Package V_{CC} = 12V 2.5 W (typ)**
- **P_O at 10% THD+N @ 1kHz into 8Ω Bridged DDPAK Package V_{CC} = 12V 5 W (typ)**

DESCRIPTION

The LM4752 is a stereo audio amplifier capable of delivering 11W per channel of continuous average output power to a 4Ω load, or 7W per channel into 8Ω using a single 24V supply at 10% THD+N.

The LM4752 is specifically designed for single supply operation and a low external component count. The gain and bias resistors are integrated on chip, resulting in a 11W stereo amplifier in a compact 7 pin TO-220 package. High output power levels at both 20V and 24V supplies and low external component count offer high value for compact stereo and TV applications. A simple mute function can be implemented with the addition of a few external components.

TYPICAL APPLICATION

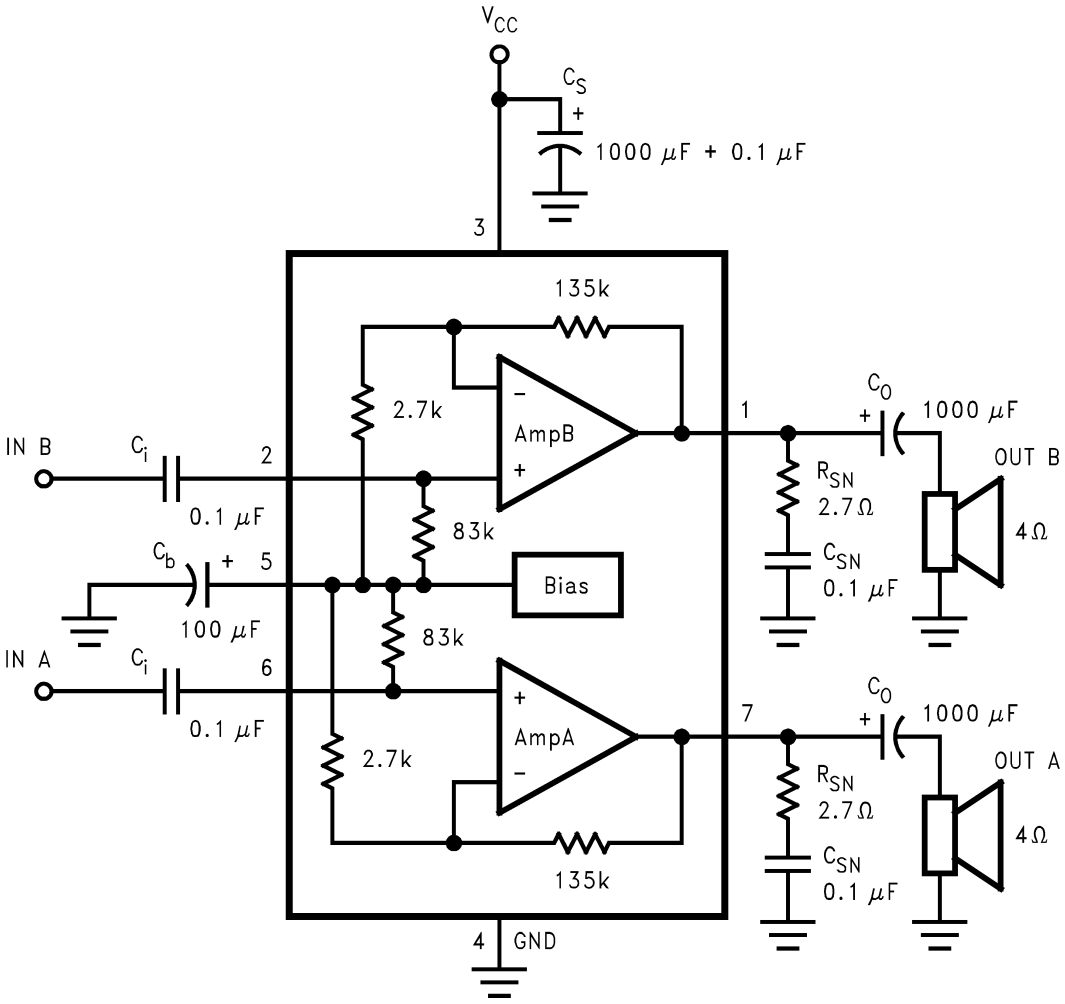
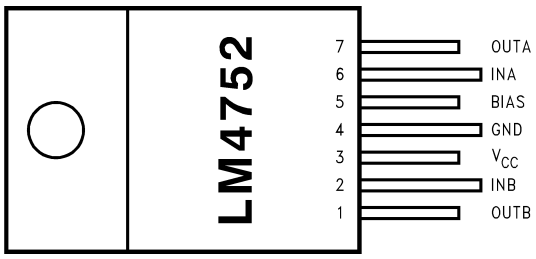
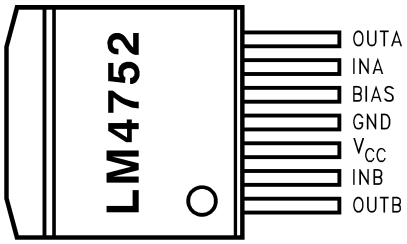


Figure 1. Typical Audio Amplifier Application Circuit

CONNECTION DIAGRAMS



Plastic Package (Top View)
See Package Number NDZ



7 Pin DDPAK Package (Top View)
See Package Number KTW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage		40V
Input Voltage		±0.7V
Input Voltage at Output Pins(4)		GND – 0.4V
Output Current		Internally Limited
Power Dissipation(5)		62.5W
ESD Susceptibility(6)		2 kV
Junction Temperature		150°C
Soldering Information	NDZ Package (10 sec)	250°C
Storage Temperature		−40°C to 150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) All voltages are measured with respect to the GND pin (4), unless otherwise specified.
(4) The outputs of the LM4752 cannot be driven externally in any mode with a voltage lower than -0.4V below GND or permanent damage to the LM4752 will result.
(5) For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of θ_{JC} = 2°C/W (junction to case). Refer to the section DETERMINING MAXIMUM POWER DISSIPATION for more information.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

OPERATING RATINGS

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	9V to 32V
θ_{JC}	2°C/W
θ_{JA}	79°C/W

ELECTRICAL CHARACTERISTICS

The following specifications apply to each channel with V_{CC} = 24V, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4752		Units (Limits)
			Typical(1)	Limit(2)	
I_{total}	Total Quiescent Power Supply Current	V_{INAC} = 0V, V_o = 0V, R_L = ∞	10.5	20	mA(max)
				7	mA(min)
P_o	Output Power (Continuous	f = 1 kHz, THD+N = 10%, R_L = 8Ω	7		W
	Average per Channel)	f = 1 kHz, THD+N = 10%, R_L = 4Ω		10	W(min)
		V_{CC} = 20V, R_L = 8Ω	4		W
		V_{CC} = 20V, R_L = 4Ω	7		W
		f = 1 kHz, THD+N = 10%, R_L = 4Ω V_S = 12V, DDPAK Pkg.	2.5		W
THD+N	Total Harmonic Distortion plus Noise	f = 1 kHz, P_o = 1 W/ch, R_L = 8Ω	0.08		%
V_{OSW}	Output Swing	R_L = 8Ω, V_{CC} = 20V	15		V
		R_L = 4Ω, V_{CC} = 20V	14		V
X_{talk}	Channel Separation	See Figure 1	55		dB
		f = 1 kHz, V_o = 4 Vrms, R_L = 8Ω			
PSRR	Power Supply Rejection Ratio	See Figure 1	50		dB
		V_{CC} = 22V to 26V, R_L = 8Ω			
V_{ODV}	Differential DC Output Offset Voltage	V_{INAC} = 0V	0.09	0.4	V(max)
SR	Slew Rate		2		V/µs
R_{IN}	Input Impedance		83		kΩ
PBW	Power Bandwidth	3 dB BW at P_o = 2.5W, R_L = 8Ω	65		kHz
A_{VCL}	Closed Loop Gain (Internally Set)	R_L = 8Ω	34	33	dB(min)
				35	dB(max)
e_{in}	Noise	IHF-A Weighting Filter, R_L = 8Ω	0.2		mVrms
		Output Referred			
I_o	Output Short Circuit Current Limit	V_{IN} = 0.5V, R_L = 2Ω		2	A(min)

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits ensure that all parts tested in production meet the stated values.

TEST CIRCUIT

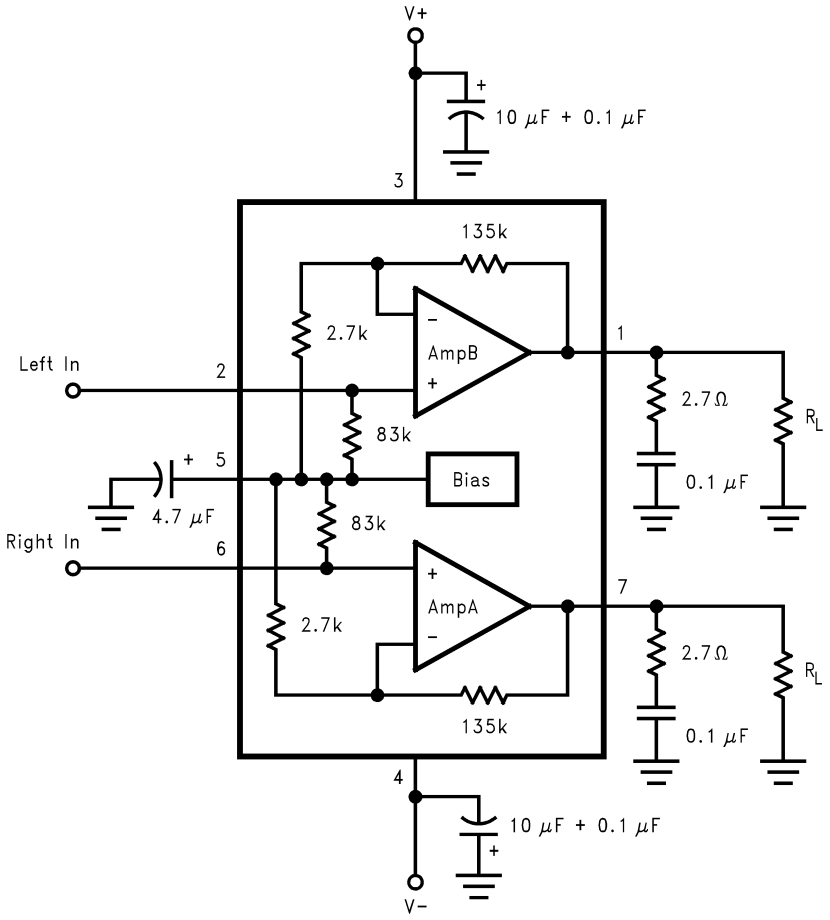


Figure 2. Test Circuit

TYPICAL APPLICATION WITH MUTE

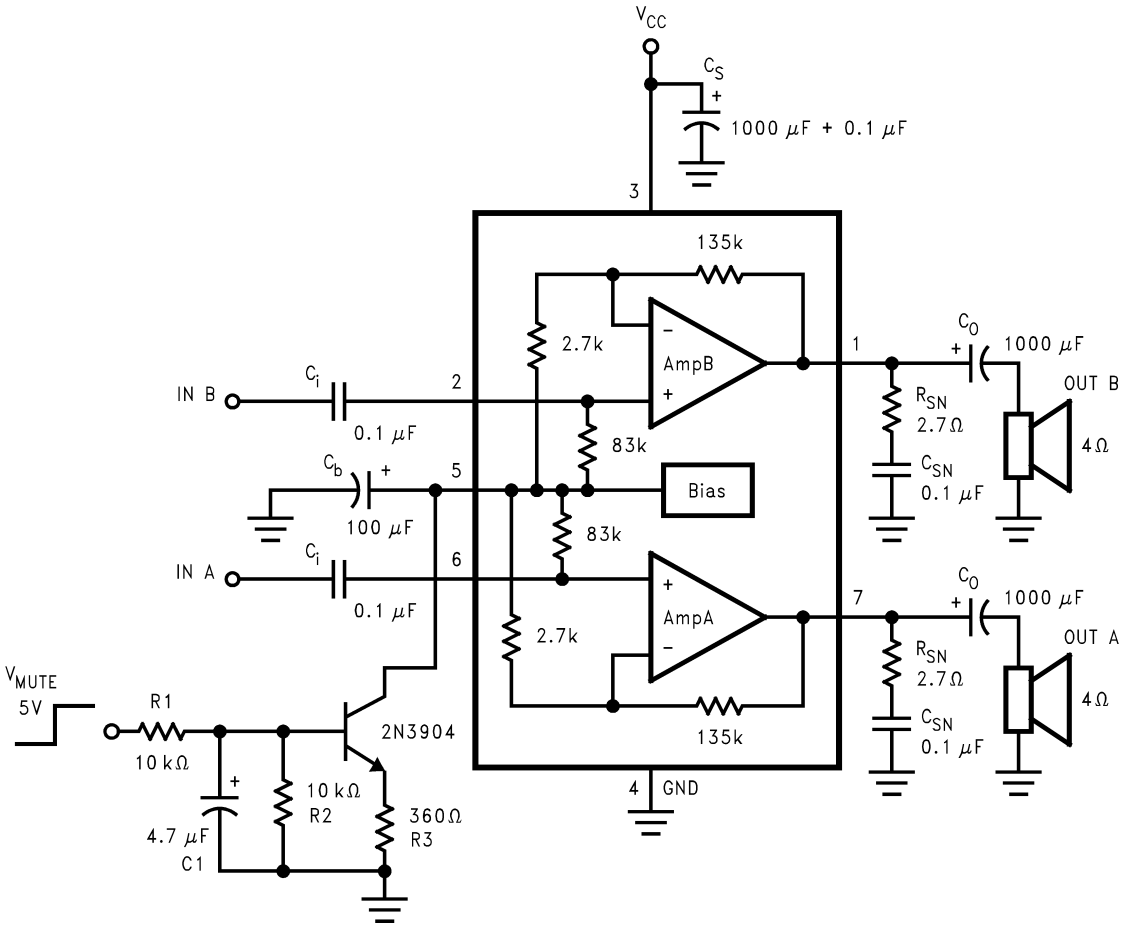


Figure 3. Application with Mute Function

EQUIVALENT SCHEMATIC DIAGRAM

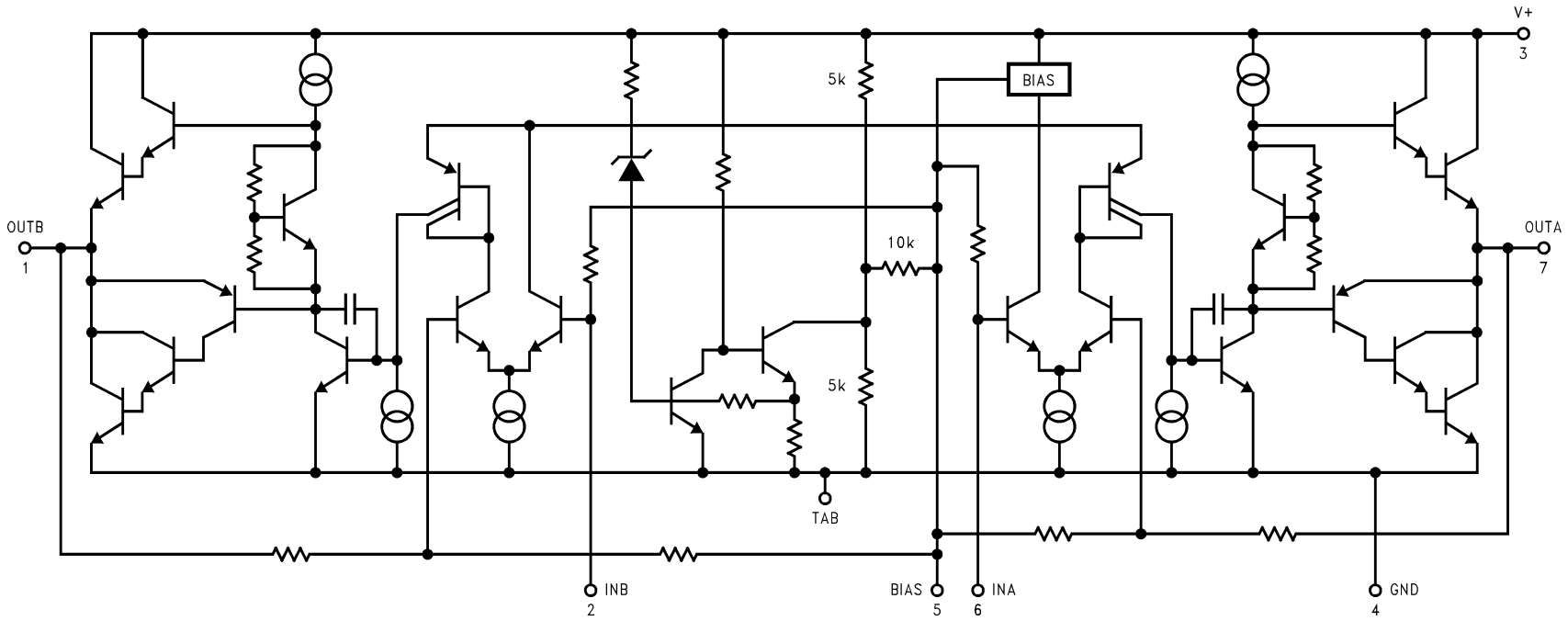


Figure 4.

SYSTEM APPLICATION CIRCUIT

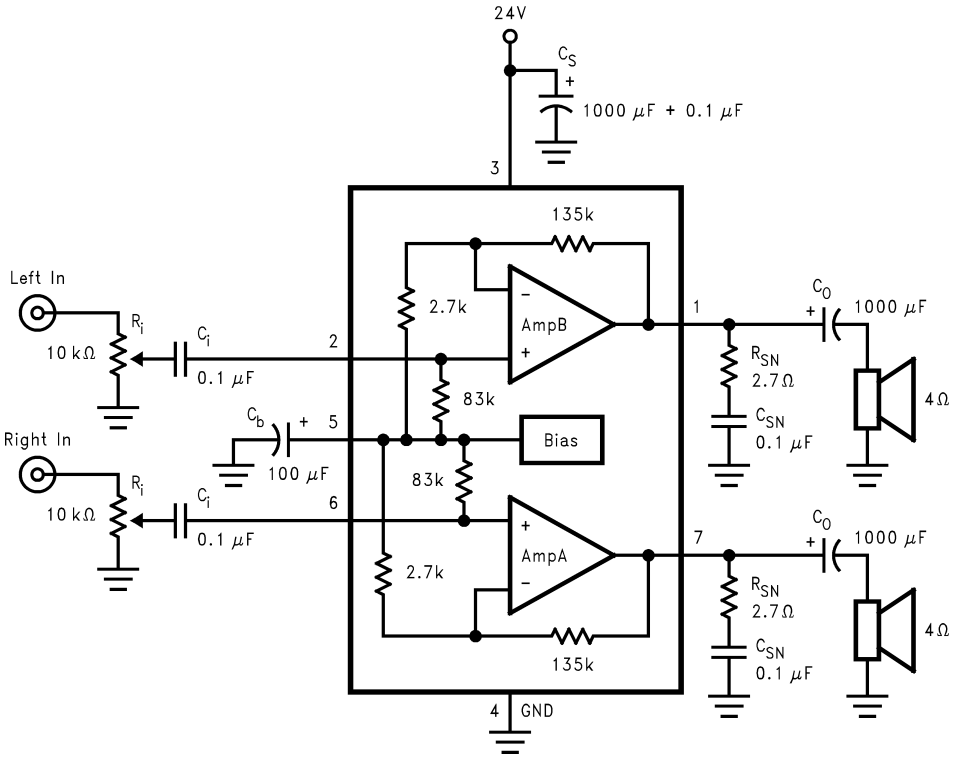


Figure 5. Circuit for External Components Description

EXTERNAL COMPONENTS DESCRIPTION

Components		Function Description
1, 2	Cs	Provides power supply filtering and bypassing.
3, 4	Rsn	Works with Csn to stabilize the output stage from high frequency oscillations.
5, 6	Csn	Works with Rsn to stabilize the output stage from high frequency oscillations.
7	Cb	Provides filtering for the internally generated half-supply bias generator.
8, 9	Ci	Input AC coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a high pass filter with fc =1/(2 • π • Rin • Cin).
10, 11	Co	Output AC coupling capacitor which blocks DC voltage at the amplifier's output terminal. Creunderates a high pass filter with fc =1/(2 • π • Rout • Cout).
12, 13	Ri	Voltage control - limits the voltage level to the amplifier's input terminals.

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Output Power

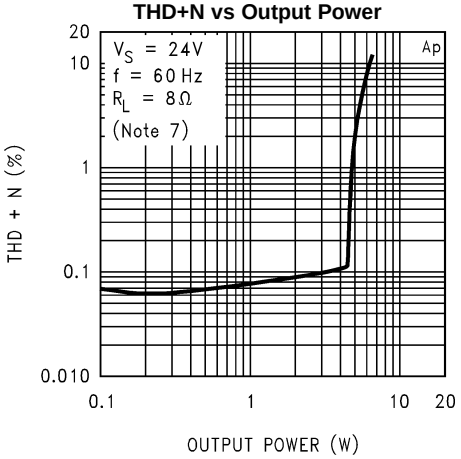


Figure 6.

THD+N vs Output Power

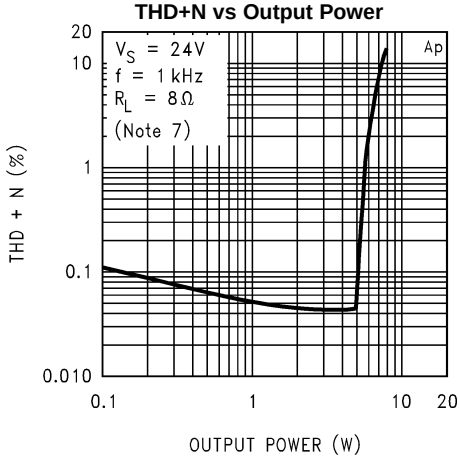


Figure 7.

THD+N vs Output Power

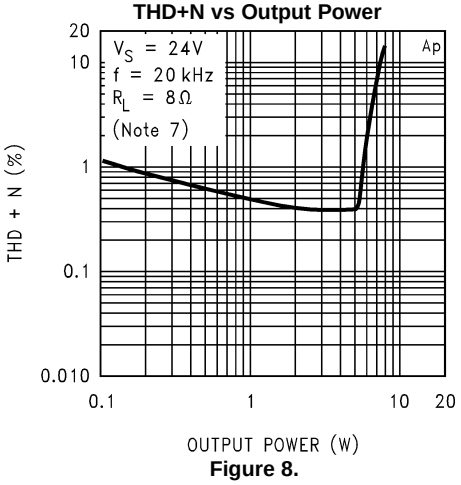


Figure 8.

THD+N vs Output Power

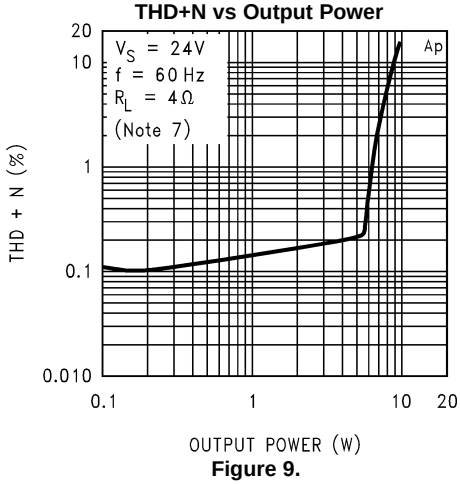


Figure 9.

THD+N vs Output Power

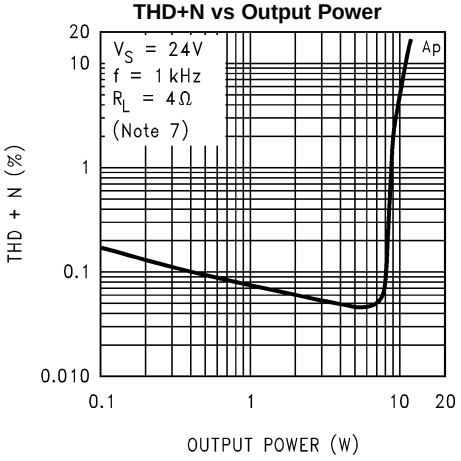


Figure 10.

THD+N vs Output Power

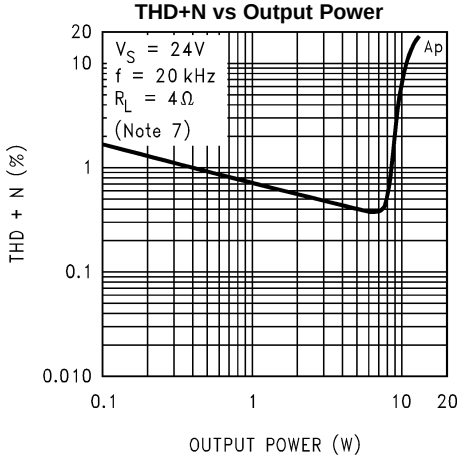


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

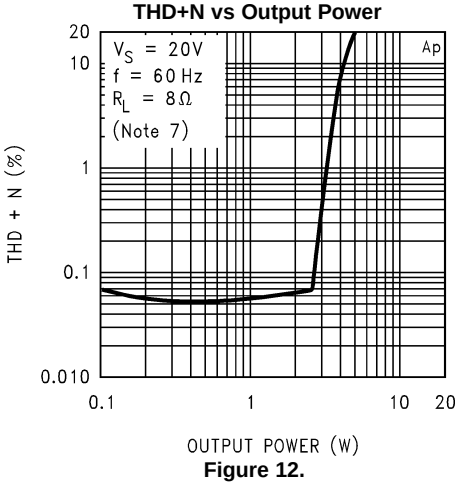


Figure 12.

THD+N vs Output Power

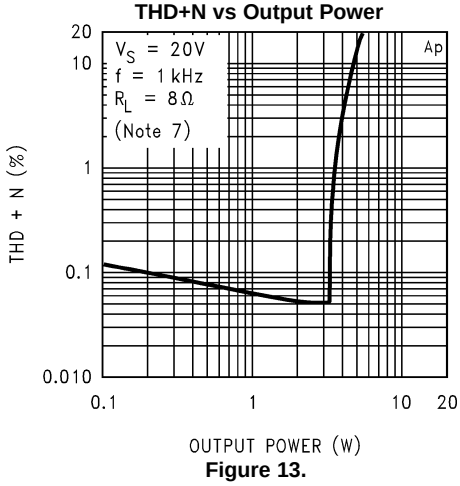


Figure 13.

THD+N vs Output Power

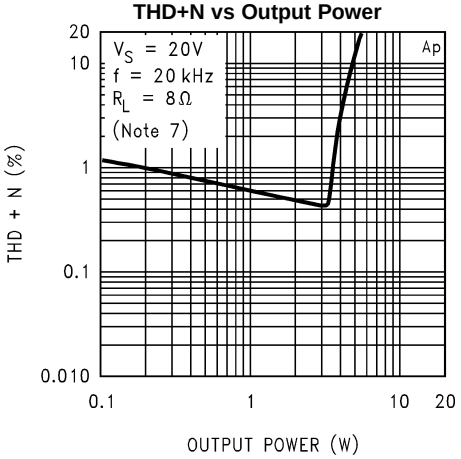


Figure 14.

THD+N vs Output Power

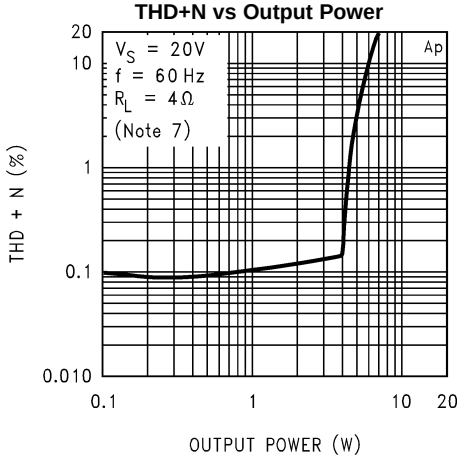


Figure 15.

THD+N vs Output Power

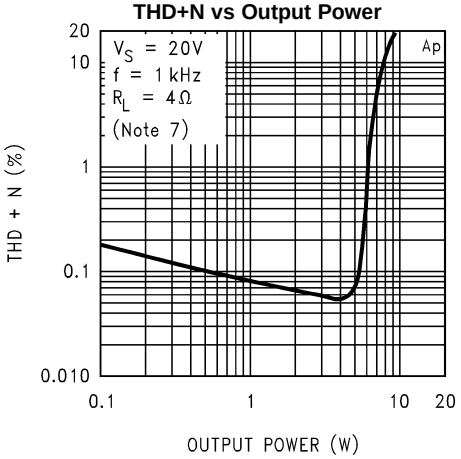


Figure 16.

THD+N vs Output Power

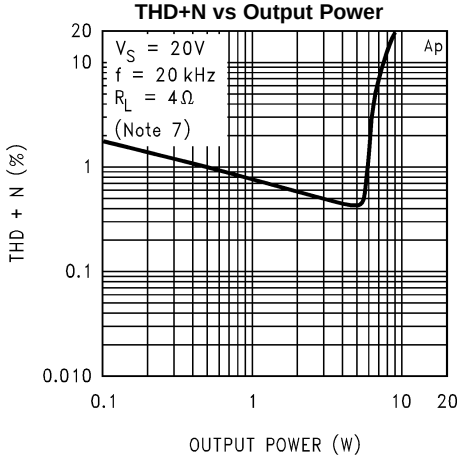


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

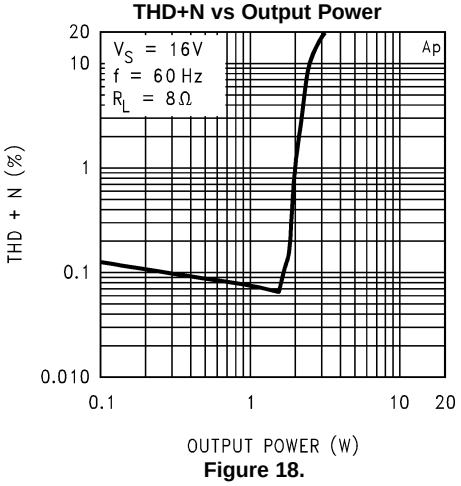


Figure 18.

THD+N vs Output Power

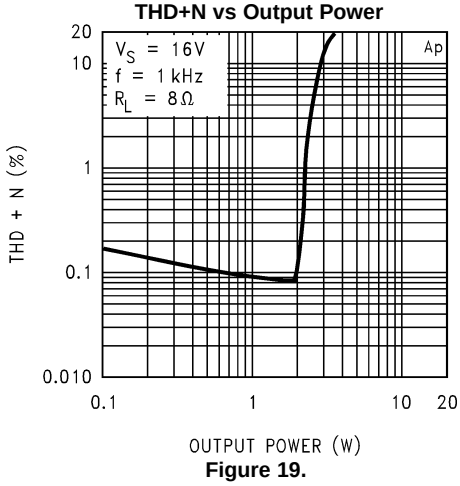


Figure 19.

THD+N vs Output Power

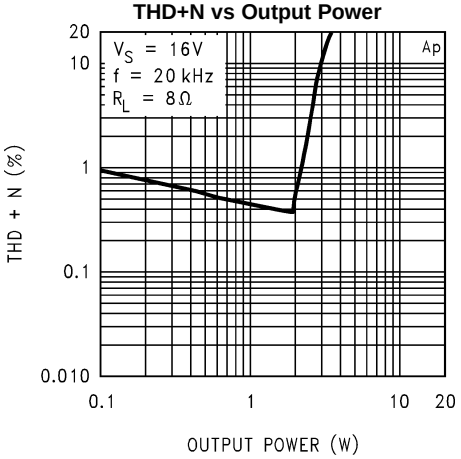


Figure 20.

THD+N vs Output Power

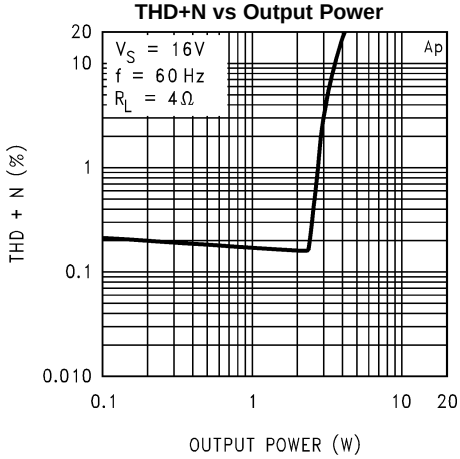


Figure 21.

THD+N vs Output Power

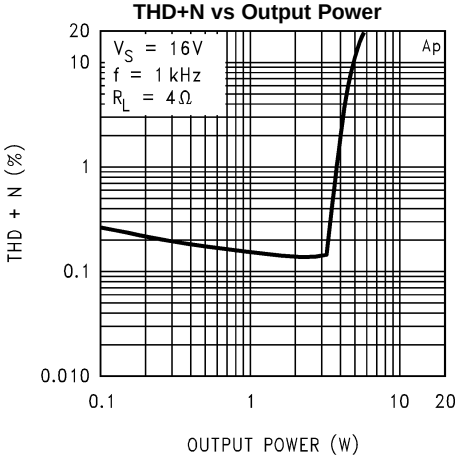


Figure 22.

THD+N vs Output Power

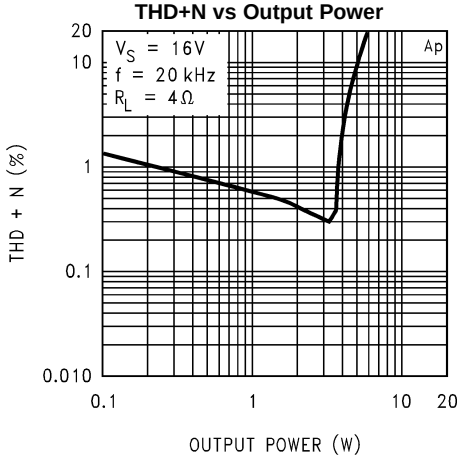


Figure 23.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power

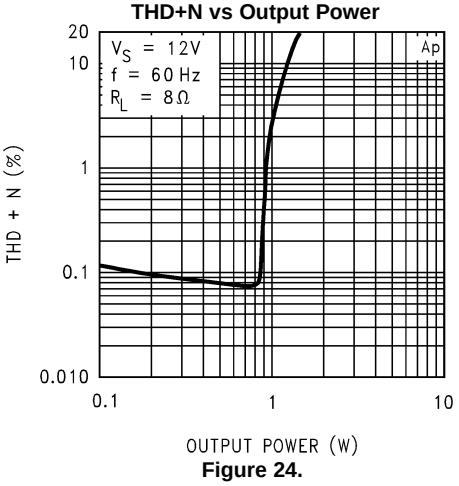


Figure 24.

THD+N vs Output Power

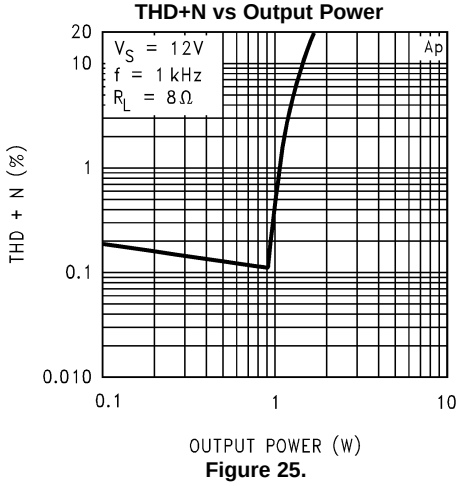


Figure 25.

THD+N vs Output Power

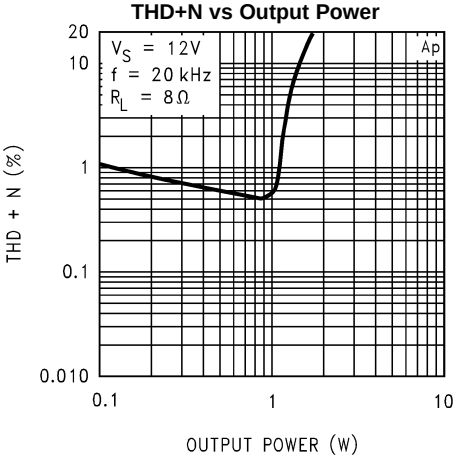


Figure 26.

THD+N vs Output Power

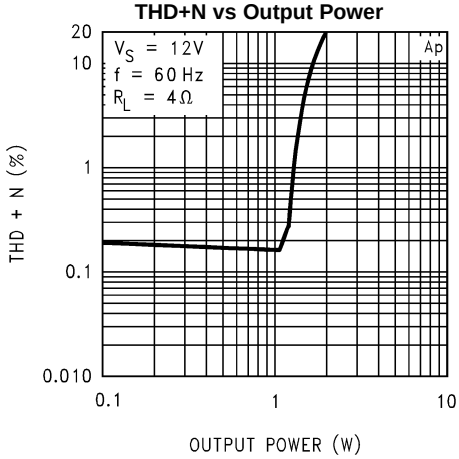


Figure 27.

THD+N vs Output Power

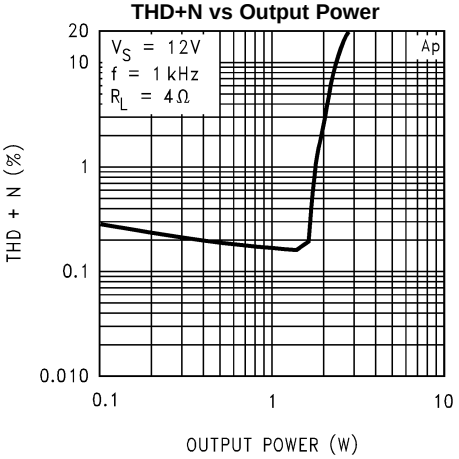


Figure 28.

THD+N vs Output Power

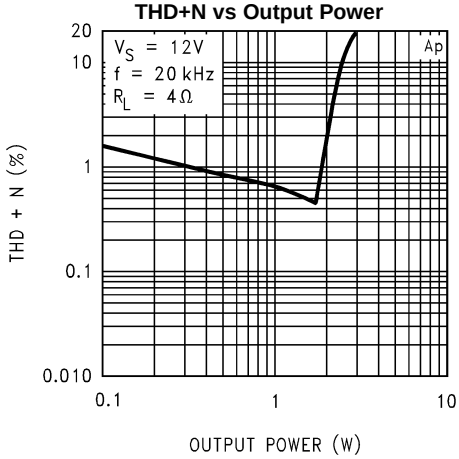


Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Power vs Supply Voltage

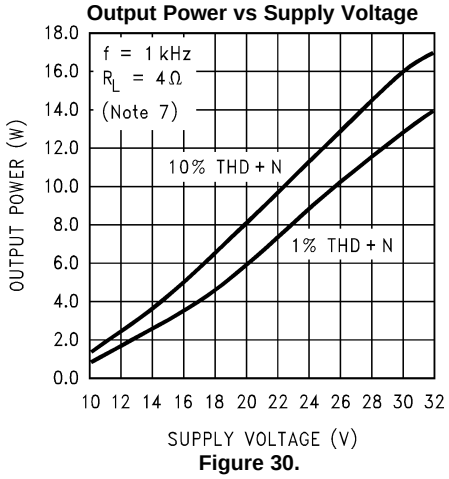


Figure 30.

Output Power vs Supply Voltage

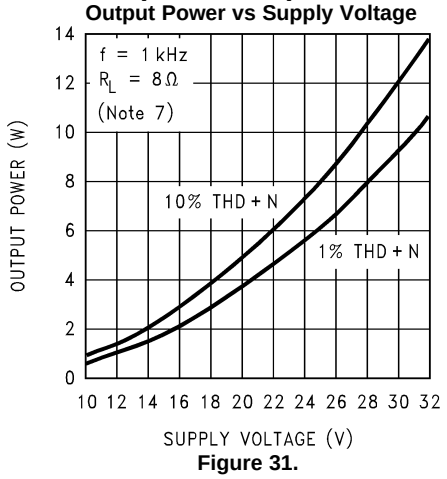


Figure 31.

Frequency Response

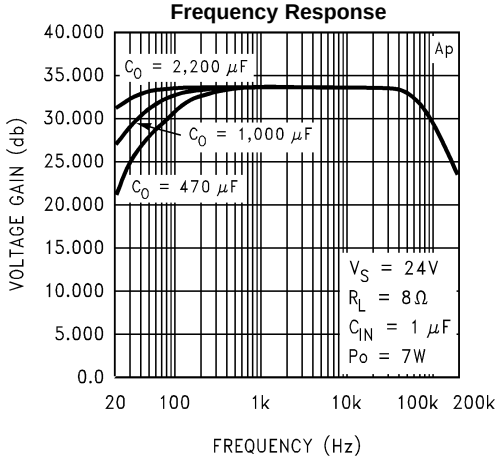


Figure 32.

THD+N vs Frequency

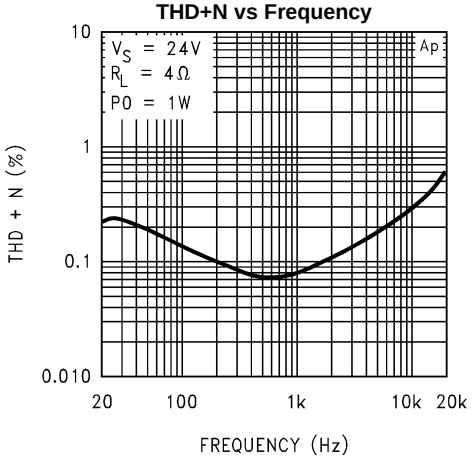


Figure 33.

THD+N vs Frequency

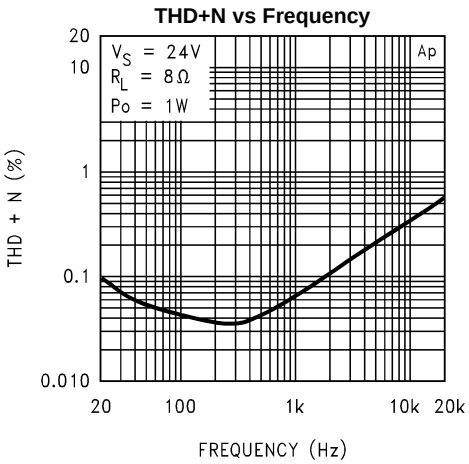


Figure 34.

Frequency Response

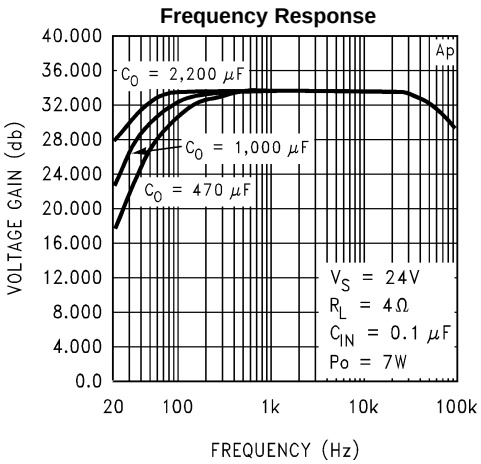


Figure 35.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Channel Separation

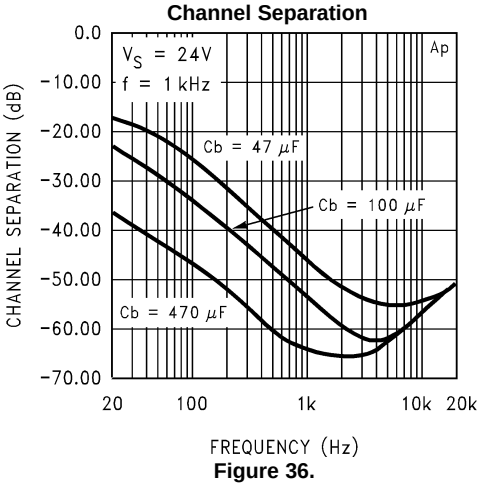


Figure 36.

PSRR vs Frequency

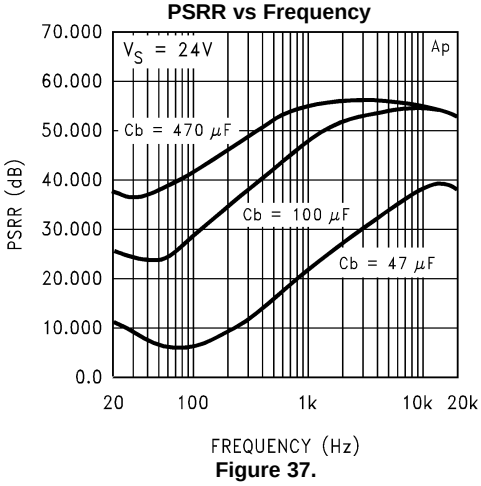


Figure 37.

Supply Current vs Supply Voltage

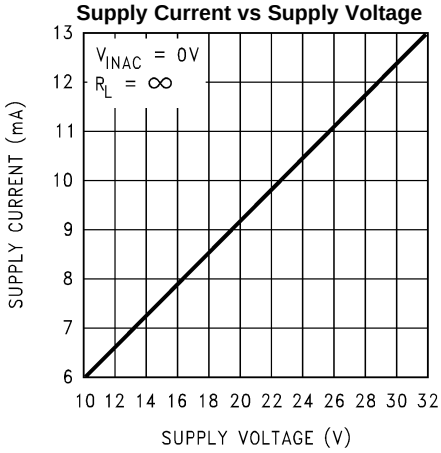


Figure 38.

Power Derating Curve

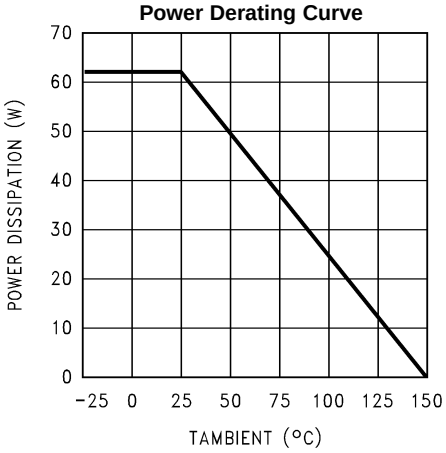


Figure 39.

Power Dissipation vs Output Power

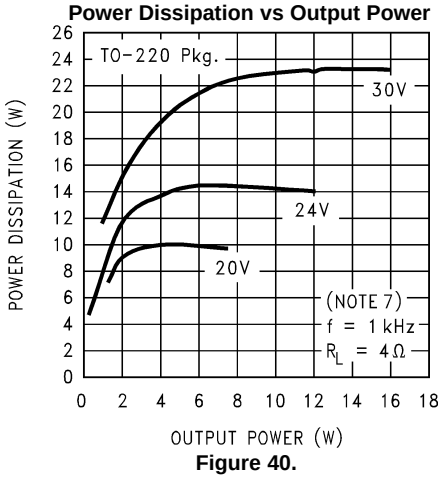


Figure 40.

Power Dissipation vs Output Power

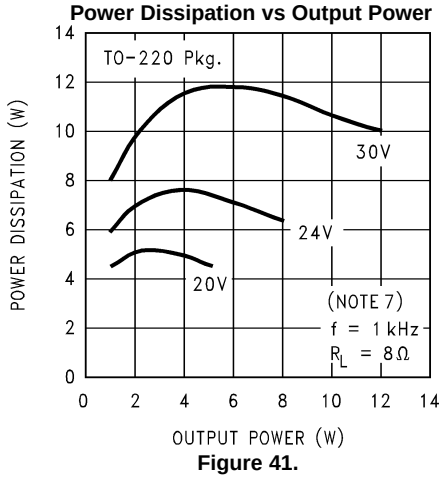


Figure 41.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Dissipation vs Output Power

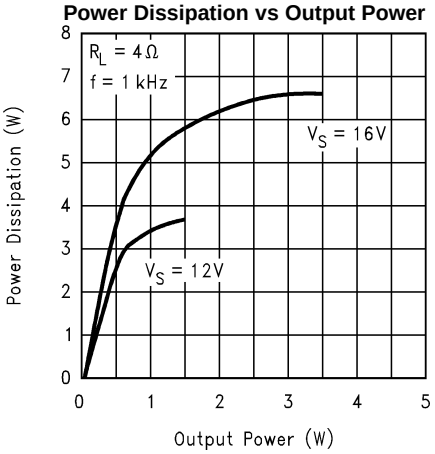


Figure 42.

Power Dissipation vs Output Power

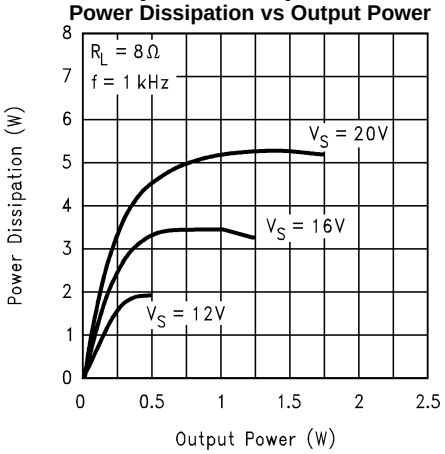


Figure 43.

APPLICATION INFORMATION

CAPACITOR SELECTION AND FREQUENCY RESPONSE

With the LM4752, as in all single supply amplifiers, AC coupling capacitors are used to isolate the DC voltage present at the inputs (pins 2,6) and outputs (pins 1,7). As mentioned earlier in the EXTERNAL COMPONENTS DESCRIPTION section these capacitors create high-pass filters with their corresponding input/output impedances. The Typical Application Circuit shown in Figure 1 shows input and output capacitors of 0.1 µF and 1,000 µF respectively. At the input, with an 83 kΩ typical input resistance, the result is a high pass 3 dB point occurring at 19 Hz. There is another high pass filter at 39.8 Hz created with the output load resistance of 4Ω. Careful selection of these components is necessary to ensure that the desired frequency response is obtained. The Frequency Response curves in the TYPICAL PERFORMANCE CHARACTERISTICS section show how different output coupling capacitors affect the low frequency rolloff.

APPLICATION CIRCUIT WITH MUTE

With the addition of a few external components, a simple mute circuit can be implemented, such as the one shown in Figure 3. This circuit works by externally pulling down the half supply bias line (pin 5), effectively shutting down the input stage.

When using an external circuit to pull down the bias, care must be taken to ensure that this line is not pulled down too quickly, or output “pops” or signal feedthrough may result. If the bias line is pulled down too quickly, currents induced in the internal bias resistors will cause a momentary DC voltage to appear across the inputs of each amplifier's internal differential pair, resulting in an output DC shift towards V_{SUPPLY}. An R-C timing circuit should be used to limit the pull-down time such that output “pops” and signal feedthroughs will be minimized. The pull-down timing is a function of a number of factors, including the external mute circuitry, the voltage used to activate the mute, the bias capacitor, the half-supply voltage, and internal resistances used in the half-supply generator. Table 1 shows a list of recommended values for the external mute circuitry.

Table 1. Values for Mute Circuit

V_{MUTE}	R1	R2	C1	R3	C_B	V_{CC}
5V	10 kΩ	10 kΩ	4.7 µF	360Ω	100 µF	21V–32V
V_S	20 kΩ	1.2 kΩ	4.7 µF	180Ω	100 µF	15V–32V
V_S	20 kΩ	910Ω	4.7 µF	180Ω	47 µF	22V–32V

OPERATING IN BRIDGE-MODE

Though designed for use as a single-ended amplifier, the LM4752 can be used to drive a load differentially (bridge-mode). Due to the low pin count of the package, only the non-inverting inputs are available. An inverted signal must be provided to one of the inputs. This can easily be done with the use of an inexpensive op-amp configured as a standard inverting amplifier. An LF353 is a good low-cost choice. Care must be taken, however, for a bridge-mode amplifier must theoretically dissipate four times the power of a single-ended type. The load seen by each amplifier is effectively half that of the actual load being used, thus an amplifier designed to drive a 4Ω load in single-ended mode should drive an 8Ω load when operating in bridge-mode.

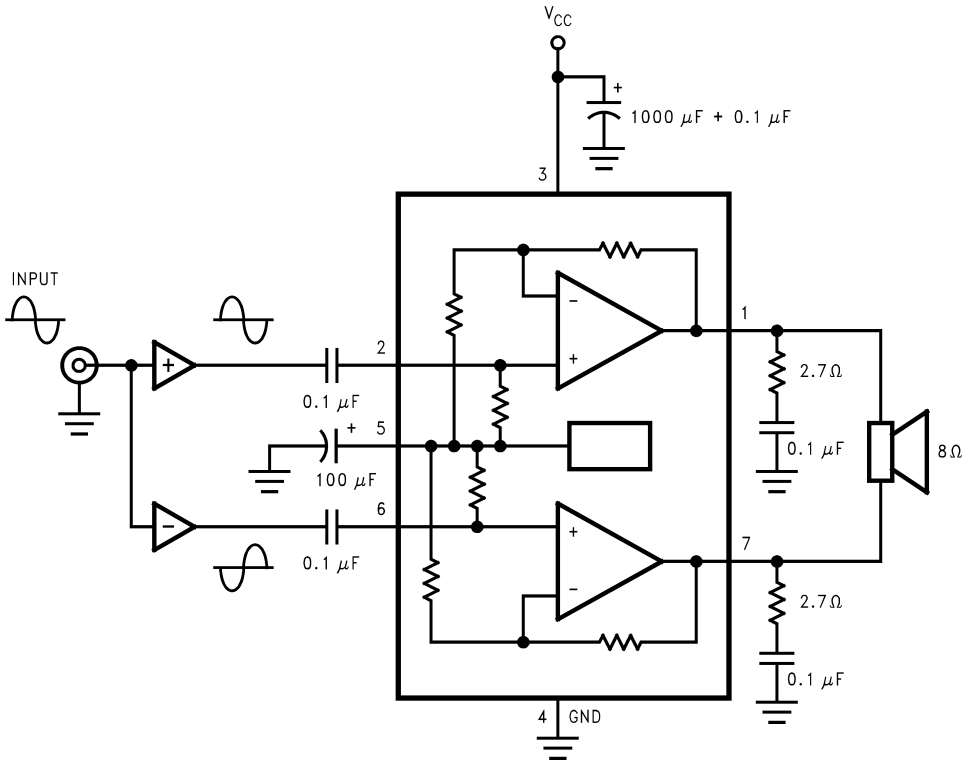


Figure 44. Bridge-Mode Application

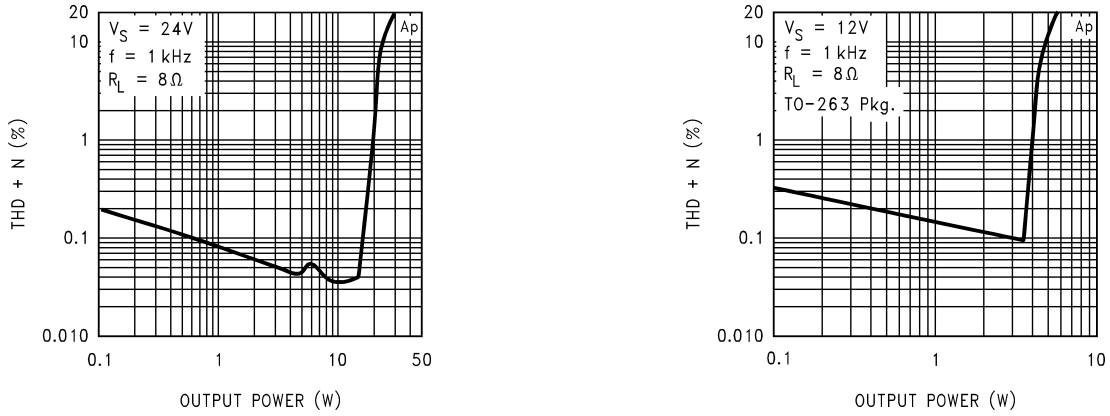


Figure 45. THD+N vs. P_{OUT} for Bridge-Mode Application

PREVENTING OSCILLATIONS

With the integration of the feedback and bias resistors on-chip, the LM4752 fits into a very compact package. However, due to the close proximity of the non-inverting input pins to the corresponding output pins, the inputs should be AC terminated at all times. If the inputs are left floating, the amplifier will have a positive feedback path through high impedance coupling, resulting in a high frequency oscillation. In most applications, this termination is typically provided by the previous stage's source impedance. If the application will require an external signal, the inputs should be terminated to ground with a resistance of 50 kΩ or less on the AC side of the input coupling capacitors.

UNDERVOLTAGE SHUTDOWN

If the power supply voltage drops below the minimum operating supply voltage, the internal under-voltage detection circuitry pulls down the half-supply bias line, shutting down the preamp section of the LM4752. Due to the wide operating supply range of the LM4752, the threshold is set to just under 9V. There may be certain applications where a higher threshold voltage is desired. One example is a design requiring a high operating supply voltage, with large supply and bias capacitors, and there is little or no other circuitry connected to the main power supply rail. In this circuit, when the power is disconnected, the supply and bias capacitors will discharge at a slower rate, possibly resulting in audible output distortion as the decaying voltage begins to clip the output signal. An external circuit may be used to sense for the desired threshold, and pull the bias line (pin5) to ground to disable the input preamp. Figure 46 shows an example of such a circuit. When the voltage across the zener diode drops below its threshold, current flow into the base of Q1 is interrupted. Q2 then turns on, discharging the bias capacitor. This discharge rate is governed by several factors, including the bias capacitor value, the bias voltage, and the resistor at the emitter of Q2. An equation for approximating the value of the emitter discharge resistor, R, is given below:

$$R = (0.7V) / (C_B \bullet (V_S / 2) / 0.1s) \quad (1)$$

Note that this is only a linearized approximation based on a discharge time of 0.1s. The circuit should be evaluated and adjusted for each application.

As mentioned earlier in the Application Circuit with Mute section, when using an external circuit to pull down the bias line, the rate of discharge will have an effect on the turn-off induced distortions. Please refer to the Application Circuit with Mute section for more information.

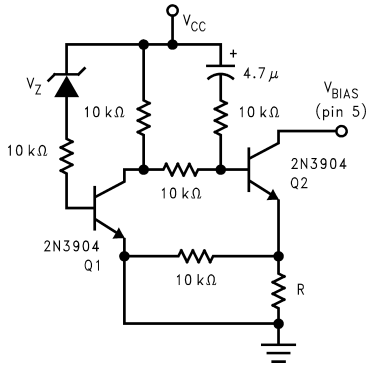


Figure 46. External Undervoltage Pull-Down

THERMAL CONSIDERATIONS

HEAT SINKING

Proper heatsinking is necessary to ensure that the amplifier will function correctly under all operating conditions. A heatsink that is too small will cause the die to heat excessively and will result in a degraded output signal as the internal thermal protection circuitry begins to operate.

The choice of a heatsink for a given application is dictated by several factors: the maximum power the IC needs to dissipate, the worst-case ambient temperature of the circuit, the junction-to-case thermal resistance, and the maximum junction temperature of the IC. The heat flow approximation equation used in determining the correct heatsink maximum thermal resistance is given below:

$$T_J - T_A = P_{DMAX} \bullet (\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (2)$$

where

- P_{DMAX} = maximum power dissipation of the IC
- T_J(°C) = junction temperature of the IC
- T_A(°C) = ambient temperature
- θ_{JC}(°C/W) = junction-to-case thermal resistance of the IC
- θ_{CS}(°C/W) = case-to-heatsink thermal resistance (typically 0.2 to 0.5 °C/W)
- θ_{SA}(°C/W) = thermal resistance of heatsink

When determining the proper heatsink, the above equation should be re-written as:

$$\theta_{SA} \leq [(T_J - T_A) / P_{DMAX}] - \theta_{JC} - \theta_{CS} \quad (3)$$

DDPAK HEATSINKING

Surface mount applications will be limited by the thermal dissipation properties of printed circuit board area. The DDPAK package is not recommended for surface mount applications with V_S > 16V due to limited printed circuit board area. There are DDPAK package enhancements, such as clip-on heatsinks and heatsinks with adhesives, that can be used to improve performance.

Standard FR-4 single-sided copper clad will have an approximate Thermal resistance (θ_{SA}) ranging from:

1.5 × 1.5 in. sq.	20–27°C/W	(T_A=28°C, Sine wave testing, 1 oz. Copper)
2 × 2 in. sq.	16–23°C/W	

The above values for θ_{SA} vary widely due to dimensional proportions (i.e. variations in width and length will vary θ_{SA}).

For audio applications, where peak power levels are short in duration, this part will perform satisfactory with less heatsinking/copper clad area. As with any high power design proper bench testing should be undertaken to assure the design can dissipate the required power. Proper bench testing requires attention to worst case ambient temperature and air flow. At high power dissipation levels the part will show a tendency to increase saturation voltages, thus limiting the undistorted power levels.

DETERMINING MAXIMUM POWER DISSIPATION

For a single-ended class AB power amplifier, the theoretical maximum power dissipation point is a function of the supply voltage, V_S, and the load resistance, R_L and is given by the following equation:

(single channel)

$$P_{DMAX} (W) = [V_S^2 / (2 \cdot \pi^2 \cdot R_L)] \quad (4)$$

The above equation is for a single channel class-AB power amplifier. For dual amplifiers such as the LM4752, the equation for calculating the total maximum power dissipated is:

(dual channel)

$$P_{DMAX} (W) = 2 \cdot [V_S^2 / (2 \cdot \pi^2 \cdot R_L)] \quad (5)$$

or

$$V_S^2 / (\pi^2 \cdot R_L) \quad (6)$$

(Bridged Outputs)

$$P_{DMAX} (W) = 4[V_S^2 / (2\pi^2 \cdot R_L)] \quad (7)$$

HEATSINK DESIGN EXAMPLE

Determine the system parameters:

V_S = 24V Operating Supply Voltage

R_L = 4Ω Minimum load impedance

T_A = 55°C Worst case ambient temperature

Device parameters from the datasheet:

T_J = 150°C Maximum junction temperature

θ_{JC} = 2°C/W Junction-to-case thermal resistance

Calculations:

$$2 \cdot P_{DMAX} = 2 \cdot [V_S^2 / (2 \cdot \pi^2 \cdot R_L)] = (24V)^2 / (2 \cdot \pi^2 \cdot 4\Omega) = 14.6W \quad (8)$$

$$\theta_{SA} \leq [(T_J - T_A) / P_{DMAX}] - \theta_{JC} - \theta_{CS} = [(150°C - 55°C) / 14.6W] - 2°C/W - 0.2°C/W = 4.3°C/W \quad (9)$$

Conclusion: Choose a heatsink with $\theta_{SA} \leq$ 4.3°C/W.

DDPAK HEATSINK DESIGN EXAMPLES

Example 1: (Stereo Single-Ended Output)

Given: T_A=30°C

T_J=150°C

R_L=4Ω

V_S=12V

θ_{JC}=2°C/W

P_{DMAX} from P_D vs P_O Graph:

$P_{DMAX} \approx 3.7W$ (10)

Calculating P_{DMAX}:

$P_{DMAX} = V_{CC}^2 / (\pi^2 R_L) = (12V)^2 / \pi^2(4\Omega)) = 3.65W$ (11)

Calculating Heatsink Thermal Resistance:

$\theta_{SA} < [(T_J - T_A) / P_{DMAX}] - \theta_{JC} - \theta_{CS}$ (12)

$\theta_{SA} < 120°C / 3.7W - 2.0°C/W - 0.2°C/W = 30.2°C/W$ (13)

Therefore the recommendation is to use 1.5 × 1.5 square inch of single-sided copper clad.

Example 2: (Stereo Single-Ended Output)

Given: T_A=50°C

T_J=150°C

R_L=4Ω

V_S=12V

θ_{JC}=2°C/W

P_{DMAX} from P_D vs P_O Graph:

$P_{DMAX} \approx 3.7W$ (14)

Calculating P_{DMAX}:

$P_{DMAX} = V_{CC}^2 / (\pi^2 R_L) = (12V)^2 / (\pi^2(4\Omega)) = 3.65W$ (15)

Calculating Heatsink Thermal Resistance:

$\theta_{SA} < [(T_J - T_A) / P_{DMAX}] - \theta_{JC} - \theta_{CS}$ (16)

$\theta_{SA} < 100°C / 3.7W - 2.0°C/W - 0.2°C/W = 24.8°C/W$ (17)

Therefore the recommendation is to use 2.0 × 2.0 square inch of single-sided copper clad.

Example 3: (Bridged Output)

Given: T_A=50°C

T_J=150°C

R_L=8Ω

V_S=12V

θ_{JC}=2°C/W

Calculating P_{DMAX}:

$P_{DMAX} = 4[V_{CC}^2 / (2\pi^2 R_L)] = 4(12V)^2 / (2\pi^2(8\Omega)) = 3.65W$ (18)

Calculating Heatsink Thermal Resistance:

$\theta_{SA} < [(T_J - T_A) / P_{DMAX}] - \theta_{JC} - \theta_{CS}$ (19)

$\theta_{SA} < 100°C / 3.7W - 2.0°C/W - 0.2°C/W = 24.8°C/W$ (20)

Therefore the recommendation is to use 2.0 × 2.0 square inch of single-sided copper clad.

LAYOUT AND GROUND RETURNS

Proper PC board layout is essential for good circuit performance. When laying out a PC board for an audio power amplifer, particular attention must be paid to the routing of the output signal ground returns relative to the input signal and bias capacitor grounds. To prevent any ground loops, the ground returns for the output signals should be routed separately and brought together at the supply ground. The input signal grounds and the bias capacitor ground line should also be routed separately. The 0.1 µF high frequency supply bypass capacitor should be placed as close as possible to the IC.

PC BOARD LAYOUT—COMPOSITE

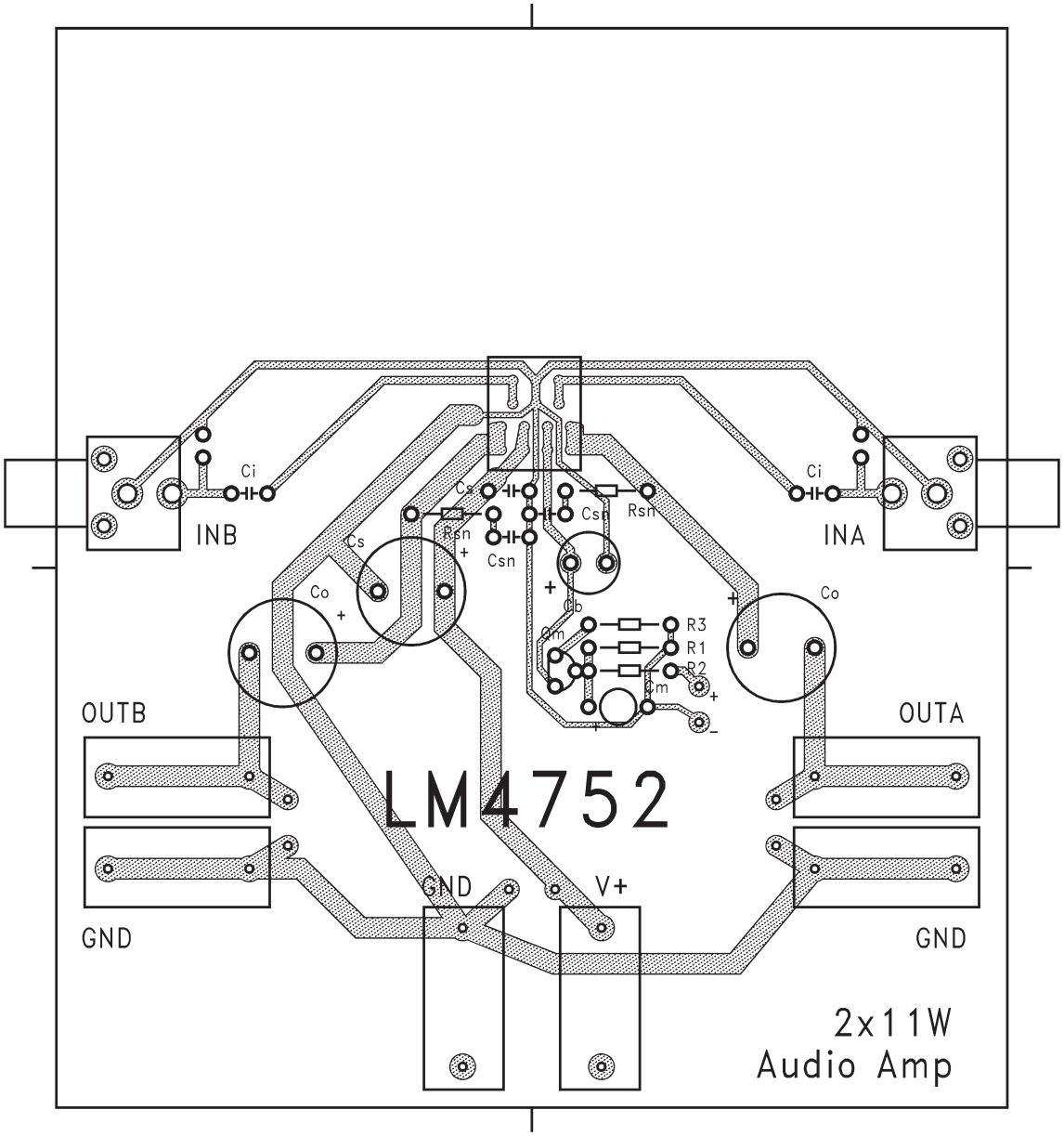


Figure 47.

PC BOARD LAYOUT—SILK SCREEN

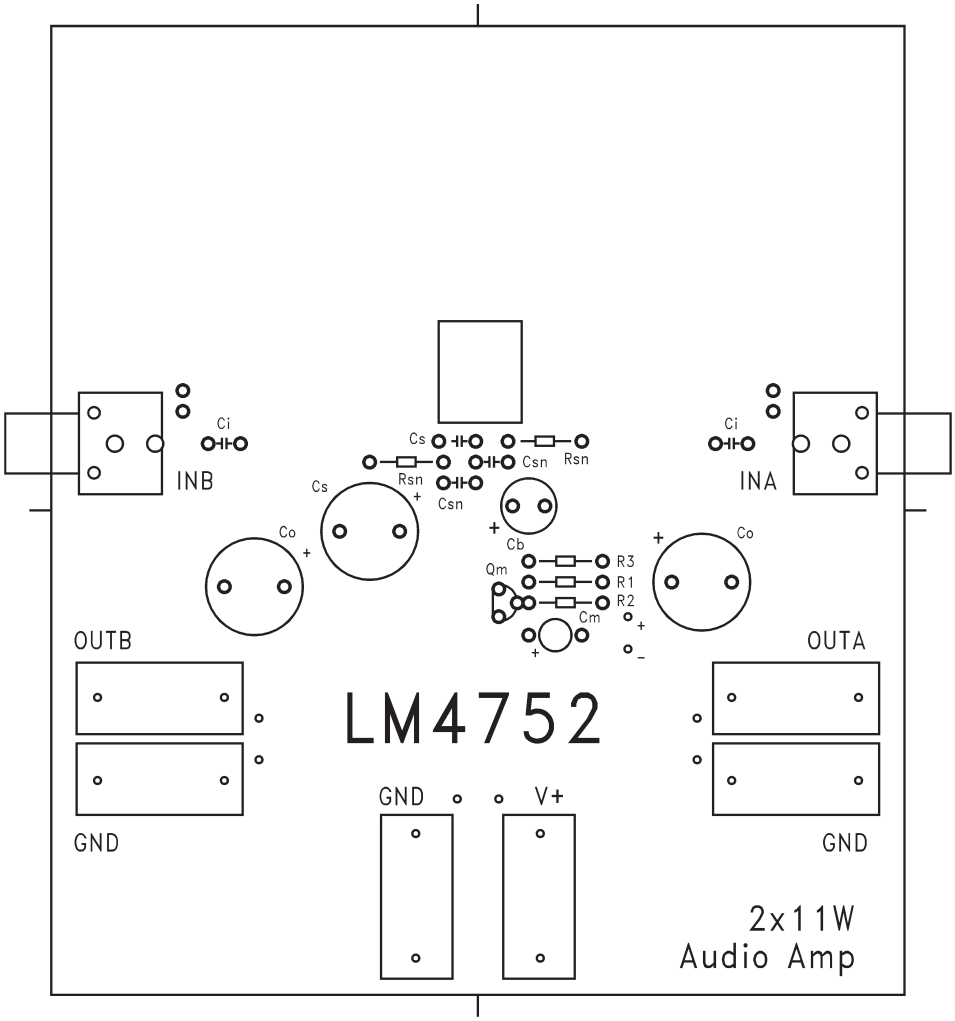


Figure 48.

PC BOARD LAYOUT—SOLDER SIDE

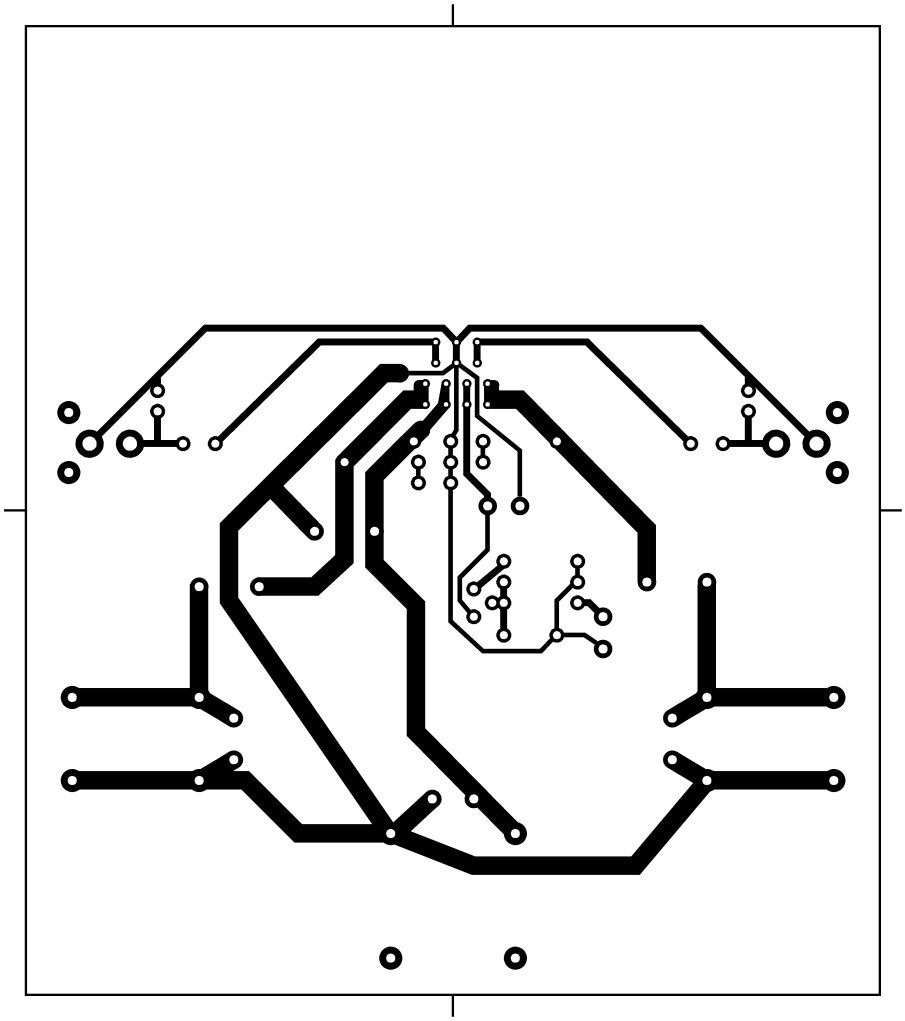


Figure 49.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4752TS/NOPB	Active	Production	DDPAK/TO-263 (KTW) | 7	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	0 to 70	LM4752TS
LM4752TS/NOPB.B	Active	Production	DDPAK/TO-263 (KTW) | 7	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	0 to 70	LM4752TS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

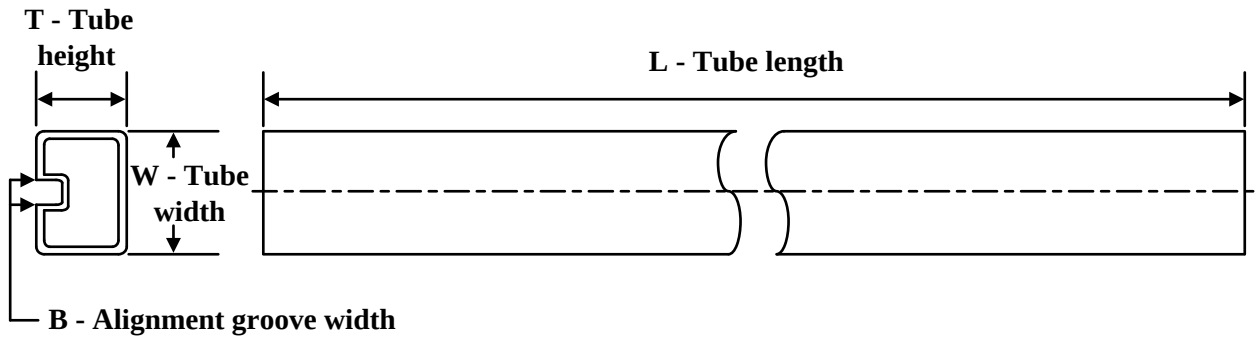
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

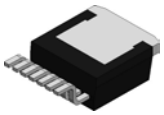
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4752TS/NOPB	KTW	TO-263	7	45	502	25	8204.2	9.19
LM4752TS/NOPB.B	KTW	TO-263	7	45	502	25	8204.2	9.19

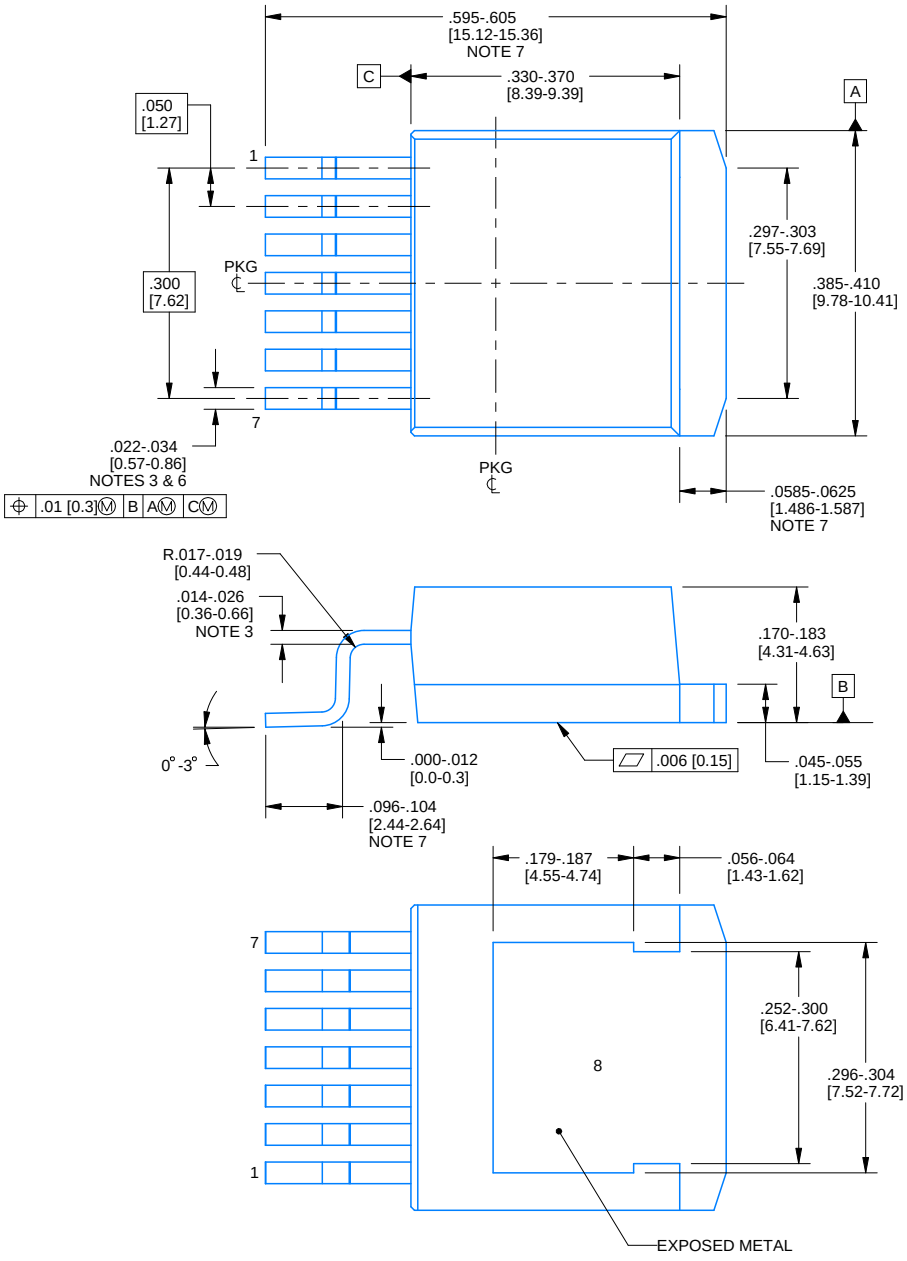
KTW0007A



PACKAGE OUTLINE

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



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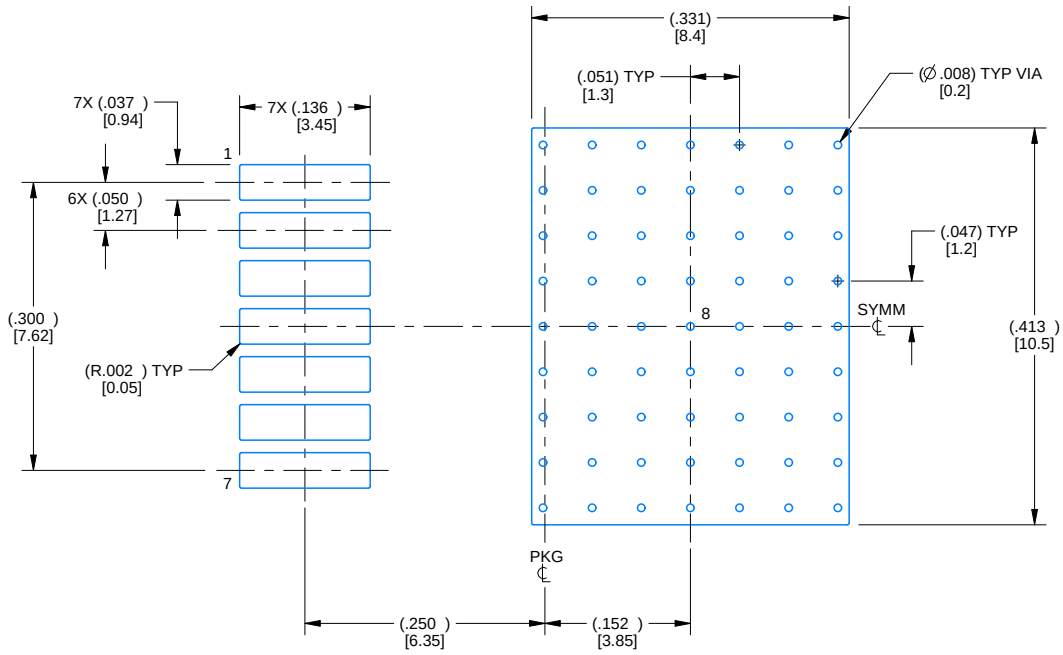
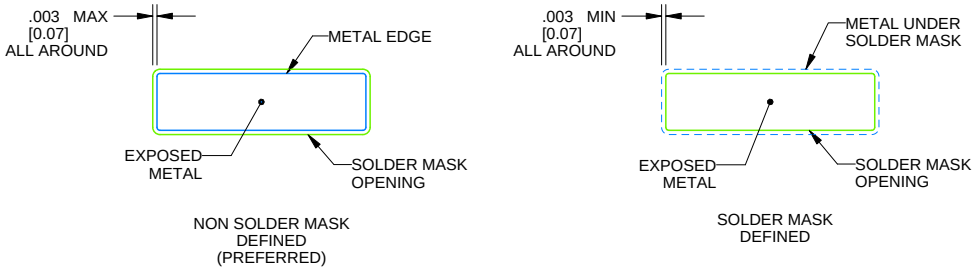
NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead width and height dimensions apply to the plated lead.
4. Leads are not allowed above the Datum B.
5. Stand–off height is measured from lead tip with reference to Datum B.
6. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum bdimension by more than 0.003”.
7. Falls within JEDEC MO–169 with the exception of the dimensions indicated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X



SOLDER MASK DETAILS

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NOTES: (continued)

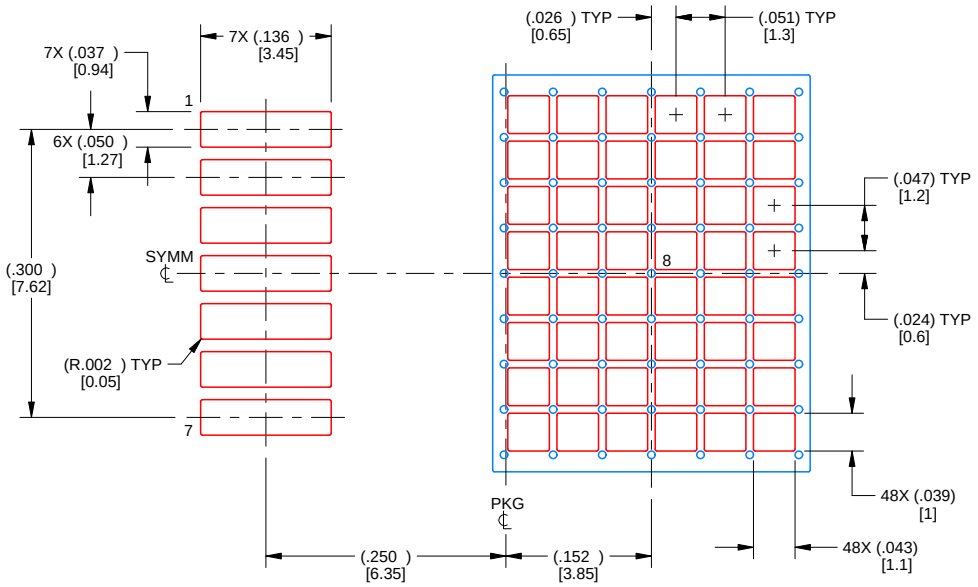
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTW0007A

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 5X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 8: 60%

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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