LM4549B 具有采样率转换和 TI 3D Sound 功能的 AC '97 版本 2.1 多通道音频编解码器

1 特性

- 兼容 AC '97 版本 2.1
- 4kHz 至 48kHz 范围内的高质量采样率转换（单位增量为 1Hz）
- 多编解码器支持
- 具有独立增益控制的真正线路电平输出
- 德州仪器 (TI) 的 3D Sound 立体声增强电路
- 高级电源管理支持
- 外部放大器断电 (EAPD) 控制
- PC 蜂鸣器在初始化或冷复位过程中直通至线路输出
- 3.3V 和 5V 数字电源选项
- 扩展温度范围：−40°C ≤ T_A ≤ 85°C
- 主要技术规格
  - 模拟混合器动态范围：97dB（典型值）
  - 数模转换器 (DAC) 动态范围： 89dB（典型值）
  - 模数转换器 (ADC) 动态范围：90dB（典型值）

2 应用

- PCI 卡和 AMR 卡中的桌面 PC 音频系统，或采用带有 AC 链路的主板芯片组的桌面 PC 音频系统
- MDC 卡中的便携式 PC 系统，或采用带有 AC 链路的芯片组或加速器的便携式 PC 系统
- 一般和多通道音频系统
- 汽车远程信息处理

3 说明

LM4549B 器件是一款用于 PC 系统的音频编解码器，它与 PC99 完全兼容并执行 AC '97 版本 2.1 架构的模拟密集型功能。 利用 18 位 Σ-Δ ADC 和 DAC，LM4549B 可提供 90dB 的动态范围。

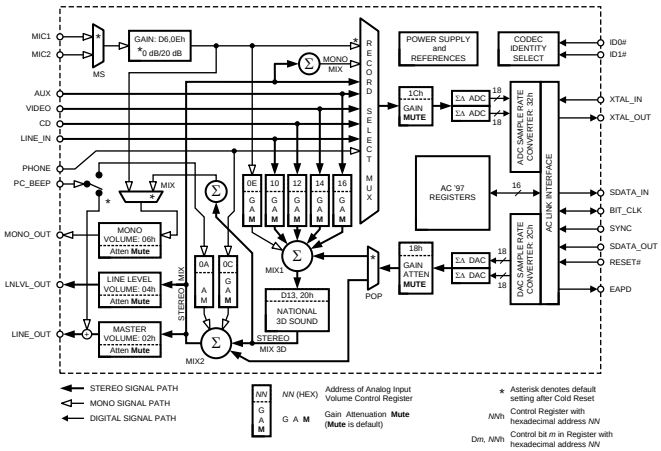
LM4549B 专门用于提供高品质音频路径，以及在 PC 音频系统中提供所有模拟功能。 该器件具有全双工立体声 ADC 和 DAC 以及模拟混合器，可接入 4 个立体声输入和 4 个单声道输入。 混合器的每个输入都具有独立的增益、衰减和静音控制功能。混合器可驱动 1 个单声道输出和 2 个立体声输出，每个输出均具备衰减和静音控制功能。 LM4549B 支持德州仪器的 3D Sound 立体声增强功能，并且具备全面的采样率转换能力。 该器件可以 1Hz 为分辨率在 4kHz - 48kHz 范围内对 ADC 和 DAC 的采样率单独进行编程。 ADC 的采样时序和 DAC 的采样请求时序是完全确定的，这样便于任务调度和应用软件开发。 这些特性和扩展级温度范围使得 LM4549B 同样适用于非 PC 编解码器应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM4549B	LQFP (48)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

功能方框图



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4 修订历史

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Original (May 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format ... 17

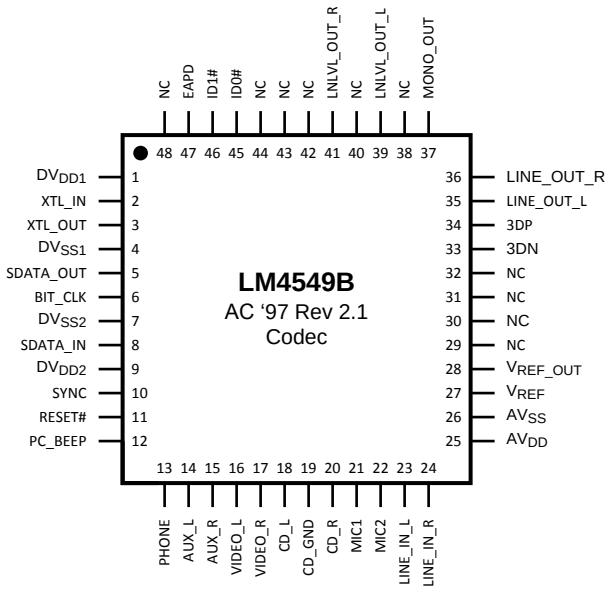
5 说明（续）

LM4549B 可使用扩展 AC 链路配置将多个编解码器连接在一起。在这种配置中，每个编码器都有一个专用的串行数据信号连接至控制器。 LM4549B 系统支持输入帧（编解码器到控制器）上同时传输多达 8 通道的数据流，而输出帧（控制器到编解码器）将 2 条数据流传输至多个编解码器。 LM4549B 还可用于采用德州仪器 LM4550B 的系统中，从而支持输出帧上同时传输多达 6 通道的数据流。

AC '97 架构分离了 PC 音频系统的模拟功能和数字功能，提升了系统设计的灵活性和器件性能。

6 Pin Configuration and Functions

PT Package
48-Pin LQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AUX_L	14	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Record Select Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the Aux Volume register, 16h. The AUX_L level can be muted (along with AUX_R) or adjusted from +12 dB to -34.5 dB in 1.5 -dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
AUX_R	15	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Record Select Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the Aux Volume register, 16h. The AUX_R level can be muted (along with AUX_L) or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
CD_GND	19	I	AC Ground Reference This input is the reference for the signals on both CD_L and CD_R. CD_GND is not a DC ground and should be AC-coupled to the stereo source ground common to both CD_L and CD_R. The three inputs, CD_GND, CD_L and CD_R act together as a quasi-differential stereo input with CD_GND providing AC common-mode feedback to reject ground noise. This can improve the input SNR for a stereo source with a good common ground but precision resistors may be needed in any external attenuators to achieve the necessary balance between the two channels.
CD_L	18	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Input Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the CD Volume register, 12h. The CD_L level can be muted (along with CD_R) or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. Stereo Mix 3D is mixed into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
CD_R	20	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Input Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the CD Volume register, 12h. The CD_R level can be muted (along with CD_L) or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
LINE_IN_L	23	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Record Select Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the Line In Volume register, 10h. The LINE_IN_L level can be muted (along with LINE_IN_R) or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
LINE_IN_R	24	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Input Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the Line In Volume register, 10h. The LINE_IN_R level can be muted (along with LINE_IN_L) or adjusted from +12 dB to -34.5 dB in 1.5 dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
LINE_OUT_L	35	O	Left Stereo Channel Output This line level output (1 Vrms nominal) is fed from the left channel of the Stereo Mix signal from MIX2 via the Master Volume register, 02h. The LINE_OUT_L amplitude can be muted (along with LINE_OUT_R) or adjusted from 0 dB to -46.5 dB in 1.5-dB steps.
LINE_OUT_R	36	O	Right Stereo Channel Output This line level output (1 Vrms nominal) is fed from the right channel of the Stereo Mix signal from MIX2 via the Master Volume register, 02h. The LINE_OUT_R amplitude can be muted (along with LINE_OUT_L) or adjusted from 0 dB to -46.5 dB in 1.5-dB steps.
LNLVL_OUT_L	39	O	Left Stereo Channel Output This line level output (1 Vrms nominal) is fed from the left channel of the Stereo Mix signal from MIX2 via the Line Level Volume register, 04h. The LNLVL_OUT_L amplitude can be muted (along with LNLVL_OUT_R) or adjusted from 0 dB to - 46.5 dB in 1.5-dB steps
LNLVL_OUT_R	41	O	Right Stereo Channel Output This line level output (1 Vrms nominal) is fed from the right channel of the Stereo Mix signal from MIX2 via the Line Level Volume register, 04h. The LNLVL_OUT_R amplitude can be muted (along with LNLVL_OUT_L) or adjusted from 0 dB to - 46.5 dB in 1.5-dB steps
MIC1	21	I	Mono microphone input Either MIC1 or MIC2 can be muxed to a programmable boost amplifier with selection by the MS bit (bit D8) in the General Purpose register, 20h. The boost amplifier gain (0 dB or 20 dB) is set by the 20dB bit (D6) in the Mic Volume register, 0Eh. Nominal input levels at the two gain settings are 1 Vrms and 0.1 Vrms respectively. The amplifier output is selectable (Record Select register, 1Ah) by either the right or left channels of the Record Select Mux for conversion on either or both channels of the stereo ADCs. The amplifier output can also be accessed at the stereo mixer MIX1 (muting and mixing adjustments via Mic Volume register, 0Eh) where it is mixed equally into both left and right channels of Stereo Mix 3D for access to the stereo outputs Line Out and Line Level Out. Access to the Mono analog output is selected by a mux controlled by the MIX bit (D9) in General Purpose register, 20h.
MIC2	22	I	Mono microphone input Either MIC1 or MIC2 can be muxed to a programmable boost amplifier with selection by the MS bit (bit D8) in the General Purpose register, 20h. The boost amplifier gain (0 dB or 20 dB) is set by the 20dB bit (D6) in the Mic Volume register, 0Eh. Nominal input levels at the two gain settings are 1 Vrms and 0.1 Vrms respectively. The amplifier output is selectable (Record Select register, 1Ah) by either the right or left channels of the Record Select Mux for conversion on either or both channels of the stereo ADCs. The amplifier output can also be accessed at the stereo mixer MIX1 (muting and mixing adjustments via Mic Volume register, 0Eh) where it is mixed equally into both left and right channels of Stereo Mix 3D for access to the stereo outputs Line Out and Line Level Out. Access to the Mono analog output is selected by a mux controlled by the MIX bit (D9) in General Purpose register, 20h.
MONO_OUT	37	O	Mono Output This mono line level output (1 Vrms nominal) is fed from either a microphone input (MIC1 or MIC2, after boost amplifier) or from the mono sum of the left and right Stereo Mix 3D channels from MIX1. The optional TI 3D Sound enhancement can be disabled (default) by the 3D bit (bit D13) in the General Purpose register, 20h. Choice of input is by the MIX bit (D9) in the same register. MIX=0 selects a microphone input. Output level can be muted or adjusted from 0 dB to -46.5 dB in 1.5-dB steps through the Mono Volume register, 06h.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PC_BEEP	12	I	Mono Input This line level (1 Vrms nominal) mono input is mixed equally into both channels of the Stereo Mix signal at MIX2 under the control of the PC_Beep Volume control register, 0Ah. The PC_BEEP level can be muted or adjusted from 0 dB to -45 dB in 3 dB steps. The Stereo Mix signal feeds both the Line Out and Line Level Out analog outputs and is also selectable at the Record Select Mux. During Initialization or Cold Reset, (reset pin held active low), PC_BEEP is switched directly to both channels of the Line Out stereo output, bypassing all volume controls. This allows signals such as PC power-on self-test tones to be heard through the audio system of the PC before the codec registers are configured.
PHONE	13	I	Mono Input This line level (1 Vrms nominal) mono input is selectable at the Record Select Mux for conversion by either channel of the stereo ADC. It can also be mixed equally into both channels of the Stereo Mix signal at MIX2 under the control of the Phone Volume register, 0Ch. The PHONE level can be muted or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. The Stereo Mix signal feeds both the Line Out and Line Level Out analog stereo outputs and is also selectable at the Record Select Mux.
VIDEO_L	16	I	Left Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the left channel of the stereo Record Select Mux for conversion by the left channel ADC. It can also be mixed into the left channel of the Stereo Mix 3D signal at MIX1 under the control of the Video Volume register, 14h. The VIDEO_L level can be muted (along with VIDEO_R) or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
VIDEO_R	17	I	Right Stereo Channel Input This line level input (1 Vrms nominal) is selectable at the right channel of the stereo Record Select Mux for conversion by the right channel ADC. It can also be mixed into the right channel of the Stereo Mix 3D signal at MIX1 under the control of the Video Volume register, 14h. The VIDEO_R level can be muted (along with VIDEO_L) or adjusted from +12 dB to -34.5 dB in 1.5-dB steps. Stereo Mix 3D is combined into the Stereo Mix signal at MIX2 for access to the stereo outputs Line Out and Line Level Out.
DIGITAL I/O AND CLOCKING			
BIT_CLK	6	I/O	AC Link clock An OUTPUT when in Primary Codec mode. This pin provides a 12.288 MHz clock for the AC Link. The clock is derived (internally divided by two) from the 24.576 MHz signal at the crystal input (XTL_IN). This pin is an INPUT when the codec is configured in any of the Secondary Codec modes and would normally use the AC Link clock generated by a Primary Codec.
EAPD	47	O	External Amplifier Power Down control signal This output is set by the EAPD bit (bit D15) in the Powerdown Control/ Status register, 26h. As with the other logic outputs, the output voltage is set by DV_{DD}. This pin is intended to be connected to the shutdown pin on an external power amplifier. For normal operation the default value of EAPD = 0 will enable the external amplifier allowing an input on PC_BEEP to be heard during Cold Reset.
ID0#	45	I	Codec Identity ID1# and ID0# determine the Codec Identity for multiple codec use. The Codec Identity configures the codec in either Primary or one of three Secondary Codec modes. These Identity pins are of inverted polarity relative to the Codec Identity bits ID1, ID0 (bits D15, D14) in the read-only Extended Audio ID register, 28h. If the ID0# pin (pin 45) is connected to ground then the ID0 bit (D14, reg 28h) will be set to “1”. Similarly, connection to DV_{DD} will set the ID0 bit to “0”. If left open (NC), ID0# is pulled high by an internal pull-up resistor.
ID1#	46	I	Codec Identity ID1# and ID0# determine the codec address for multiple codec use. The Codec Identity configures the codec in either Primary or one of three Secondary Codec modes. These Identity pins are of inverted polarity relative to the Codec Identity bits ID1, ID0 (bits D15, D14) in the read-only Extended Audio ID register, 28h. If the ID1# pin (pin 46) is connected to ground then the ID1 bit (D15, reg 28h) will be set to “1”. Similarly, connection to DV_{DD} will set the ID1 bit to “0”. If left open (NC), ID1# is pulled high by an internal pull-up resistor.
RESET#	11	I	Cold Reset This active low signal causes a hardware reset which returns the control registers and all internal circuits to their default conditions. RESET# MUST be used to initialize the LM4549B after Power On when the supplies have stabilized. Cold Reset also clears the codec from both ATE and Vendor test modes. In addition, while active, it switches the PC_BEEP mono input directly to both channels of the LINE_OUT stereo output.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SDATA_IN	8	O	Output from codec This is the output for AC Link Input Frames from the LM4549B codec to an AC '97 Digital Audio Controller. These frames can contain both codec status data and PCM audio data from the ADCs. The LM4549B clocks data from this output on the rising edge of BIT_CLK.
SDATA_OUT	5	I	Input to codec This is the input for AC Link Output Frames from an AC '97 Digital Audio Controller to the LM4549B codec. These frames can contain both control data and DAC PCM audio data. This input is sampled by the LM4549B on the falling edge of BIT_CLK.
SYNC	10	I	AC Link frame marker and Warm Reset This input defines the boundaries of AC Link frames. Each frame lasts 256 periods of BIT_CLK. In normal operation SYNC is a 48 kHz positive pulse with a duty cycle of 6.25% (16/256). SYNC is sampled on the falling edge of BIT_CLK and the codec takes the first positive sample of SYNC as defining the start of a new AC Link frame. If a subsequent SYNC pulse occurs within 255 BIT_CLK periods of the frame start it will be ignored. SYNC is also used as an active high input to perform an (asynchronous) Warm Reset. Warm Reset is used to clear a power down state on the codec AC Link interface.
XTL_IN	2	I	24.576-MHz crystal or oscillator input To complete the oscillator circuit use a fundamental mode crystal operating in parallel resonance and connect a 1MΩ resistor across pins 2 and 3. Choose the load capacitors (Figure 22, *C1, C2*) to suit the crystal (e.g. C1 = C2 = 33 pF for a crystal designed for a 20 pF load. Assumes that each 'Input + trace' capacitance = 7 pF) This pin may also be used as the input for an external oscillator (24.576 MHz nominal) at standard logic levels (V_{IH}, V_{IL}). This pin is only used when the codec is in Primary mode. It may be left open (NC) for any Secondary mode.
XTL_OUT	3	O	24.576-MHz crystal output Used with XTAL_IN to configure a crystal oscillator. When the codec is used with an external oscillator this pin should be left open (NC). When the codec is configured in a Secondary mode this pin is not used and may be left open (NC).
POWER SUPPLIES AND REFERENCES			
AV_{DD}	25	I	Analog supply
AV_{SS}	26	I	Analog ground
DV_{DD1}	1	I	Digital supply
DV_{DD2}	9	I	Digital supply
DV_{SS1}	4	I	Digital ground
DV_{SS2}	7	I	Digital ground
V_{REF}	27	O	Nominal 2.2-V internal reference Not intended to sink or source current. Use short traces to bypass (3.3-µF, 0.1-µF) this pin to maximize codec performance. See text.
V_{REF_OUT}	28	O	Nominal 2.2-V reference output Can source up to 5 mA of current and can be used to bias a microphone.
3D SOUND AND NO-CONNECTS (NC)			
3DN	34	O	These pins are used to complete the TI 3D Sound stereo enhancement circuit. Connect a 0.022 µF capacitor between pins 3DP and 3DN. TI 3D Sound can be turned on and off via the 3D bit (D13) in the General Purpose register, 20h. TI 3D Sound uses a fixed-depth type stereo enhancement circuit hence the 3D Control register, 22h is read-only and is not programmable. If TI 3D Sound is not needed, these pins should be left open (NC).
3DP	33		

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	29	NC	These pins are not used and should be left open (NC). For second source applications these pins may be connected to a noise-free supply or ground (*e.g.* AV_{DD} or AV_{SS}), either directly or through a capacitor.
	30		
	31		
	32		
	38		
	40		
	42		
	43		
	44		
	48		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply Voltage		6	6	V
Input Voltage		−0.3	V_{DD} +0.3	V
Junction Temperature			150	°C
Soldering Information	Vapor Phase (60 sec.)		215	°C
	Infrared (15 sec.)		220	
Storage Temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 3	±2000	V
		Pin 3	±750	
	Machine Model (MM)	All pins except 3	±200	
		Pin 3	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature $T_{MIN} \le T_A \le T_{MAX}$(1)	−40	85	°C
Analog Supply	4.2	5.5	V
Digital Supply	3	5.5	V

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $R_{\theta JA}$, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A)/R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4549B, T_{JMAX} = 150°C. The typical junction-to-ambient thermal resistance is 74°C/W for package number PT0048A.

7.4 Thermal Information

THERMAL METRIC[1]		LM4549B PT (LQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

The following specifications apply for AV_{DD} = 5 V, DV_{DD} = 3.3 V, Fs = 48 kHz, single codec configuration, (primary mode) unless otherwise noted. Limits apply for T_A= 25°C. The reference for 0 dB is 1 Vrms unless otherwise specified.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP[3]	MAX[4]	UNIT
AV_{DD}	Analog Supply		4.2		5.5	V
DV_{DD}	Digital Supply		3		5.5	V
D_{IDD}	Digital Quiescent Power Supply Current	DV_{DD} = 5 V		34		mA
		DV_{DD} = 3.3 V		19		
A_{IDD}	Analog Quiescent Power Supply Current	AV_{DD} = 5.5 V		53		mA
I_{DSD}	Digital Shutdown Current	PR543210 = 111111		19		µA
I_{ASD}	Analog Shutdown Current	PR543210 = 111111		70		µA
V_{REF}	Reference Voltage	No pullup resistor		2.16		V
PSRR	Power Supply Rejection Ratio			40		dB
ANALOG LOOPTHROUGH MODE[5]						
	Dynamic[6]	CD Input to Line Output, -60 dB Input THD+N	90	97		dB
THD	Total Harmonic Distortion	V_O = -3 dB, f = 1 kHz, R_L = 10 kΩ		0.013%	0.02%	
ANALOG INPUT SECTION						
V_{IN}	Line Input Voltage	LINE_IN, AUX, CD, VIDEO, PC_BEEP, PHONE		1		Vrms
V_{IN}	Mic Input with 20 dB Gain			0.1		Vrms
V_{IN}	Mic Input with 0 dB Gain			1		Vrms
Xtalk	Crosstalk	CD Left to Right		-95		dB
Z_{IN}	Input Impedance[6]	All Analog Inputs	10	40		kΩ
C_{IN}	Input Capacitance[6]			3.7	7	pF
	Interchannel Gain Mismatch	CD Left to Right		0.1		dB
RECORD GAIN AMPLIFIER - ADC						
A_S	Step Size	0 dB to 22.5 dB		1.5		dB
A_M	Mute Attenuation[6]			86		dB

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Loopthrough mode describes a path from an analog input through the analog mixer to an analog output
(6) These specifications are ensured by design and characterization; they are not production tested.

Electrical Characteristics (continued)

The following specifications apply for AV_{DD} = 5 V, DV_{DD} = 3.3 V, Fs = 48 kHz, single codec configuration, (primary mode) unless otherwise noted. Limits apply for T_A= 25°C. The reference for 0 dB is 1 Vrms unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP(3)	MAX(4)	UNIT
MIXER SECTION						
A_S	Step Size	+12 dB to -34.5 dB		1.5		dB
A_M	Mute Attenuation			86		dB
ANALOG TO DIGITAL CONVERTERS						
	Resolution			18		Bits
	Dynamic(6)	-60 dB Input THD+N, A-Weighted	86	90		dB
	Frequency Response	-1 dB Bandwidth		20		kHz
DIGITAL TO ANALOG CONVERTERS						
	Resolution			18		Bits
	Dynamic(6)	-60 dB Input THD+N, A-Weighted	82	89		dB
THD	Total Harmonic Distortion	V_{IN} = -3 dB, f = 1 kHz, R_L = 10 kΩ		0.01%		
	Frequency Response			20 - 21		kHz
	Group Delay(6)	Sample Frequency = 48 kHz		0.36	1	ms
	Out of Band Energy(7)			-40		dB
	Stop Band Rejection			70		dB
D_T	Discrete Tones			-96		dB
ANALOG OUTPUT SECTION						
A_S	Step Size	0 dB to -46.5 dB		1.5		dB
A_M	Mute Attenuation			86		dB
Z_{OUT}	Output Impedance(6)	All Analog Outputs		220		Ω
DIGITAL I/O(6)						
V_{IH}	High level input voltage		0.65 x DV_{DD}			V
V_{IL}	Low level input voltage				0.35 x DV_{DD}	V
V_{OH}	High level output voltage	I_O = 2.5 mA	0.90 x DV_{DD}			V
V_{OL}	Low level output voltage	I_O = 2.5 mA			0.10 x DV_{DD}	V
I_L	Input Leakage Current	AC Link inputs			±10	µA
I_L	Tri state Leakage Current	High impedance AC Link outputs			±10	µA
C_{IN}	AC-Link I/O capacitance(6)	SDout, BitClk, SDin, Sync, Reset# only		4	7.5	pF
I_{DR}	Output drive current	AC Link outputs		5		mA

(7) Out of band energy is measured from 28.8 kHz to 100 kHz relative to a 1-Vrms DAC output.

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
F_{BC}	BIT_CLK frequency			12.288		MHz
T_{BCP}	BIT_CLK period			81.4		ns
T_{CH}	BIT_CLK high	Variation of BIT_CLK duty cycle from 50%			±20%	
F_{SYNC}	SYNC frequency			48		kHz
T_{SP}	SYNC period			20.8		µs
T_{SH}	SYNC high pulse width			1.3		µs
T_{SL}	SYNC low pulse width			19.5		µs
T_{DSETUP}	Setup Time for codec data input	SDATA_OUT to falling edge of BIT_CLK	10	3.5		ns

Timing Requirements (continued)

			MIN	NOM	MAX	UNIT
T_{DHOLD}	Hold Time for codec data input(1)	Hold time of SDATA_OUT from falling edge of BIT_CLK	10	5.3		ns
T_{SSETUP}	Setup Time for codec SYNC input(1)	SYNC to falling edge of BIT_CLK	10	3.8		ns
T_{SHOLD}	Hold Time for codec SYNC input(1)	Hold time of SYNC from falling edge of BIT_CLK	10			ns
T_{CO}	Output Valid Delay	Output Delay of SDATA_IN from rising edge of BIT_CLK		5.2	15	ns
T_{RISE}	Rise Time(1)	BIT_CLK, SYNC, SDATA_IN or SDATA_OUT			6	ns
T_{FALL}	Fall Time(1)	BIT_CLK, SYNC, SDATA_IN or SDATA_OUT			6	ns
T_{RST_LOW}	RESET# active low pulse width(1)	For Cold Reset	1			µs
$T_{RST2CLK}$	RESET# inactive to BIT_CLK start up	For Cold Reset	162.8	271		ns
T_{SH}	SYNC active high pulse width(1)	For Warm Reset	1			µs
$T_{SYNC2CLK}$	SYNC inactive to BIT_CLK start up	For Warm Reset	162.8			ns
T_{S2_PDOWN}	AC Link Power Down Delay	Delay from end of Slot 2 to BIT_CLK, SDATA_IN low			1	µs
$T_{SUPPLY2RST}$	Power-On Reset	Time from minimum valid supply levels to end of Reset	1			µs
T_{SU2RST}	Setup to trailing edge of RESET#(1)	For ATE Test Mode	15			ns
T_{RST2HZ}	Rising edge of RESET# to Hi-Z(1)	For ATE Test Mode			25	ns

(1) These specifications are ensured by design and characterization; they are not production tested.

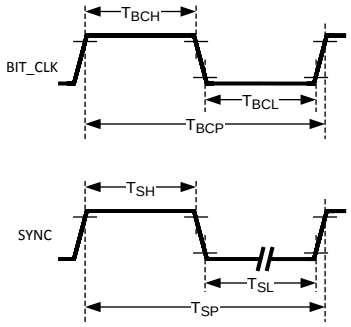


Figure 1. Clocks

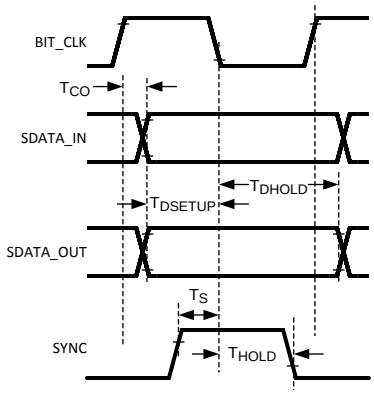


Figure 2. Data Delay, Setup and Hold

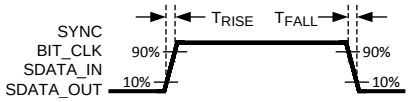


Figure 3. Digital Rise and Fall

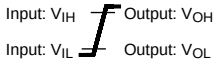


Figure 4. Legend

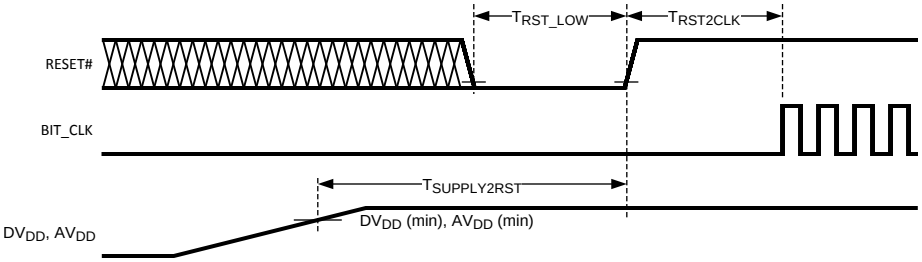


Figure 5. Power-On Reset

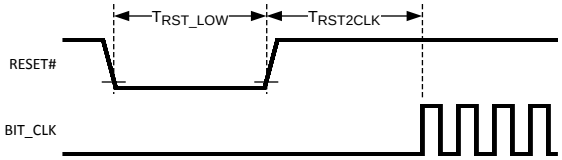


Figure 6. Cold Reset

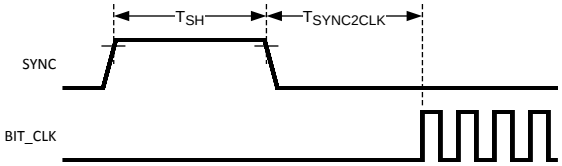


Figure 7. Warm Reset

7.7 Typical Characteristics

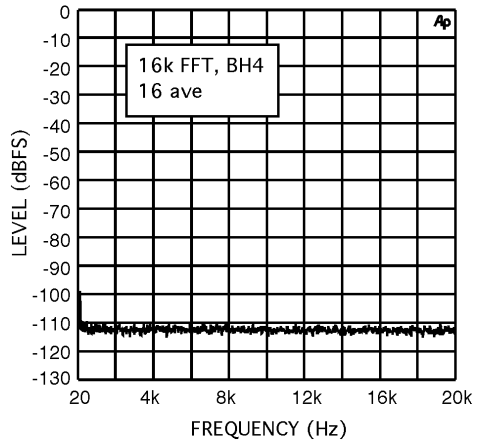


Figure 8. ADC Noise Floor

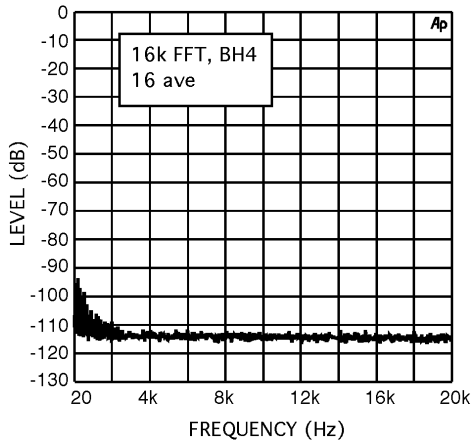


Figure 9. DAC Noise Floor

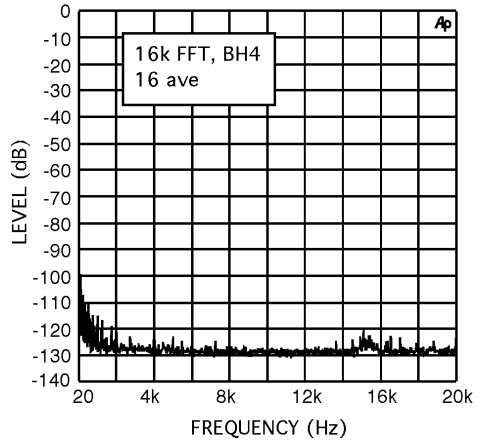


Figure 10. Line Out Noise Floor (Analog Loopthrough)

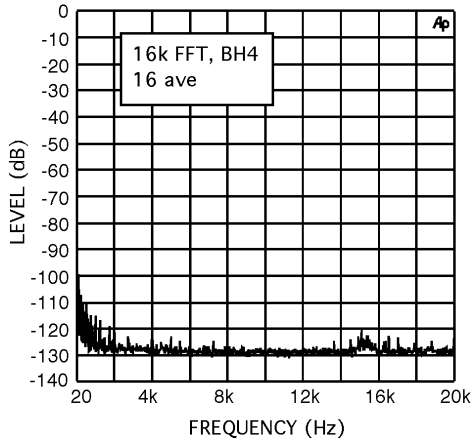


Figure 11. Line Level Out Noise Floor (Analog Loopthrough)

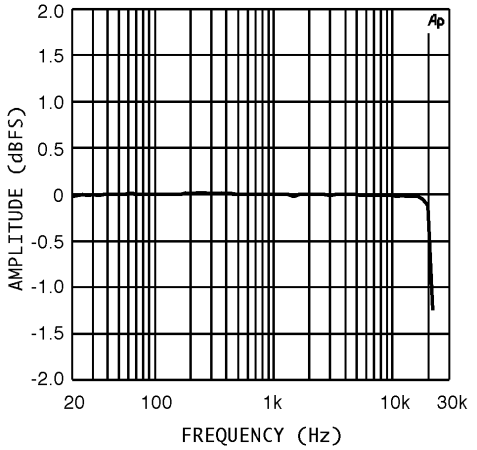


Figure 12. ADC Frequency Response

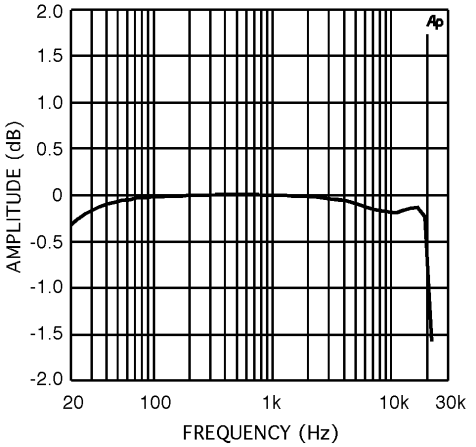


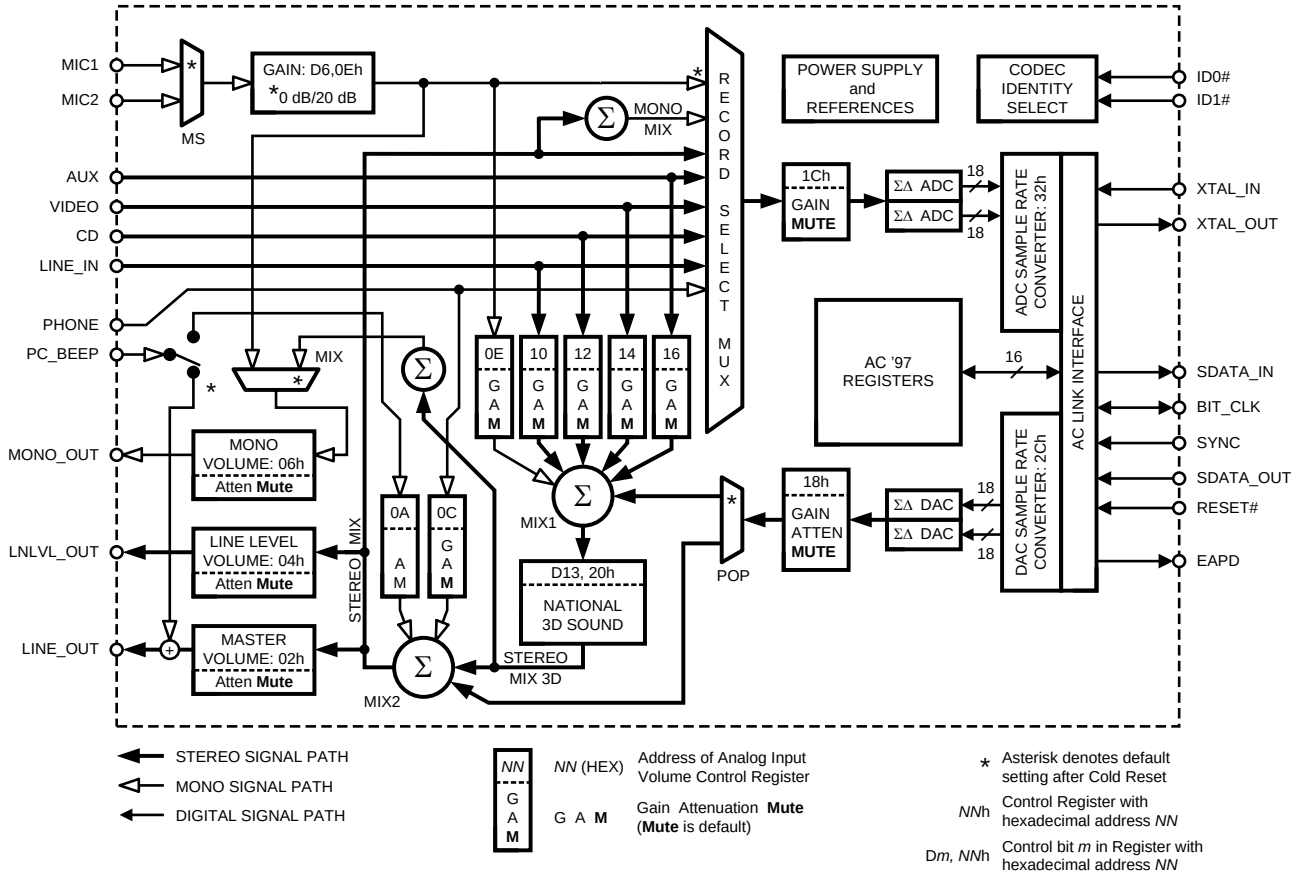
Figure 13. DAC Frequency Response

8 Detailed Description

8.1 Overview

The LM4549B codec can mix, process and convert among analog (stereo and mono) and digital (AC Link format) inputs and outputs. There are four stereo and four mono analog inputs and two stereo and one mono analog outputs. A single codec supports data streaming on two input and two output channels of the AC Link digital interface simultaneously.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ADC Inputs and Outputs

All four of the stereo analog inputs and three of the mono analog inputs can be selected for conversion by the 18-bit stereo ADC. Digital output from the left and right channel ADCs is always located in AC Link Input Frame slots 3 and 4 respectively. Input level to either ADC channel can be muted or adjusted from the Record Gain register, 1Ch. Adjustments are in 1.5 dB steps over a gain range of 0 dB to +22.5 dB and both channels mute together (mute bit D15). Input selection for the ADC is through the Record Select Mux controlled from the Record Select register, 1Ah, together with microphone selection controlled by the MS bit (bit D8) in the General Purpose register, 20h. One of the stereo inputs, CD_IN, uses a quasi-differential 3-pin interface where both stereo channel inputs are referenced to the third pin, CD_GND. CD_GND should be AC coupled to the source ground and provides common-mode feedback to cancel ground noise. It is not a DC ground. The other three stereo inputs, LINE_IN, AUX and VIDEO are 2-pin interfaces, single-ended for each stereo channel, with analog ground

Feature Description (continued)

(AV_{SS}) as the signal reference. Either of the two mono microphone inputs can be muxed to a programmable boost amplifier before selection for either channel of the ADC. The Microphone Mux is controlled by the Microphone Selection (MS) bit (D8) in the General Purpose register (20h) and the 20 dB programmable boost is enabled by the 20dB bit (D6) in register 0Eh. The mono PHONE input may also be selected for either ADC channel.

8.3.2 Analog Mixing: MIX1

Five analog inputs are available for mixing at the stereo mixer, MIX1 – all four stereo and one mono, namely the microphone input selected by MS (D8, reg 20h). Digital input to the codec can be directed to either MIX1 or to MIX2 after conversion by the 18-bit stereo DAC and level adjustment by the PCM Out Volume control register (18h). Each input to MIX1 may be muted or level adjusted using the appropriate Mixer Input Volume Register: Mic Volume (0Eh), Line_In Volume (10h), CD Volume (12h), Video Volume (14h), Aux Volume (16h) and PCM Out Volume (18h). The mono microphone input is mixed equally into left and right stereo channels but stereo mixing is orthogonal, that is, left channels are only mixed with other left channels and right with right. The left and right amplitudes of any stereo input may be adjusted independently however mute for a stereo input acts on both left and right channels.

8.3.3 DAC Mixing and 3D Processing

Control of routing the DAC output to MIX1 or MIX2 is by the POP bit (D15) in the General Purpose register, 20h. If MIX1 is selected (default, POP=0) then the DAC output is available for processing by the TI 3D Sound circuitry. If MIX2 is selected, the DAC output will bypass the 3D processing. This allows analog inputs to be enhanced by the analog 3D Sound circuitry prior to mixing with digital audio. The digital audio may then use alternative digital 3D enhancements. TI 3D Sound circuitry is enabled by the 3D bit (D13) in the General Purpose register, 20h, and is a fixed depth implementation. The 3D Control register, 22h, is therefore not programmable (read-only). The 3D Sound circuitry defaults to disabled after reset.

8.3.4 Analog Mixing: MIX2

MIX2 combines the output of MIX1 (Stereo Mix 3D) with the two mono analog inputs, PHONE and PC_BEEP; each are level-adjusted by the input control registers Phone Volume (0Ch) and PC_Beep Volume (0Ah) respectively. If selected by the POP bit (D15, reg 20h), the DAC output is also summed into MIX2.

8.3.5 Stereo Mix

The output of MIX2 is the signal, Stereo Mix. Stereo Mix is used to drive both the Line output (LINE_OUT) and the Line Level output (LNLVL_OUT) and can also be selected as the input to the ADC by the Record Select Mux. In addition, the two channels of Stereo Mix are summed to form a mono signal (Mono Mix) also selectable by the Record Select Mux as an input to either channel of the ADC.

8.3.6 Stereo Outputs

The output volume from LINE_OUT and LNLVL_OUT can be muted or adjusted by 0 dB to 45 dB in nominal 3-dB steps under the control of the output volume registers Master Volume (02h) and Line Level Volume (04h) respectively. As with the input volume registers, adjustments to the levels of the two stereo channels can be made independently but both left and right channels share a mute bit (D15).

8.3.7 Mono Output

The mono output (MONO_OUT) is driven by one of two signals selected by the MIX bit (D9) in the General Purpose register, 20h. The signal selected by default (MIX = 0) is the mono summation of the two channels of Stereo Mix 3D, the stereo output of the mixer MIX1. Setting the control bit MIX = 1, selects a microphone input, MIC1 or MIC2. The choice of microphone is controlled by the Microphone Select (MS) bit (D8) also in the General Purpose register, 20h.

Feature Description (continued)

8.3.8 Analog Loopthrough and Digital Loopback

Analog Loopthrough refers to an all-analog signal path from an analog input through the mixers to an analog output. Digital Loopback refers to a mixed-mode analog and digital signal path from an analog input through the ADC, looped-back (LPBK bit – D7, 20h) through the DAC and mixers to an analog output. This is an 18-bit digital loopback at 48 kHz, bypassing the the SRC logic even if an SRC rate other than 48 kHz is selected.

8.3.9 Resets

COLD RESET is performed when RESET# (pin 11) is pulled low for > 1 µs. It is a complete reset. All registers and internal circuits are reset to their default state. It is the only reset which clears the ATE and Vendor test modes.

WARM RESET is performed when SYNC (pin 10) is held high for > 1 µs and the codec AC Link digital interface is in power down (PR4 = 1, Power-down Control / Status register, 26h). It is used to clear PR4 and power up the AC Link digital interface but otherwise does not change the contents of any internal circuitry.

REGISTER RESET is performed when any value is written to the RESET register, 00h. It resets all registers to their default state and will modify circuit configurations accordingly but does not reset any other internal circuits.

8.3.10 Backwards Compatibility

The LM4549B is improved compared with the LM4549A. If it is required to build a board that will use either part, a 10-kΩ resistor must be added from the V_{REF} pin (pin 27) to AV_{DD} for the LM4549A. It is not required for the LM4549B. Addition of this resistor will slightly increase the temperature coefficient of the internal bandgap reference and decrease the THD performance, but overall performance will still be better than the LM4549A. The LM4549A requires that pins 1 and 9 (DV_{DD}) connect directly to a 27 nH. inductor before going to the 3.3-V digital supply and the bypass capacitors. The inductor is not required for the LM4549B and should not be used.

8.4 Device Functional Modes

8.4.1 Low Power Modes

The LM4549B provides 6 bits to control the powerdown state of internal analog and digital subsections and clocks. It also provides one bit intended to control an external analog power amplifier. These 7 bits (PR0 – PR5, EAPD) are located in the 8 MSBs of the Powerdown Control/Status register, 26h. The status of the four main analog subsections is given by the 4 LSBs in the same register, 26h.

The power-down bits are implemented in compliance with AC '97 Rev 2.1 to support the standard device power management states D0 – D3 as defined in the ACPI and PCI Bus Power Management Specification.

PR0 controls the power-down state of the ADC and associated sampling rate conversion circuitry. PR1 controls power down for the DAC and the DAC sampling rate conversion circuitry. PR2 powers down the mixer circuits (MIX1, MIX2, TI 3D Sound, Mono Out, Line Out). PR3 powers down V_{REF} in addition to all the same mixer circuits as PR2. PR4 powers down the AC Link Digital Interface – see Figure 14 for signal power-down timing. PR5 disables internal clocks but leaves the crystal oscillator and BIT_CLK running (needed for minimum Primary mode power-down dissipation in multi-codec systems). PR6 is not used. EAPD controls the External Amplifier Power-Down pin (pin 47).

After a subsection has undergone a power-down cycle, the appropriate status bit(s) in the Power-Down Control/Status register (26h) must be polled to confirm readiness. In particular the startup time of the V_{REF} circuitry depends on the value of the decoupling capacitors on pin 27 (3.3 µF, 0.1 µF in parallel is recommended).

When the AC Link Digital Interface is powered down the codec output signals SDATA_IN and BIT_CLK (Primary mode) are cleared to zero and no control data can be passed between controller and codec(s). This power-down state can be cleared in two ways: Cold Reset (RESET# = 0) or Warm Reset (SYNC = 1, no BIT_CLK). Cold Reset sets all registers back to their default values (including clearing PR4) whereas Warm Reset only clears the PR4 bit and restarts the AC Link Digital Interface leaving all register contents otherwise unaffected. For Warm

Device Functional Modes (continued)

Reset (see Figure 7), the SYNC input is used asynchronously. The LM4549B codec allows the AC Link digital interface powerdown state to be cleared immediately so that its duration can be essentially as short as T_{SH}, the Warm Reset pulse width. However for conformance with AC '97 Rev 2.1, Warm Reset should not be applied within four frame times of power down that is, the AC Link powerdown state should be allowed to last at least 82.8 µs.

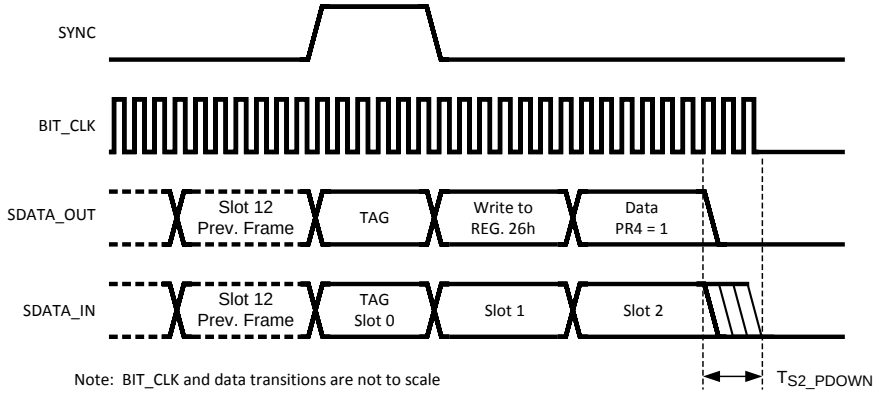


Figure 14. AC Link Power-Down Timing

8.4.2 Test Modes

AC '97 Rev 2.1 defines two test modes: ATE test mode and Vendor test mode. Cold Reset is the only way to exit either of them. The ATE test mode is activated if SDATA_OUT is sampled high by the trailing edge (zero-to-one transition) of RESET#. In ATE test mode the codec AC Link outputs SDATA_IN and BIT_CLK are configured to a high impedance state to allow tester control of the AC Link interface for controller testing. ATE test mode timing parameters are given in the *Electrical Characteristics* table. The Vendor test mode is entered if SYNC is sampled high by the zero-to-one transition of RESET#. Neither of these entry conditions can occur in normal AC Link operation but take care to avoid mistaken activation of the test modes when using non-standard controllers.

8.5 Programming

8.5.1 AC Link Serial Interface Protocol

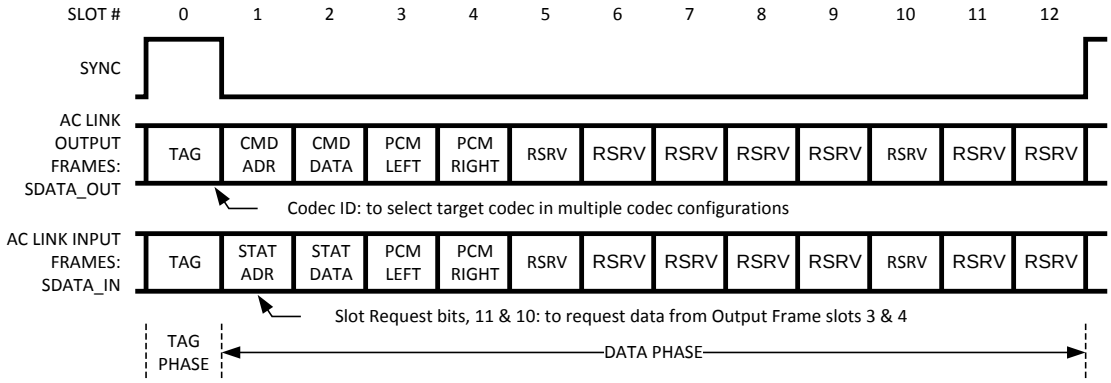


Figure 15. AC Link Bidirectional Audio Frame

Programming (continued)

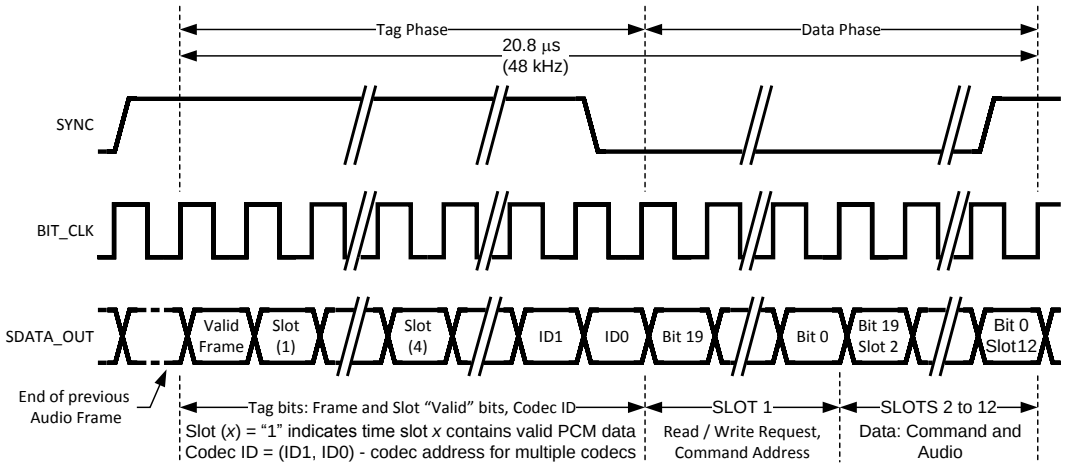


Figure 16. AC Link Output Frame

8.5.1.1 AC Link Output Frame: SDATA_OUT, Controller Output to LM4549B Input

The AC Link Output Frame carries control and PCM data to the LM4549B control registers and stereo DAC. Output Frames are carried on the SDATA_OUT signal which is an output from the AC '97 Digital Controller and an input to the LM4549B codec. As shown in Figure 15, Output Frames are constructed from thirteen time slots: one Tag Slot followed by twelve Data Slots. Each Frame consists of 256 bits with each of the twelve Data Slots containing 20 bits. Input and Output Frames are aligned to the same SYNC transition. Note that since the LM4549B is a two channel codec, it only accepts data in 4 of the twelve Data Slots – 2 for control, one each for PCM data to the left and right channel DACs. Data Slot 3 & 4 are used to stream data to the stereo DAC for all modes selected by the Identity pins ID1#, ID0#.

A new Output Frame is signaled with a low-to-high transition of SYNC. SYNC should be clocked from the controller on a rising edge of BIT_CLK and, as shown in Figure 16 and Figure 17, the first tag bit in the Frame ("Valid Frame") should be clocked from the controller by the next rising edge of BIT_CLK and sampled by the LM4549B on the following falling edge. The AC '97 Controller should always clock data to SDATA_OUT on a rising edge of BIT_CLK and the LM4549B always samples SDATA_OUT on the next falling edge. SYNC is sampled with the falling edge of BIT_CLK.

The LM4549B checks each Frame to ensure 256 bits are received. If a new Frame is detected (a low-to-high transition on SYNC) before 256 bits are received from the old Frame then the new Frame is ignored *i.e.* the data on SDATA_OUT is discarded until a valid new Frame is detected.

The LM4549B expects to receive data MSB first, in an MSB justified format.

8.5.1.1.1 SDATA_OUT: Slot 0 – Tag Phase

The first bit of Slot 0 is designated the "Valid Frame" bit. If this bit is 1, it indicates that the current Output Frame contains at least one slot of valid data and the LM4549B will check further tag bits for valid data in the expected Data Slots. With the codec in Primary mode, a controller will indicate valid data in a slot by setting the associated tag bit equal to 1. Since it is a two channel codec the LM4549B can only receive data from four slots in a given frame and so only checks the valid-data bits for 4 slots. In Primary mode these tag bits are for: slot 1 (Command Address), slot 2 (Command Data), slot 3 (PCM data for left DAC) and slot 4 (PCM data for right DAC).

The last two bits in the Tag contain the Codec ID used to select the target codec to receive the frame in multiple codec systems. When the frame is being sent to a codec in one of the Secondary modes the controller does not use bits 14 and 13 to indicate valid Command Address and Data in slots 1 and 2. Instead, this role is performed by the Codec ID bits – operation of the Extended AC Link assumes that the controller would not access a secondary codec unless it was providing valid Command Address and/or Data. When in one of the secondary modes the LM4549B only checks the tag bits for the Codec ID and for valid data in the two audio data slots 3 & 4.

Programming (continued)

When sending an Output Frame to a Secondary mode codec, a controller should set tag bits 14 and 13 to zero.

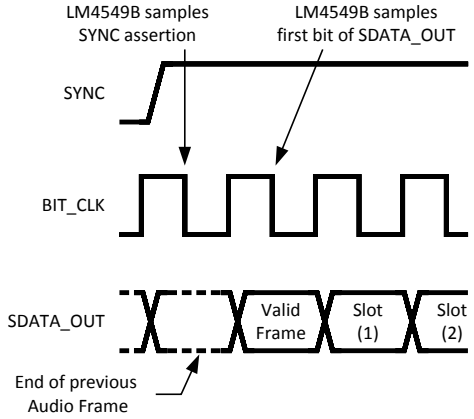


Figure 17. Start of AC Link Output Frame

Table 1. Slot 0, Output Frame

Bit	Description	Comment	
15	Valid Frame	1 =	Valid data in at least one slot.
14	Control register address	1 =	Valid Control Address in Slot 1 (Primary codec only)
13	Control register data	1 =	Valid Control Data in Slot 2 (Primary codec only)
12	Left DAC data in Slot 3	1 =	Valid PCM Data in Slot 3 (Primary & all Secondary modes)
11	Right DAC data in Slot 4	1 =	Valid PCM Data in Slot 4 (Primary & all Secondary modes)
10:2	Not Used	Controller should stuff these slots with “0”s	
1,0	Codec ID (ID1, ID0)	The codec ID is used in a multi-codec system to identify the target Secondary codec for the Control Register address and/or data sent in the Output Frame	

8.5.1.1.2 SDATA_OUT: Slot 1 – Read/Write, Control Address

Slot 1 is used by a controller to indicate both the address of a target register in the LM4549B and whether the access operation is a register read or register write. The MSB of slot 1 (bit 19) is set to 1 to indicate that the current access operation is 'read'. Bits 18 through 12 are used to specify the 7-bit register address of the read or write operation. The least significant twelve bits are reserved and should be stuffed with zeros by the AC '97 controller.

Table 2. Slot 1, Output Frame

Bits	Description	Comment
19	Read/Write	1 = Read 0 = Write
18:12	Register Address	Identifies the Status/Command register for read/write
11:0	Reserved	Controller should set to "0"

8.5.1.1.3 SDATA_OUT: Slot 2 – Control Data

Slot 2 is used to transmit 16-bit control data to the LM4549B when the access operation is 'write'. The least significant four bits should be stuffed with zeros by the AC '97 controller. If the access operation is a register read, the entire slot, bits 19 through 0 should be stuffed with zeros.

Table 3. Slot 2, Output Frame

Bits	Description	Comment
19:4	Control Register Write Data	Controller should stuff with zeros if operation is “read”
3:0	Reserved	Set to "0"

8.5.1.1.4 SDATA_OUT: Slots 3 & 4 – PCM Playback Left/Right Channels

Slots 3 and 4 are 20-bit fields used to transmit PCM data to the left and right channels of the stereo DAC for all codec Primary and Secondary modes. Any unused bits should be stuffed with zeros. The LM4549B DACs have 18-bit resolution and will therefore use the 18 MSBs of the 20-bit PCM data (MSB justified).

Table 4. Slots 3 & 4, Output Frame

Bits	Description	Comment
19:0	PCM DAC Data (Left /Right Channels)	Slots used to stream data to DACs for all Primary or Secondary modes. Set unused bits to "0"

8.5.1.1.5 SDATA_OUT: Slots 5 to 12 – Reserved

These slots are not used by the LM4549B and should all be stuffed with zeros by the AC '97 Controller.

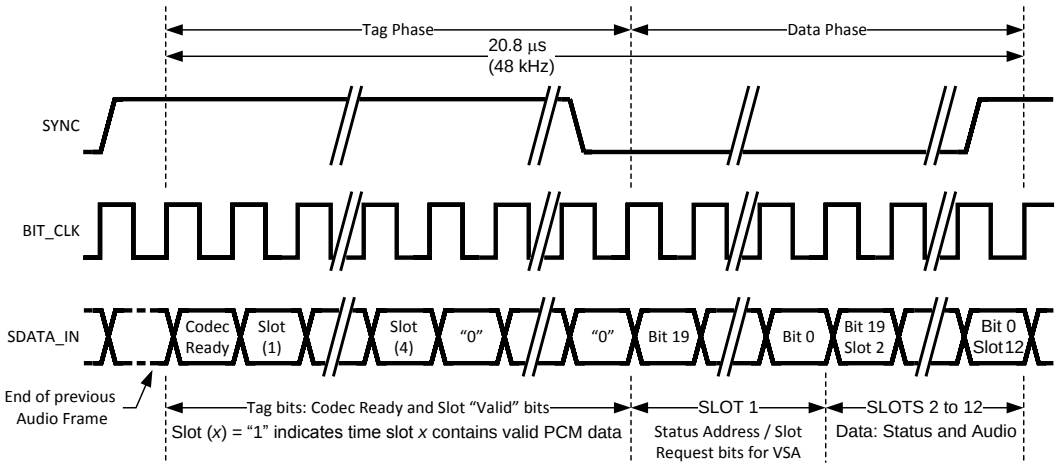


Figure 18. AC Link Input Frame

8.5.1.2 AC Link Input Frame: SDATA_IN, Controller Input from LM4549B Output

The AC Link Input Frame contains status and PCM data from the LM4549B control registers and stereo ADC. Input Frames are carried on the SDATA_IN signal which is an input to the AC '97 Digital Audio Controller and an output from the LM4549B codec. As shown in Figure 15, Input Frames are constructed from thirteen time slots: one Tag Slot followed by twelve Data Slots. The Tag Slot, Slot 0, contains 16 bits of which 5 are used by the LM4549B. One is used to indicate that the AC Link interface is fully operational and the other 4 to indicate the validity of the data in the four of the twelve following Data Slots that are used by the LM4549B. Each Frame consists of 256 bits with each of the twelve data slots containing 20 bits.

A new Input Frame is signaled with a low-to-high transition of SYNC. SYNC should be clocked from the controller on a rising edge of BIT_CLK and, as shown in Figure 18 and Figure 19, the first tag bit in the Frame (“Codec Ready”) is clocked from the LM4549B by the next rising edge of BIT_CLK. The LM4549B always clocks data to SDATA_IN on a rising edge of BIT_CLK and the controller is expected to sample SDATA_IN on the next falling edge. The LM4549B samples SYNC on the falling edge of BIT_CLK.

Input and Output Frames are aligned to the same SYNC transition.

The LM4549B checks each Frame to ensure 256 bits are received. If a new Frame is detected (a low-to-high transition on SYNC) before 256 bits are received from an old Frame then the new Frame is ignored, that is, no valid data is sent on SDATA_IN until a valid new Frame is detected.

The LM4549B transmits data MSB first, in a MSB justified format. All reserved bits and slots are stuffed with 0s by the LM4549B.

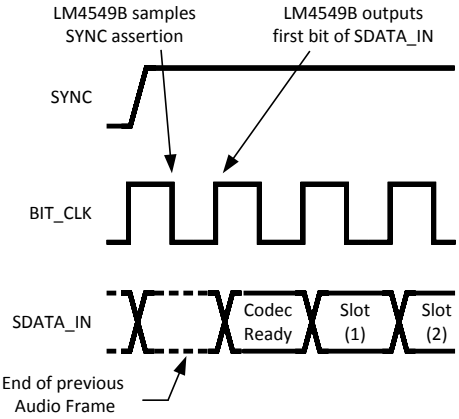


Figure 19. Start of AC Link Input Frame

8.5.1.2.1 SDATA_IN: Slot 0 – Codec/Slot Status Bits

The first bit (bit 15, "Codec Ready") of slot 0 in the AC Link Input Frame indicates when theAC Link digital interface of the codec and the status and control registers are fully operational. The digital controller is then able to read the LSBs from the Power-Down Control/Stat register (26h) to determine the status of the four main analog subsections. It is important to check the status of these subsections after Initialization, Cold Reset, or the use of the power-down modes in order to minimize the risk of distorting analog signals passed before the subsections are ready.

The 4 bits 14, 13, 12 and 11 indicate that the data in slots 1, 2, 3 and 4, respectively, are valid.

Table 5. Slot 0, Input Frame

Bit	Description	Comment	
15	Codec Ready Bit	1 =	AC Link Interface Ready
14	Slot 1 data valid	1 =	Valid Status Address or Slot Request
13	Slot 2 data valid	1 =	Valid Status Data
12	Slot 3 data valid	1 =	Valid PCM Data (Left ADC)
11	Slot 4 data valid	1 =	Valid PCM Data (Right ADC)

8.5.1.2.2 SDATA_IN: Slot 1 – Status Address / Slot Request Bits

This slot echoes (in bits 18 – 12) the 7-bit address of the codec control/status register received from the controller as part of a read-request in the previous frame. If no read-request was received, the codec stuffs these bits with zeros.

Bits 11, 10 are Slot Request bits that support the Variable Rate Audio (VRA) capabilities of the LM4549B. For all codec Primary and Secondary modes, the left and right channels of the DAC take PCM data from slots 3 and 4 in the Output Frame respectively. The codec uses bits 11 and 10 to request DAC data from these two slots. If bits 11 and 10 are set to 0, the controller should respond with valid PCM data in slots 3 and 4 of the next Output Frame. If bits 11 and 10 are set to 1, the controller should not send data.

The codec has full control of the slot request bits. By default, data is requested in every frame, corresponding to a sample rate equal to the frame rate (SYNC frequency) – 48 kHz when XTAL_IN = 24.576 MHz. To send samples at a rate below the frame rate, a controller should set VRA = 1 (bit 0 in the Extended Audio Control/Status register, 2Ah) and program the desired rate into the PCM DAC Rate register, 2Ch. Both DAC channels operate at the same sample rate. Values for common sample rates are given in the *Register Maps* section (Sample Rate Control Registers, 2Ch, 32h) but any rate between 4 kHz and 48 kHz (to a resolution of 1

Hz) is supported. Slot Requests from the LM4549B are issued completely deterministically. For example if a sample rate of 8000 Hz is programmed into 2Ch then the LM4549B will always issue a slot request in every sixth frame. A frequency of 9600 Hz will result in a request every fifth frame while a frequency of 8800 Hz will cause slot requests to be spaced alternately five and six frames apart. This determinism makes it easy to plan task scheduling on a system controller and simplifies application software development.

The LM4549B will ignore data in Output Frame slots that do not follow an Input Frame with a Slot Request. For example, if the LM4549B is expecting data at a 8000 Hz rate yet the AC '97 Digital Audio Controller continues to send data at 48000 Hz, then only those one-in-six audio samples that follow a Slot Request will be used by the DAC. The rest will be discarded.

Bits 9 – 2 are request bits for slots not used by the LM4549B and are stuffed with zeros. Bits 1 and 0 are reserved and are also stuffed with zeros.

Table 6. Slot 1, Input Frame

Bits	Description	Comment	
19	Reserved	Stuffed with 0 by LM4549B	
18:12	Status Register Index	Echo of the requested Status Register address.	
11	Slot 3 Request bit (For left DAC PCM data)	0 =	Controller should send valid data in Slot 3 of the next Output Frame.
		1 =	Controller should not send Slot 3 data.
10	Slot 4 Request bit (For right DAC PCM data)	0 =	Controller should send valid data in Slot 4 of the next Output Frame.
		1 =	Controller should not send Slot 4 data.
9:2	Unused Slot Request bits	Stuffed with 0s by LM4549B	
1,0	Reserved	Stuffed with 0s by LM4549B	

8.5.1.2.3 SDATA_IN: Slot 2 – Status Data

This slot returns 16-bit status data read from a codec control and status register. The codec sends the data in the frame following a read-request by the controller (bit 15, slot 1 of the Output Frame). If no read-request was made in the previous frame the codec will stuff this slot with zeros.

Table 7. Slot 2, Input Frame

Bits	Description	Comment
19:4	Status Data	Data read from a codec control/status register. Stuffed with 0s if no read-request in previous frame.
3:0	Reserved	Stuffed with 0s by LM4549B

8.5.1.2.4 SDATA_IN: Slot 3 – PCM Record Left Channel

This slot contains sampled data from the left channel of the stereo ADC. The signal to be digitized is selected using the Record Select register (1Ah) and subsequently routed through the Record Select Mux and the Record Gain amplifier to the ADC.

This is a 20-bit slot and the digitized 18-bit PCM data is transmitted in an MSB justified format. The remaining 2 LSBs are stuffed with zeros.

Table 8. Slot 3, Input Frame

Bits	Description	Comment
19:2	PCM Record Left Channel data	18-bit PCM sample from left ADC
1:0	Reserved	Stuffed with 0s by LM4549B

8.5.1.2.5 SDATA_IN: Slot 4 – PCM Record Right Channel

This slot contains sampled data from the right channel of the stereo ADC. The signal to be digitized is selected using the Record Select register (1Ah) and subsequently routed through the Record Select Mux and the Record Gain amplifier to the ADC.

This is a 20-bit slot and the digitized 18-bit PCM data is transmitted in an MSB justified format. The remaining 2 LSBs are stuffed with zeros.

Table 9. Slot 4, Input Frame

Bits	Description	Comment
19:2	PCM Record Right Channel data	18-bit PCM sample from right ADC
1:0	Reserved	Stuffed with "0"s by LM4549B

8.5.1.2.6 SDATA_IN: Slots 5 to 12 – Reserved

Slots 5 – 12 of the AC Link Input Frame are not used for data by the LM4549B and are always stuffed with zeros.

8.5.2 Multiple Codecs

8.5.2.1 Extended AC Link

Up to four codecs can be supported on the extended AC Link. These multiple codec implementations should run off a common BIT_CLK generated by the Primary Codec. All codecs share the AC '97 Digital Controller output signals, SYNC, SDATA_OUT, and RESET#. Each codec, however, supplies its own SDATA_IN signal back to the controller, with the result that the controller requires one dedicated input pin per codec. (Figure 20).

By definition there can be one Primary Codec and up to three Secondary Codecs on an extended AC Link. The Primary Codec has a Codec Identity = (ID1, ID0) = ID = 00 while Secondary Codecs may have identities equal to 01, 10 or 11. The Codec Identity is used as a chip select function. This allows the Command and Status registers in any of the codecs to be individually addressed although the access mechanism for Secondary Codecs differs slightly from that for a Primary.

The Identity control pins, ID1#, ID0# (pins 46 and 45) are internally pulled up to DV_{DD}. The Codec may therefore be configured as 'Primary' either by leaving ID1#, ID0# open (NC) or by strapping them externally to DV_{DD} (Digital Supply).

The difference between Primary and Secondary codec modes is in their timing source and in the Tag Bit handling in Output Frames for Command/Status register access. For a timing source, a Primary codec divides down by 2 the frequency of the signal on XTAL_IN and also generates this as the BIT_CLK output for the use of the controller and any Secondary codecs. Secondary codecs use BIT_CLK as an input and as their timing source and do not use XTAL_IN or XTAL_OUT. The use of Tag Bits is described below.

8.5.2.2 Secondary Codec Register Access

For Secondary Codec access, the controller must set the tag bits for Command Address and Data in the Output Frame as invalid (that is, equal to 0). The Command Address and Data tag bits are in slot 0, bits 14 and 13 and Output Frames are those in the SDATA_OUT signal from controller to codec. The controller must also place the non-zero value (01, 10, or 11) corresponding to the Identity (ID1, ID0) of the target Secondary Codec into the Codec ID field (slot 0, bits 1 and 0) in that same Output Frame. The value set in the Codec ID field determines which of the three possible Secondary Codecs is accessed. Unlike a Primary Codec, a Secondary Codec will disregard the Command Address and Data tag bits when there is a match between the 2-bit Codec ID value (slot 0, bits 1 and 0) and the Codec Identity (ID1, ID0). Instead it uses the Codec-ID/Identity match to indicate that the Command Address in slot 1 and (if a *write*) the Command Data in slot 2 are valid.

When reading from a Secondary Codec, the controller must send the correct Codec ID bits (that is, the target Codec Identity in slot 0, bits 1 and 0) along with the read-request bit (slot 1, bit 19) and target register address (slot 1, bits 18 – 12). To write to a Secondary Codec, a controller must send the correct Codec ID bits when slot 1 contains a valid target register address and *write* indicator bit and slot 2 contains valid target register data. A write operation is only valid if the register address and data are both valid and sent within the same frame. When accessing the Primary Codec, the Codec ID bits are cleared and the tag bits 14 and 13 resume their role indicating the validity of Command Address and Data in slots 1 and 2.

The use of the tag bits in Input Frames (carried by the SDATA_IN signal) is the same for Primary and Secondary Codecs.

The Codec Identity is determined by the inverting input pins ID1#, ID0# (pins 46 and 45) and can be read as the value of the ID1, ID0 bits (D15, D14) in the Extended Audio ID register, 28h of the target codec.

Slots in the AC Link Output Frame are always mapped to carry data to the left DAC channel in slot 3 and data to the right DAC channel in slot 4. Similarly, slots in AC Link Input Frames are always mapped such that PCM data from the left ADC channel is carried by slot 3 and PCM data from the right ADC channel by slot 4. Output Frames are those carried by the SDATA_OUT signal from the controller to the codec while Input Frames are those carried by the SDATA_IN signal from the codec to the controller.

8.5.2.2.1 Slot 0: TAG bits in Output Frames (Controller to Codec)

Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Valid Frame	Slot 1 Valid	Slot 2 Valid	Slot 3 Valid	Slot 4 Valid	X	X	X	X	X	X	X	X	X	ID1	ID0

8.5.2.2.2 Extended Audio ID register (28h): Support for Multiple Codecs

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	X001h

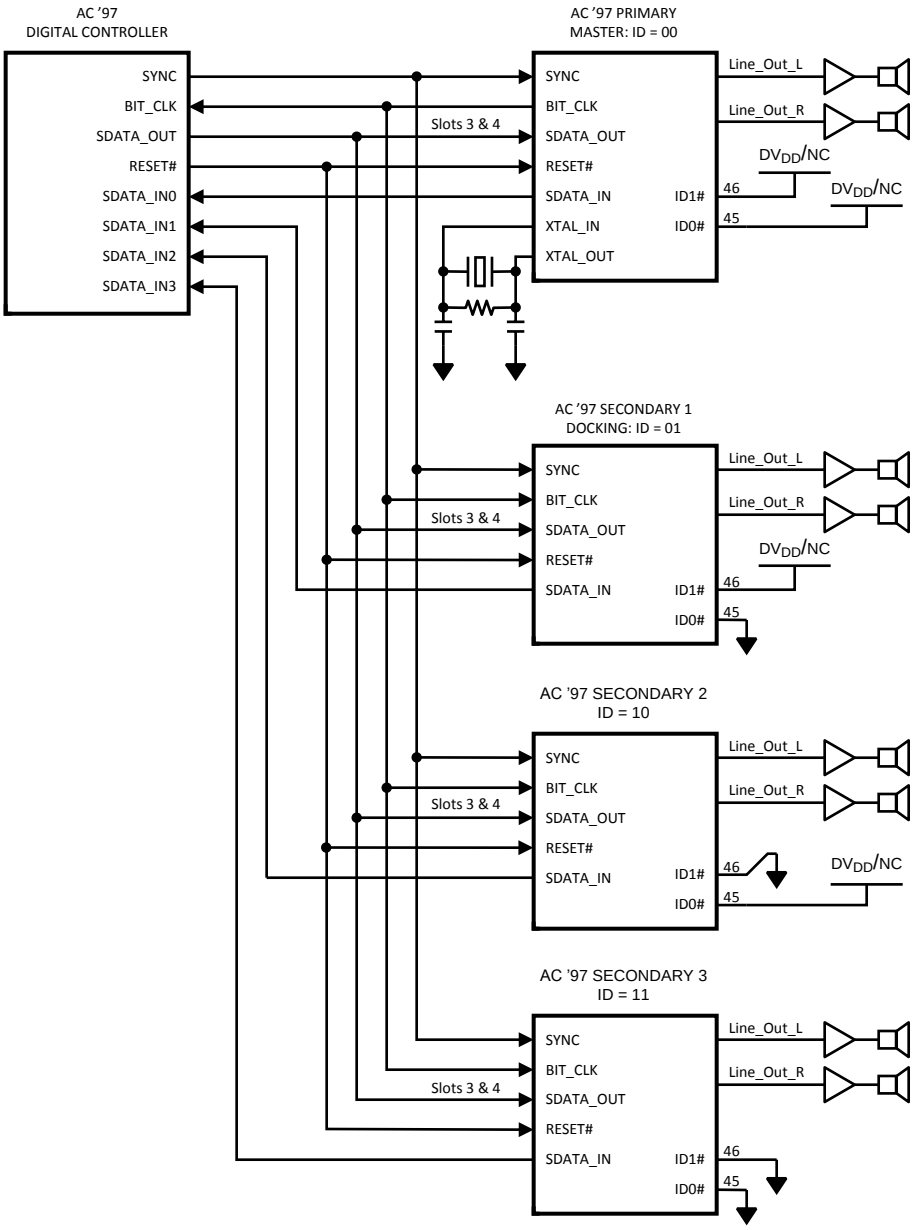


Figure 20. Multiple Codecs using Extended AC Link

8.6 Register Maps

Table 10. LM4549B Register Map

	REG	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
	00h	Reset	X	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0D40h
Output Volume	02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
	04h	Line Level Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
	06h	Mono Volume	Mute	X	X	X	X	X	X	X	X	X	MM5	MM4	MM3	MM2	MM1	MM0	8000h
Input Volume	0Ah	PC_Beep Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
	0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
	0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
	10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
	18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
ADC Sources	1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
	1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
	20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
	22h	3D Control (Read Only)	X	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0101h
X	24h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
	26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
	28h	Extended Audio ID	ID1	ID0	X	X	X	X	0	0	0	0	X	X	0	X	0	VRA	X001h
	2Ah	Extended Audio Control/Status	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h
	2Ch	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
	32h	PCM ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
X	5Ah	Vendor Reserved 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
X	74h	Vendor Reserved 2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
X	7Ah	Vendor Reserved 3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
	7Ch	Vendor ID1	0	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	4E53h
	7Eh	Vendor ID2	0	1	0	0	0	0	1	1	0	1	0	0	1	0	0	1	4349h

8.6.1 Reset Register (00h)

Writing any value to this register causes a Register Reset which changes all registers back to their default values. If a read is performed on this register, the LM4549B will return a value of 0D40h. This value can be interpreted in accordance with the AC '97 Specification to indicate that TI 3D Sound is implemented and 18-bit data is supported for both the ADCs and DACs.

8.6.2 Master Volume Register (02h)

This output register allows the output level from either channel of the stereo LINE_OUT to be muted or attenuated over the range 0 dB – 46.5 dB in nominal 1.5-dB steps. There are 6 bits of volume control for each channel and both stereo channels can be individually attenuated. The mute bit (D15) acts simultaneously on both stereo channels of LINE_OUT. The AC'97 specification states that *support for the MSB of the level is optional*. All six bits may be written to the register, but if the MSB is a 1, the MSB is ignored and the register will be set to 0 11111. This will be the value when the register is read, allowing the software driver to detect whether the MSB is supported or not.

Table 11. Master Volume Register (02h)

Mute	Mx5:Mx0	Function
0	0 00000	0 dB attenuation
0	0 11111	46.5 dB attenuation
0	1 xxxxx	As Written
0	0 11111	As read back
1	X XXXXX	mute(1)
Default: 8000h		

(1) Default settings

8.6.3 Line Level Volume Register (04h)

This output register allows the level from both channels of LNLVL_OUT to be muted or individually attenuated over the range 0 dB to –46.5 dB in nominal 1.5-dB steps. There are 6 bits of volume control for each channel plus one mute bit. The mute bit (D15) acts on both channels. Operation of this register and LNLVL_OUT matches that of the Master Volume register and the LINE_OUT output.

8.6.4 Mono Volume Register (06h)

This output register allows the level from MONO_OUT to be muted or attenuated over the range 0 dB – 46.5 dB in nominal 1.5-dB steps. There are 6 bits of volume control and one mute bit (D15). All 6 bits may be written to the register, but if the MSB is a 1, the MSB is ignored and the register will be set to 0 11111. This will be the value when the register is read, allowing the software driver to detect whether the MSB is supported or not.

Table 12. Mono Volume Register (06h) Functions

Mute	MM5:MM0	Function
0	0 00000	0 dB attenuation
0	0 11111	46.5 dB attenuation
0	1 xxxxx	As written
0	0 11111	As read back
1	X XXXXX	mute(1)
Default: 8000h		

(1) \Default settings

8.6.5 PC Beep Volume Register (0Ah)

This input register adjusts the level of the mono PC_BEEP input to the stereo mixer MIX2 where it is summed equally into both channels of the Stereo Mix signal. PC_BEEP can be both muted and attenuated over a range of 0 dB to –45 dB in nominal 3 dB-steps. Note that the default setting for the PC_Beep Volume register is 0 dB attenuation rather than mute.

Table 13. PC Beep Volume Register (0Ah) Functions

Mute	PV3:PV0	Function
0	0000	0 dB attenuation(1)
0	1111	45 dB attenuation
1	XXXX	mute(1)
Default: 0000h		

(1) Default settings

8.6.6 Mixer Input Volume Registers (Index 0Ch - 18h)

These input registers adjust the volume levels into the stereo mixers MIX1 and MIX2. Each channel may be adjusted over a range of +12 dB gain to –34.5 dB attenuation in 1.5-dB steps. For stereo ports, volumes of the left and right channels can be independently adjusted. Muting a given port is accomplished by setting the MSB to 1. Setting the MSB to 1 for stereo ports mutes both the left and right channels. The Mic Volume register (0Eh) controls an additional 20 dB boost for the selected microphone input by setting the 20dB bit (D6).

Table 14. Mixer Input Volume Registers (Index 0Ch - 18h) Functions

Mute	Gx4:Gx0	Function
0	0 0000	+12 dB gain
0	0 1000	0 dB gain
0	1 1111	–34.5 dB attenuation
1	X XXXX	mute(1)
Default:	8008h (mono registers) 8808h (stereo registers)	

(1) Default settings

8.6.7 Record Select Register (1Ah)

This register independently controls the sources for the right and left channels of the stereo ADC. The default value of 0000h corresponds to selecting the (mono) Mic input for both channels.

Table 15. Record Select Register (1Ah) Functions

SL2:SL0	Source for Left Channel ADC
0	Mic input(1)
1	CD input (L)
2	VIDEO input (L)
3	AUX input (L)
4	LINE_IN input (L)
5	Stereo Mix (L)
6	Mono Mix
7	PHONE input

(1) Default settings

SR2:SR0	Source for Right Channel ADC
0	Mic input(1)
1	CD input (R)
2	VIDEO input (R)
3	AUX input (R)
4	LINE_IN input (R)
5	Stereo Mix (R)
6	Mono Mix

(1) Default settings

SR2:SR0	Source for Right Channel ADC
7	PHONE input
Default: 0000h	

8.6.8 Record Gain Register (1Ch)

This register controls the input levels for both channels of the stereo ADC. The inputs come from the Record Select Mux and are selected via the Record Select Control register, 1Ah. The gain of each channel can be individually programmed from 0dB to +22.5 dB in 1.5-dB steps. Both channels can also be muted by setting the MSB to 1.

Table 16. Record Gain Register (1Ch) Functions

Mute	Gx3:Gx0	Function
0	1111	22.5 dB gain
0	0000	0 dB gain
1	XXXX	mute(1)
Default: 8000h		

(1) Default settings

8.6.9 General Purpose Register (20h)

This register controls many miscellaneous functions implemented on the LM4549B. The miscellaneous control bits include POP which allows the DAC output to bypass the TI 3D Sound circuitry, 3D which enables or disables the TI 3D Sound circuitry, MIX which selects the MONO_OUT source, MS which controls the Microphone Selection mux and LPBK which connects the output of the stereo ADC to the input of the stereo DAC. LPBK provides a mixed-mode analog and digital loopback path between analog inputs and analog outputs. This is an 18 bit digital loopback at 48 kHz, bypassing the SRC logic, even if a sample rate other than 48 kHz is selected.

Table 17. General Purpose Register (20h) Functions

BIT	Function		
POP	PCM Out Path:	0(1) =	3D allowed
		1 =	3D bypassed
3D	TI 3D Sound:	0(1) =	off
		1 =	on
MIX	Mono output select:	0(1) =	Mix
		1 =	Mic
MS	Mic select:	0(1) =	MIC1
		1 =	MIC2
LPBK	ADC/DAC Loopback:	0(1) =	No Loopback
		1 =	Loopback
Default: 0000h			

(1) Default settings

8.6.10 3D Control Register (22h)

This read-only (0101h) register indicates, in accordance with the AC '97 Rev 2.1 Specification, the fixed depth and center characteristics of the TI 3D Sound stereo enhancement.

8.6.11 Power-Down Control / Status Register (26h)

This read/write register is used both to monitor subsystem readiness and also to program the LM4549B power-down states. The 4 LSBs indicate status and 7 of the 8 MSBs control power down.

The 4 LSBs of this register indicate the status of the 4 audio subsections of the codec: Reference voltage, Analog mixers and amplifiers, DAC section, ADC section. When the "Codec Ready" indicator bit in the AC Link Input Frame (SDATA_IN: slot 0, bit 15) is a "1", it indicates that the AC Link and AC '97 registers are in a fully operational state and that control and status information can be transferred. It does NOT indicate that the codec is ready to send or receive audio PCM data or to pass signals through the analog I/O and mixers. To determine that readiness, the Controller must check that the 4 LSBs of this register are set to 1 indicating that the appropriate audio subsections are ready.

The power-down bits PR0 – PR5 control internal subsections of the codec. They are implemented in compliance with AC '97 Rev 2.1 to support the standard device power management states D0 – D3 as defined in the ACPI and PCI Bus Power Management Specification.

PR0 controls the powerdown state of the ADC and associated sampling rate conversion circuitry. PR1 controls power down for the DAC and the DAC sampling rate conversion circuitry. PR2 powers down the mixer circuits (MIX1, MIX2, TI 3D Sound, Mono Out, Line Out). PR3 powers down V_{REF} in addition to all the same mixer circuits as PR2. PR4 powers down the AC Link digital interface – see Figure 14 for signal power-down timing. PR5 disables internal clocks. PR6 is not used. EAPD controls the External Amplifier Power Down bit.

Table 18. Power-Down Control (26h)

BIT#	BIT	Function: Status	
0	ADC	1 =	ADC section ready to transmit data
1	DAC	1 =	DAC section ready to accept data
2	ANL	1 =	Analog mixers ready
3	REF	1 =	V_{REF} is up to nominal level

Table 19. Status Register (26h)

BIT#	BIT	Function: Powerdown	
8	PR0	1 =	Power-down ADCs and Record Select Mux
9	PR1	1 =	Power-down DACs
10	PR2	1 =	Power-down Analog Mixer (V_{REF} still on)
11	PR3	1 =	Power-down Analog Mixer (V_{REF} off)
12	PR4	1 =	Power-down AC Link digital interface (BIT_CLK off)
13	PR5	1 =	Disable Internal Clock
14	PR6	Not Used	
15	EAPD	External Amplifier Power Down	
		0(1) =	Set EAPD Pin to 0 (pin 47)
Default: 000Fh If ready; otherwise 000Xh			

(1) Default settings

8.6.12 Extended Audio ID Register (28h)

This read-only (X001h) register identifies which AC '97 Extended Audio features are supported. The LM4549B features VRA (Variable Rate Audio) and ID1, ID0 (Multiple Codec support). VRA is indicated by a 1 in bit 0. The two MSBs, ID1 and ID0, show the current Codec Identity as defined by the Identity pins ID1#, ID0#. Note that the external logic connections to ID1#, ID0# (pins 46 and 45) are inverse in polarity to the value of the Codec Identity (ID1, ID0) held in bits D15, D14. Codec mode selections are shown in the table below.

Table 20. Extended Audio ID Register (28h) Codec Identity Mode

Pin 46 (ID1#)	Pin 45 (ID0#)	D15,28h (ID1)	D14,28h (ID0)	Codec Identity Mode
NC/DV_{DD}	NC/DV_{DD}	0	0	Primary
NC/DV_{DD}	GND	0	1	Secondary 1
GND	NC/DV_{DD}	1	0	Secondary 2
GND	GND	1	1	Secondary 3

8.6.13 Extended Audio Status/Control register (2Ah)

This read/write register provides status and control of the variable sample rate capabilities in the LM4549B. Setting the LSB of this register to 1 enables Variable Rate Audio (VRA) mode and allows DAC and ADC sample rates to be programmed through registers 2Ch and 32h respectively.

Table 21. Extended Audio Status/Control register (2Ah) Functions

BIT	Function	
VRA	0[1] =	VRA off (Frame-rate sampling)
	1 =	VRA on
Default: 0000h		

(1) Default settings

8.6.14 Sample Rate Control Registers (2Ch, 32h)

These read/write registers are used to set the sample rate for the left and right channels of the DAC (PCM DAC Rate, 2Ch) and the ADC (PCM ADC Rate, 32h). When Variable Rate Audio is enabled via bit 0 of the Extended Audio Control/Status register (2Ah), the sample rates can be programmed, in 1 Hz increments, to be any value from 4 kHz to 48 kHz. The value required is the hexadecimal representation of the desired sample rate, for example 8000_{10} = 1F40h. Below is a list of the most common sample rates and the corresponding register (hex) values.

Table 22. Common Sample Rates

SR15:SR0	Sample Rate (Hz)
1F40h	8000
2B11h	11025
3E80h	16000
5622h	22050
AC44h	44100
BB80h[1]	48000[1]

(1) Default settings

8.6.15 Vendor ID Registers (7Ch, 7Eh)

These two read-only (4E53h, 4349h) registers contain TI's Vendor ID and TI's LM45xx codec version designation. The first 24 bits (4Eh, 53h, 43h) represent the three ASCII characters “NSC” which is TI's Vendor ID for Microsoft's Plug and Play. The last 8 bits are the two binary coded decimal characters, *4, 9* and identify the codec to be an LM45*49*B.

8.6.16 Reserved Registers

Do not write to reserved registers. In particular, do not write to registers 24h, 5Ah, 74h and 7Ah. All registers not listed in the LM4549B Register Map are reserved. Reserved registers will return 0000h if read.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM4549B is an audio codec used for PC systems. It is typically used in systems which are fully PC99-compliant and performs analog functions of the AC '97 Rev 2.1 architecture.

9.2 Typical Application

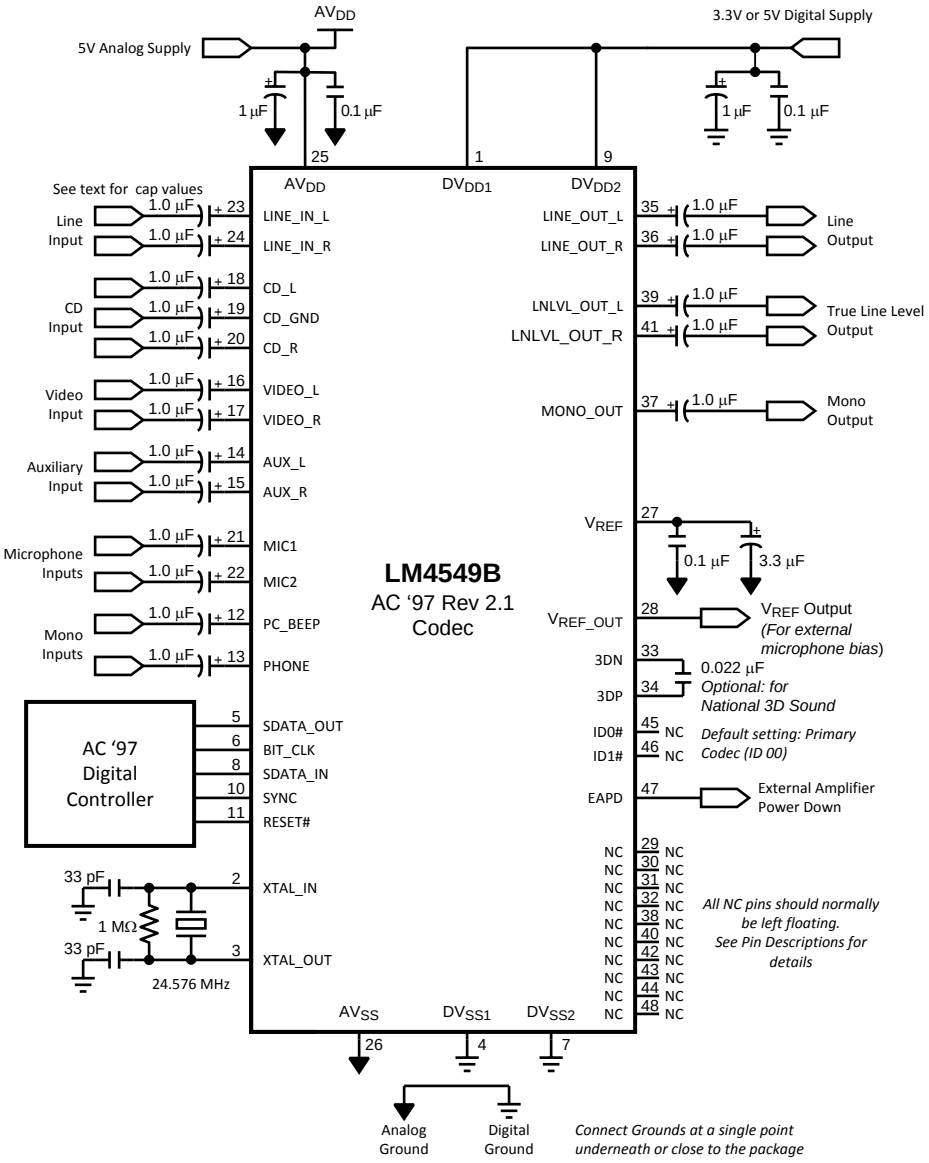


Figure 21. LM4549B Typical Application Circuit, Single Codec, 1-Vrms Inputs

Typical Application (continued)

9.2.1 Design Requirements

For this example the following application parameters exist:

- Single Codec Output
- 1-Vrms input

This design is provided for a high-quality audio path and provides all analog functionality for a PC audio system.

The design has a single codec output with 1-Vrms input.

9.2.2 Detailed Design Procedure

For all analog inputs a 1-uF capacitor should be tied to the input for proper decoupling. If the pin is unused then a 1-uF capacitor should be used and tied to ground.

For analog input pins, a proper lowpass filter will be needed to filter out any high frequencies depending on the application. Please see Figure 22.

Digital and Analog voltage supplies should have proper decoupling capacitors that cover low- and high-frequency spikes. In this application, the user chooses to go with 1-uF and 0.1-uF capacitors.

9.3 System Example

In Figure 22, the LM4549B is integrated into a system with a single code, 1-Vrms and 2-Vrms inputs, and EMC output filters.

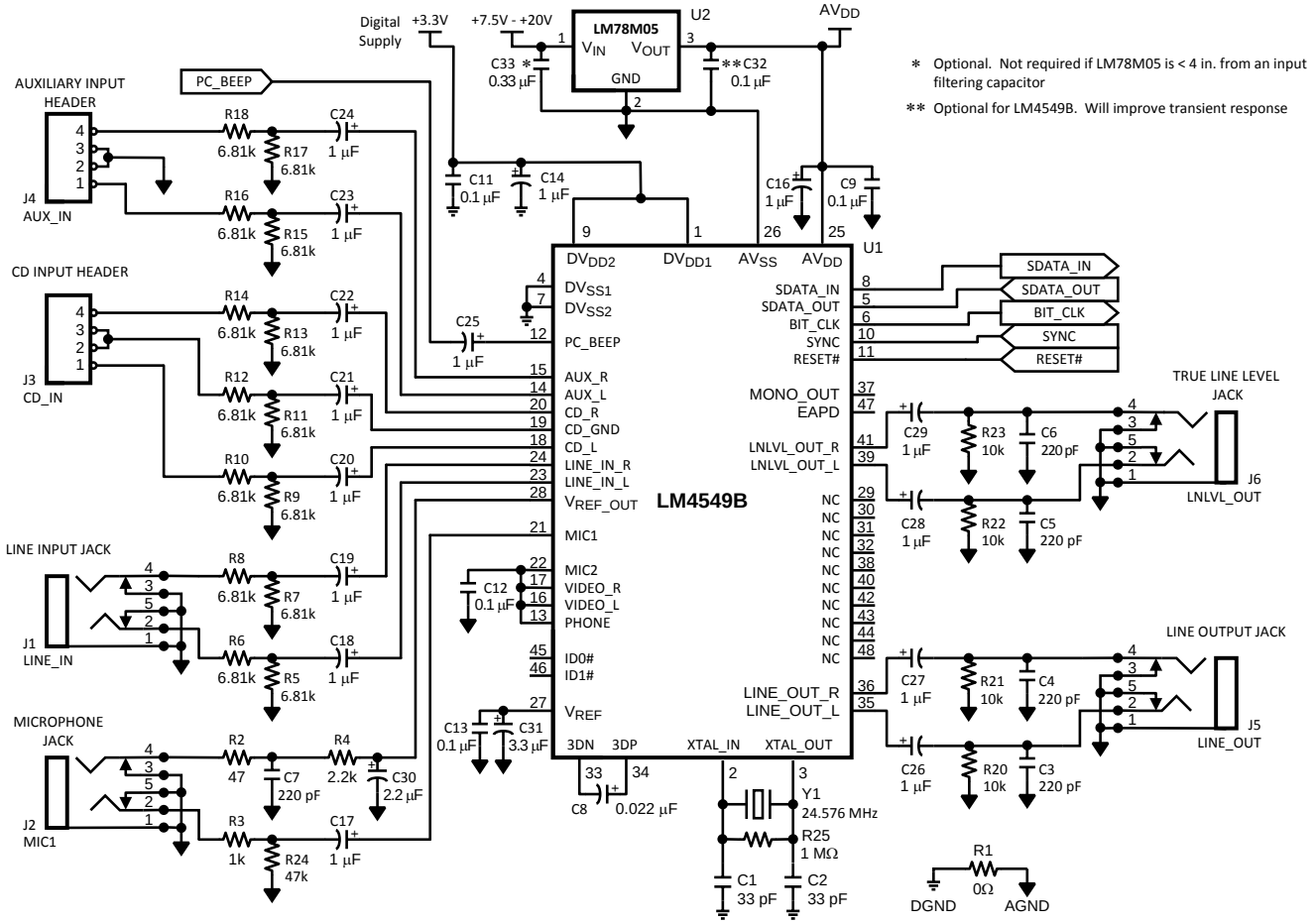


Figure 22. LM4549B Reference Design, Typical Application

9.3.1 Improving System Performance

The audio codec is capable of dynamic range performance in excess of 90 db, but the user must pay careful attention to several factors to achieve this. A primary consideration is keeping analog and digital grounds separate, and connecting them together in only one place. Some designers show the connection as a 0-Ω resistor, which allows naming the nets separately. Although it is possible to use a 2-layer board, TI recommends that a minimum of four layers be used, with the two inside layers being analog ground and digital ground. If EMI is a system consideration, then as many as eight layers have been successfully used. The 12- and 25-MHz. clocks can have significant harmonic content depending on the rise and fall times. Bypass capacitors should be very close to the package. The analog VDD pins should be supplied from a separate regulator to reduce noise. By operating the digital portion on 3.3 V instead of 5 V, an additional 0.5- to 0.7-db improvement can be obtained.

System Example (continued)

The bandgap reference and the anti-pop slow turnon circuit were improved in the LM4549B. A pullup resistor is not required on V_{REF}, pin 27. For an existing design, the 10-kΩ resistor can be left on the PCB, but the temperature coefficient will improve with no resistor on this pin. In addition, the THD will improve by 0.2–0.5 dB. The external capacitor is charged by an internal current source, ramping the voltage slowly. This results in slow turn-on of the audio stages, eliminating “pops and clicks”. Thus, turn-on performance is also improved. The pullup resistor, in conjunction with the internal impedance and the external capacitor, form a frequency dependent divider from the analog supply. Noise on the analog supply will be coupled into the audio path, with approximately 30 dB. of attenuation. Although this is not a large amount if the noise on the supply is tens of millivolts, it will prevent SNR from exceeding 80 dB.

In Figure 21 and Figure 22, the input coupling capacitors are shown as 1-µF capacitors. This is only necessary for extending the response down to 20 Hz. for music applications. For telematics or voice applications, the lower 3-dB point can be much higher. Using a specified input resistance of 10 kΩ, (40 kΩ typical), a 0.1-µF capacitor may be used. The lower 3-dB point will still be below 300 Hz. By using a smaller capacitor, the package size may be reduced, leading to a lower system cost.

10 Power Supply Recommendations

The LM4549B is designed to operate from an analog input voltage supply range between 4.2 V and 5.5 V.

The digital input voltage supply range is between 3 V and 5.5 V.

TI recommends connecting 1-µF and 0.1-µF decoupling capacitors in series on both the analog and digital supply pins.

11 Layout

11.1 Layout Guidelines

- The LM4549B must be initialized by using RESET# to perform a Power-On Reset.
- Don't leave unused Analog inputs floating. Tie all unused inputs together and connect to Analog Ground through a capacitor (that is, 0.1-µF).
- Do not leave CD_GND floating when using the CD stereo input. CD_GND is the AC signal reference for the CD channels and should be connected to the CD source ground (Analog Ground may also be acceptable) through a 1-µF capacitor.
- If using a non-standard AC Link controller take care to keep the SYNC and SDATA_IN signals low during Cold Reset to avoid entering the ATE or Vendor test modes by mistake.
- The PC_Beep input should be muted if not used since it defaults to 0-dB gain on reset, unlike the mute default of the other analog inputs.

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4549BVH/NOPB	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	LM4549 BVH
LM4549BVH/NOPB.A	Active	Production	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	LM4549 BVH
LM4549BVHX/NOPB	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LM4549 BVH
LM4549BVHX/NOPB.A	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	LM4549 BVH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

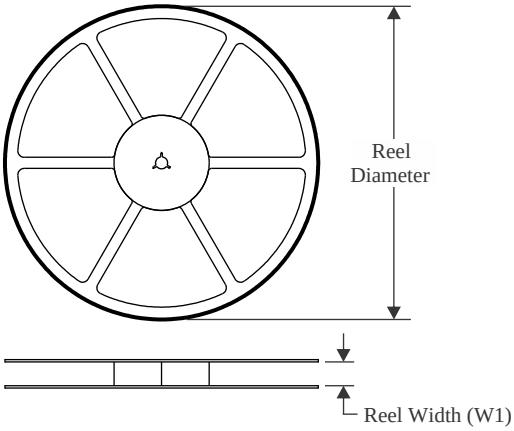
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

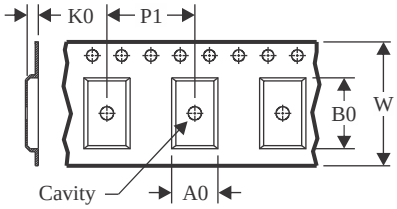
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

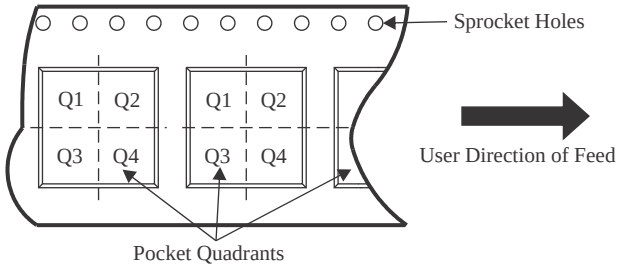


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

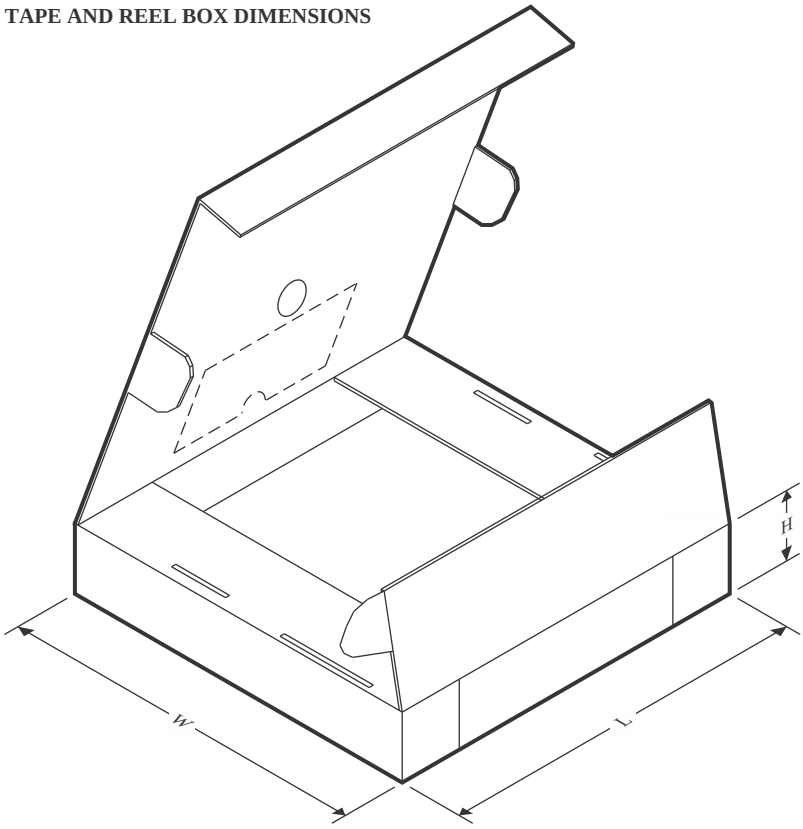
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4549BVHX/NOPB	LQFP	PT	48	1000	330.0	16.4	9.3	9.3	2.2	12.0	16.0	Q2

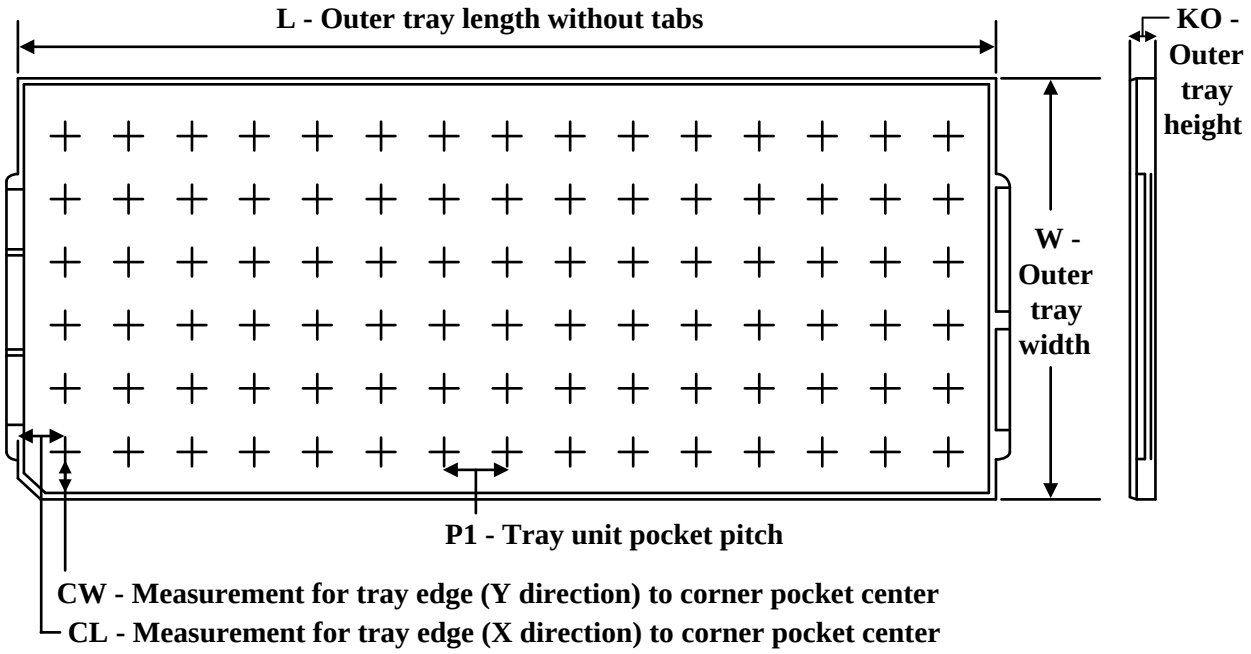
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4549BVHX/NOPB	LQFP	PT	48	1000	356.0	356.0	36.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

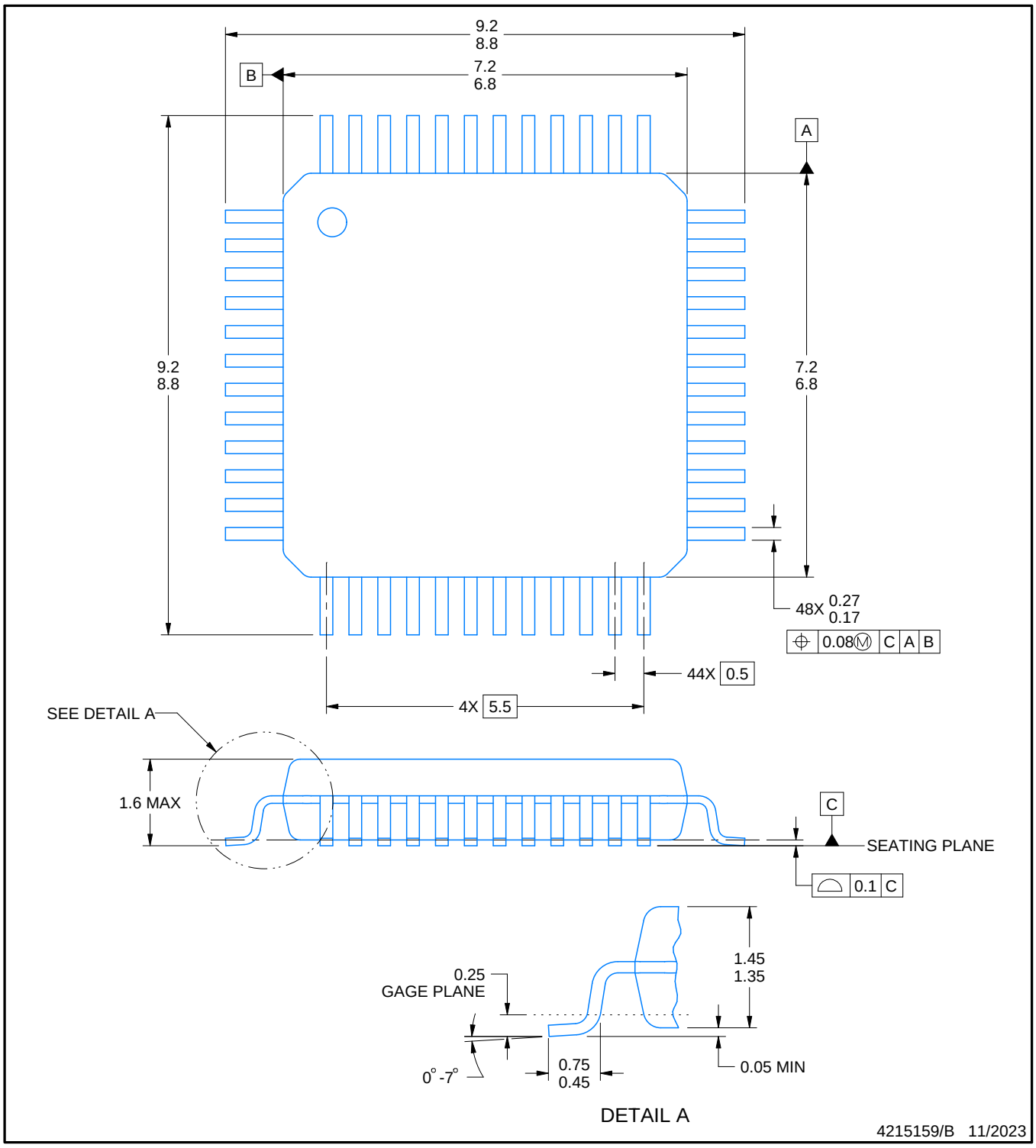
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM4549BVH/NOPB	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
LM4549BVH/NOPB.A	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PT0048A

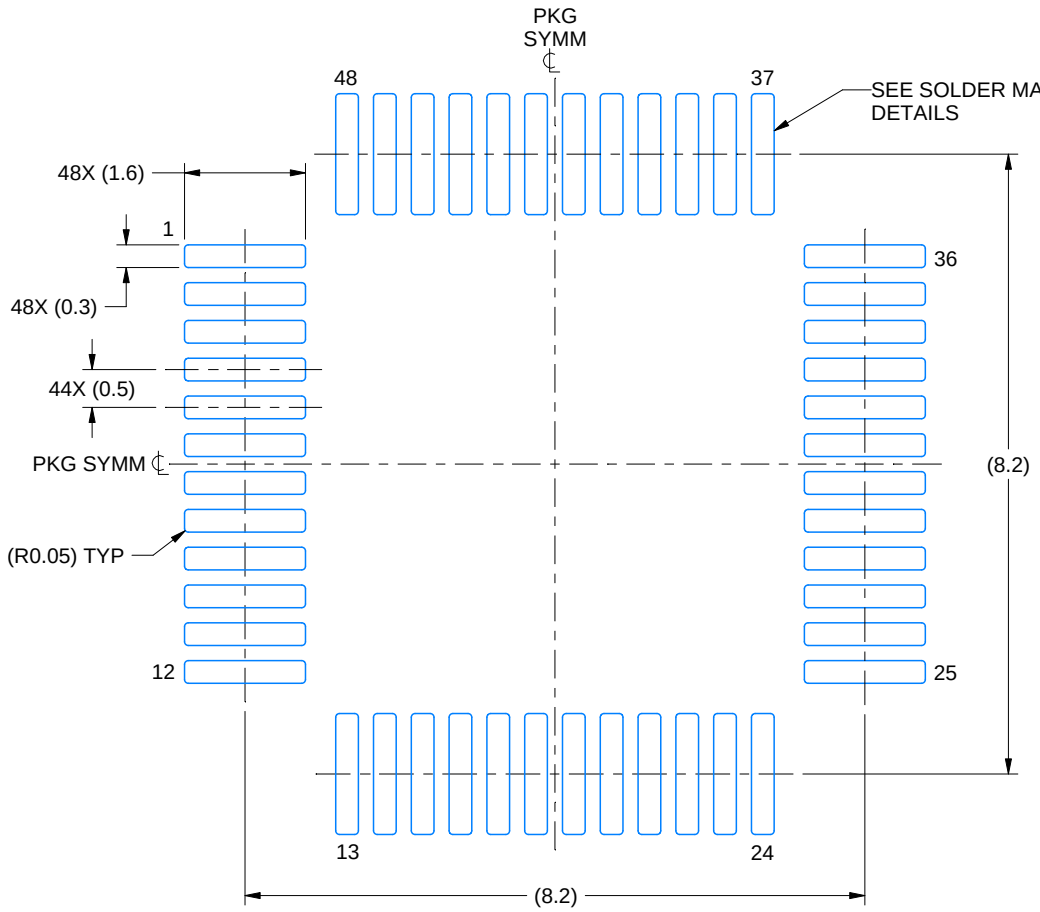
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

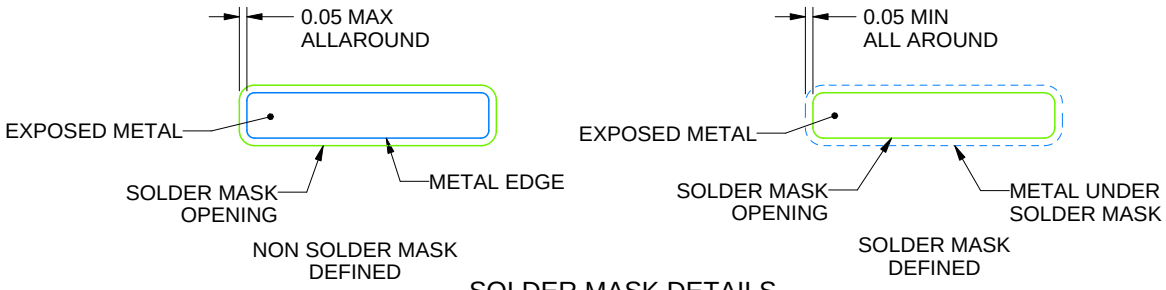


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

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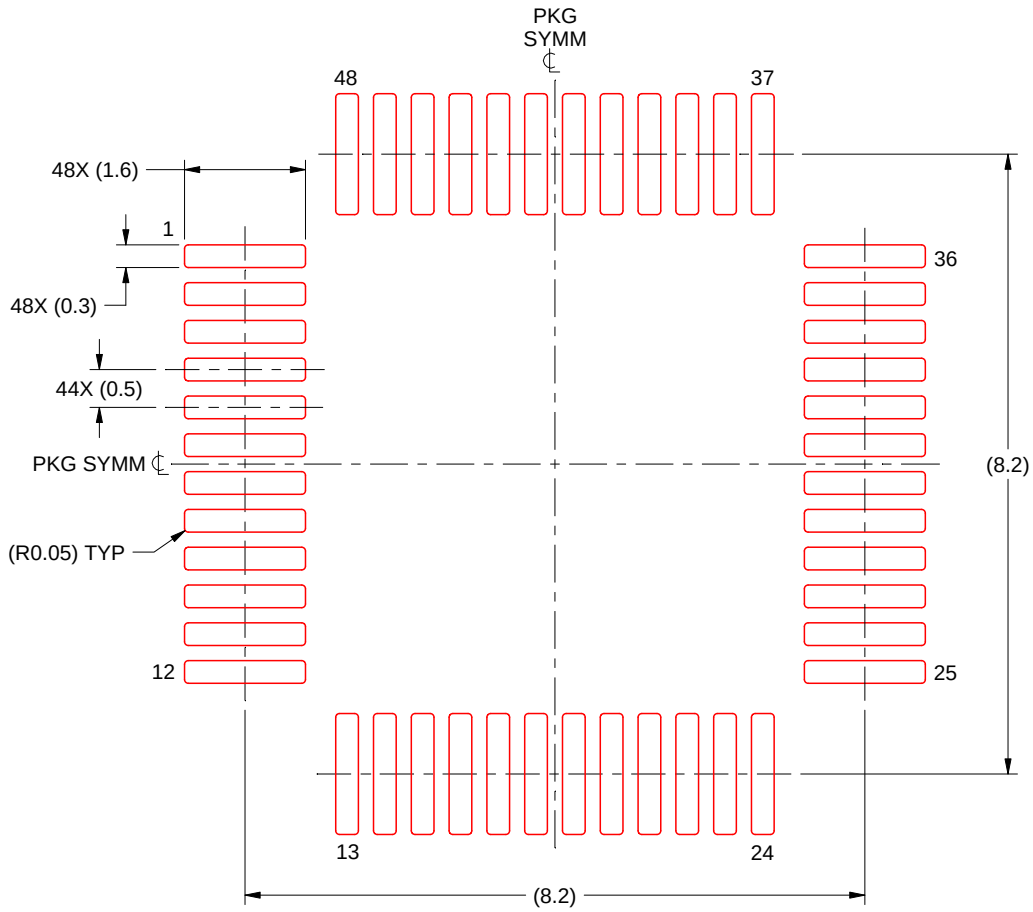
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月