Check for Samples: LM3544

FEATURES

- **Compatible with USB1.1 and USB 2.0**
- **90mΩ (typ.) High-Side MOSFET Switch**
- **500mA Continuous Current per Port**
- **7 ms Fault Flag Delay Filters Hot-Plug Events**
- **Industry Standard Pin Order**
- **Short Circuit Protection with Power-Saving Current Foldback**
- **Thermal Shutdown Protection**
- **Undervoltage Lockout**
- **Recognized by UL and Nemko CB**
- **Input Voltage Range: 2.7V to 5.5V**
- **5µA Maximum Standby Supply Current**
- **16-Pin SOIC Package**
- **Ambient Temperature Range: −40°C to 85°C**

APPLICATIONS

- **USB Root, Self-Powered, and Bus-Powered Hubs**
- **USB Devices such as Monitors and Printers**
- **General Purpose High Side Switch Applications**

DESCRIPTION

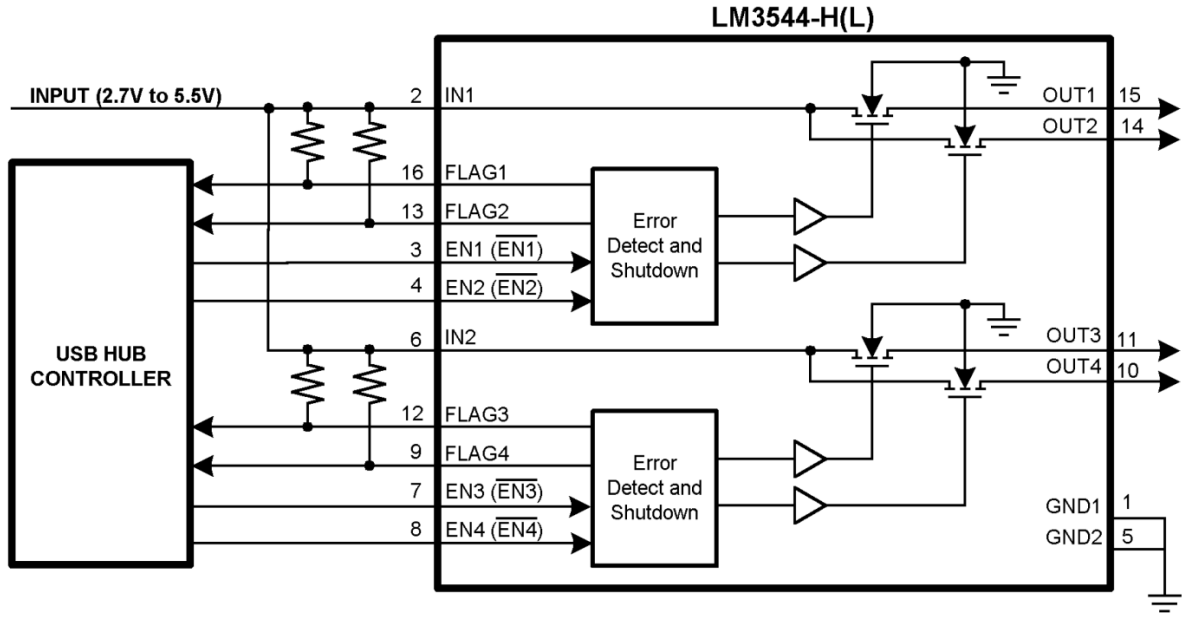
The LM3544 is a quad high-side power switch that is an excellent choice for use in Root, Self-Powered and Bus- Powered USB (Universal Serial Bus) Hubs. Independent port enables, flag signals to alert USB controllers of error conditions, controlled start-up in hot-plug events, and short circuit protection all satisfy USB requirements.

The LM3544 accepts input voltages between 2.7V and 5.5V. The Enable logic inputs, available in active-high and active-low versions, can be powered off any voltage in the 2.7V to 5.5V range. The LM3544 limits the continuous current through a single port to 1.25A (max.) when it is shorted to ground.

The low on-state resistance of the LM3544 switches ensures the LM3544 will satisfy USB voltage drop requirements, even when current through a switch reaches 500 mA. Thus, High-Powered USB Functions, Low-Powered USB functions, and Bus-Powered USB Hubs can all be powered off a Root or Self-Powered USB Hub containing the LM3544.

Added features of the LM3544 include current fold-back to reduce power consumption in current overload conditions, thermal shutdown to prevent device failure caused by high current overheating, and undervoltage lockout to keep switches from operating if the input voltage is below acceptable levels.

Functional Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Connection Diagrams

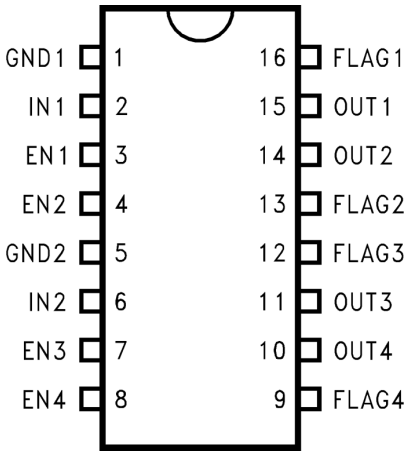


Figure 1. LM3544-H
16-Pin SOIC
Top View

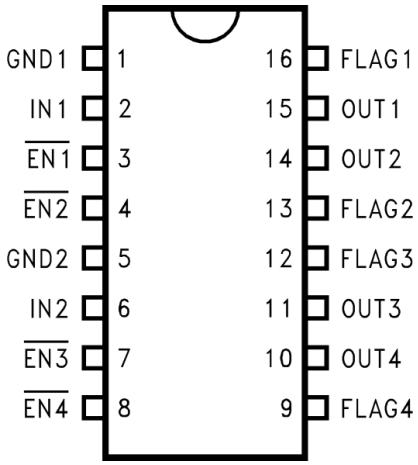


Figure 2. LM3544-L
16-Pin SOIC
Top View

Typical Application Circuit

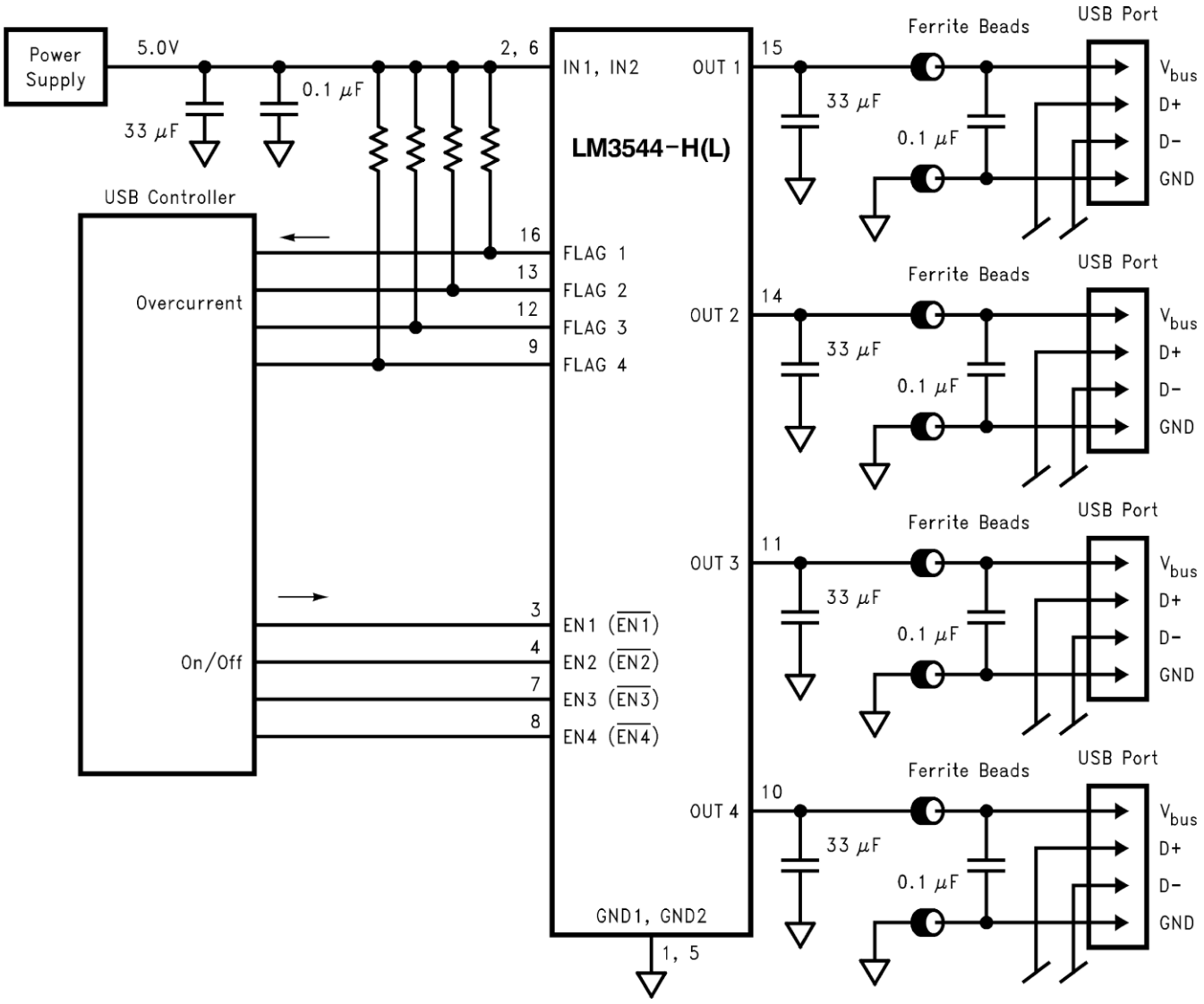


Figure 3. The LM3544 used in a Self-Powered or Root USB Hub

ABSOLUTE MAXIMUM RATINGS(1)(2)

Voltage at IN_X and OUT_X pins	−0.3V to 6V
Voltage at $EN_X(\overline{EN_X})$ and $FLAG_X$ pins	−0.3V to 5.5V
Power Dissipation(3)	Internally Limited
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature Range (Soldering, 5 sec.)	260°C
ESD Rating(4)	2 kV

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(3) The maximum allowable power dissipation is a function of the Maximum Junction Temperature (T_{JMAX}), Junction to Ambient Thermal Resistance (θ_{JA}), and the Ambient Temperature (TA). The LM3544 in the 16-pin SOIC package has a T_{JMAX} of 150°C and a θ_{JA} of 130°C/W. The maximum allowable power dissipation at any temperature is $P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the part will go into thermal shutdown.
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	2.7V to 5.5V
Continuous Output Current Range (Each Output)	0 mA to 500 mA
Junction Temperature Range	−40°C to 125°C

DC ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5.0V, $EN_X = V_{IN}$ (LM3544-H) or EN_X = 0V (LM3544-L).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	On Resistance	V_{IN} = 5V, I_{OUTX} = 0.5A		90	125	mΩ
		V_{IN} = 3.3V, I_{OUTX} = 0.5A		95	130	
I_{OUT}	OUT_X Continuous Output Current	3.0V ≤ V_{IN} ≤ 5.5V	**0.5**			A
$I_{LEAK-OUT}$	OUT_X Leakage Current	EN_X = 0 ($\overline{EN_X}$ = VI_N); TJ = 25°C		0.01	1	µA
		EN_X = 0 ($\overline{EN_X}$ = V_{IN}); − 40 ≤ TJ ≤ 125°C			**10**	µA
I_{SC}	OUT_X Short-Circuit Current(1)	OUT_X Connected to GND		0.8	1.25	A
OC_{THRESH}	Overcurrent Threshold			2.0	3.2	A
V_{L_FLAG}	$FLAG_X$ Output-Low Voltage	I($FLAG_X$) = 10 mA		0.1	**0.3**	V
$I_{LEAK-FLAG}$	$FLAG_X$ Leakage Current	2.7 ≤ V_{FLAG} ≤ 5.5V			1	µA
$I_{LEAK-EN}$	EN_X Input Leakage Current	EN_X/EN_X = 0V or $EN_X/EN_X = V_{IN}$	**-0.5**		**0.5**	µA
V_{IH}	EN/$\overline{EN}$ Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V	2.4			V
V_{IL}	EN/$\overline{EN}$ Input Logic Low	4.5V ≤ V_{IN} ≤ 5.5V			0.8	V
		2.7V ≤ V_{IN} ≤ 4.5V			0.4	V
V_{UVLO}	Under-Voltage Lockout Threshold			1.8		V
I_{DDON}	Operational Supply Current	$EN_X = V_{IN}$ (EN_X = 0); T_J = 25°C		375	600	µA
		$EN_X = V_{IN}$ (EN_X = 0); −40°C ≤ T_J ≤ 125°C			**800**	µA
I_{DDOFF}	Shutdown Supply Current	EN_X = 0 ($EN_X = V_{IN}$); T_J = 25°C			1	µA
		−40°C ≤ T_J ≤ 125°C			**5**	µA

(1) Thermal Shutdown will protect the device from permanent damage.

AC ELECTRICAL CHARACTERISTICS

Limits are for T_J = 25°C and V_{IN} = 5.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	OUT_X Rise Time(1)	C_L = 33 µF, I_{LOAD} = 500 mA		1.5		ms
t_f	OUT_X Fall Time(2)	C_L = 33 µF, I_{LOAD} = 500 mA		0.9		ms
t_{ON}	Turn-on Delay(3)	C_L = 33 µF, I_{LOAD} = 500 mA		2.9		ms
t_{OFF}	Turn-off Delay(4)	C_L = 33 µF, I_{LOAD} = 500 mA		0.7		ms
t_F	Flag Delay(5)	I_{FLAG} = 10 mA		7		ms

(1) Time for OUT_X to rise from 10% to 90% of its enabled steady-state value after EN_X ($\overline{EN}_X$) is asserted.
(2) Time for OUT_X to fall from 10% to 90% of its enabled steady-state value after EN_X ($\overline{EN}_X$) is deasserted.
(3) Time between EN_X rising through V_{IH} ($\overline{EN}_X$ falling through V_{IL}) and OUT_X rising through 90% of its enabled steady-state voltage.
(4) Time between EN_X falling through V_{IL} ($\overline{EN}_X$ rising through V_{IH}) and OUT_X falling through 10% of its enabled steady-state voltage.
(5) Time between EN_X rising through V_{IN} ($\overline{EN}_X$ falling through V_{IN}) and $FLAG_X$ falling through 0.3V when OUT_X is connected to GND.

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
2, 6	IN 1, 2	Supply Inputs: These pins are the inputs to the power switches and the supply input for the IC. In most applications they are connected together externally and to a single input voltage supply.
1, 5	GND 1, 2	Grounds: Must be connected together and to a common ground.
15, 14, 11, 10	OUT 1, 2, 3, 4	Switch Outputs: These pins are the outputs of the high side switches.
3, 4, 7, 8	LM3544-H: EN 1, 2, 3, 4 (LM3544-L: $\overline{EN}$ 1, 2, 3, 4)	Enable (Inputs): Active-high (or active-low) logic enable inputs.
16, 13, 12, 9	FLAG 1, 2, 3,4	Fault Flag (Outputs): Active-low open drain outputs. Indicates over-current, UVLO or thermal shutdown. See APPLICATION INFORMATION for more details.

TYPICAL PERFORMANCE CHARACTERISTICS

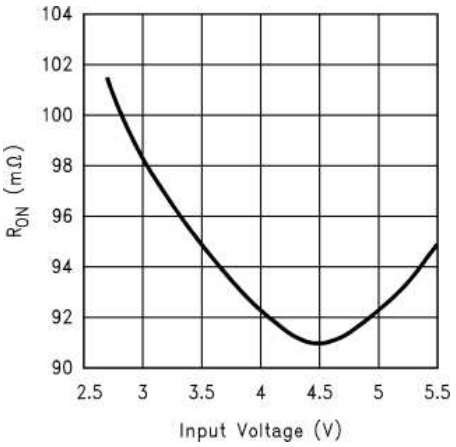


Figure 4. R_{ON} vs Input Voltage

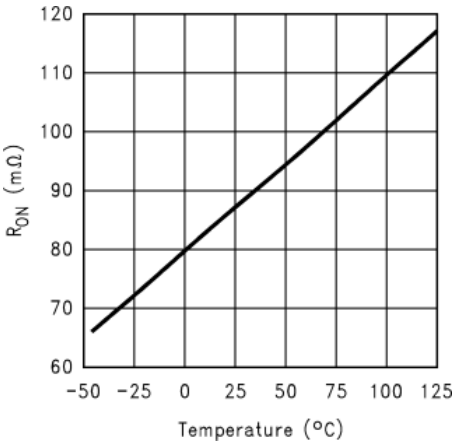


Figure 5. R_{ON} vs Junction Temperature

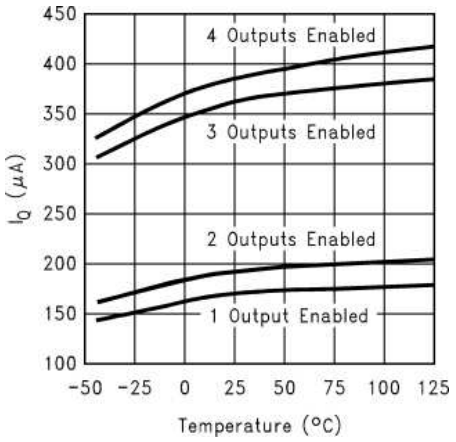


Figure 6. Quiescent Current, Output(s) Enabled vs Junction Temperature

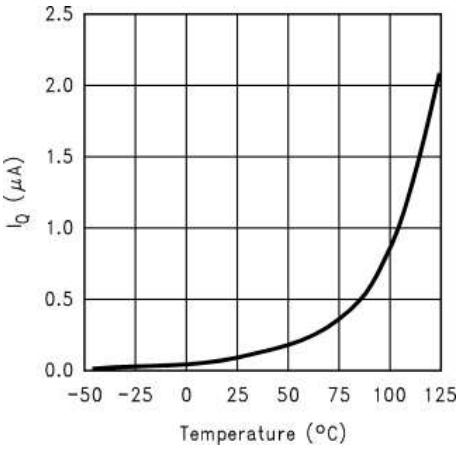


Figure 7. Quiescent Current, Output(s) Disabled vs Junction Temperature

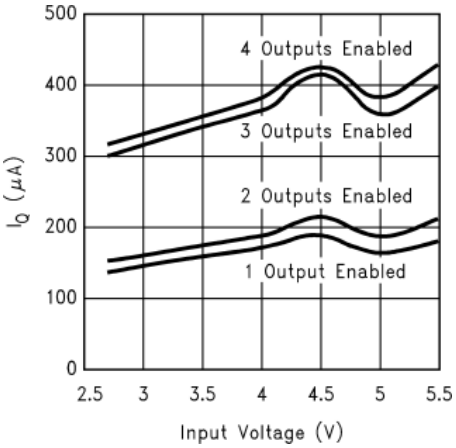


Figure 8. Quiescent Current, Output(s) Enabled vs Input Voltage

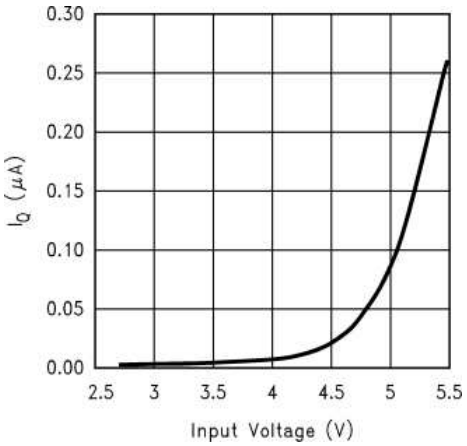


Figure 9. Quiescent Current, Output(s) Disabled vs Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

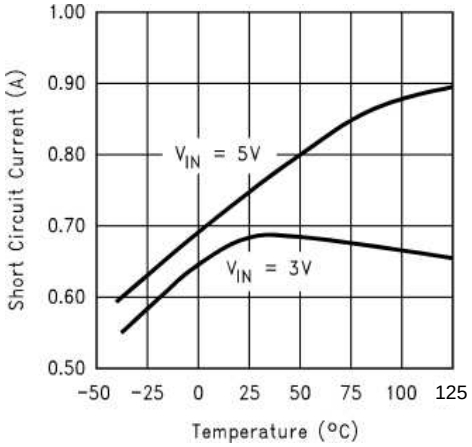


Figure 10. Short-Circuit Output Current vs Junction Temperature(1)

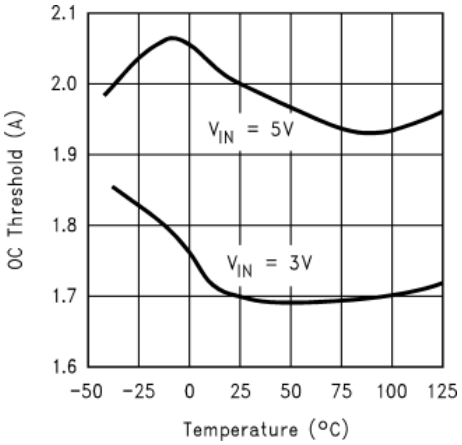


Figure 11. Over-Current Threshold vs Junction Temperature(1)

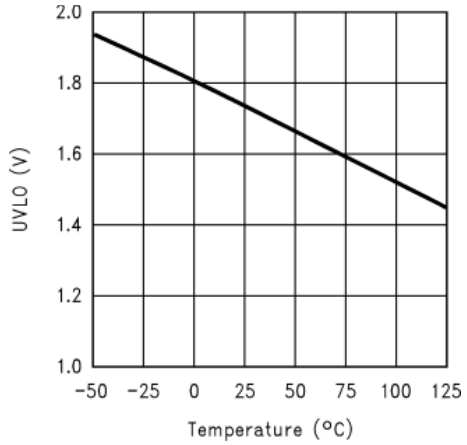


Figure 12. Under-Voltage Lockout (UVLO) Threshold vs Junction Temperature

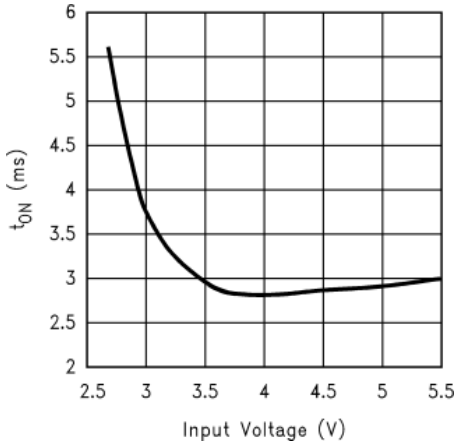


Figure 13. Turn-On Delay vs Input Voltage (C_{IN} = 33 µF, C_{OUT} = 33 µF)

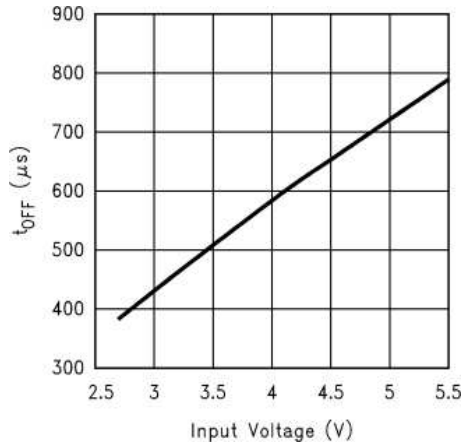


Figure 14. Turn-Off Delay vs Input Voltage (C_{IN} = 33 µF, C_{OUT} = 33 µF)

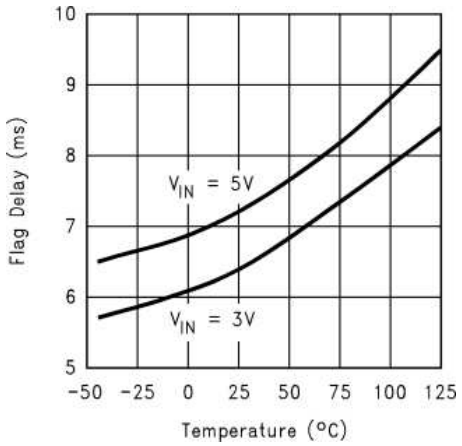


Figure 15. Fault Flag Delay Time vs Junction Temperature

(1) Output is shorted to Ground through a 100 mΩ resistor.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

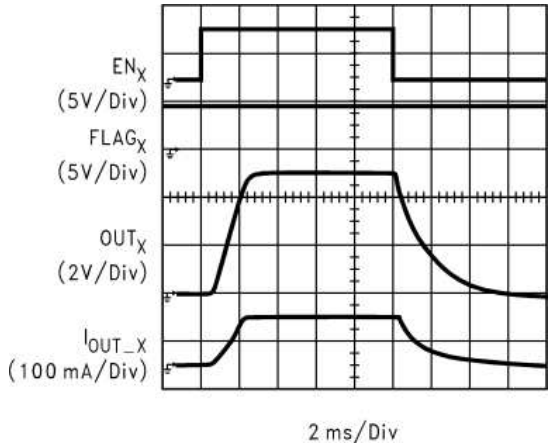


Figure 16. Turn-On/Turn-Off Response with 47Ω/33µF Load

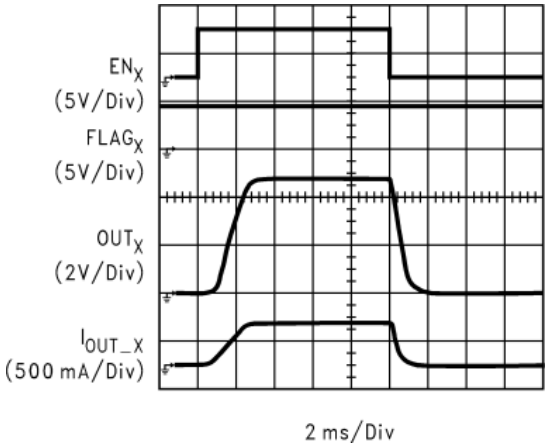


Figure 17. Turn-On/Turn-Off Response with 10Ω/33µF Load

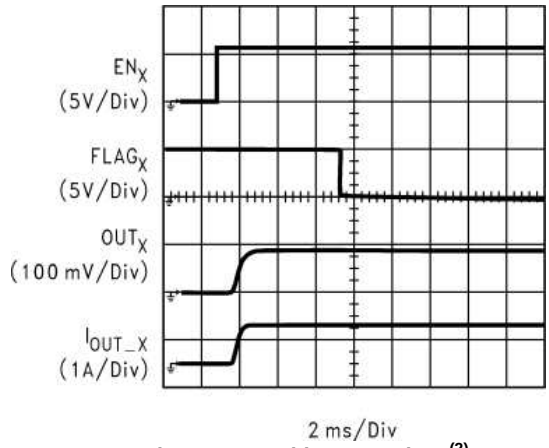


Figure 18. Enable Into a Short(2)

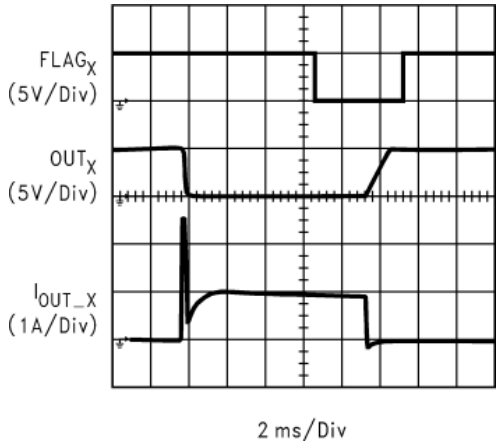


Figure 19. Short Connected to Enabled Device(2)

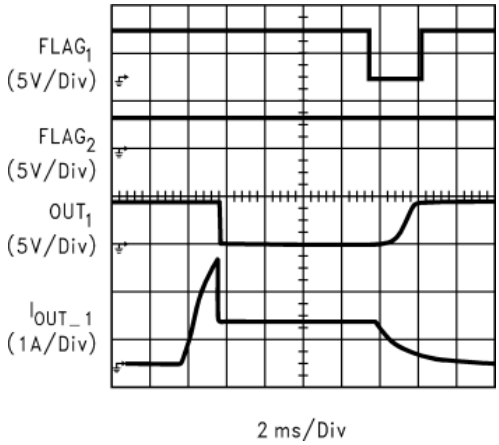


Figure 20. Over-Current Response with Ramped Load on OUT1 and Fixed Load on OUT2(3)

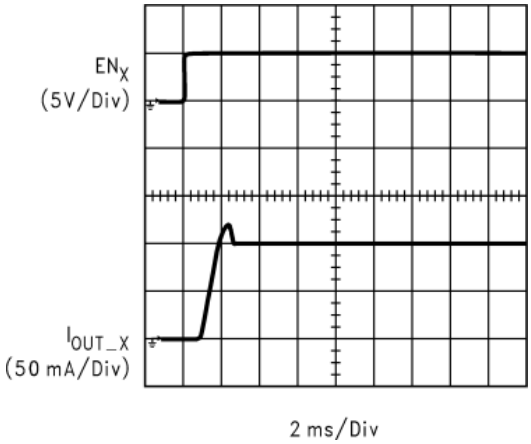


Figure 21. Inrush Current to Downstream Device when LM3544 is Enabled(4)

(2) Output is shorted to Ground through a 100 mΩ resistor.
(3) Output is shorted to Ground through a 100 mΩ resistor.
(4) Load is two capacitors and one resistor in parallel to model an actual USB load condition. The first capacitor has a value of 33 µF to model the LM3544 output capacitor. The second capacitor has a value of 10 µF to model the maximum allowable input capacitance of the downstream device. The resistor is a 47Ω resistor to model the maximum allowable input resistance of the downstream device.

FUNCTIONAL DESCRIPTION

POWER SWITCHES

The power switches that comprise the four ports of the LM3544 are N-Channel MOSFETs. They have a typical onstate drain-to-source resistance of 90 mΩ when the input voltage is 5 V. When enabled, each switch will supply a 500 mA minimum current to its load. In the unlikely event that a switch is enabled and the output voltage of that switch is pulled above the input voltage, the bi-directional nature of the switch results in current to flow from the output to the input. When a switch is disabled, current flow through the switch is prevented in both directions.

CHARGE PUMP AND DRIVER

The gate voltages of the high-side NFET power switches are supplied by an internal charge-pump and driver circuit combination. The charge pump is a low-current, switched capacitor circuit that efficiently generates voltages above the LM3544 input supply. The charge pump output is used to supply a transconductance amplifier driver circuit that controls the gate voltages of the power switches. Rise and fall times on the gates are typically kept between 2 ms and 4 ms to limit large current surges and associated electromagnetic interference (EMI).

ENABLE (EN_X OR $\overline{EN}_X$)

The LM3544 comes in two versions: an active-high enable version, LM3544-H, and an active-low enable version, LM3544-L. In the LM3544-H, the EN_X pins are active-high logic inputs that, when asserted, turn on the associated power supply switch(es). Power supply switches are controlled by the $\overline{EN}_X$ active-low logic inputs in the LM3544-L. With all four ports disabled on either version of the LM3544, less than 5 µA of supply current is consumed. Both types of enable inputs, active-high and active-low, are TTL and CMOS logic compatible.

INPUT AND OUTPUT

The power supply to the control circuitry and the drains of the power-switch MOSFETs are connected to the two input pins, IN1 and IN2. These two pins are connected externally in most standard applications. The two ground nodes GND1 and GND2 must be connected externally in all applications. Pins OUT1, OUT2, OUT3, and OUT4 are connections to the source nodes of the power-switch MOSFETs. In a typical application circuit, current flows through the switches from IN1 and IN2 to OUT_X toward the load.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage Lockout (UVLO) prevents the MOSFET switches from turning on until the input voltage exceeds a typical value of 1.8V.

If the input voltage drops below the UVLO threshold, the MOSFET switches are opened and fault flags are activated. UVLO flags function only when one or more of the ports is enabled. If a port is enabled in a UVLO condition, flags corresponding to the enabled port and its dual (port 1 is paired with port 2, port 3 is paired with port 4) are asserted.

CURRENT LIMIT AND FOLD-BACK

The current limit circuit is designed to protect the system supply, the LM3544 switches, and the load from potential damage resulting from excessive currents. If a direct short occurs on an output of the LM3544, the input capacitor(s) rapidly discharge through the part, activating current limit circuitry. The threshold for activating current limiting is 2.0A (typ.). Protection is achieved by momentarily opening the MOSFET switch and then gradually turning it on. Turn-on is halted when the current through the switch reaches the current-limit level of 1.0A (typ.) The current is held at this level until either the excessive load/short is removed or the part overheats and thermal shutdown occurs (see THERMAL SHUTDOWN). The fault flag of a switch is asserted whenever the switch is current limiting.

If a port on the LM3544 is enabled into a short condition, the output current of that port will rise to the current-limit level and hold there.

When a port is in a current-limit condition, the LM3544 senses the output voltage on that port and, if it is less than 1.0V (typ.), will reduce the output current through that port. This operation is shown in Figure 22, below. The current reduction, or foldback, reduces power dissipation through the overloaded MOSFET switch. An additional advantage of the foldback feature is the reduction of power required from the source supply when one or more output ports are shorted.

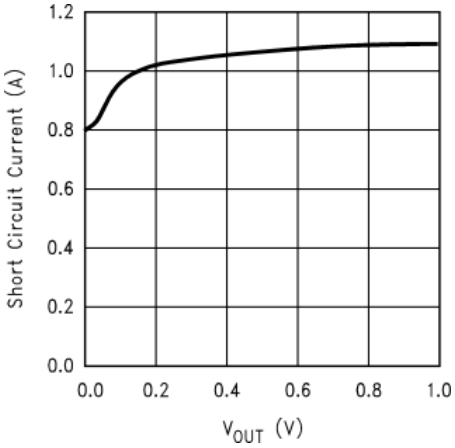


Figure 22. Short-Circuit Output Current (with Foldback) vs. Output Voltage

THERMAL SHUTDOWN

The LM3544 is internally protected against excessive power dissipation by a two-stage thermal protection circuit. If the device temperature rises to approximately 145°C, the thermal shutdown circuitry turns off any switch that is current limited. Non-overloaded switches continue to function normally. If the die temperature rises above 160°C, all switches are turned off and all four fault flag outputs are activated. Hysteresis ensures that a switch turned off by thermal shutdown will not be turned on again until the die temperature is reduced to 135°C. Shorted switches will continue to cycle off and on, due to the rising and falling die temperature, until the short is removed.\

The thermal shutdown function is shown graphically in Figure 23 and Figure 24.

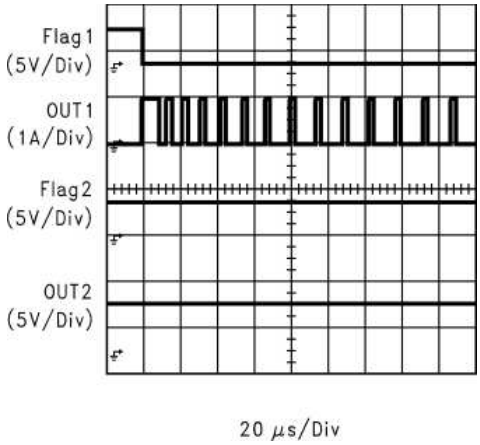


Figure 23. Thermal Shutdown Characteristics when only the First-Stage Thermal-Shutdown Mode is Needed

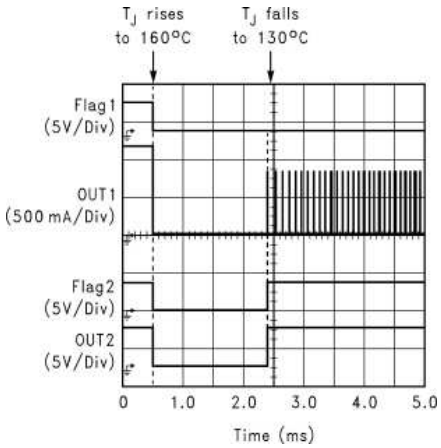


Figure 24. Thermal Shutdown Characteristics when both First-Stage and Second-Stage Thermal-Shutdown Modes are Needed

In Figure 23, port 1 is enabled into a short. When this occurs, the MOSFET switch of port 1 repeatedly opens and closes as the device temperature rises and falls between 145°C and 135°C. In this example, the device temperature never rises above 160°C. The second stage thermal shutdown is not used and port 2 remains operational.

When port 1 is enabled into a short in the example illustrated in Figure 24, the device temperature immediately rises above 160°C. A higher ambient temperature or a larger number of shorted outputs can cause the junction temperature to increase, resulting in the difference in behavior between the current example and the previous one. When the junction temperature reaches 160°C, all four ports are disabled (ports 3 and 4 are not shown in the figure) and all four fault-flag signals are asserted. Just prior to time index 2.5 ms, the device temperature falls below 135°C, all four ports activate, and all four fault flags are removed. The short condition remains on port 1, however. For the remainder of the example, the device temperature cycles between 135°C and 145°C, causing port 1 to repeatedly turn on and off but allowing the un-shorted ports to function normally.

SOFT START

When a power switch is enabled, high levels of current will flow instantaneously through the LM3544 to charge the large capacitance at the output of the port. This is likely to exceed the over-current threshold of the device, at which point the LM3544 will enter its current-limit mode. The amount of current used to charge the output capacitor is then set by the current-limit circuitry. The device will exit the current-limit mode when the current needed to continue to charge the output capacitor is less than the LM3544 current-limit level.

FAULT FLAG

The fault flags are open-drain outputs, each capable of sinking up to a 10 mA load current to typically 100 mV above ground.

A parasitic diode exists between the flag pins and VIN pins. Pulling the flag pins to voltages higher than V_{IN} will forward bias this diode and will cause an increase in supply current. This diode will also clamp the voltage on the flag pins to a diode drop above V_{IN}.

The fault flag is active (pulled low) when any of the following conditions are present: under-voltage, current-limit, or thermal-shutdown.

The LM3544 has an internal delay in reporting fault conditions that is typically 7 ms in length. In start-up, the delay gives the device time to charge the output capacitor(s) and exit the current-limit mode before a flag signal is set. This delay also prevents flag signal glitches from occurring when brief changes in operating conditions momentarily place the LM3544 into one of its three error conditions. If an error condition still exists after the delay interval has elapsed, the appropriate fault flag(s) will be asserted (pulled low) until the error condition is removed. In most applications, the 7 ms internal flag delay eliminates the need to extend the delay with an external RC delay network.

APPLICATION INFORMATION

OUTPUT FILTERING

The schematic in Figure 3 shows a typical application circuit for the LM3544. The USB specification requires 120 µF at the output of each hub. A four-port hub with 33 µF tantalum capacitors at each port output meets the specification. These capacitors provide short-term transient current to drive downstream devices when hot-plug events occur. Capacitors with low equivalent-series-resistance should be used to lower the inrush current flow through the LM3544 during a hot-plug event.

The rapid change in currents seen during a hot plug event can generate electromagnetic interference (EMI). To reduce this effect, ferrite beads in series between the outputs of the LM3544 and the downstream USB port are recommended. Beads should also be placed between the ground node of the LM3544 and the ground nodes of connected downstream ports. In order to keep voltage drop across the beads to a minimum, wire with small DC resistance should be used through the ferrite beads. A 0.01 µF - 0.1 µF ceramic capacitor is recommended on each downstream port directly between the V_{bus} and ground pins to further reduce EMI effects.

POWER SUPPLY FILTERING

A sizable capacitor should be connected to the input of the LM3544 to ensure the voltage drop on this node is less than 330 mV during a heavy-load hot-plug event. A 33 µF, 16V tantalum capacitor is recommended. The input supply should be further bypassed with a 0.01 µF - 0.1 µF ceramic capacitor, placed close to the device. The ceramic capacitor reduces ringing on the supply that can occur when a short is present at the output of a port.

EXTENDING THE FAULT FLAG DELAY

While the 7 ms (typical) internal delay in reporting flag conditions is adequate for most applications, the delay can be extended by connecting external RC filters to the FLAG pins, as shown in Figure 25.

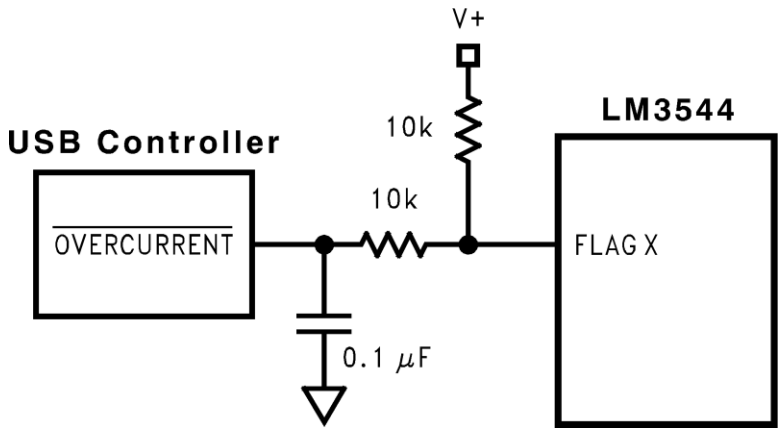


Figure 25. Typical Circuit for Lengthening the Internal Flag Delay

POWER DISSIPATION AND JUNCTION TEMPERATURE

A few simple calculations will allow a designer to calculate the approximate operating temperature of the LM3544 for a given application. The large currents possible through the low resistance power MOSFET combined with the high thermal resistance of the SOIC package, in relation to power packages, make this estimate an important design step. Begin the estimate by determining RON at the expected operating temperature using the graphs in the Typical Performance Characteristics section of this datasheet. Next, calculate the power dissipation through the switch with Equation 1.

$$PD = R_{ON} * I_{DS}\ 2 \quad (1)$$

NOTE

The equation for power dissipation neglects the portion that comes from LM3544 quiescent current, because this value will almost always be insignificant.

Using this figure, determine the junction temperature with Equation 2:

$T_J = PD * \theta_{JA} + T_A$

where

- θJA = SOIC Thermal Resistance: 130°C/W and TA = Ambient Temperature (°C). (2)

Compare the calculated temperature with the expected temperature used to estimate R_{ON}. If they do not reasonably match, re-estimate R_{ON} using a more appropriate operating temperature and repeat the calculations. Reiterate as necessary.

PCB LAYOUT CONSIDERATIONS

In order to meet the USB requirements for voltage drop, droop and EMI, each component used in this circuit must be evaluated for its contribution to the circuit performance. These principles are illustrated in Figure 26. The following PCB layout rules and guidelines are recommended:

1. Place the switch as close to the USB connector as possible. Keep all V_{bus} traces as short as possible and use at least 50-mil, 1 ounce copper for all V_{bus} traces. Solder plating the traces will reduce the trace resistance.
2. Avoid vias as much as possible. If vias are used, use multiple vias in parallel and/or make them as large as possible.
3. Place the output capacitor and ferrite beads as close to the USB connector as possible.
4. If ferrite beads are used, use wires with minimum resistance and large solder pads to minimize connection resistance.

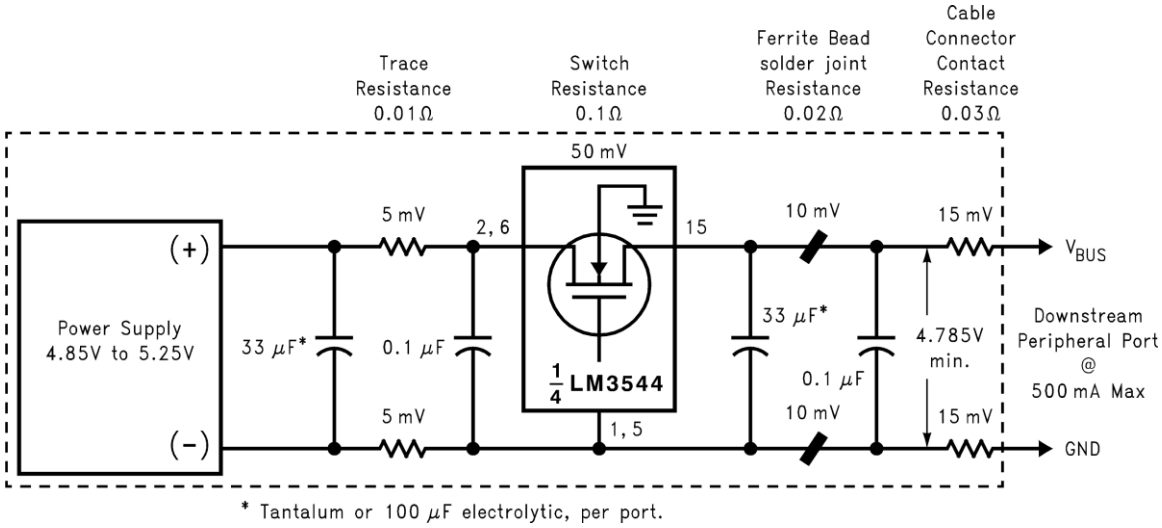


Figure 26. Self-Powered Hub Connections and Per-Port Voltage Drop

TYPICAL APPLICATIONS

ROOT AND SELF-POWERED USB HUBS

The LM3544 has been designed primarily for use in root and self-powered USB hubs. In this application, the switches of the LM3544 are used to connect the power source of the hub to the power bus used by downstream devices and to protect the hub from dangerously excessive loads and shorts to ground. A high-power bus-powered function, low-power bus-powered function, or a bus-powered hub can be driven through a single port of the LM3544. A schematic of a circuit that uses the LM3544 for power-supply switching in a typical root or self-powered hub was shown earlier in this datasheet in Figure 3.

Voltage drop requirements of USB power supplies require the power outputs of the root and self-powered hubs to be no less than 4.75V. For this reason, it is recommended that a 5V power supply with a ±3% output voltage tolerance is used in this application. Combining a 3% supply with a low resistance PCB design and the low on-resistance of the LM3544 power switches will ensure that the hub power outputs meet the USB voltage drop specification even with a 500mA load, the maximum allowed in the USB standard.

BUS-POWERED USB HUBS

The LM3544 is capable of performing the power supply switching functions required in Bus-Powered hubs. Use here is very similar to the configuration used in root and self-powered hubs. With bus-powered hubs, however, there is no internal power supply to drive the input pins of the LM3544. Instead, the input pins should be connected to the power bus supplied by the upstream hub.

USB BUS-POWERED FUNCTIONS AND GENERAL IN-RUSH CURRENT LIMITING APPLICATIONS

The LM3544 can be placed at the power-supply input of USB bus-powered functions, or other similar devices, to protect them from high in-rush currents. If the current being delivered to the device were to exceed the 2.0A over-current threshold (typ.) of the LM3544, switches in violation would open to protect the device from damage.

In addition to in-rush current limiting, the LM3544 can be used in high-power bus-powered functions to keep current levels of the function in compliance during power-up. The USB specification requires the staged switching of power when connecting high-power functions to the bus. When a high-power function is initially connected to the bus, it must not draw more than one unit supply (100mA). After a connection is detected and enumerated, and if the upstream device is capable of supplying the required power, the high power function may draw up to five unit loads (500mA). With the proper control signals, the LM3544 can be used to achieve this staged power connection. When the function is connected to the bus, one or more of the LM3544 switches can be closed to connect bus power only to circuitry needed during the connection and enumeration process. If the function is to be powered fully, remaining switches on the LM3544 can be closed to connect all blocks of the function to the power bus. Figure 27 illustrates how the LM3544 can be connected for use in bus powered functions.

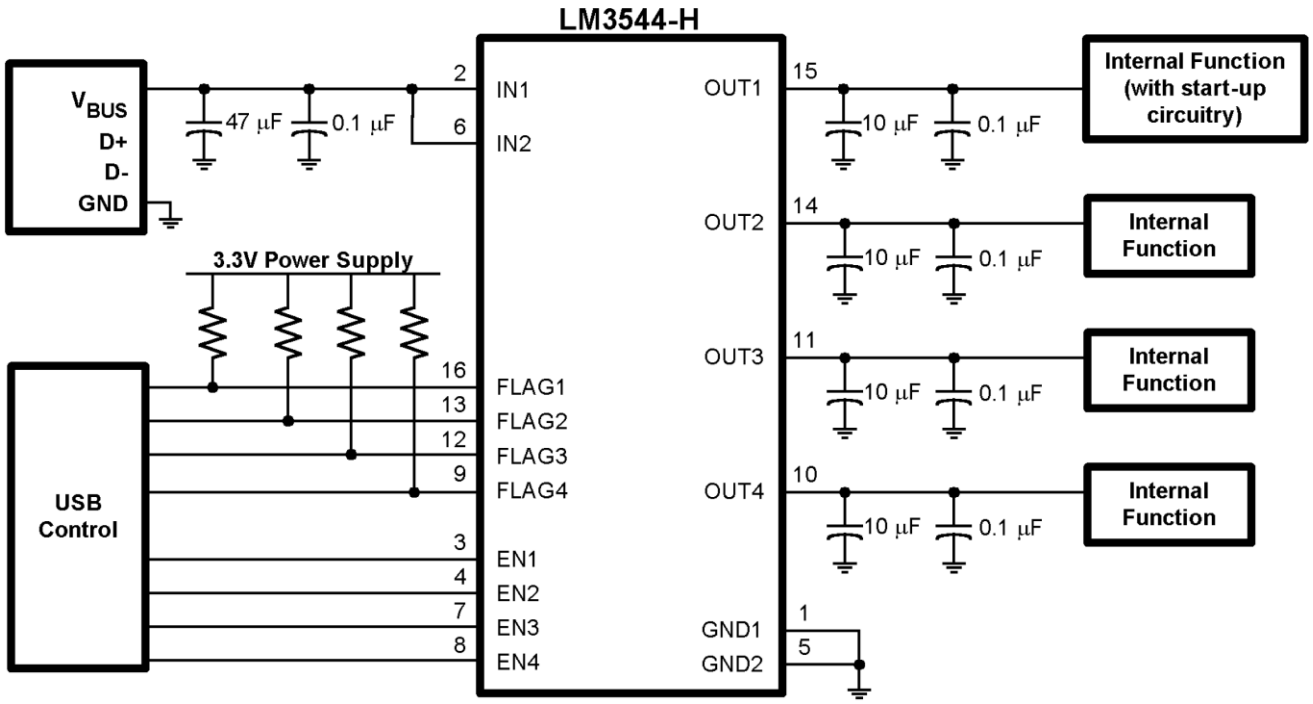


Figure 27. Using the LM3544 in USB Bus-Powered Functions

WAKE-ON-USB AND REMOTE WAKE-UP APPLICATIONS

The LM3544 can be used in desktop and notebook PC based root hubs to switch the power connection of USB devices between the main power source, used when the device is active, and a reduced power auxiliary supply. The auxiliary supply, used when the device is in suspend mode, can dramatically decrease the power consumption of a computer that contains devices that spend extended periods of time in suspend mode. This application also works especially well with devices configured for remote wake-up capabilities (i.e.: using a keystroke on a mouse or keyboard to awaken a suspended PC). A schematic showing an example of how the LM3544 can be configured to switch the power connection of a device between two separate sources is shown in Figure 28, below.

In the example, the logic signals EN and SRC control the power supply connections. If the EN signal is low, all four LM3544 switches will be open and neither supply will be connected to the bus. If EN and SRC are both high, switch 1 and switch 3 close, connecting the main power supply to the two bus power outputs. When EN is high and SRC is low, the auxiliary supply is connected to the power outputs through switches 2 and 4.

In order to allow the power-switching circuit to smoothly transition from one supply to another, delay networks must be placed before the enable pins. These delay networks account for the turn-on delay of the LM3544 switches by slowing the fall time of the enable signals. Rise times of these signals are not affected by the delay networks. Glitch free transition is assured as long as both supplies remain within operating specifications for a minimum of 5 ms after the logic signal SRC is toggled.

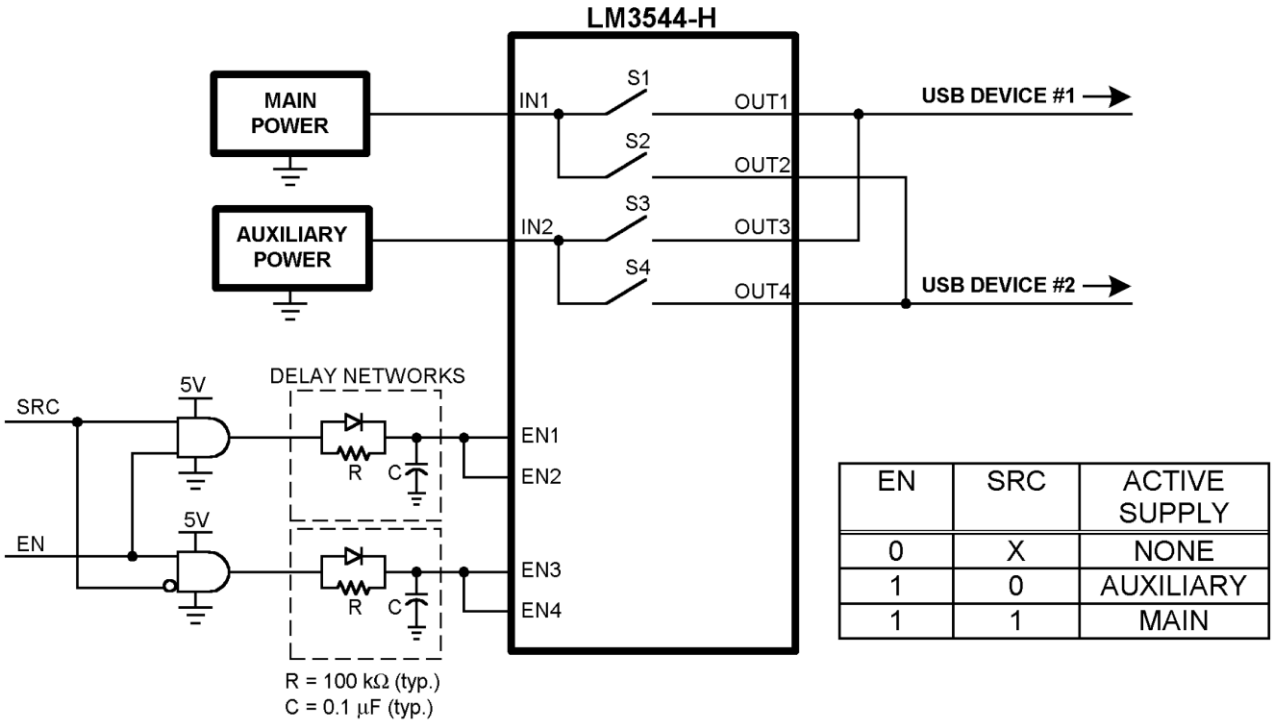


Figure 28. Using the LM3544 in a Wake-on-USB Application

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3544M-L/NOPB	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3544M-L
LM3544M-L/NOPB.A	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3544M-L
LM3544MX-L/NOPB	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3544M-L
LM3544MX-L/NOPB.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM3544M-L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

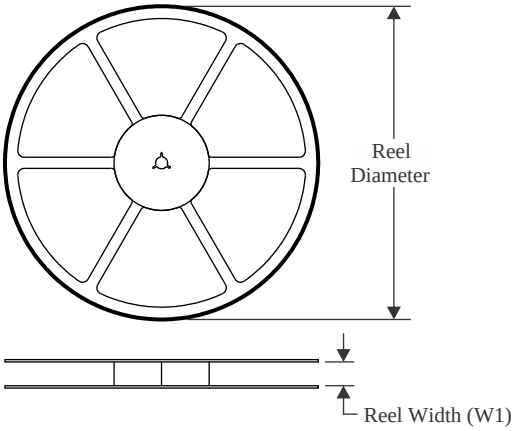
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

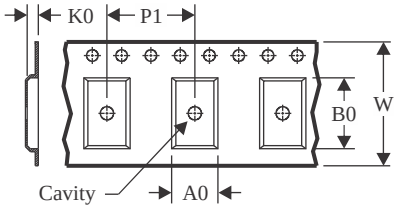
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

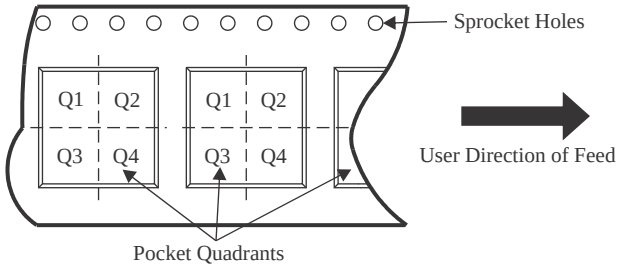


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

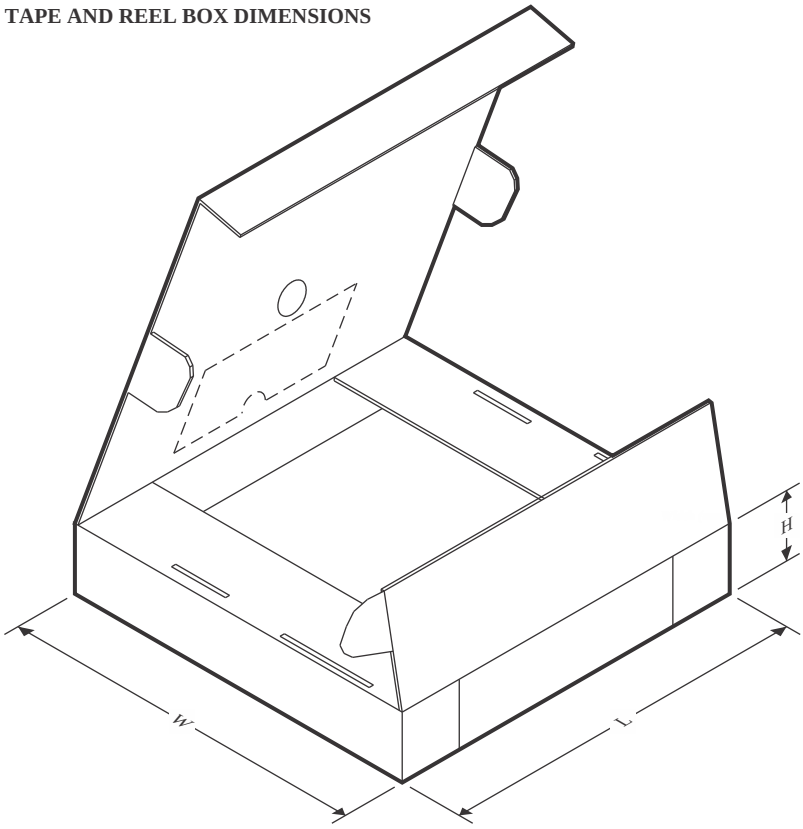
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3544MX-L/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

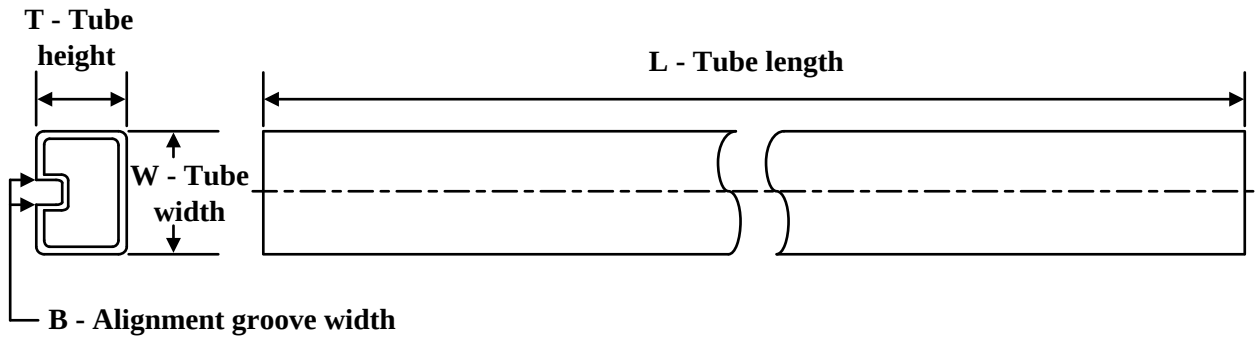
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3544MX-L/NOPB	SOIC	D	16	2500	356.0	356.0	35.0

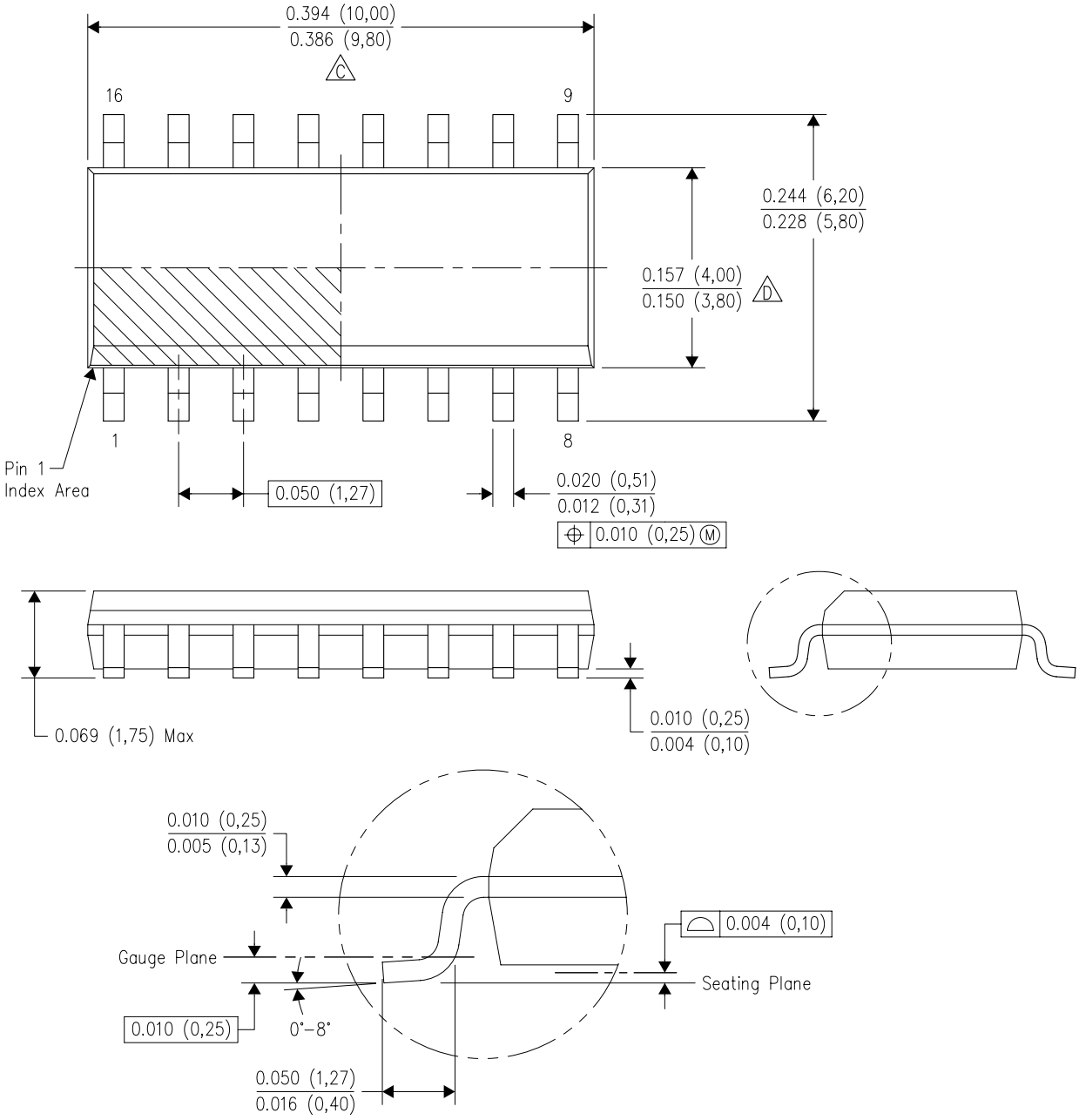
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3544M-L/NOPB	D	SOIC	16	48	495	8	4064	3.05
LM3544M-L/NOPB.A	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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Last updated 10/2025