LF156QML JFET Input Operational Amplifiers

Check for Samples: LF156QML

FEATURES

- **Advantages**
  - **Replace Expensive Hybrid and Module FET Op Amps**
  - **Rugged JFETs Allow Blow-Out Free Handling Compared with MOSFET Input Devices**
  - **Excellent for Low Noise Applications Using Either High or Low Source Impedance—Very Low 1/f Corner**
  - **Offset Adjust Does Not Degrade Drift or Common-Mode Rejection as in Most Monolithic Amplifiers**
  - **New Output Stage Allows Use of Large Capacitive Loads (5,000 pF) Without Stability Problems**
  - **Internal Compensation and Large Differential Input Voltage Capability**

APPLICATIONS

- **Precision High Speed Integrators**
- **Fast D/A and A/D Converters**
- **High Impedance Buffers**
- **Wideband, Low Noise, Low Drift Amplifiers**
- **Logarithmic Amplifiers**
- **Photocell Amplifiers**
- **Sample and Hold Circuits**

COMMON FEATURES

- **Low Input Bias Current: 30pA**
- **Low Input Offset Current: 3pA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Input Noise Current: 0.01 pA / $\sqrt{Hz}$**
- **High Common-Mode Rejection Ratio: 100 dB**
- **Large DC Voltage Gain: 106 dB**

UNCOMMON FEATURES

- **Extremely Fast Settling**
  - **Time to 0.01% 1.5µs**
- **Fast Slew Rate 12V/µs**
- **Wide Gain Bandwidth 5MHz**
- **Low Input Noise Voltage 12 nV / $\sqrt{Hz}$**

DESCRIPTION

This is the first monolithic JFET input operational amplifier to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). This amplifier features low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The device is also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Connection Diagrams

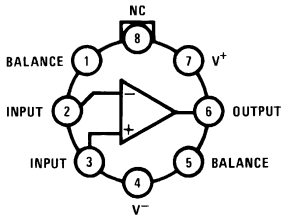
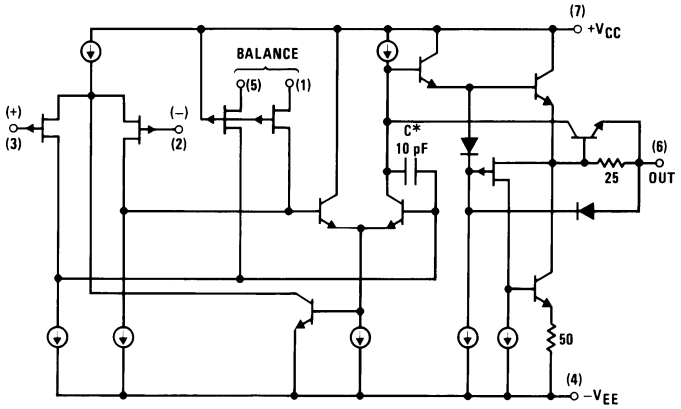


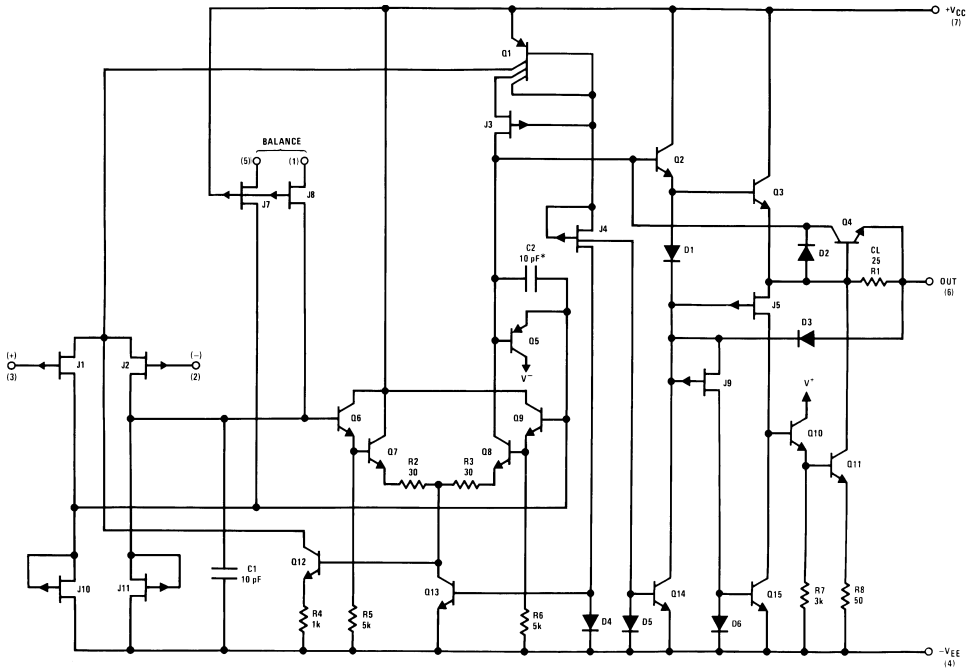
Figure 1. Top View
TO-99 Package (LMC)
See Package Number LMC

Simplified Schematic



*3pF in LF357 series.

Detailed Schematic



*C = 3pF in LF357 series.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage			±22V
Differential Input Voltage			±40V
Input Voltage Range(2)			±20V
Output Short Circuit Duration			Continuous
T_{Jmax}			150°C
Power Dissipation at T_A = 25°C(3)(4)		Still Air	560 mW
		500 LF/Min Air Flow	1200 mW
Thermal Resistance	θ_{JA}	Still Air	162°C/W
		400 LF/Min Air Flow	89°C/W
	θ_{JC}		32°C/W
Storage Temperature Range			−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 10 sec.)			300°C
ESD tolerance(5)			1200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate condition for which the device is functional, but do not ensure specific performance limits . For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}(maximum junction temperature), θ_{JA}(package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_D=(T_{Jmax}-T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(4) Maximum power dissipation (P_{Dmax})is defined by the package characteristics. Operating the part near the P_{Dmax} may cause the part to operate outside specified limits.
(5) Human body model, 100pF discharged through 1.5KΩ.

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LF156 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±5V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		V_{CC} = ±20V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
I_{IO}	Input Offset Current	V_{CC} = ±20V		-0.02	0.02	nA	1
				-20	20	nA	2, 3
$+I_{IB}$	Input Bias Current	V_{CC} = ±20V		-0.1	0.1	nA	1
				-10	50	nA	2, 3
		V_{CC} = ±20V, V_{CM} = -16V		-0.1	0.1	nA	1
				-10	50	nA	2, 3
		V_{CC} = ±20V, V_{CM} = 16V		-0.1	3.5	nA	1
				-10	60	nA	2, 3
$-I_{IB}$	Input Bias Current	V_{CC} = ±20V		-0.1	0.1	nA	1
				-10	50	nA	2, 3
		V_{CC} = ±20V, V_{CM} = -16V		-0.1	0.1	nA	1
				-10	50	nA	2, 3
		V_{CC} = ±20V, V_{CM} = 16V		-0.1	3.5	nA	1
				-10	60	nA	2, 3
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 20V to 10V, $-V_{CC}$ = -20V		85		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	$-V_{CC}$ = -20V to -10V, $+V_{CC}$ = 20V		85		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V		85		dB	1, 2, 3
I_{CC}	Power Supply Current				7.0	mA	1
					14	mA	2, 3
$+I_{OS}$	Short Circuit Current	V_O = 0V		-45	-15	mA	1
				-35	-10	mA	2
				-65	-15	mA	3
$-I_{OS}$	Short Circuit Current	V_O = 0V		15	45	mA	1
				10	35	mA	2
				15	65	mA	3
V_{CM}	Common Mode Voltage Range		See (1)	-11	11	V	1, 2, 3
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ		12		V	4, 5, 6
		R_L = 2KΩ	See (1)	10		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ			-12	V	4, 5, 6
		R_L = 2KΩ	See (1)		-10	V	4, 5, 6
A_{VS}	Large Signal Voltage Gain	R_L = 2KΩ, V_O = 0 to 10V		50		V/mV	4
				25		V/mV	5, 6
		R_L = 2KΩ, V_O = 0 to -10V		50		V/mV	4
				25		V/mV	5, 6

(1) Parameter specified by CMRR test.

LF156 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = ±5V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
+SR	Slew Rate	A_V = 1, R_{LOAD} = 2KΩ, C_L = 100pfd, V_I = -5V to +5V		7.5		V/µS	7
-SR	Slew Rate	A_V = 1, R_L = 2KΩ, C_L = 100pF, V_I = +5V to -5V		7.5		V/µS	7

Typical DC Performance Characteristics

Input Bias Current

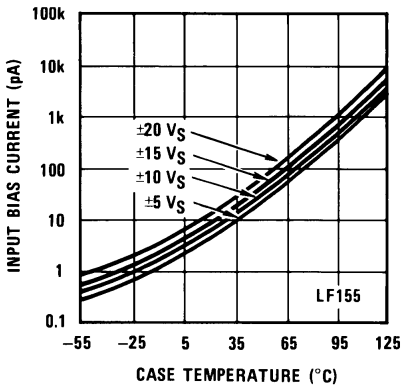


Figure 2.

Input Bias Current

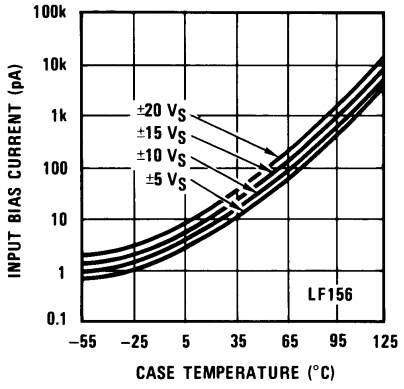


Figure 3.

Input Bias Current

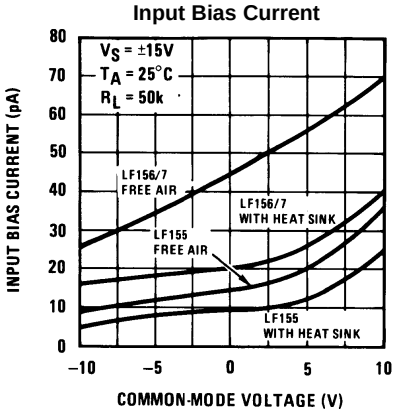


Figure 4.

Voltage Swing

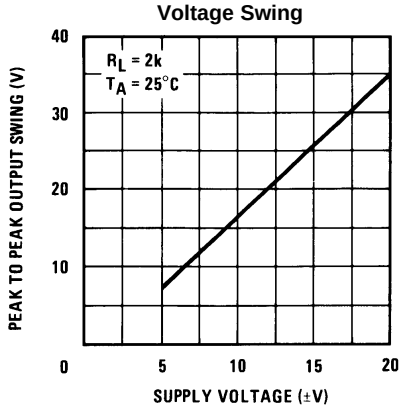


Figure 5.

Supply Current

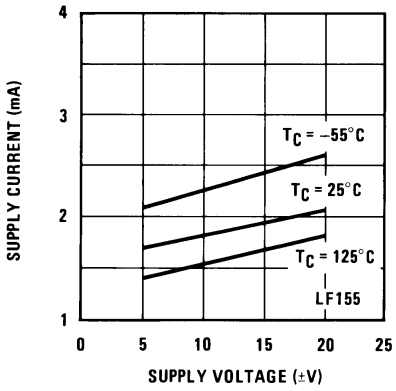


Figure 6.

Supply Current

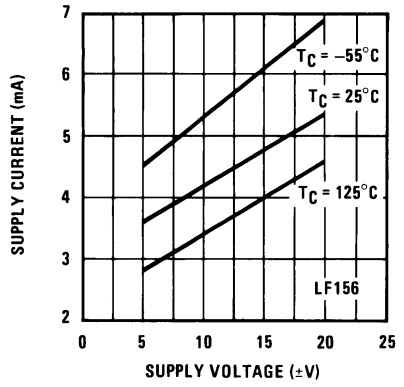


Figure 7.

Typical DC Performance Characteristics (continued)

Negative Current Limit

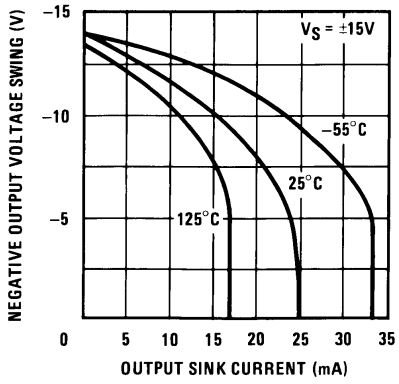


Figure 8.

Positive Current Limit

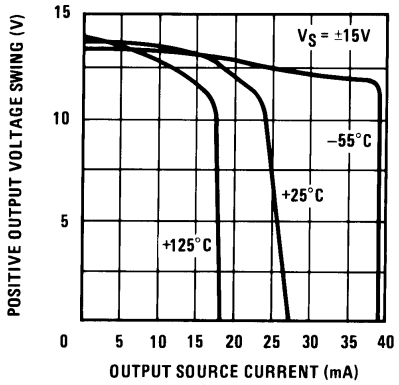


Figure 9.

Positive Common-Mode Input Voltage Limit

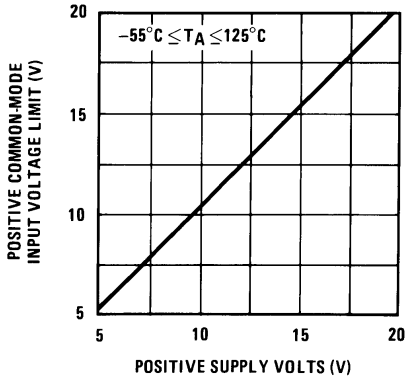


Figure 10.

Negative Common-Mode Input Voltage Limit

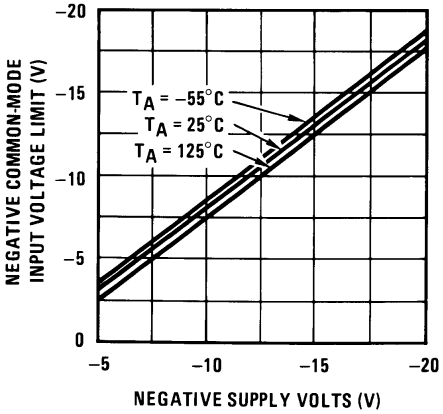


Figure 11.

Open Loop Voltage Gain

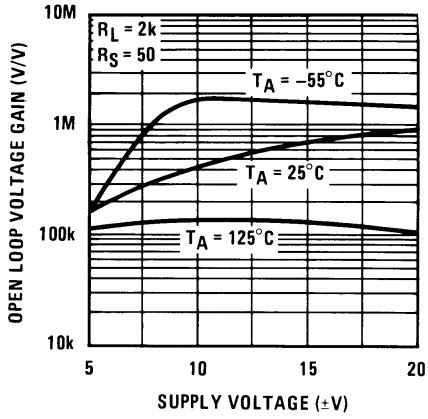


Figure 12.

Output Voltage Swing

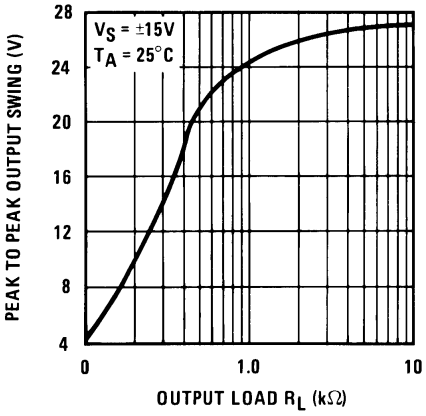


Figure 13.

Typical AC Performance Characteristics

Gain Bandwidth

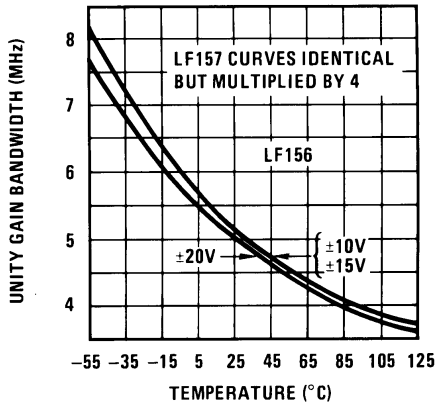


Figure 14.

Normalized Slew Rate

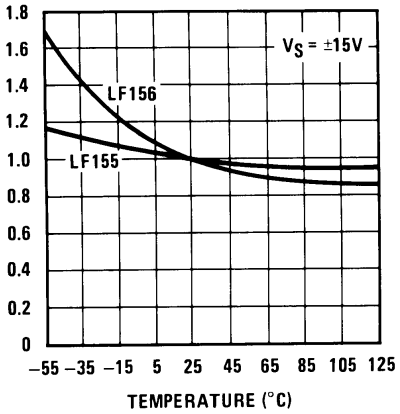


Figure 15.

Output Impedance

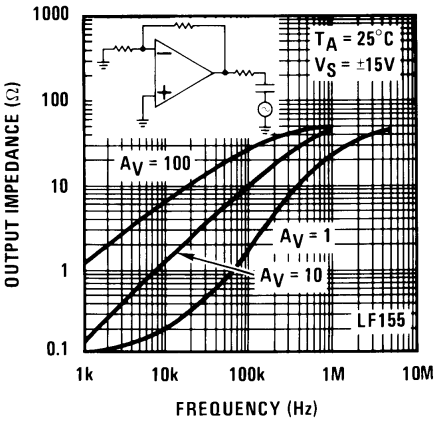


Figure 16.

Output Impedance

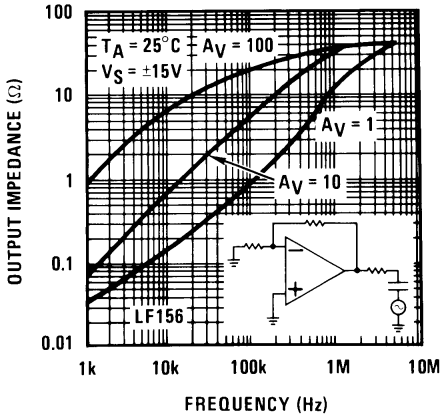


Figure 17.

LF156 Small Signal Pulse Response, A_V = +1

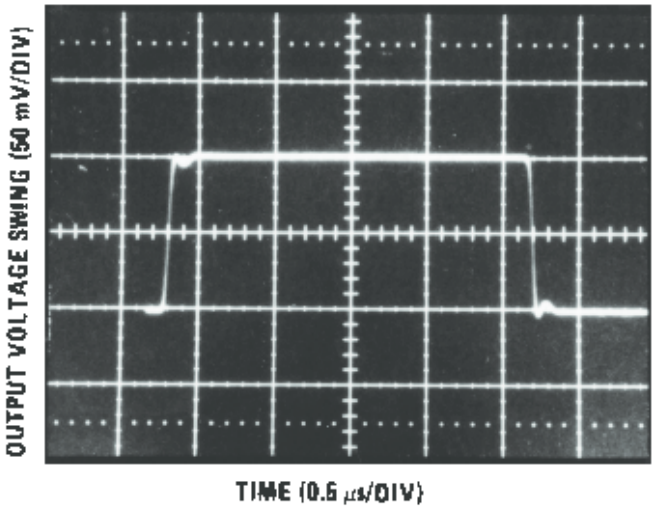


Figure .

LF156 Large Signal Puls Response, A_V = +1

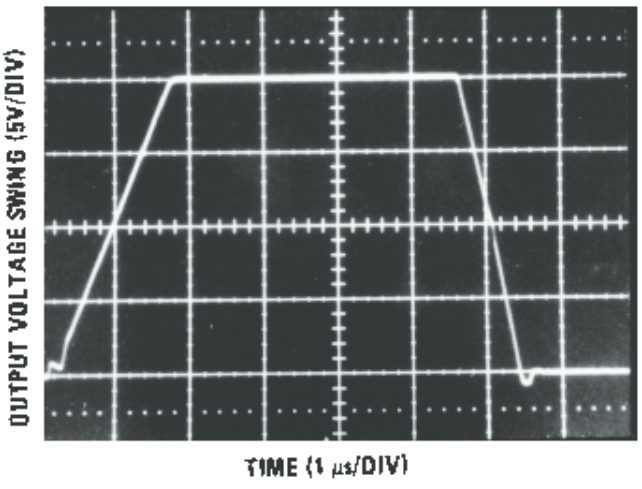


Figure 18.

Typical AC Performance Characteristics (continued)

Inverter Settling Time

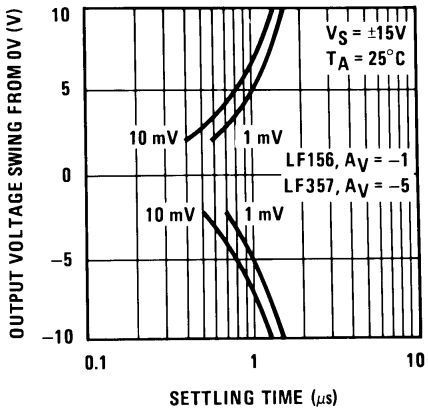


Figure 19.

Open Loop Frequency Response

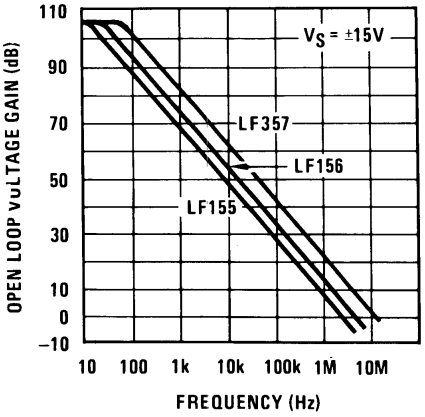


Figure 20.

Bode Plot

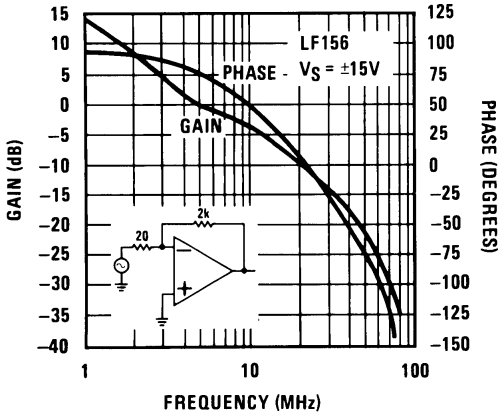


Figure .

Common-Mode Rejection Ratio

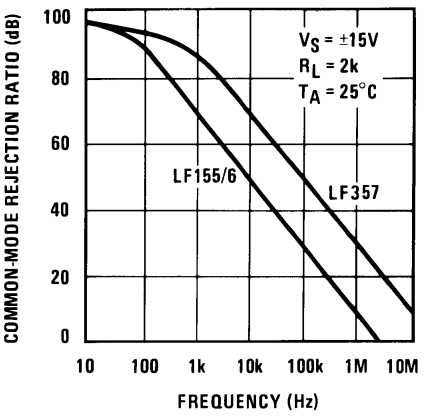


Figure 21.

Power Supply Rejection Ratio

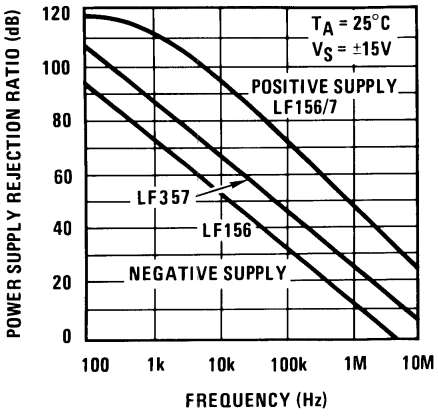


Figure 22.

Undistorted Output Voltage Swing

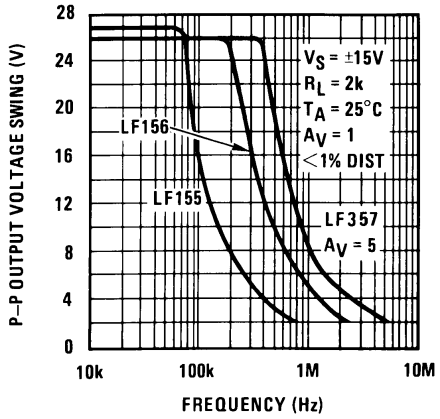


Figure 23.

Typical AC Performance Characteristics (continued)

Equivalent Input Noise Voltage

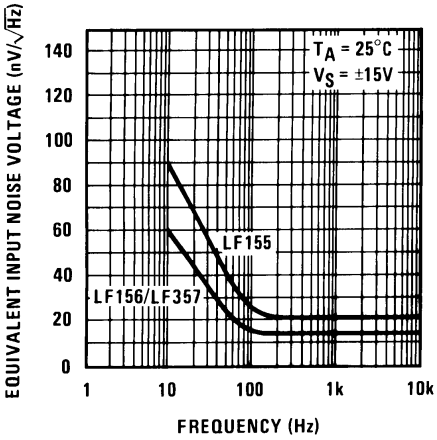


Figure 24.

Equivalent Input Noise Voltage (Expanded Scale)

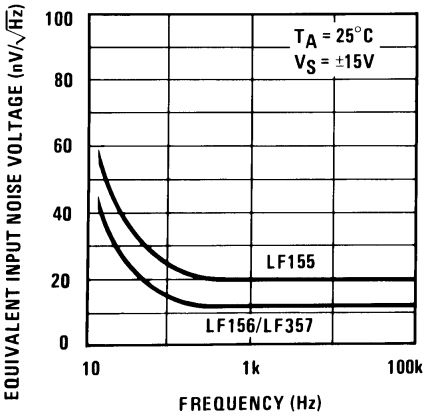


Figure 25.

APPLICATION HINTS

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

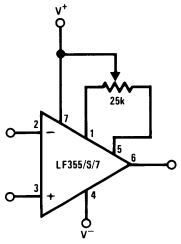
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

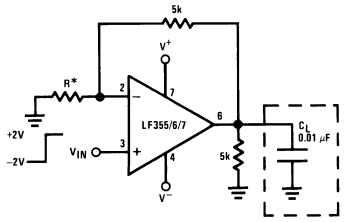
Typical Circuit Connections

Figure 26. V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

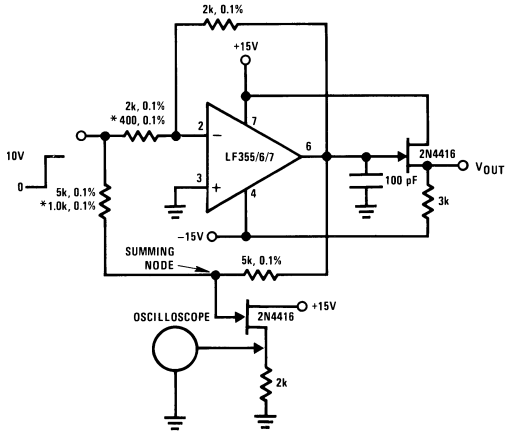
Figure 27. Driving Capacitive Loads



* LF156 R = 5k
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\mu F$.
Overshoot ≤ 20%
Settling time (t_s) ≈ 5µs

Typical Applications

Figure 28. Settling Time Test Circuit



- Settling time is tested with the LF156 connected as unity gain inverter.
- FET used to isolate the probe capacitance
- Output = 10V step

Figure 29. Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit) LF356

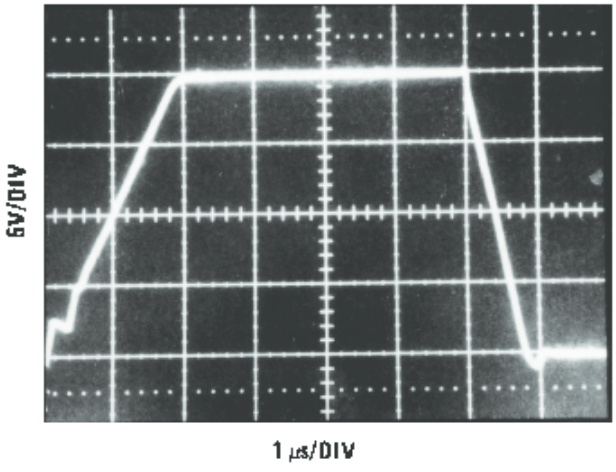
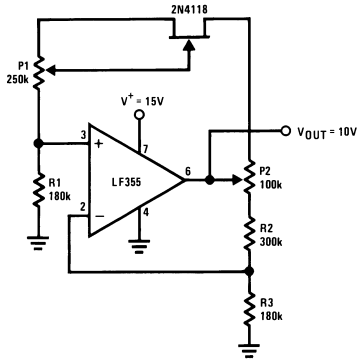
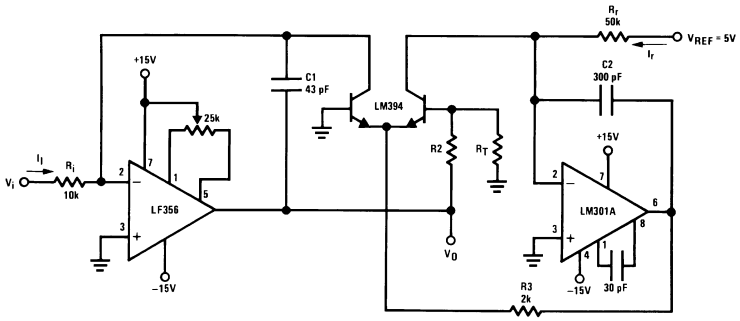


Figure 30. Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust

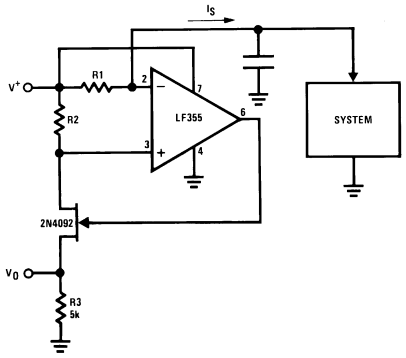
Figure 31. Fast Logarithmic Converter



- Dynamic range: $100\mu A \le I_i \le 1mA$ (5 decades), $|V_O| = 1V$/decade
- Transient response: 3μs for $\Delta I_i = 1$ decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

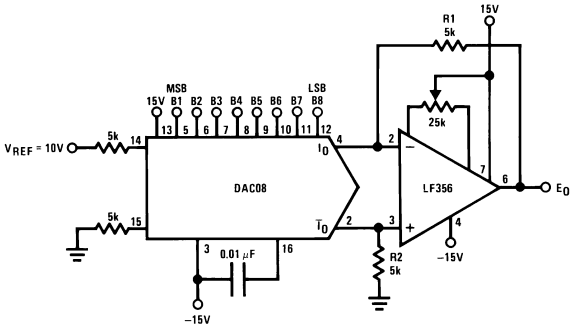
$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\ Ri}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)}$$

Figure 32. Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors

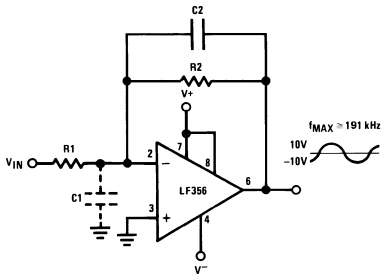
Figure 33. 8-Bit D/A Converter with Symmetrical Offset Binary Operation



- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

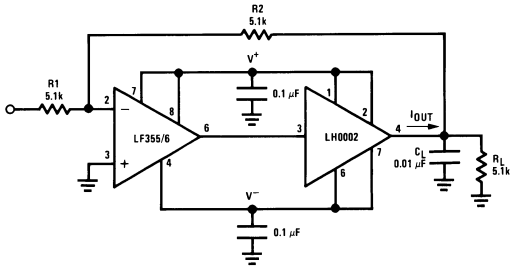
E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Figure 34. Wide BW Low Noise, Low Drift Amplifier



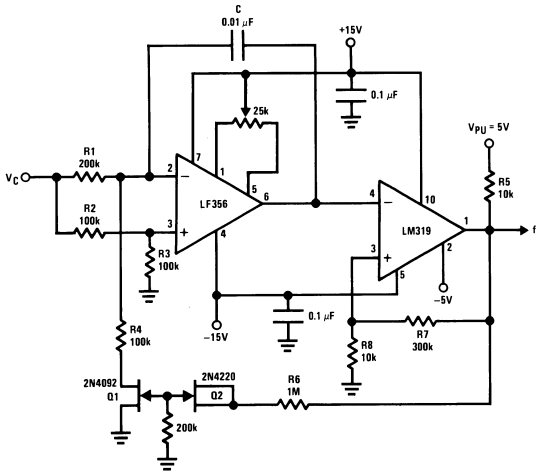
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$
- Parasitic input capacitance C1 ≃ 3pF interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

Figure 35. Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)}$≅150mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s$ (with C_L shown)
- No additional phase shift added by the current amplifier

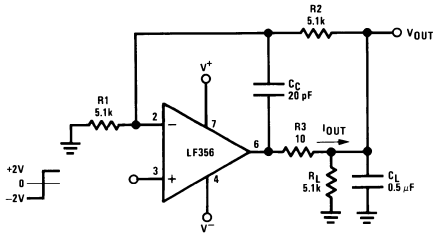
Figure 36. 3 Decades VCO



$$f = \frac{V_C\,(R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \leq V_C \leq 30V,\ 10\,Hz \leq f \leq 10\,kHz$$

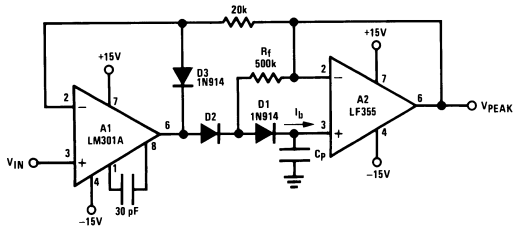
R1, R4 matched. Linearity 0.1% over 2 decades.

Figure 37. Isolating Large Capacitive Loads



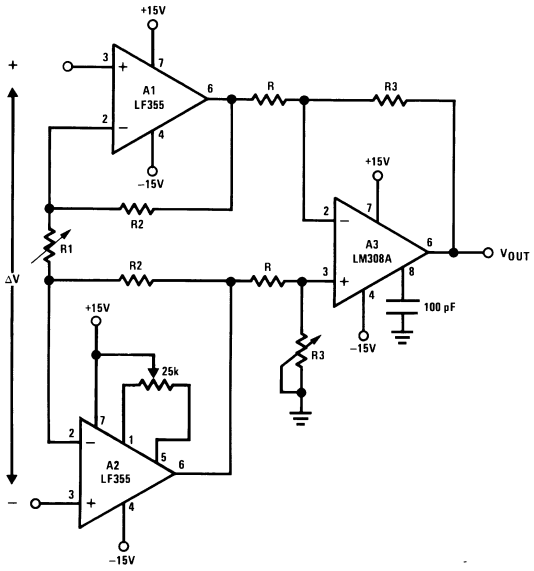
- Overshoot 6%
- t_s 10μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$: $\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s$ (with C_L shown)

Figure 38. Low Drift Peak Detector



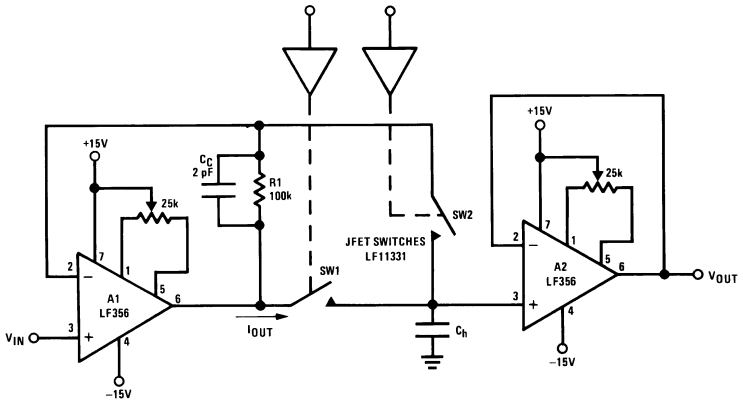
- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $\frac{1}{2}\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Figure 39. High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V$, $V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Figure 40. Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

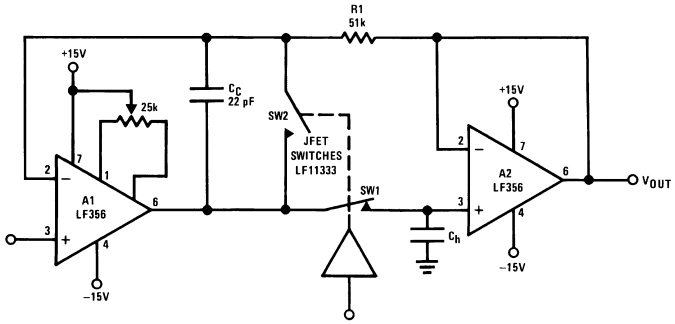
$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right] 1/2 \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA} \quad (1)$$

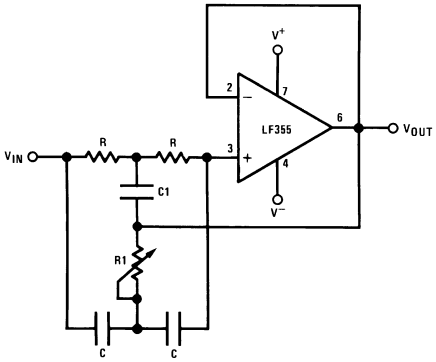
- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

Figure 41. High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.
  - No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added
  - propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

Figure 42. High Q Notch Filter



- 2R1 = R = 10MΩ
  - 2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

Revision History

Date Released	Revision	Section	Originator	Changes
03/10/06	A	New Released, Corporate format. Electrical Section Delete Drift Value table.	R. Malone	New Release, Corporate format 1 MDS data sheet converted into a Corp. data sheet format. Following MDS data sheet will be Archived MNLF156-X, Rev. 2A0. Delete Drift Value table from Electrical Section. Reson: Referenced product is 883 only.
03/25/13	A	All	-	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF156H/883	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	No	Call TI	Call TI	-55 to 125	LF156H/883 Q ACO LF156H/883 Q >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

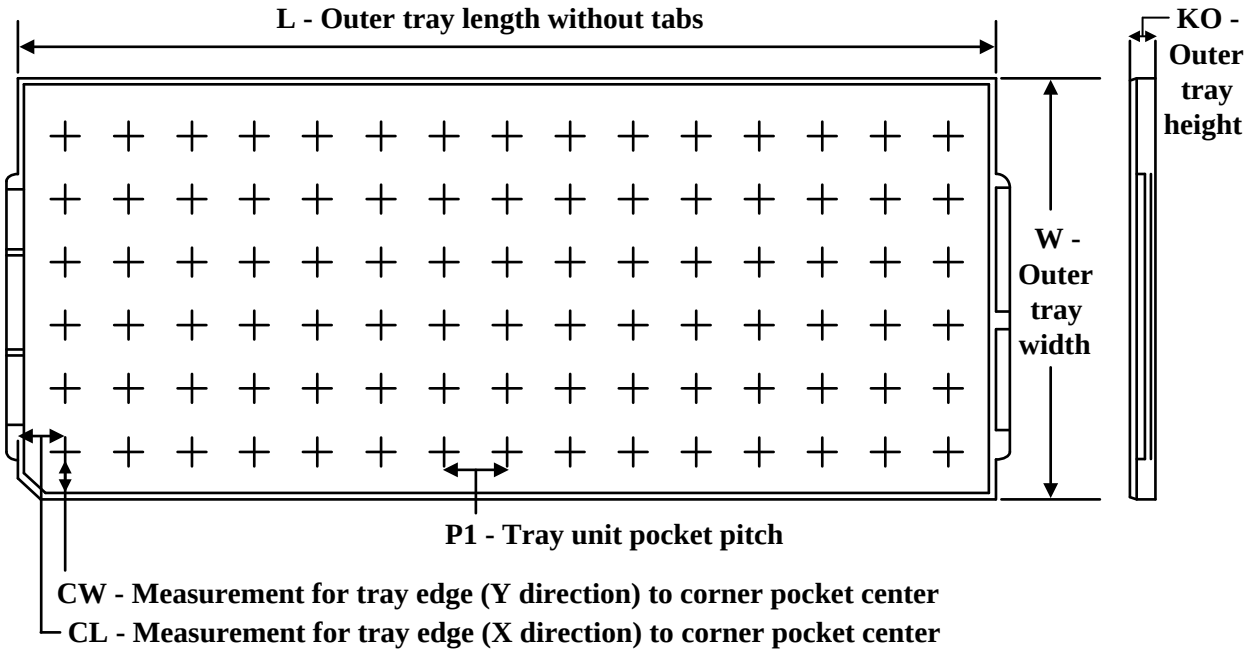
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

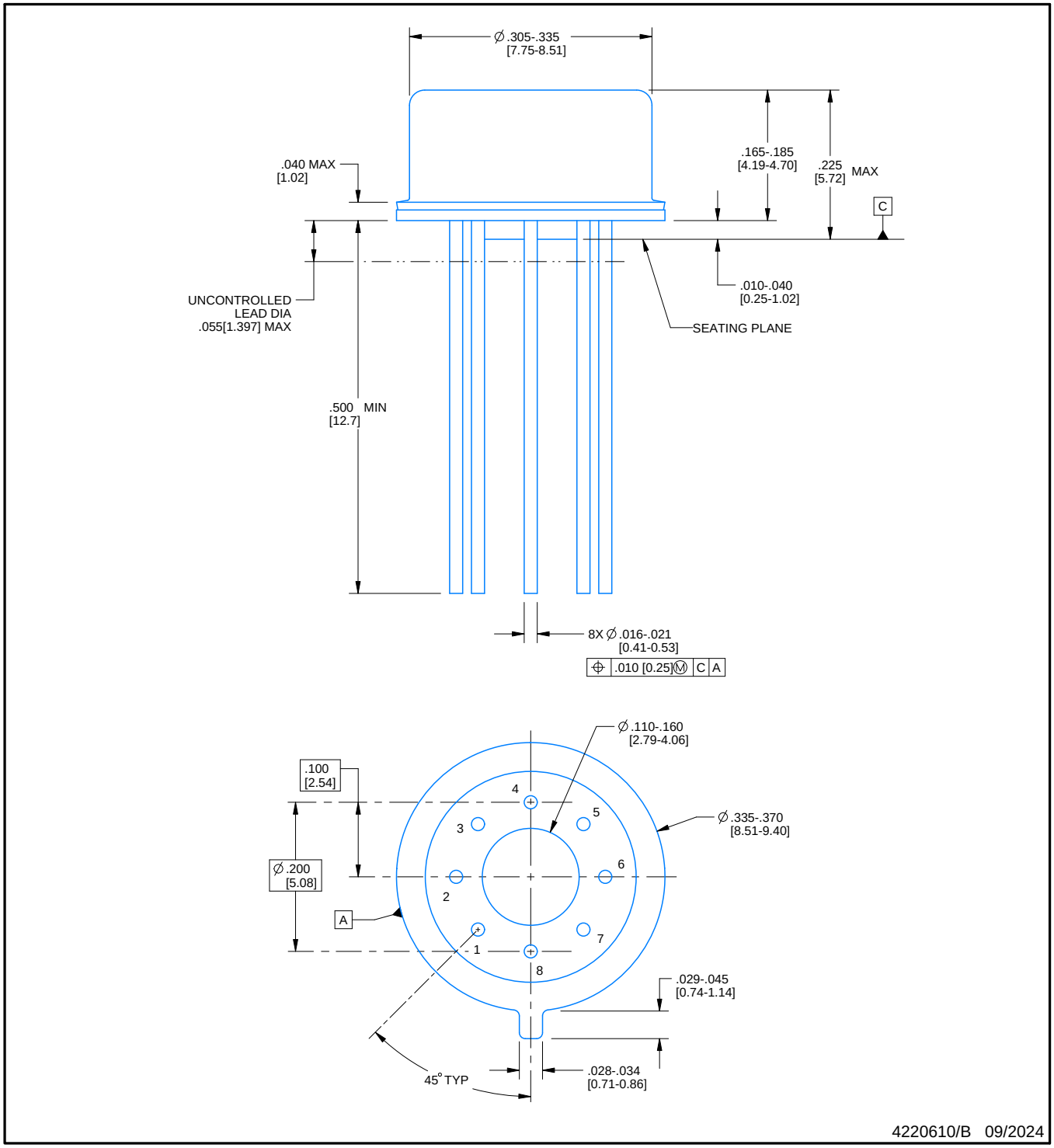
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LF156H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

PACKAGE OUTLINE

LMC0008A

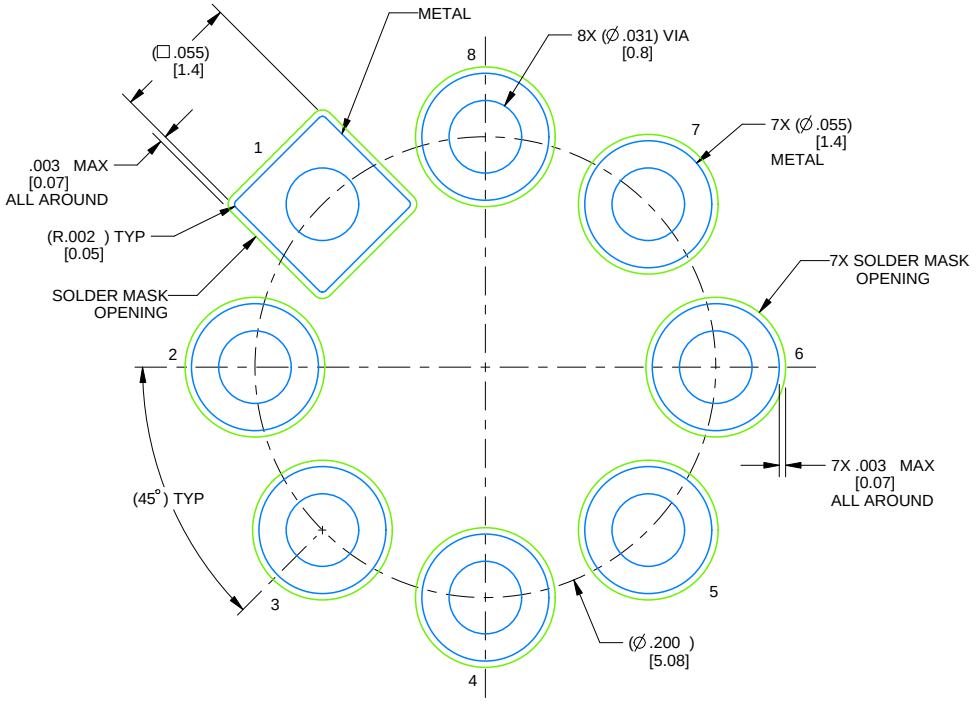
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

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