ISO7420FCC 低功耗双通道数字隔离器

1 特性

- 信号传输速率：50Mbps（5V 电源供电时）
- 在默认模式下，输出为低电平
- 输入引脚上的集成噪声滤波器
- 低功耗：典型值为每通道 I_{CC}
  - 1Mbps 时为 1.8mA，25Mbps 时为 3.9mA（5V 电源供电时）
  - 1Mbps 时为 1.4mA，25Mbps 时为 2.6mA（3.3V 电源供电时）
- 低传播延迟：典型值为 20ns（5V 电源供电时）
- 通道到通道输出偏斜：最大值为 2ns
- 3.3V 和 5V 电平转换
- 宽 T_A 额定范围：-40°C 至 125°C
- 60KV/µs 瞬态抗扰度，典型值（5V 电源供电时）
- 低辐射
- 隔离隔栅寿命：> 25 年
- 工作电压范围为 2.7V 至 5.5V
- 窄体 SOIC-8 封装
- 安全及监管认证
  - 符合 DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 标准的 $4242V_{PK}$ 隔离
  - 符合 UL 1577 标准且长达 1 分钟的 $2.5KV_{RMS}$ 隔离
  - CSA 组件验收通知 5A、IEC 60950-1 和 IEC 61010-1 终端设备标准
  - GB4943.1-2011 CQC 认证

2 应用

- 在下列应用中的光电耦合器替代产品：
  - 工业用 FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™数据总线
  - 伺服控制接口
  - 电机控制
  - 电源
  - 电池组

3 说明

ISO7420FCC 提供符合 UL 标准的长达 1 分钟的高达 $2500V_{RMS}$电流隔离，以及符合 VDE 标准的 $4242V_{PK}$。这个器件有两个隔离通道。每个通道有一个逻辑输入和输出缓冲器，这两个器件由一个二氧化硅 (SiO_2) 绝缘隔栅进行分离。与隔离式电源一起使用，这个器件可防止数据总线或者其它电路上的噪音电流进入本地接地，并且干扰或损坏敏感电路。后缀 F 表示在失效防护条件下的低输出选项（参阅表2）。该器件具有集成噪声滤波器，可适用于严苛环境，在这种环境下，短噪声脉冲可能会出现在器件输入引脚上。

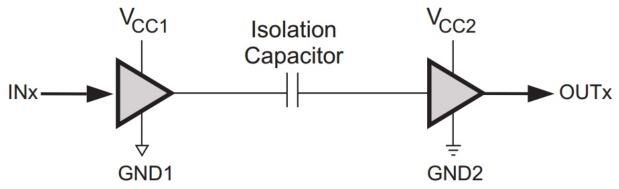
ISO7420FCC 具有晶体管-晶体管逻辑电路 (TTL) 输入阈值，工作电压范围为 2.7V 至 5.5V。通过 2.7V 或 3.3V 电源供电时，所有输入均可耐受 5V 电压。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
ISO7420FCC	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



English Data Sheet: SLLSED3

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (January 2014) to Revision C — Page

- 已添加 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- VDE 标准更改为 DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 1
- 将 VDE 标准更改为“DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12” 1
- Changed Note 1 Figure 12 10
- Changed Figure 13 10

Changes from Revision A (July 2013) to Revision B — Page

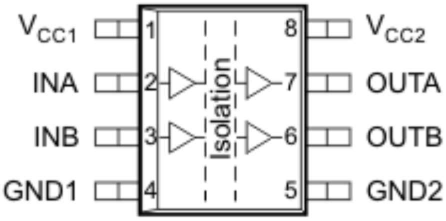
- 更改了“安全及监管认证”列表 1
- Changed the V_{IH} MAX value From: V_{CC} To: 5.5V in the RECOMMENDED OPERATING CONDITIONS table 4
- Changed the V_{PR} and V_{IOTM} parameter From: DIN EN 60747-5-2 To: DIN EN 60747-5-5 in the INSULATION CHARACTERISTICS table 13
- Changed the REGULATORY INFORMATION table 13
- Changed the title of Figure 16 From: θ_{JC} Thermal Derating Curve per DIN EN 60747-5-2 To: θ_{JC} Thermal Derating Curve per DIN EN 60747-5-5 14

Changes from Original (June 2013) to Revision A — Page

- Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} 5
- Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} and removed Note 1 5
- Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} and removed Note 1 6
- Changed Figure 3 X axis values 8

5 Pin Configuration and Functions

ISO7420: D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	–	Ground connection for V_{CC1}
GND2	5	–	Ground connection for V_{CC2}
INA	2	I	Input, channel A
INB	3	I	Input, channel B
OUTA	7	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	–	Power supply, V_{CC1}
V_{CC2}	8	–	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
V_{IO}	Voltage at INx, OUTx	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
$T_{J(Max)}$	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.7		5.5	V
I_{OH}	High-level output current ($V_{CC} \geq 3$ V)		–4			mA
	High-level output current ($V_{CC} < 3$ V)		-2			mA
I_{OL}	Low-level output current				4	mA
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
t_{ui}	Input pulse duration	≥ 4.5-V Operation	20			ns
		< 4.5-V Operation	25			
1 / t_{ui}	Signaling rate	≥ 4.5-V Operation	0		50	Mbps
		< 4.5-V Operation	0		40	
T_J (1)	Junction temperature		–40		136	°C
T_A	Ambient temperature		-40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Power Dissipation Characteristics* table.

6.4 Thermal Information

THERMAL METRIC (1)		ISO7420FCC D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_{CC1} and V_{CC2} = 5 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 12.		V_{CC2} – 0.5	4.8		V
		I_{OH} = –20 μA; see Figure 12.		V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 12.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 12.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				450		mV
I_{IH}	High-level input current	INx = V_{CC1}				10	μA
I_{IL}	Low-level input current	INx = 0 V		–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V; see Figure 14.		25	60		kV/μs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC1} or 0 V, AC Input: C_L = 15pF		0.5	1.1	mA
I_{CC2}					3	4.6	
I_{CC1}		10 Mbps	C_L = 15pF		1	1.5	
I_{CC2}					4	6	
I_{CC1}		25 Mbps			1.7	2.5	
I_{CC2}					6	8.5	
I_{CC1}		50 Mbps			2.7	4	
I_{CC2}					8.5	12	

6.6 Electrical Characteristics: V_{CC1} and V_{CC2} = 3.3 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 12.		V_{CC2} – 0.5	3		V
		I_{OH} = –20 μA; see Figure 12.		V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 12.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 12.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				425		mV
I_{IH}	High-level input current	INx = V_{CC1}				10	μA
I_{IL}	Low-level input curre	INx = 0 V		-10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V; see Figure 14.		25	40		kV/μs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC1} or 0 V, AC Input: C_L = 15pF		0.3	0.8	mA
I_{CC2}					2.4	3.3	
I_{CC1}		10 Mbps	C_L = 15pF		0.6	1.2	
I_{CC2}					3.1	4.5	
I_{CC1}		25 Mbps			1	2	
I_{CC2}					4.2	6.1	
I_{CC1}		40 Mbps			1.3	2.3	
I_{CC2}					5.3	7.5	

6.7 Electrical Characteristics: V_{CC1} and V_{CC2} = 2.7 V

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 12.		V_{CC2} – 0.3	2.5		V
		I_{OH} = –20 μA; see Figure 12.		V_{CC2} – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 12.			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 12.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				350		mV
I_{IH}	High-level input current	INx = V_{CC1}				10	μA
I_{IL}	Low-level input current	INx = 0 V		–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V; see Figure 14.		25	35		kV/μs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC1} or 0 V, AC Input: C_L = 15pF		0.15	0.4	mA
I_{CC2}					2.1	3.1	
I_{CC1}		10 Mbps	C_L = 15pF		0.4	0.7	
I_{CC2}					2.7	4	
I_{CC1}		25 Mbps			0.7	1.2	
I_{CC2}					3.6	5	
I_{CC1}		40 Mbps			1	1.7	
I_{CC2}					4.4	6.3	

6.8 Power Dissipation Characteristics

THERMAL METRIC			ISO7420FCC	UNIT
			D (SOIC)	
			8 PINS	
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-Mbps 50% duty-cycle square wave	120	mW

6.9 Switching Characteristics: V_{CC1} and V_{CC2} = 5 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 12.	10	20	37	ns
PWD[1]	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$			2.5	5	ns
$t_{sk(o)}$ [2]	Channel-to-channel output skew time				2	ns
$t_{sk(pp)}$ [3]	Part-to-part skew time				12	ns
t_r	Output signal rise time	See Figure 12.		2.5		ns
t_f	Output signal fall time			2.5		ns
t_{GS}	Pulse width of glitches suppressed by the input filter			12		ns
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 13.		8		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.10 Switching Characteristics: V_{CC1} and V_{CC2} = 3.3 V ± 10%

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 12.	10	22	40	ns
PWD[1]	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$				3	ns
$t_{sk(o)}$ [2]	Channel-to-channel output skew time				2	ns
$t_{sk(pp)}$ [3]	Part-to-part skew time				19	ns
t_r	Output signal rise time	See Figure 12.		3		ns
t_f	Output signal fall time			3		ns
t_{GS}	Pulse width of glithes suppressed by the input filter			12.5		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 13.		8		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.11 Switching Characteristics: V_{CC1} and V_{CC2} = 2.7 V

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 12.	15	26	45	ns
PWD[1]	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$				3	ns
$t_{sk(o)}$ [2]	Channel-to-channel output skew time				2	ns
$t_{sk(pp)}$ [3]	Part-to-part skew time				22	ns
t_r	Output signal rise time	See Figure 12.		3		ns
t_f	Output signal fall time			3		ns
t_{GS}	Pulse width of glitches suppressed by the input filter			13.5		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 13.		8		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.12 Typical Characteristics

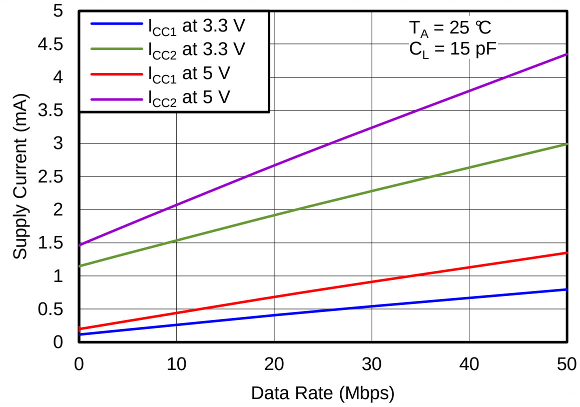


Figure 1. Supply Current Per Channel vs Data Rate

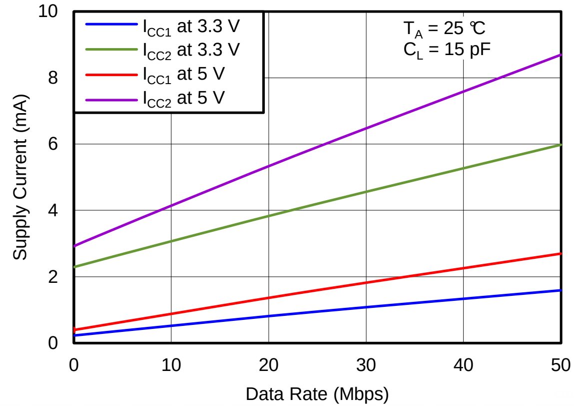


Figure 2. Supply Current for Both Channels vs Data Rate

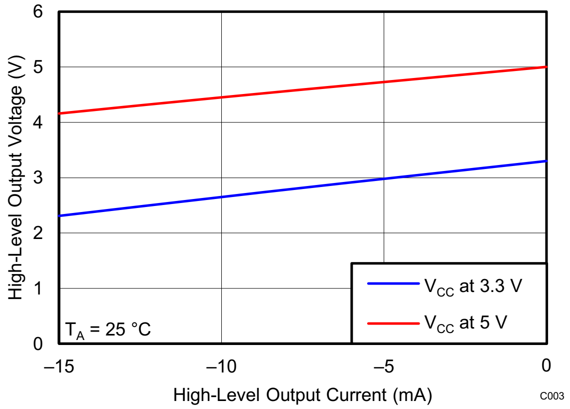


Figure 3. High-Level Output Voltage vs High-Level Output Current

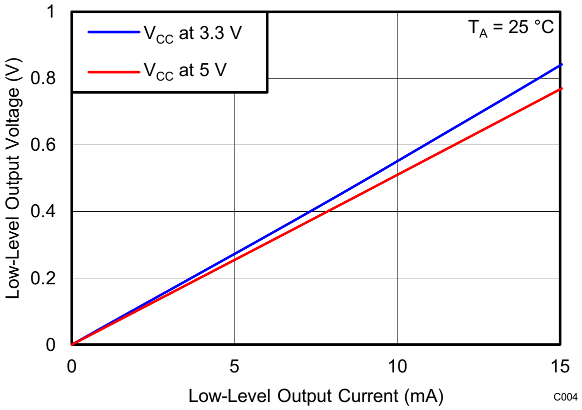


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

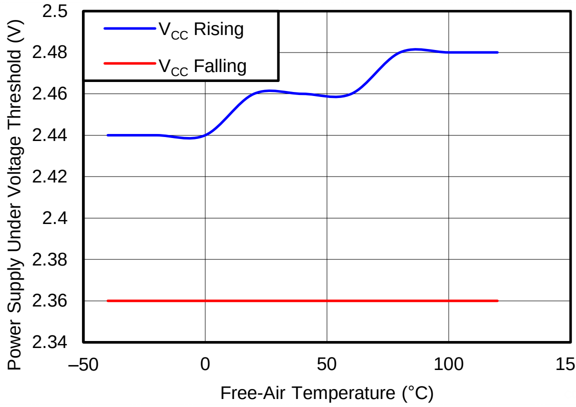


Figure 5. V_{CC1} and V_{CC2} Undervoltage Threshold vs Free-Air Temperature

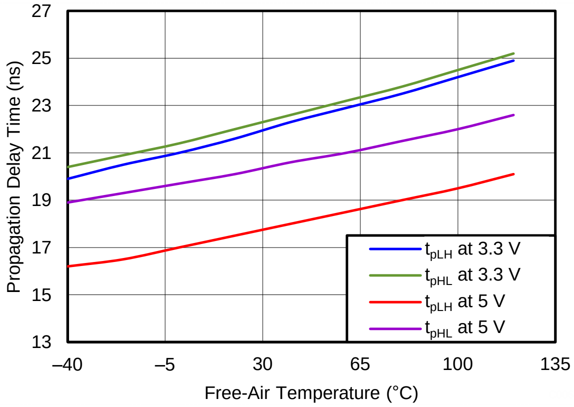


Figure 6. Propagation Delay Time vs Free-Air Temperature

Typical Characteristics (continued)

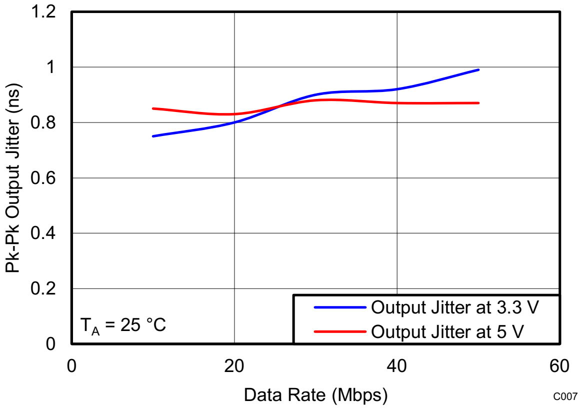


Figure 7. Output Jitter vs Data Rate

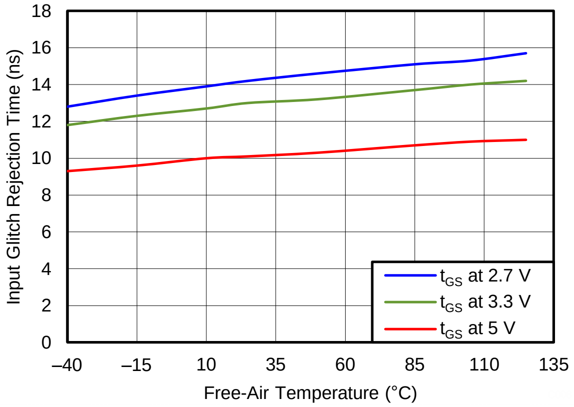


Figure 8. Input Glitch Suppression Time vs Free-Air Temperature

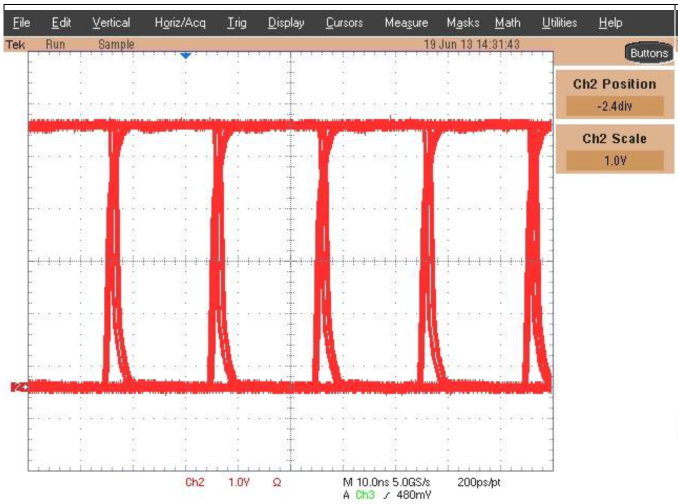


Figure 9. Eye Diagram at 50 Mbps, 5V at 25°C

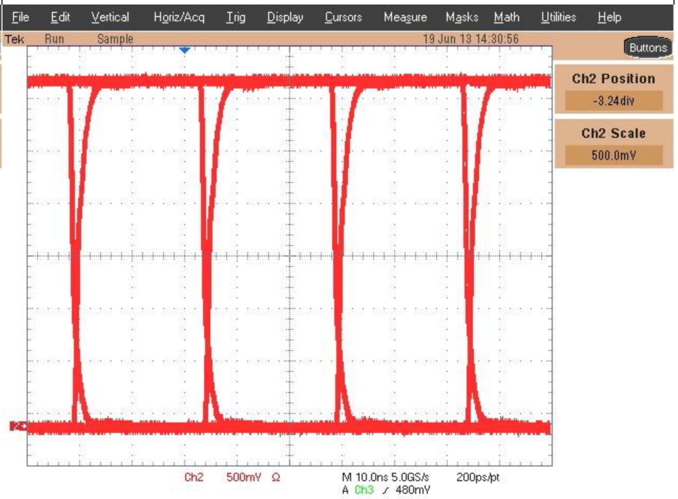


Figure 10. Eye Diagram at 40 Mbps, 3.3V at 25°C

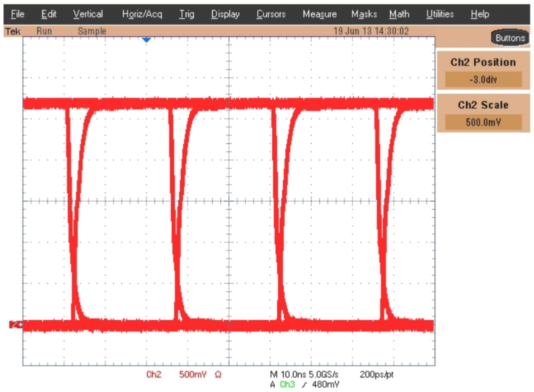
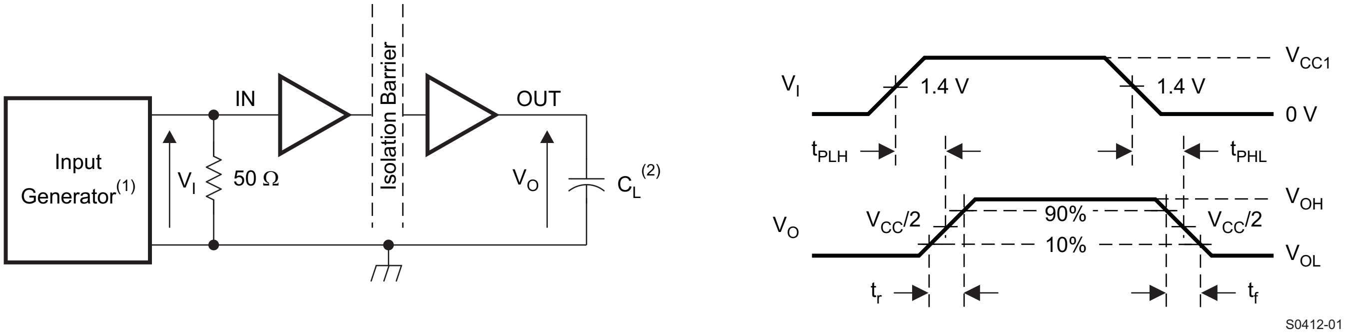


Figure 11. Eye Diagram at 40 Mbps, 2.7V at 25°C

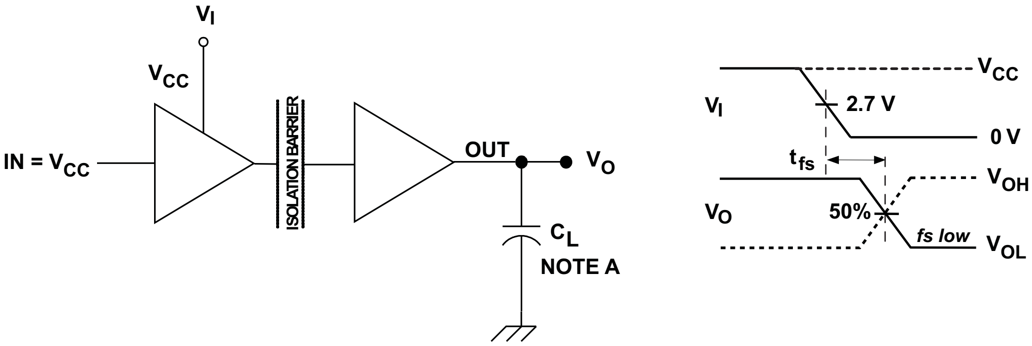
7 Parameter Measurement Information



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

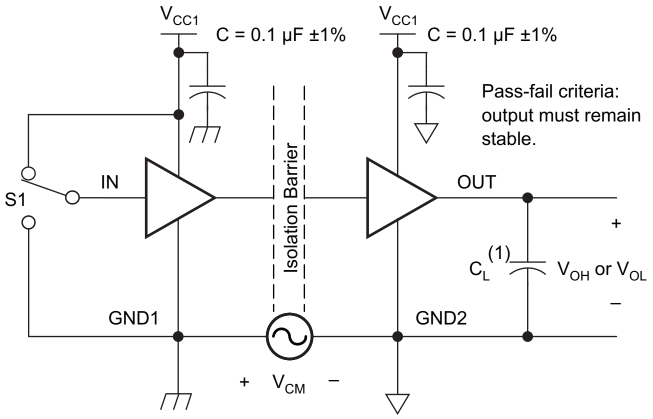
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 12. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 15 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 50 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

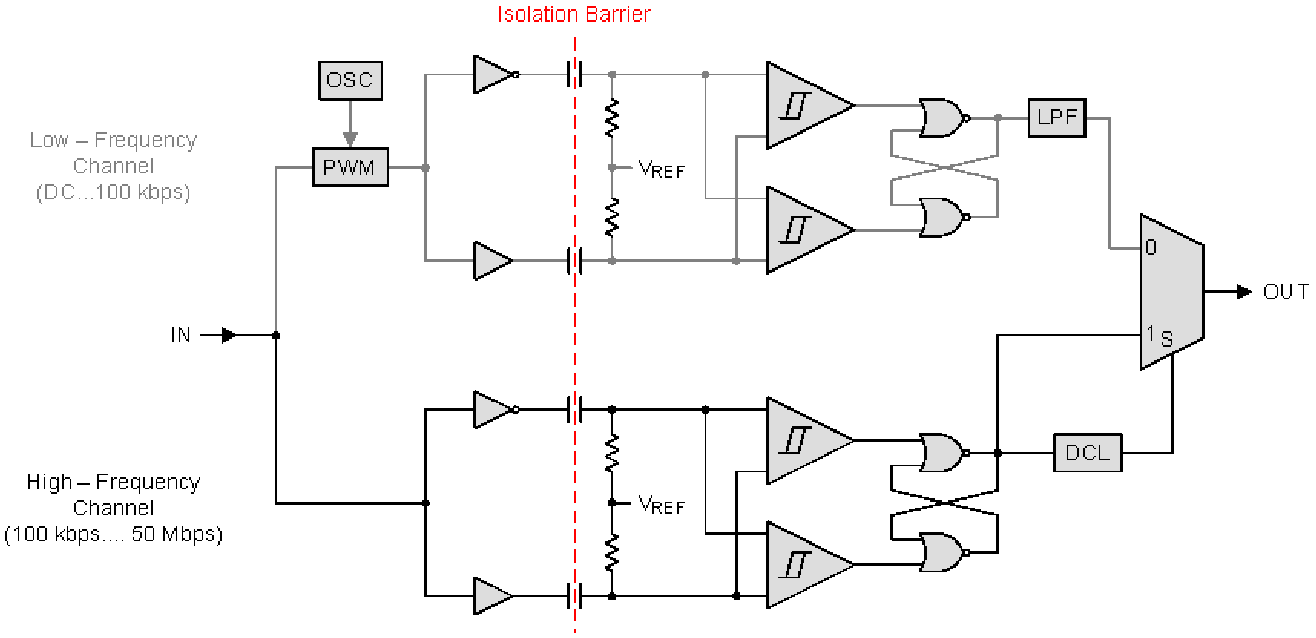


Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

8.3.1 Insulation and Safety-Related Specifications for SOIC-8 Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(1)				
V_{IORM}	Maximum working isolation voltage		566	V_{PK}
V_{PR}	Input-to-output test voltage	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC	906	V_{PK}
		Method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	
		After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	680	
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PK}
R_S	Isolation resistance	V_{IO} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 sec (qualification) V_{TEST} = 1.2 x V_{ISO}= 3000 V_{RMS}, t = 1 sec (100% production)	2500	V_{RMS}

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Material group		II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III

8.3.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Isolation voltage, 4242 V_{PK}; Maximum Working Isolation Voltage, 566 V_{PK}	3000 V_{RMS} Isolation Rating; 400 V_{RMS} Basic and 200 V_{RMS} Reinforced Insulation maximum working voltage per CSA 60950-1-07+A1 and IEC 60950-1 (2nd Ed)+A1; 300 V_{RMS} Basic and 150 V_{RMS} Reinforced Insulation maximum working voltage per CSA 61010-1-12 and IEC 61010-1 (3rd Ed)	Single Protection, 2500 V_{RMS} (1)	Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109540

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

8.3.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 115.1°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			197	mA
		θ_{JA} = 115.1°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			302	
		θ_{JA} = 115.1°C/W, V_I = 2.7 V, T_J = 150°C, T_A = 25°C			402	
T_S	Maximum Safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

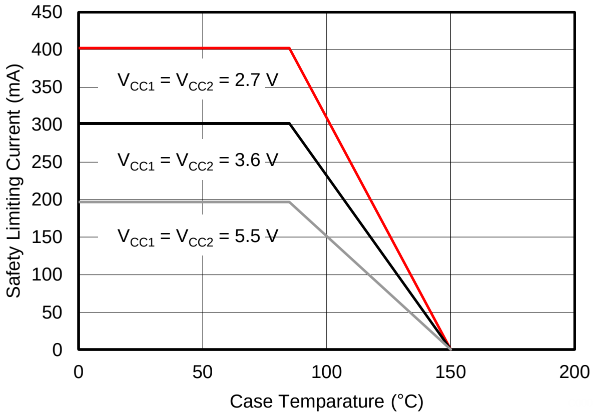


Figure 16. θ_{JC} Thermal Derating Curve per VDE

8.4 Device Functional Modes

Table 2. Function Table(1)

V_{CC1}	V_{CC2}	INPUT INA, INB	OUTPUT OUTA, OUTB
PU	PU	H	H
		L	L
		Open	L(2)
PD	PU	X	L(2)
X	PD	X	Undetermined

(1) PU = Powered up (V_{CC} ≥ 2.7 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level
(2) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics

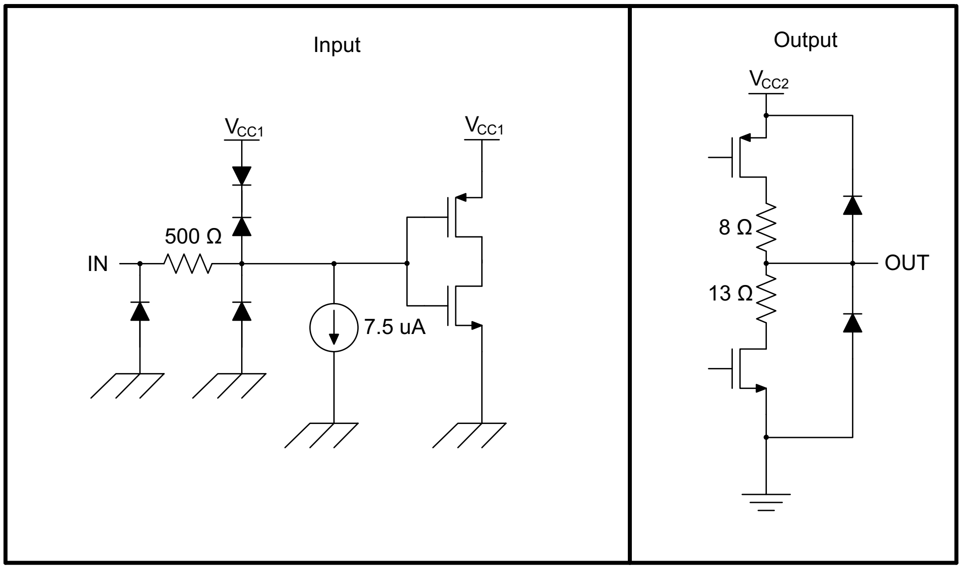


Figure 17. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO7420FCC utilize single-ended TTL-logic switching technology. Its supply voltage range is from 2.7 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (i.e. µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

ISO7420FCC can be used to isolate power MOSFETs from sensitive logic circuitry in Switch Mode Power Supplies (SMPS) as shown in Figure 18. Low default output of ISO7420FCC is critical for proper operation of power MOSFETs in such applications.

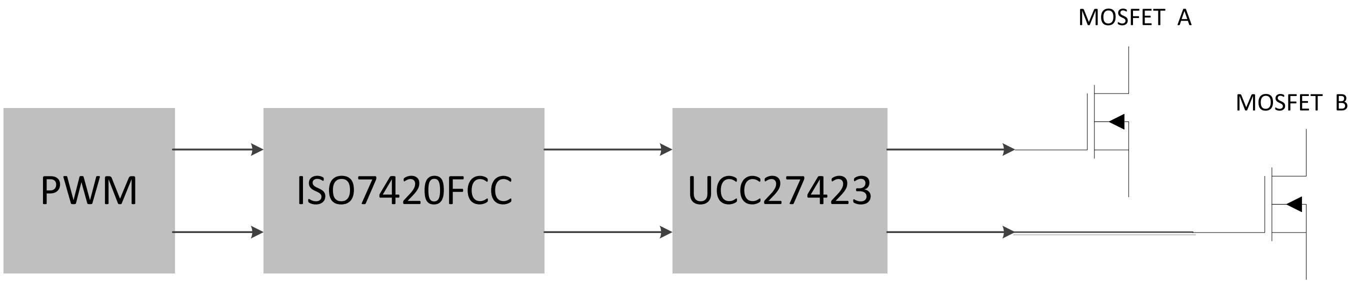


Figure 18. Isolated Switch Mode Power Supply

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7420FCC only requires two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

9.2.2.1 Supply Current Equations

9.2.2.1.1 Maximum Supply Current Equations

(Calculated over recommended operating temperature range and Silicon process variation).

At $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$:

$$I_{CC1}(\text{max}) = 1.1 + 5.80\text{E-}02 \times f \quad (1)$$

$$I_{CC2}(\text{max}) = 4.6 + 6.55\text{E-}02 \times f + 5.5\text{E-}03 \times f \times C_L \quad (2)$$

At $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$:

$$I_{CC1}(\text{max}) = 0.8 + 3.40\text{E-}02 \times f \quad (3)$$

$$I_{CC2}(\text{max}) = 3.3 + 4.60\text{E-}02 \times f + 3.6\text{E-}03 \times f \times C_L \quad (4)$$

At $V_{CC1} = V_{CC2} = 2.7\text{ V}$:

$$I_{CC1}(\text{max}) = 0.4 + 3.20\text{E-}02 \times f \quad (5)$$

$$I_{CC2}(\text{max}) = 3.1 + 3.75\text{E-}02 \times f + 2.7\text{E-}03 \times f \times C_L \quad (6)$$

Typical Application (continued)

f is data rate of each channel measured in Mbps; C_L is the capacitive load of each channel measured in pF; I_{CC1}(maximum) and I_{CC2}(max) are measured in mA.

9.2.2.1.2 Typical Supply Current Equations

(Calculated for T_A = 25°C and nominal Silicon process material).

At $V_{CC1} = V_{CC2} = 5$ V:

$$I_{CC1}(\text{typical}) = 0.5 + 4.40E\text{-}02 \times f \quad (7)$$

$$I_{CC2}(\text{typical}) = 3 + 3.50E\text{-}02 \times f + 5.0E\text{-}03 \times f \times C_L \quad (8)$$

At $V_{CC1} = V_{CC2} = 3.3$ V:

$$I_{CC1}(\text{typical}) = 0.3 + 2.60E\text{-}02 \times f \quad (9)$$

$$I_{CC2}(\text{typical}) = 2.4 + 2.25E\text{-}02 \times f + 3.3E\text{-}03 \times f \times C_L \quad (10)$$

At $V_{CC1} = V_{CC2} = 2.7$ V:

$$I_{CC1}(\text{typical}) = 0.15 + 2.10E\text{-}02 \times f \quad (11)$$

$$I_{CC2}(\text{typical}) = 2.1 + 1.75E\text{-}02 \times f + 2.7E\text{-}03 \times f \times C_L \quad (12)$$

f is Data Rate of each channel measured in Mbps; C_L is the Capacitive Load of each channel measured in pF; I_{CC1}(typ) and I_{CC2}(typ) are measured in mA.

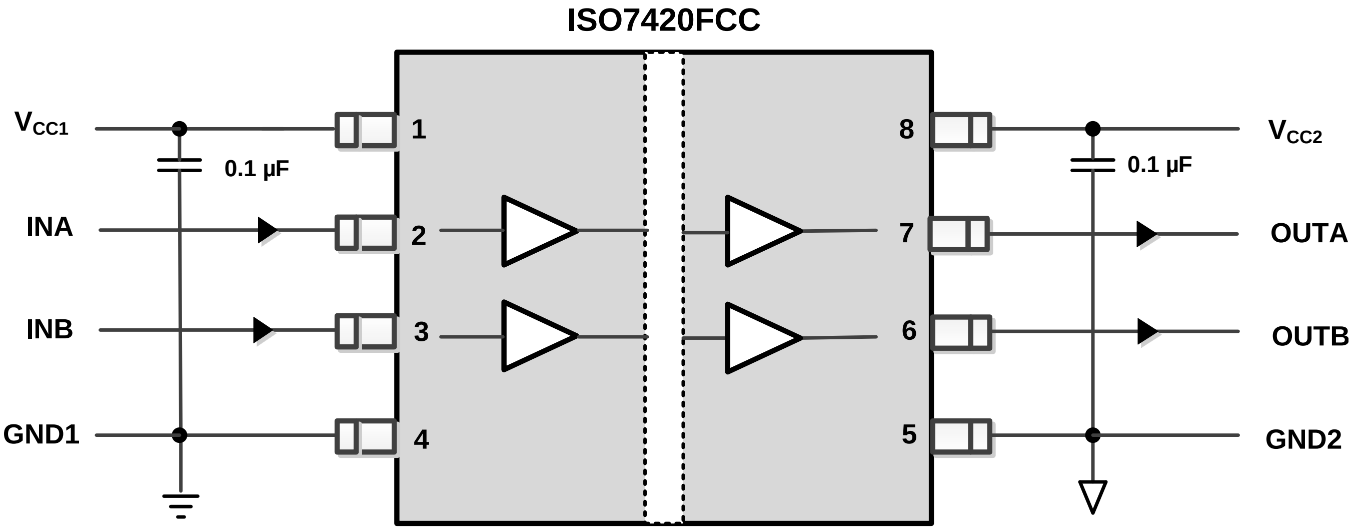


Figure 19. ISO7420FCC Typical Circuit Hook-Up

Typical Application (continued)

9.2.3 Application Curves

Figure 20 shows the INA input on Channel 1 and OUTA output on Channel 2 of an oscilloscope.

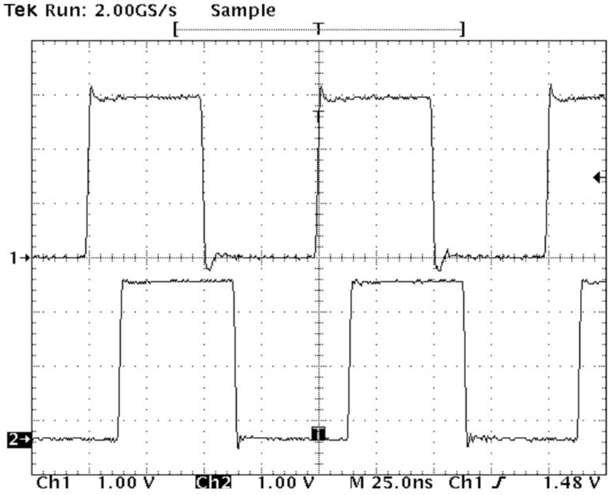


Figure 20. Typical Input and Output Waveforms

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 21). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

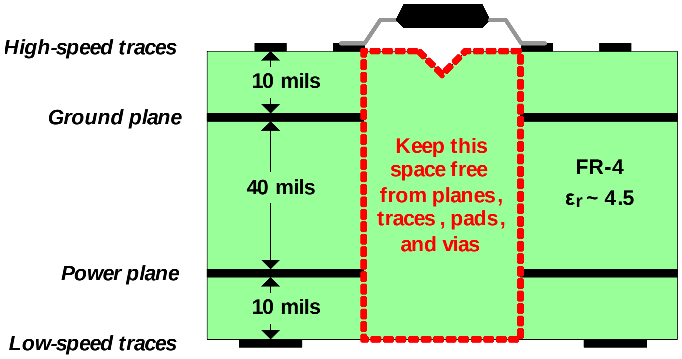


Figure 21. Recommended Layer Stack

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《用于隔离电源的 SN6501 变压器驱动器》*(SLLSEA0)
- *《LVDS 应用和数据手册》*(SLLD009)
- *《数字隔离器设计指南》*（文献编号：SLLA284）
- *《隔离相关术语》*(SLLA353)

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

DeviceNet, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7420FCCD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCD.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 125	
ISO7420FCCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7420FC
ISO7420FCCDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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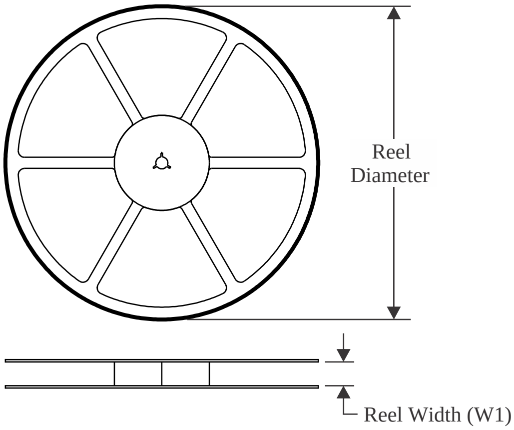
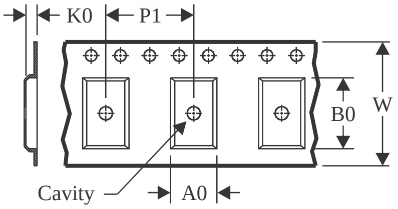
TAPE AND REEL INFORMATION

REEL DIMENSIONS

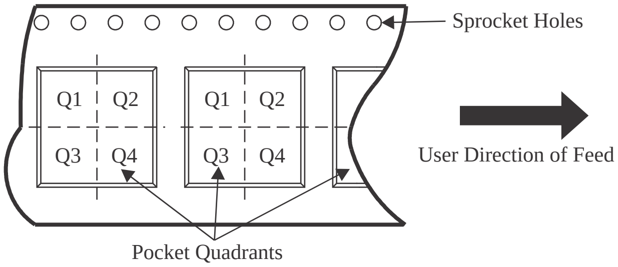


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

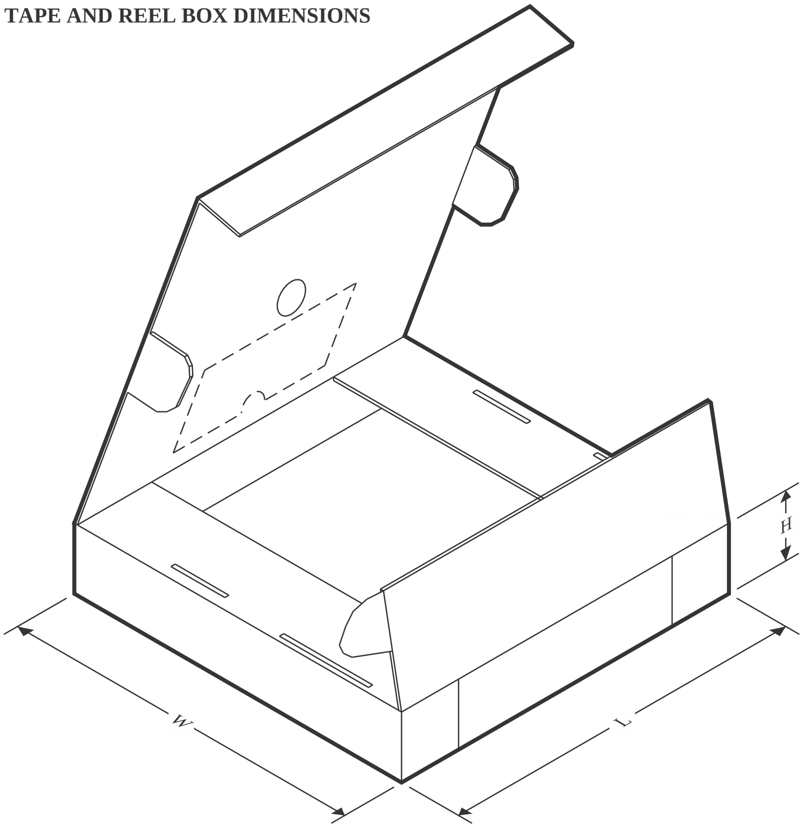
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7420FCCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

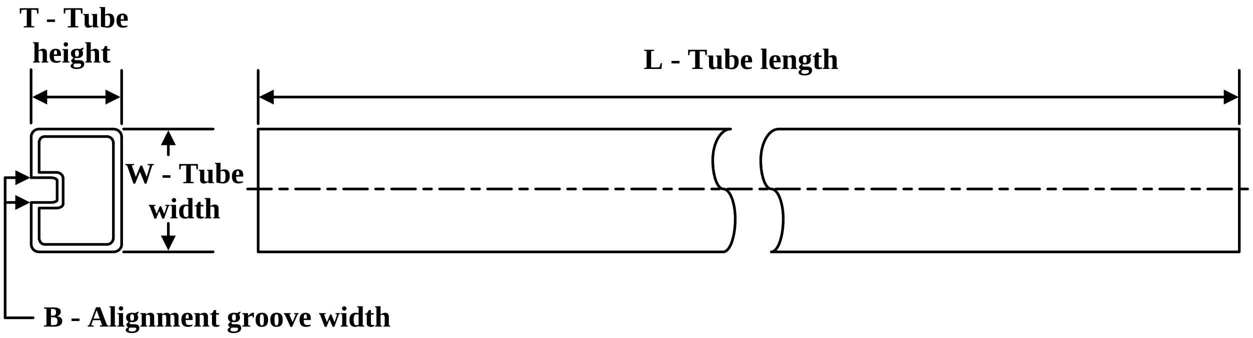
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

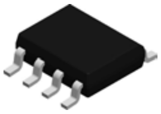
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7420FCCDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7420FCCD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7420FCCD.A	D	SOIC	8	75	505.46	6.76	3810	4

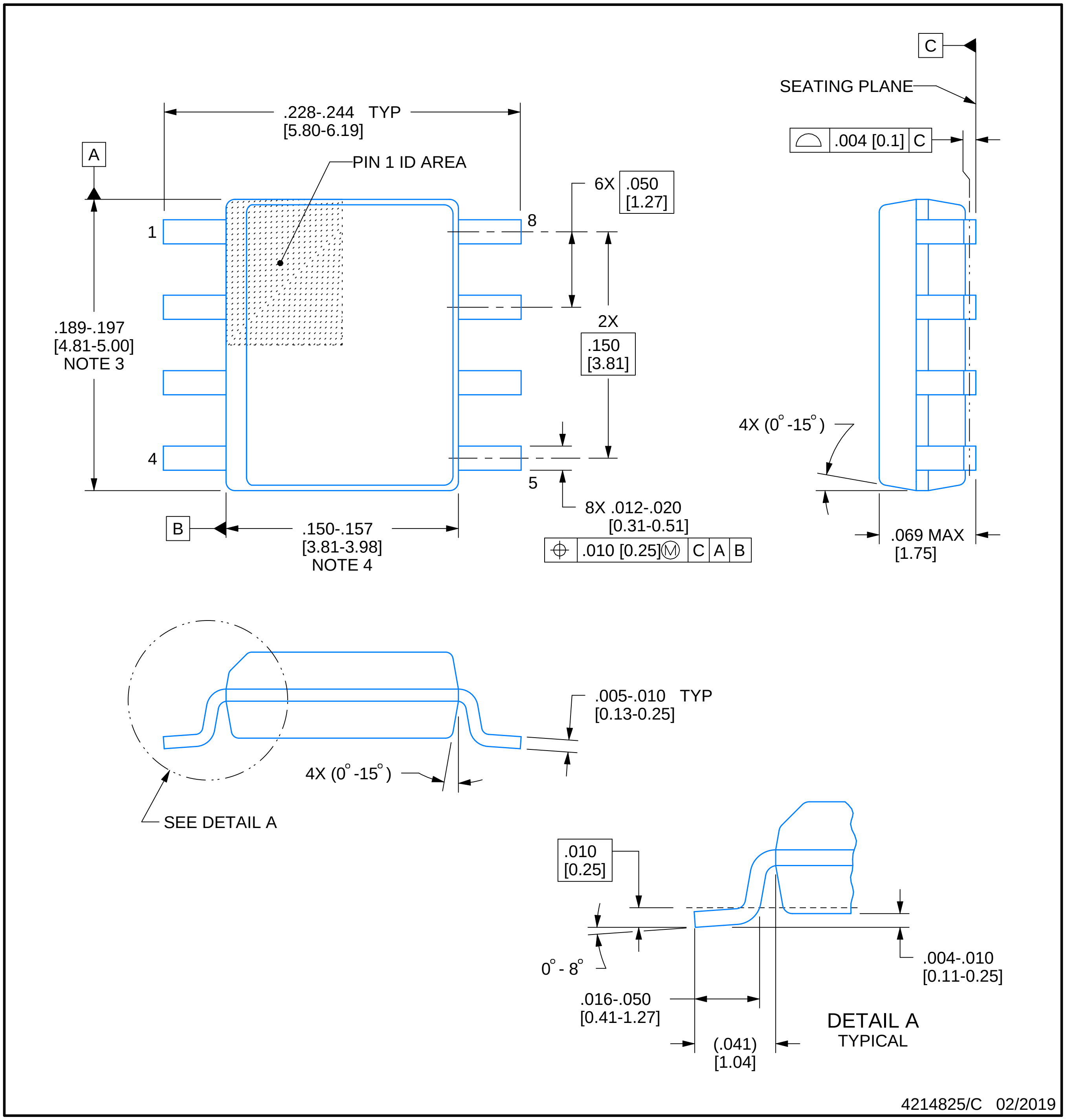


PACKAGE OUTLINE

D0008A

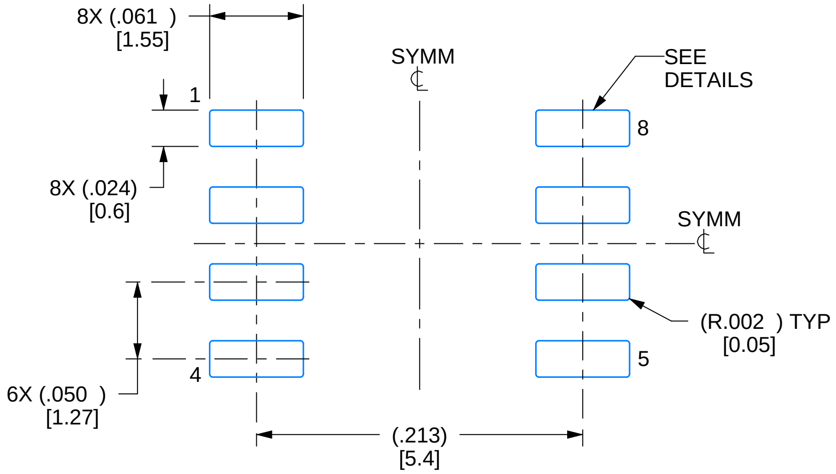
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

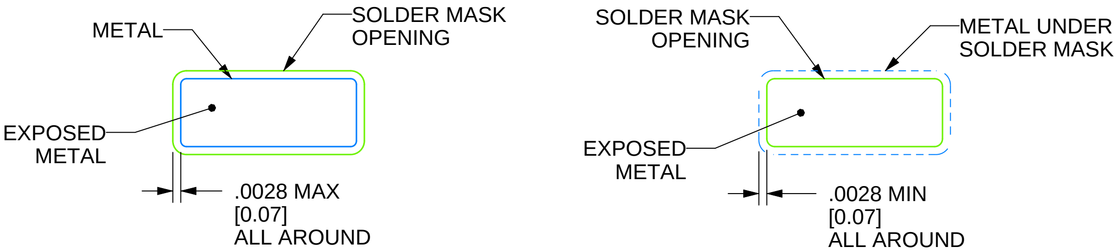


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



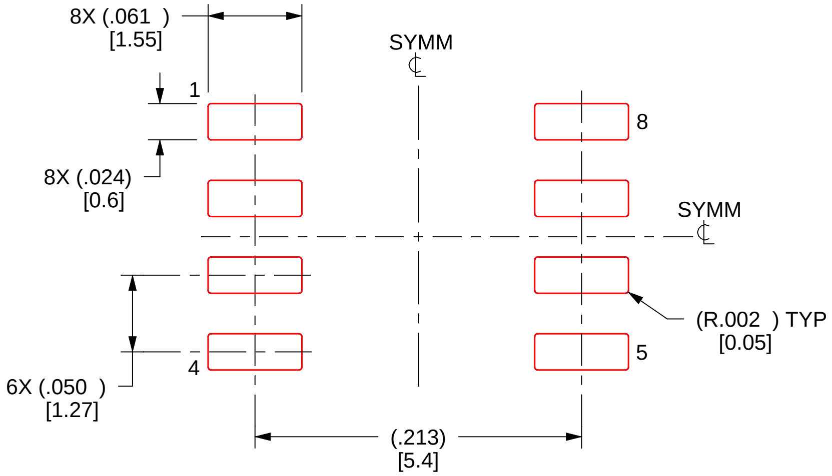
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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