

# ISO5451 具有有源保护特性的高 CMTI 2.5A 和 5A 隔离式 IGBT、MOSFET 栅极驱动器

## 1 特性

- 在  $V_{CM} = 1500V$  时，共模瞬态抗扰度 (CMTI) 的最小值为  $50kV/\mu s$ ，典型值为  $100kV/\mu s$
- 2.5A 峰值拉电流和 5A 峰值灌电流
- 短传播延迟：76ns (典型值)，110ns (最大值)
- 2A 有源米勒钳位
- 输出短路钳位
- 在检测到去饱和故障时通过  $\overline{FLT}$  发出故障报警，并通过  $\overline{RST}$  复位
- 具有就绪 (RDY) 引脚指示的输入和输出欠压锁定 (UVLO)
- 有源输出下拉特性，在低电源或输入悬空的情况下默认输出低电平
- 3V 至 5.5V 输入电源电压
- 15V 至 30V 输出驱动器电源电压
- 互补金属氧化物半导体 (CMOS) 兼容输入
- 抑制短于 20ns 的输入脉冲和瞬态噪声
- 工作温度：-40°C 至 +125°C (环境温度)
- 可耐受的浪涌隔离电压高达 10000  $V_{PK}$
- 安全相关认证：
  - 符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准的 8000  $V_{PK} V_{IOTM}$  和 1420  $V_{PK} V_{IORM}$  增强型隔离
  - 符合 UL 1577 标准且长达 1 分钟的 5700  $V_{RMS}$  隔离
  - 符合 CSA 组件验收通知 5A，IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证
  - 经 GB4943.1-2011 CQC 认证

## 2 应用

- 隔离式绝缘栅双极型晶体管 (IGBT) 和金属氧化物半导体场效应晶体管 (MOSFET) 驱动器：
  - 工业电机控制驱动
  - 工业电源
  - 太阳能逆变器
  - HEV 和 EV 电源模块
  - 感应加热

## 3 说明

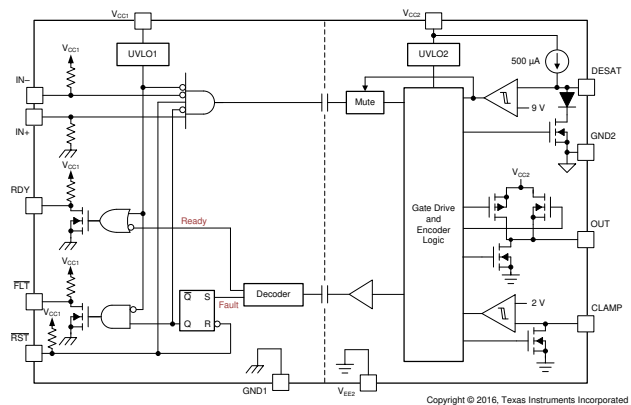
ISO5451 是一款用于 IGBT 和 MOSFET 的 5.7  $kV_{RMS}$  增强型隔离栅极驱动器，具有 2.5A 的拉电流能力和 5A 的灌电流能力。输入端由 3V 至 5.5V 的单电源供电运行。输出侧支持的电源电压范围为 15V 至 30V。两路互补 CMOS 输入控制栅极驱动器输出状态。76ns 的短暂传播时间保证了对于输出级的精确控制。

内置的去饱和 (DESAT) 故障检测功能可识别 IGBT 何时处于过载状态。当检测到 DESAT 时，栅极驱动器输出会被拉低至  $V_{EE2}$  电势，从而将 IGBT 立即关断。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
ISO5451	SOIC (16)	10.30mm × 7.50mm

(1) 有关所有的可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



## Table of Contents

1 特性.....	1	9.2 Functional Block Diagram.....	21
2 应用.....	1	9.3 Feature Description.....	22
3 说明.....	1	9.4 Device Functional Modes.....	23
4 Revision History.....	2	<b>10 Application and Implementation.....</b>	<b>24</b>
5 说明 (续).....	4	10.1 Application Information.....	24
6 Pin Configuration and Function.....	5	10.2 Typical Applications.....	24
7 Specifications.....	6	<b>11 Power Supply Recommendations.....</b>	<b>34</b>
7.1 Absolute Maximum Ratings.....	6	<b>12 Layout.....</b>	<b>35</b>
7.2 ESD Ratings.....	6	12.1 Layout Guidelines.....	35
7.3 Recommended Operating Conditions.....	6	12.2 Layout Example.....	35
7.4 Thermal Information.....	7	12.3 PCB Material.....	35
7.5 Power Ratings.....	7	<b>13 Device and Documentation Support.....</b>	<b>36</b>
7.6 Insulation Characteristics.....	8	13.1 Device Support.....	36
7.7 Safety-Related Certifications.....	9	13.2 Documentation Support.....	36
7.8 Safety Limiting Values.....	9	13.3 Receiving Notification of Documentation Updates.....	36
7.9 Electrical Characteristics.....	10	13.4 支持资源.....	36
7.10 Switching Characteristics.....	11	13.5 Trademarks.....	36
7.11 Insulation Characteristics Curves.....	12	13.6 静电放电警告.....	36
7.12 Typical Characteristics.....	13	13.7 术语表.....	36
8 Parameter Measurement Information.....	19	<b>14 Mechanical, Packaging, and Orderable Information.....</b>	<b>36</b>
9 Detailed Description.....	21		
9.1 Overview.....	21		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (January 2017) to Revision D (May 2023)	Page
• Added Additional manufacturing certification pending in the <i>Safety-Related Certifications</i> table.....	9
Changes from Revision B (December 2015) to Revision C (January 2017)	Page
• 将数据表标题从 <i>有源安全特性</i> 更改为 <i>有源保护特性</i> .....	1
• 将 <i>安全和监管认证</i> 从 “CSA 元件验收通知 5A、IEC 60950-1、IEC 60601 - 1 和 IEC 61010-1 终端设备标准” 更改为 “CSA 组件验收通知 5A、IEC 60950-1 和 IEC 60601-1 终端设备标准” .....	1
• 将 <i>安全和监管认证</i> 从 “符合 GB4943.1-2011 标准的 CQC 认证” 更改为经 GB4943.1-2011 CQC 认证.....	1
• 将 <i>安全和监管认证</i> 从 “所有认证均已计划” 更改为已通过 UL、VDE、CQC、TUV 认证并规划进行 CSA 认证 .....	1
• Changed the CSA status from planned to certified.....	9
• Changed the certifications in the <i>Safety-Related Certifications</i> table.....	9
• Added <i>Reinforced High-Voltage Capacitor Life Time Projection to Safety and Insulation Characteristics Curves</i> .....	12
• Changed the second paragraph of <i>Typical Applications</i> .....	24
• Added text "and $\overline{RST}$ input signal" to the <a href="#">节 10.2.1</a> .....	25
• Changed the <i>PCB Material</i> section.....	35
• Added the <i>Receiving Notification of Documentation Updates</i> section.....	36
• Changed the <i>Electrostatic Discharge Caution</i> section.....	36
Changes from Revision A (June 2015) to Revision B (December 2015)	Page
• 将 <a href="#">节 1</a> 的 <i>安全和监管批准</i> 从 “6000 V <sub>PK</sub> ” 更改为 8000 V <sub>PK</sub> .....	1
• 将 <a href="#">节 1</a> 的 <i>安全和监管批准</i> 从 “4250 V <sub>RMS</sub> ” 更正为 5700 V <sub>RMS</sub> .....	1
• Added the <i>Power Rating</i> table .....	7
• Moved <i>Insulation Characteristics</i> to the <i>Specifications</i> section.....	8

• Changed the Test Conditions and values for $q_{pd}$ in <i>Insulation Characteristics</i> .....	8
• Changed $R_{IO}$ Test conditions From: $100^{\circ}\text{C} \leq T_A \leq \text{max}$ To: $100^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ in <i>Insulation Characteristics</i> .....	8
• Changed $R_{IO}$ Test conditions From: $T_S$ To: $T_S = 150^{\circ}\text{C}$ in <i>Insulation Characteristics</i> .....	8
• Changed the <i>Safety-Related Certifications</i> table.....	9
• Moved <i>Safety-Related Certifications</i> to the <i>Specifications</i> section.....	9
• Moved <i>Safety Limiting Values</i> to the <i>Specification</i> section.....	9
• Added Note 1 to $I_{IH}$ in the <a href="#">§ 7.9</a> table .....	10
• Added Note 2 to $I_{IL}$ in the <a href="#">§ 7.9</a> table .....	10
• Changed <i>Thermal Derating Curve for Safety Limiting Current per VDE</i> and Added <i>Thermal Derating Curve for Safety Limiting Power per VDE</i> .....	12
• Added <i><math>I_{CC1}</math> Supply Current vs Temperature</i> to <i>Blanking Capacitor Charging Current vs Temperature</i> .....	13
• Added text ", but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue." to <i>Supply and Active Miller Clamp</i> .....	22
• Deleted ground symbol on pin 11 of <i>Global Shutdown with Inverting Input Configuration</i> .....	28
• Deleted ground symbol on pin 11 on the inverting input of <i>Auto Reset for Non-inverting and Inverting Input Configuration</i> .....	28
• Changed <i>Normal Operation - Bipolar Supply</i> and <i>Normal Operation - Unipolar Supply</i> .....	33

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**Changes from Revision \* (June 2015) to Revision A (June 2015)**
**Page**

• 将首页的“产品预发布”更改为完整数据表.....	1
• 将 <a href="#">§ 1</a> 的安全和监管批准从“8000 $V_{PK}$ $V_{IOTM}$ 和 2121 $V_{PK}$ ”更改为“6000 $V_{PK}$ $V_{IOTM}$ 和 1420 $V_{PK}$ ” .....	1
• 将 <a href="#">§ 1</a> 的安全和监管批准从“5.7 $kV_{RMS}$ ”更正为 4250 $V_{RMS}$ .....	1
• 更改了 <a href="#">§ 2</a> 列表.....	1
• Moved <i>Safety and Insulation Characteristics Curves</i> to the <i>Specifications</i> .....	12

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## 5 说明 (续)

当发生去饱和故障时，器件会通过隔离栅发送故障信号，以将输入端的  $\overline{\text{FLT}}$  输出拉为低电平并阻断隔离器的输入。 $\overline{\text{FLT}}$  的输出状态将被锁存，可通过  $\overline{\text{RST}}$  输入上的低电平有效脉冲复位。

如果在由双极输出电源供电的正常运行期间关断 IGBT，输出电压会被硬钳位为  $V_{EE2}$ 。如果输出电源为单极，那么可采用有源米勒钳位，这种钳位会在一条低阻抗路径上灌入米勒电流，从而防止 IGBT 在高电压瞬态条件下发生动态导通。

栅极驱动器是否准备就绪待运行由两个欠压锁定电路控制，这两个电路会监视输入端和输出端的电源。如果任意一端电源不足，RDY 输出会变为低电平，否则该输出为高电平。

ISO5451 采用 16 引脚小外形尺寸集成电路 (SOIC) 封装。此器件的额定工作环境温度范围为  $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$ 。

## 6 Pin Configuration and Function

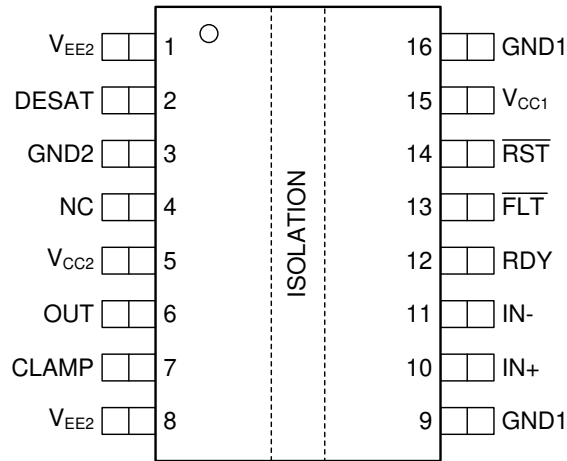


图 6-1. DW Package 16-Pin SOIC Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLAMP	7	O	Miller clamp output
DESAT	2	I	Desaturation voltage input
FLT	13	O	Fault output, low-active during DESAT condition
GND1	9, 16	—	Input ground
GND2	3	—	Gate drive common. Connect to IGBT emitter
IN+	10	I	Non-inverting gate drive voltage control input
IN -	11	I	Inverting gate drive voltage control input
NC	4	—	Not connected
OUT	6	O	Gate drive voltage output
RDY	12	O	Power-good output, active high when both supplies are good
RST	14	I	Reset input, apply a low pulse to reset fault latch
V <sub>CC1</sub>	15	—	Positive input supply (3 V to 5.5 V)
V <sub>CC2</sub>	5	—	Most positive output supply potential
V <sub>EE2</sub>	1, 8	—	Output negative supply. Connect to GND2 for unipolar-supply application

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC1</sub>	Supply voltage input side		GND1 - 0.3	6	V
V <sub>CC2</sub>	Positive supply voltage output side	(V <sub>CC2</sub> - GND2)	- 0.3	35	V
V <sub>EE2</sub>	Negative supply voltage output side	(V <sub>EE2</sub> - GND2)	- 17.5	0.3	V
V <sub>(SUP2)</sub>	Total supply output voltage	(V <sub>CC2</sub> - V <sub>EE2</sub> )	- 0.3	35	V
V <sub>OUT</sub>	Gate driver output voltage		V <sub>EE2</sub> - 0.3	V <sub>CC2</sub> + 0.3	V
I <sub>(OUTH)</sub>	Gate driver high output current	Gate driver high output current (max pulse width = 10 μs, max duty cycle = 0.2%)		2.7	A
I <sub>(OUTL)</sub>	Gate driver low output current	Gate driver high output current (max pulse width = 10 μs, max duty cycle = 0.2%)		5.5	A
V <sub>(LIP)</sub>	Voltage at IN+, IN-, $\overline{\text{FLT}}$ , RDY, $\overline{\text{RST}}$		GND1 - 0.3	V <sub>CC1</sub> + 0.3	V
I <sub>(LOP)</sub>	Output current of $\overline{\text{FLT}}$ , RDY			10	mA
V <sub>(DESAT)</sub>	Voltage at DESAT		GND2 - 0.3	V <sub>CC2</sub> + 0.3	V
V <sub>(CLAMP)</sub>	Clamp voltage		V <sub>EE2</sub> - 0.3	V <sub>CC2</sub> + 0.3	V
T <sub>J</sub>	Junction temperature		- 40	150	°C
T <sub>STG</sub>	Storage temperature		- 65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC1</sub>	Supply voltage input side		3		5.5	V
V <sub>CC2</sub>	Positive supply voltage output side	(V <sub>CC2</sub> - GND2)	15		30	V
V <sub>EE2</sub>	Negative supply voltage output side	(V <sub>EE2</sub> - GND2)	- 15		0	V
V <sub>(SUP2)</sub>	Total supply voltage output side	(V <sub>CC2</sub> - V <sub>EE2</sub> )	15		30	V
V <sub>IH</sub>	High-level input voltage	(IN+, IN-, $\overline{\text{RST}}$ )	0.7 × V <sub>CC1</sub>		V <sub>CC1</sub>	V
V <sub>IL</sub>	Low-level input voltage	(IN+, IN-, $\overline{\text{RST}}$ )	0		0.3 × V <sub>CC1</sub>	V
t <sub>UI</sub>	Pulse width at IN+, IN- for full output	(C <sub>LOAD</sub> = 1 nF)	40			ns
t <sub>RST</sub>	Pulse width at $\overline{\text{RST}}$ for resetting fault latch		800			ns
T <sub>A</sub>	Ambient temperature		- 40	25	125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO5451	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.5	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	29.2	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$	Maximum power dissipation <sup>(1)</sup>			1255	mW
$P_{ID}$	Maximum input power dissipation			175	mW
$P_{OD}$	Maximum output power dissipation			1080	mW

(1) Full chip power dissipation is de-rated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that Junction temperature does not exceed 150°C.

## 7.6 Insulation Characteristics

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	μm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category (according to IEC 60664-1)	Rated Mains Voltage ≤ 300 V <sub>RMS</sub>	I-IV	
		Rated Mains Voltage ≤ 600 V <sub>RMS</sub>	I-III	
		Rated Mains Voltage ≤ 1000 V <sub>RMS</sub>	I-II	
<b>DIN V VDE V 0884-10 (VDE V 0884-10):2006-12<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1420	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage. Time dependent dielectric breakdown (TDDB) Test, see <a href="#">Fig 7-1</a>	1000	V <sub>RMS</sub>
		DC voltage	1420	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum Transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 sec (qualification), t = 1 sec (100% production)	8000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 60065, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 10000 V <sub>PK</sub> (qualification) <sup>(3)</sup>	6250	
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> = 1704 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> = 2272 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> = 2663 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤5	
R <sub>IO</sub>	Isolation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	Ω
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	Ω
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin(2πft), f = 1 MHz	~1	pF
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstanding Isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 sec (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6840 V <sub>RMS</sub> , t = 1 sec (100% production)	5700	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device



## 7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Certified according to CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced Insulation Maximum Transient isolation voltage, 8000 V <sub>PK</sub> ; Maximum surge isolation voltage, 6250 V <sub>PK</sub> ; Maximum repetitive peak isolation voltage, 1420 V <sub>PK</sub>	Isolation Rating of 5700 V <sub>RMS</sub> ; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 V <sub>RMS</sub> max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V <sub>RMS</sub> (354 V <sub>PK</sub> ) max working voltage	Single Protection, 5700 V <sub>RMS</sub>	Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 V <sub>RMS</sub> maximum working voltage	5700 V <sub>RMS</sub> Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V <sub>RMS</sub> 5700 V <sub>RMS</sub> Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V <sub>RMS</sub>
Certification completed Certificate number: 40040142	Certification completed Master contract number:220991	Certification completed File number: E181974	Certification completed Certificate number: CQC16001141761 Additional manufacturing certification pending	Certification completed Client ID number: 77311

## 7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub> Safety input, output or supply current	R <sub>θJA</sub> = 99.6°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			349	mA
	R <sub>θJA</sub> = 99.6°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			228	
	R <sub>θJA</sub> = 99.6°C/W, V <sub>I</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			84	
	R <sub>θJA</sub> = 99.6°C/W, V <sub>I</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			42	
P <sub>S</sub> Safety input, output, or total power	R <sub>θJA</sub> = 99.6°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1255 <sup>(1)</sup>	mW
T <sub>S</sub> Maximum ambient safety temperature				150	°C

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Table 7.4](#) is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} = 15\text{ V}$ ,  $V_{EE2} = 8\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VOLTAGE SUPPLY</b>						
$V_{IT+}(UVLO1)$	Positive-going UVLO1 threshold voltage input side ( $V_{CC1} - \text{GND1}$ )				2.25	V
$V_{IT-}(UVLO1)$	Negative-going UVLO1 threshold voltage input side ( $V_{CC1} - \text{GND1}$ )		1.7			V
$V_{HYS}(UVLO1)$	UVLO1 Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) input side			0.24		V
$V_{IT+}(UVLO2)$	Positive-going UVLO2 threshold voltage output side ( $V_{CC2} - \text{GND2}$ )			12	13	V
$V_{IT-}(UVLO2)$	Negative-going UVLO2 threshold voltage output side ( $V_{CC2} - \text{GND2}$ )		9.5	11		V
$V_{HYS}(UVLO2)$	UVLO2 Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) output side			1		V
$I_{Q1}$	Input supply quiescent current			2.8	4.5	mA
$I_{Q2}$	Output supply quiescent current			3.6	6	mA
<b>LOGIC I/O</b>						
$V_{IT+}(IN, RST)$	Positive-going input threshold voltage (IN+, IN-, RST)				$0.7 \times V_{CC1}$	V
$V_{IT-}(IN, RST)$	Negative-going input threshold voltage (IN+, IN-, RST)		$0.3 \times V_{CC1}$			V
$V_{HYS}(IN, RST)$	Input hysteresis voltage (IN+, IN-, RST)			$0.15 \times V_{CC1}$		V
$I_{IH}$	High-level input leakage at (IN+) <sup>(1)</sup>	$IN+ = V_{CC1}$		100		$\mu\text{A}$
$I_{IL}$	Low-level input leakage at (IN-, RST) <sup>(2)</sup>	$IN- = \text{GND1}, \overline{RST} = \text{GND1}$		-100		$\mu\text{A}$
$I_{PU}$	Pull-up current of FLT, RDY	$V_{(RDY)} = \text{GND1}, V_{(FLT)} = \text{GND1}$		100		$\mu\text{A}$
$V_{OL}$	Low-level output voltage at FLT, RDY	$I_{(FLT)} = 5\text{ mA}$			0.2	V
<b>GATE DRIVER STAGE</b>						
$V_{(OUTPD)}$	Active output pulldown voltage	$I_{OUT} = 200\text{ mA}, V_{CC2} = \text{open}$			2	V
$V_{(OUTH)}$	High-level output voltage	$I_{OUT} = -20\text{ mA}$	$V_{CC2} - 0.5$	$V_{CC2} - 0.24$		V
$V_{(OUTL)}$	Low-level output voltage	$I_{OUT} = 20\text{ mA}$		$V_{EE2} + 13$	$V_{EE2} + 50$	mV
$I_{(OUTH)}$	High-level output peak current	$IN+ = \text{high}, IN- = \text{low}, V_{OUT} = V_{CC2} - 15\text{ V}$	1.5	2.5		A
$I_{(OUTL)}$	Low-level output peak current	$IN+ = \text{low}, IN- = \text{high}, V_{OUT} = V_{EE2} + 15\text{ V}$	3.4	5		A
<b>ACTIVE MILLER CLAMP</b>						
$V_{(CLP)}$	Low-level clamp voltage	$I_{(CLP)} = 20\text{ mA}$		$V_{EE2} + 0.015$	$V_{EE2} + 0.08$	V
$I_{(CLP)}$	Low-level clamp current	$V_{(CLAMP)} = V_{EE2} + 2.5\text{ V}$	1.6	2.5		A
$V_{(CLTH)}$	Clamp threshold voltage		1.6	2.1	2.5	V
<b>SHORT CIRCUIT CLAMPING</b>						
$V_{(CLP\_OUT)}$	Clamping voltage ( $V_{OUT} - V_{CC2}$ )	$IN+ = \text{high}, IN- = \text{low}, t_{CLP} = 10\ \mu\text{s}, I_{(OUTH)} = 500\text{ mA}$		0.8	1.3	V
$V_{(CLP\_CLAMP)}$	Clamping voltage ( $V_{CLP} - V_{CC2}$ )	$IN+ = \text{high}, IN- = \text{low}, t_{CLP} = 10\ \mu\text{s}, I_{(CLP)} = 500\text{ mA}$		1.3		V
$V_{(CLP\_CLAMP)}$	Clamping voltage at CLAMP	$IN+ = \text{High}, IN- = \text{Low}, I_{(CLP)} = 20\text{ mA}$		0.7	1.1	V
<b>DESAT PROTECTION</b>						
$I_{(CHG)}$	Blanking capacitor charge current	$V_{(DESAT)} - \text{GND2} = 2\text{ V}$	0.42	0.5	0.58	mA
$I_{(DCHG)}$	Blanking capacitor discharge current	$V_{(DESAT)} - \text{GND2} = 6\text{ V}$	9	14		mA
$V_{(DSTH)}$	DESAT threshold voltage with respect to GND2		8.3	9	9.5	V

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} = \text{GND2} = 15\text{ V}$ ,  $\text{GND2} - V_{EE2} = 8\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DSL)}$	DESAT voltage with respect to GND2, when OUT is driven low		0.4		1	V

- (1)  $I_{IH}$  for IN<sup>-</sup>, RST pin is zero as they are pulled high internally.  
(2)  $I_{IL}$  for IN<sup>+</sup> is zero, as it is pulled low internally.

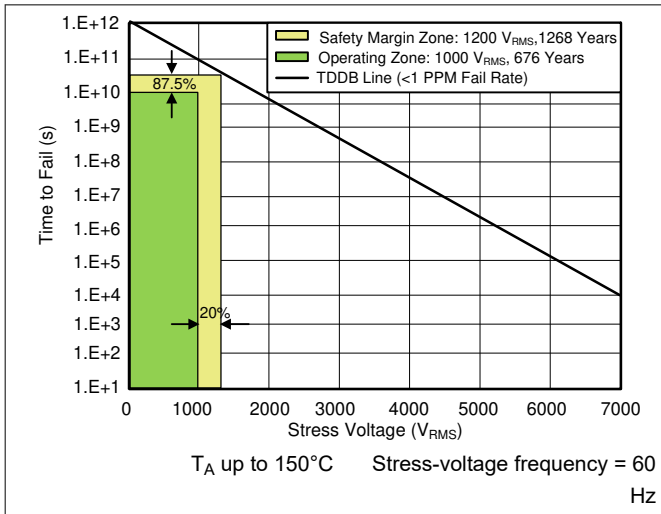
## 7.10 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} = \text{GND2} = 15\text{ V}$ ,  $\text{GND2} - V_{EE2} = 8\text{ V}$

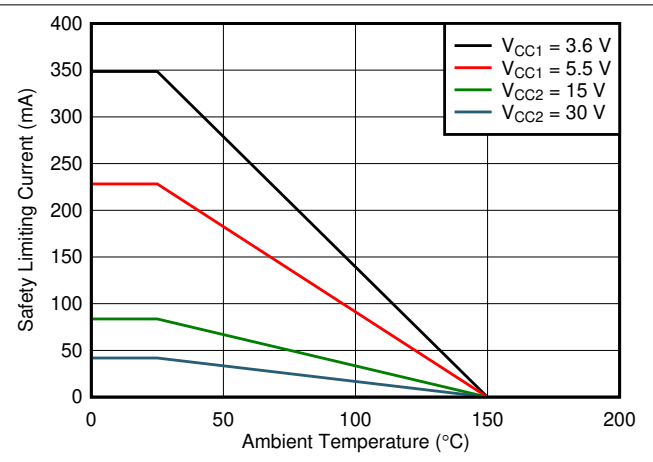
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_r$	Output signal rise time	$C_{LOAD} = 1\text{ nF}$ , see <a href="#">图 8-1</a> , <a href="#">图 8-2</a> and <a href="#">图 8-3</a>	12	20	35	ns	
$t_f$	Output signal fall time		12	20	37	ns	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay			76	110	ns	
$t_{sk-p}$	Pulse Skew $ t_{PHL} - t_{PLH} $				20	ns	
$t_{sk-pp}$	Part-to-part skew				30 <sup>(1)</sup>	ns	
$t_{GF}$	Glitch filter on IN <sup>+</sup> , IN <sup>-</sup> , RST			20	30	40	ns
$t_{DESAT(10\%)}$	DESAT sense to 10% OUT delay			300	415	500	ns
$t_{DESAT(GF)}$	DESAT glitch filter delay				330		ns
$t_{DESAT(FLT)}$	DESAT sense to FLT-low delay		see <a href="#">图 8-3</a>		2000	2420	ns
$t_{LEB}$	Leading edge blanking time		see <a href="#">图 8-1</a> and <a href="#">图 8-2</a>	330	400	500	ns
$t_{GF(RSTFLT)}$	Glitch filter on RST for resetting FLT		300		800	ns	
$C_i$	Input capacitance <sup>(2)</sup>	$V_i = V_{CC1}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1\text{ MHz}$ , $V_{CC1} = 5\text{ V}$		2		pF	
CMTI	Common-mode transient immunity	$V_{CM} = 1500\text{ V}$ , see <a href="#">图 8-4</a>	50	100		kV/ $\mu\text{s}$	

- (1) Measured at same supply voltage and temperature condition  
(2) Measured from input pin to ground.

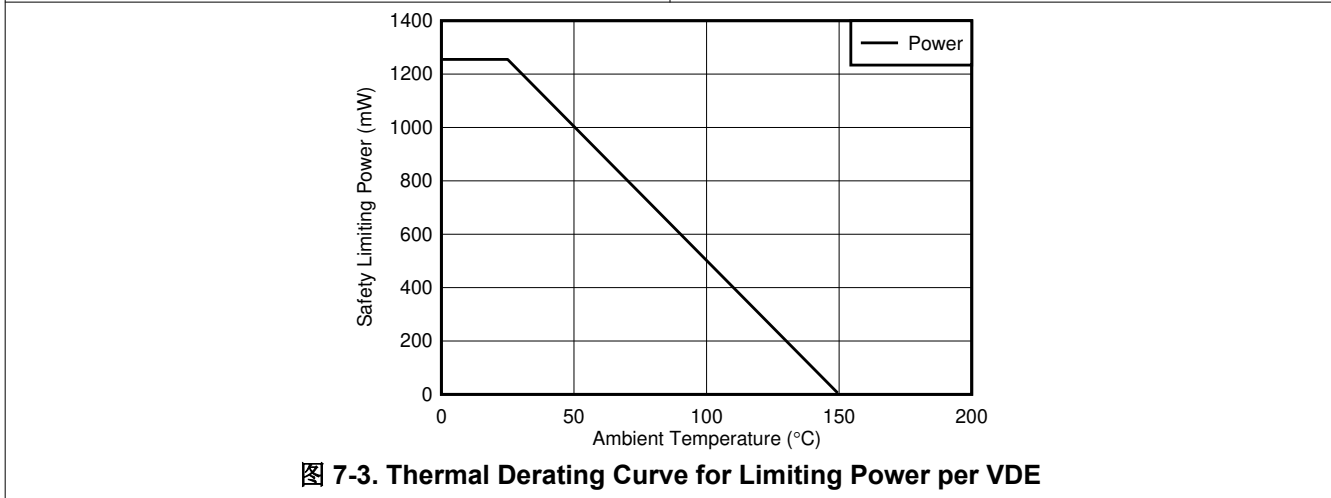
### 7.11 Insulation Characteristics Curves



**图 7-1. Reinforced High-Voltage Capacitor Lifetime Projection**



**图 7-2. Thermal Derating Curve for Limiting Current per VDE**



**图 7-3. Thermal Derating Curve for Limiting Power per VDE**

## 7.12 Typical Characteristics

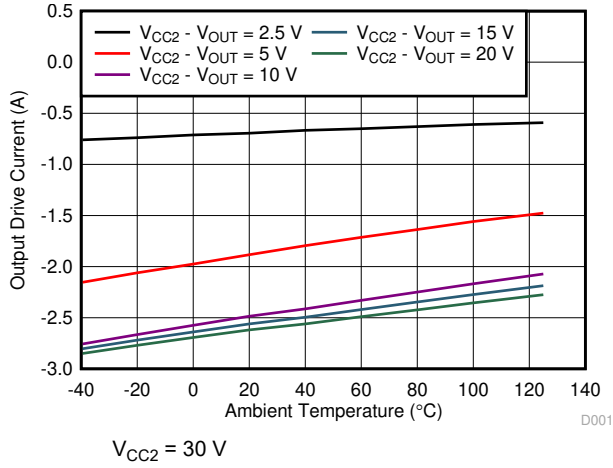


图 7-4. Output High Drive Current vs Temperature

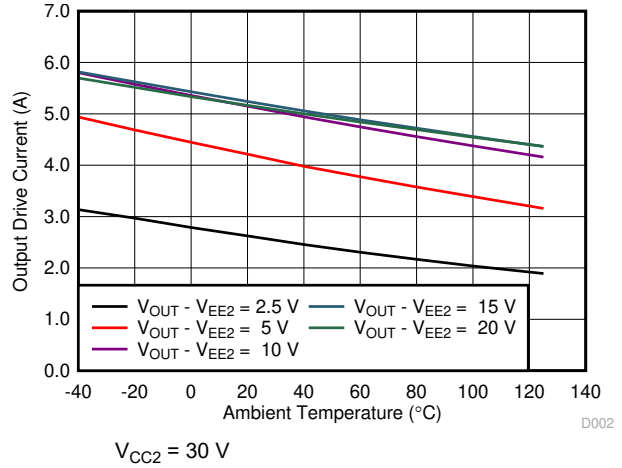


图 7-5. Output Low Drive Current vs Temperature

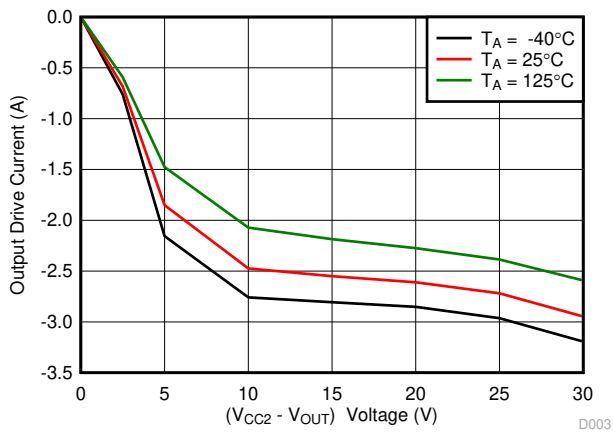


图 7-6. Output High Drive Current vs Output Voltage

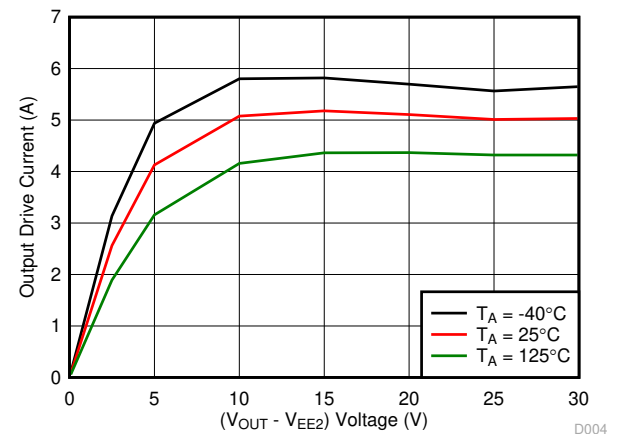


图 7-7. Output Low Drive Current vs Output Voltage

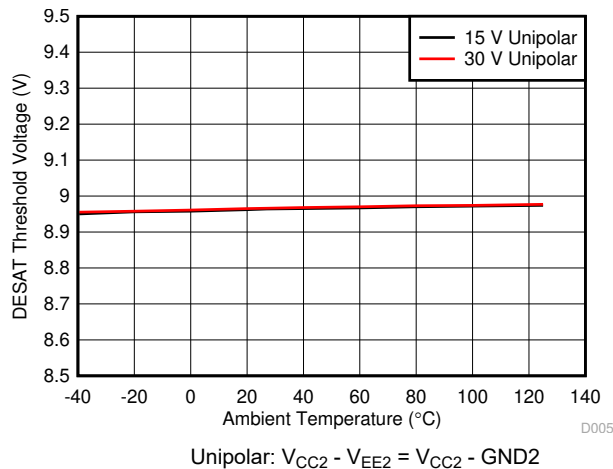
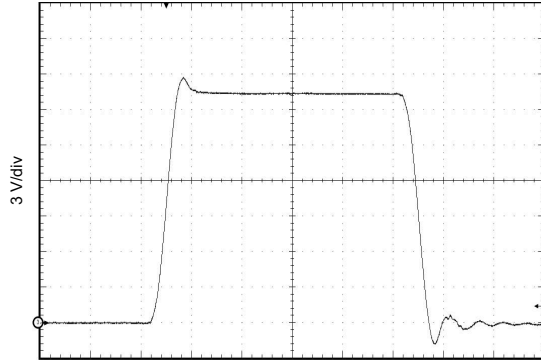


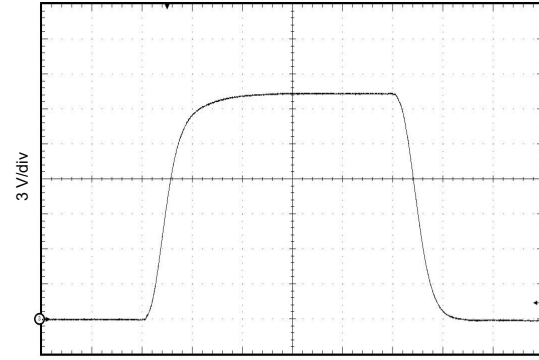
图 7-8. DESAT Threshold Voltage vs Temperature

## 7.12 Typical Characteristics (continued)



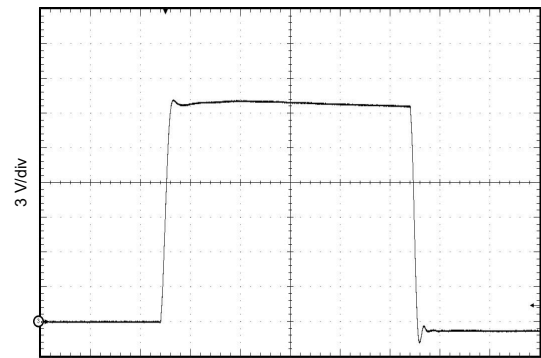
Time - 50 ns/div  
 $C_L = 1 \text{ nF}$      $R_G = 0 \ \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

图 7-9. Output Transient Waveform



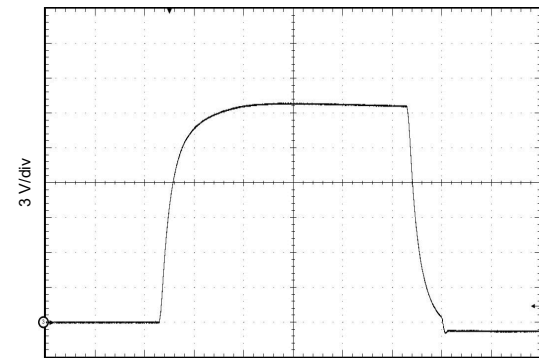
Time - 50 ns/div  
 $C_L = 1 \text{ nF}$      $R_G = 10 \ \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

图 7-10. Output Transient Waveform



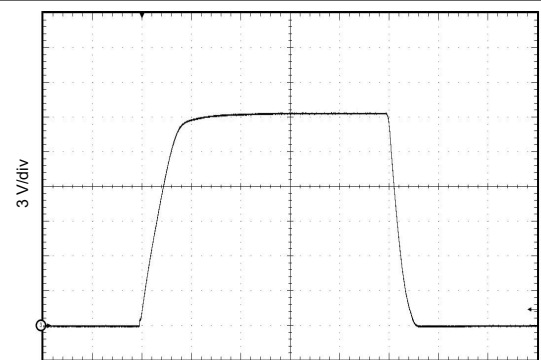
Time - 500 ns/div  
 $C_L = 10 \text{ nF}$      $R_G = 0 \ \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

图 7-11. Output Transient Waveform



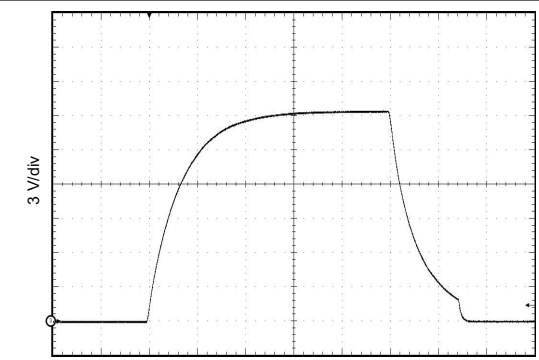
Time - 500 ns/div  
 $C_L = 10 \text{ nF}$      $R_G = 10 \ \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

图 7-12. Output Transient Waveform



Time - 1  $\mu\text{s}/\text{div}$   
 $C_L = 100 \text{ nF}$      $R_G = 0 \ \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

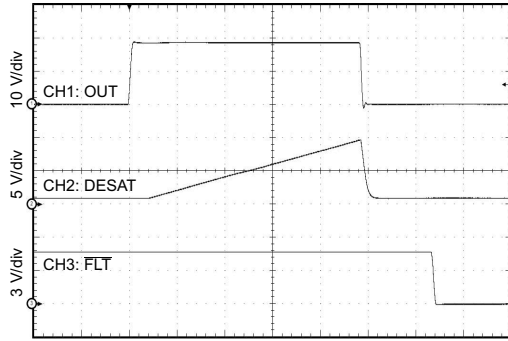
图 7-13. Output Transient Waveform



Time - 2  $\mu\text{s}/\text{div}$   
 $C_L = 100 \text{ nF}$      $R_G = 10 \ \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

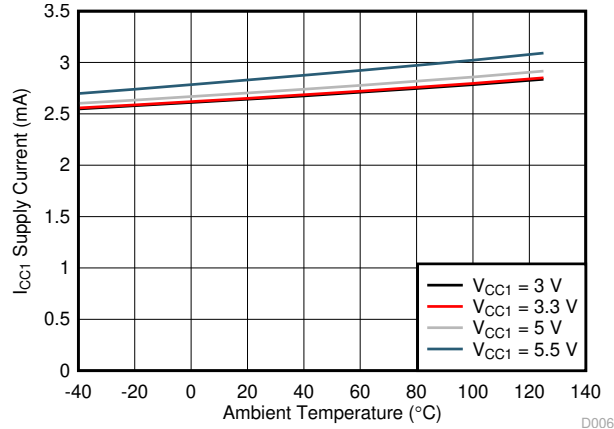
图 7-14. Output Transient Waveform

## 7.12 Typical Characteristics (continued)



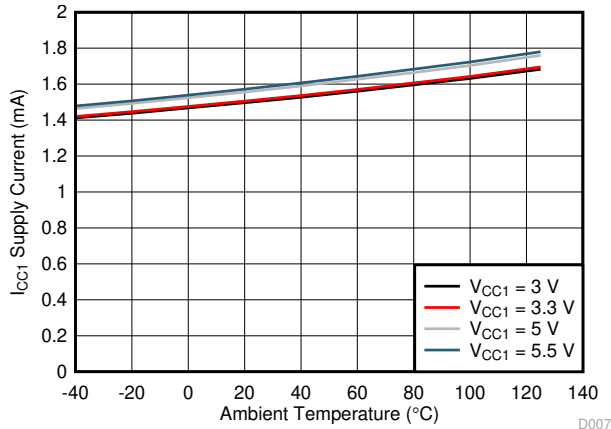
Time - 1  $\mu$ s/div  
 $C_L = 100$  nF     $R_G = 10$   $\Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20$  V

图 7-15. Output Transient Waveform DESAT and  $\overline{FLT}$



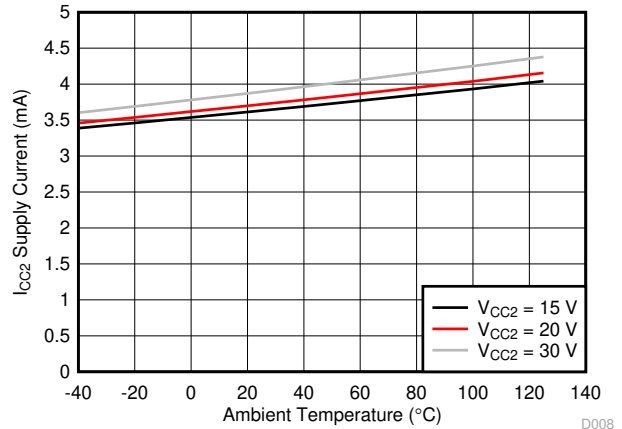
$IN+ = High$      $IN- = Low$

图 7-16.  $I_{CC1}$  Supply Current vs Temperature



$IN+ = Low$      $IN- = Low$

图 7-17.  $I_{CC1}$  Supply Current vs Temperature



Input Frequency = 1 kHz

图 7-18.  $I_{CC2}$  Supply Current vs Temperature

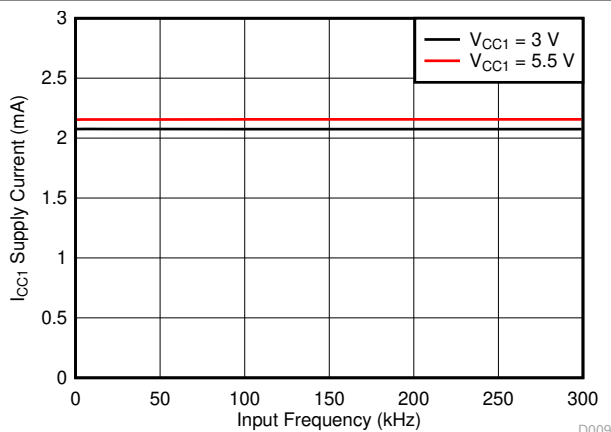
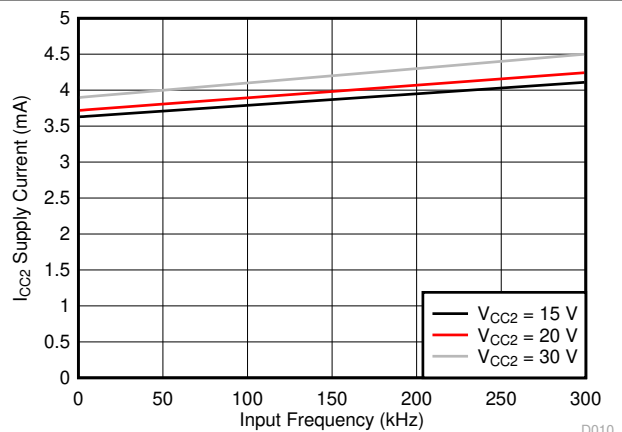


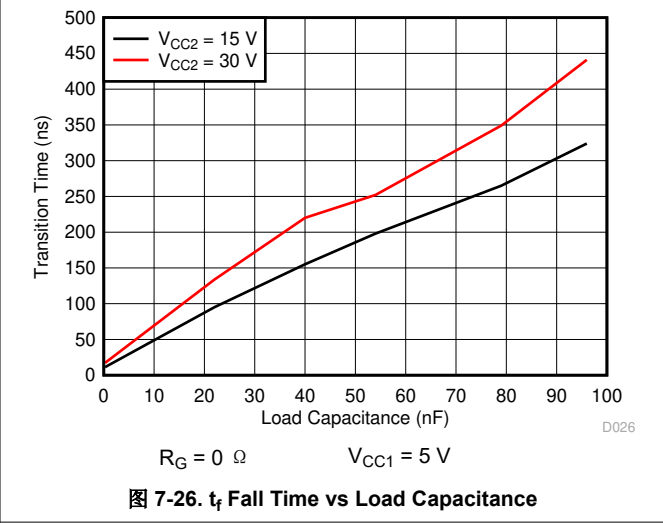
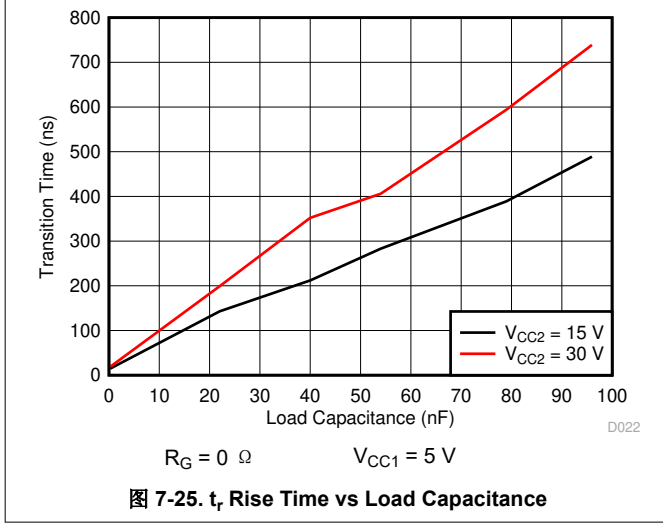
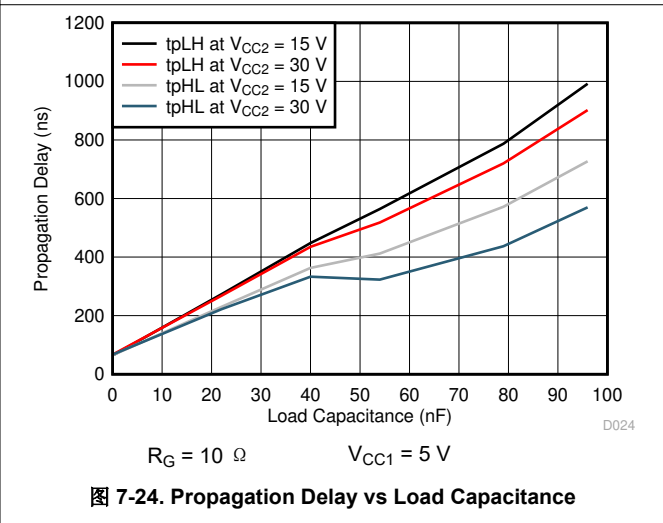
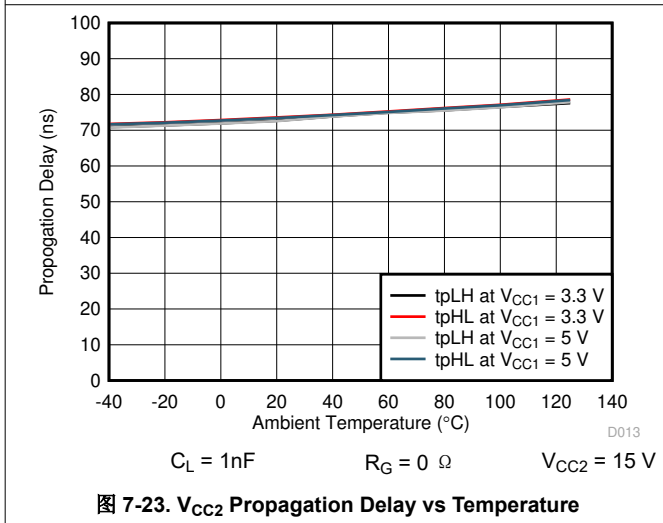
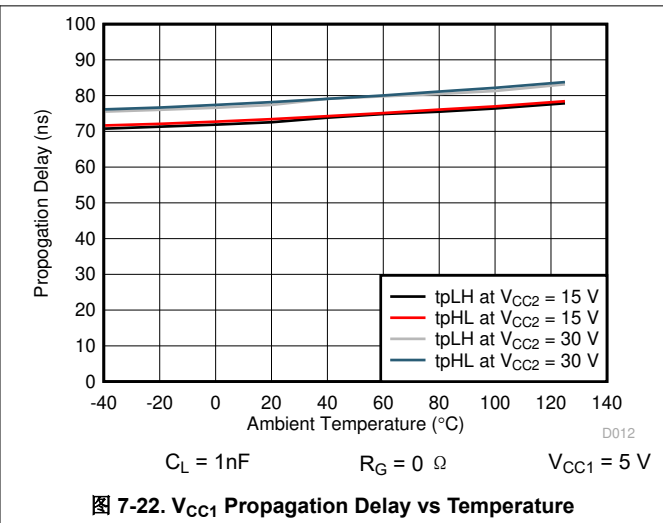
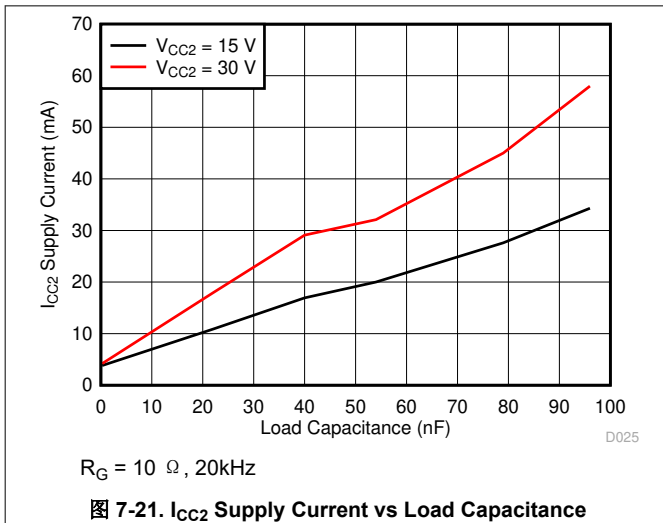
图 7-19.  $I_{CC1}$  Supply Current vs Input Frequency



No  $C_L$

图 7-20.  $I_{CC2}$  Supply Current vs Input Frequency

### 7.12 Typical Characteristics (continued)





### 7.12 Typical Characteristics (continued)

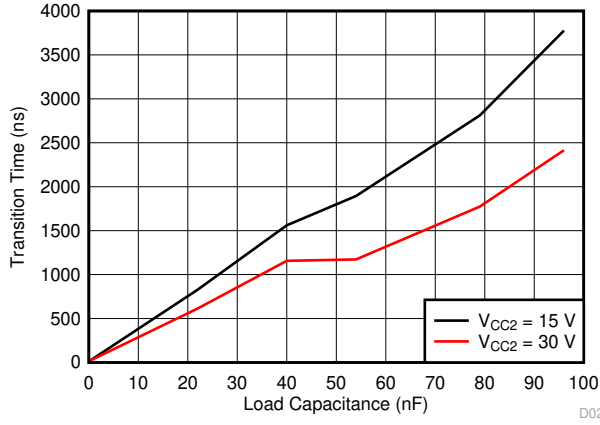


图 7-27.  $t_r$  Rise Time vs Load Capacitance

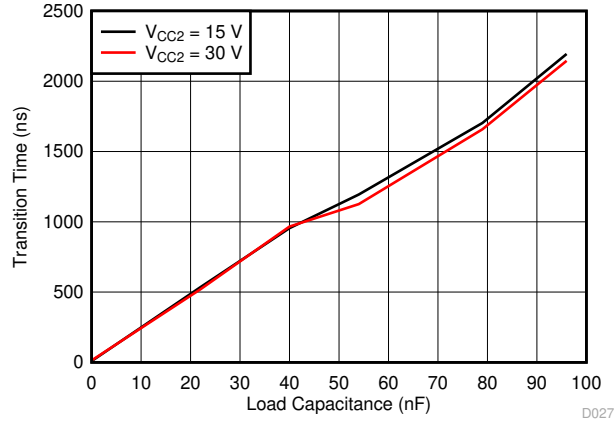


图 7-28.  $t_f$  Fall Time vs Load Capacitance

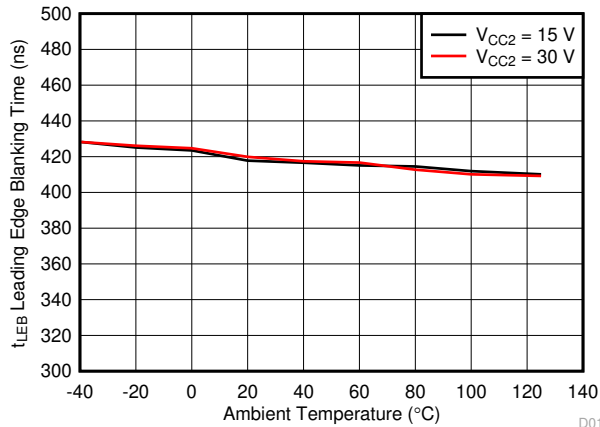


图 7-29. Leading Edge Blanking Time With Temperature

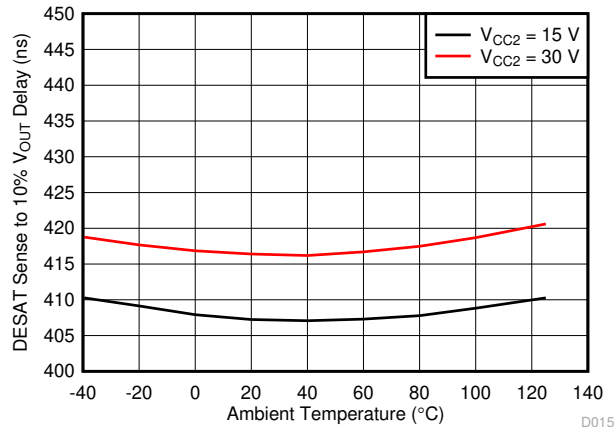


图 7-30. DESAT Sense to  $V_{OUT}$  10% Delay vs Temperature

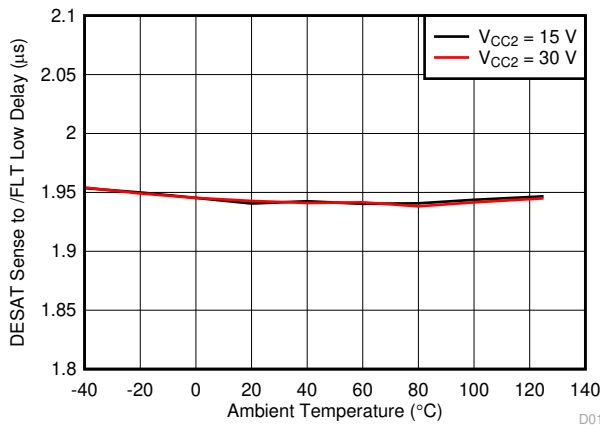


图 7-31. DESAT Sense to  $\overline{FLT}$  Low Delay vs Temperature

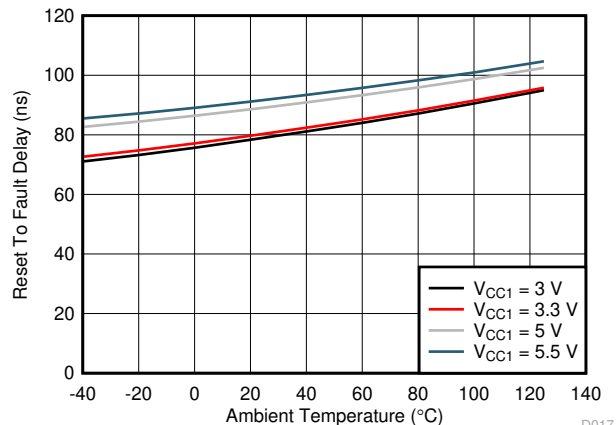


图 7-32. Reset to Fault Delay Across Temperature

### 7.12 Typical Characteristics (continued)

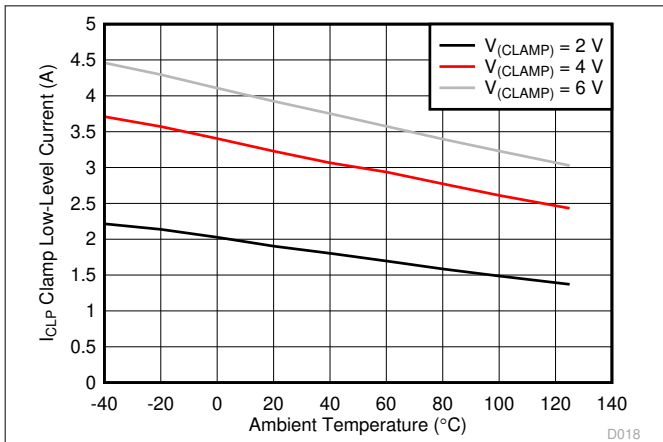


图 7-33. Miller Clamp Current vs Temperature

D018

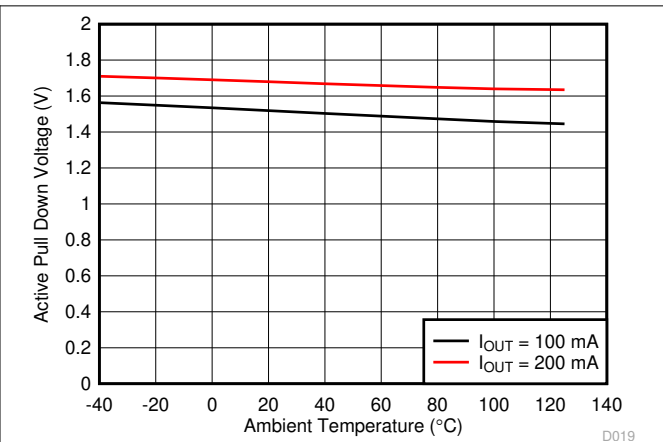


图 7-34. Active Pull Down Voltage vs Temperature

D019

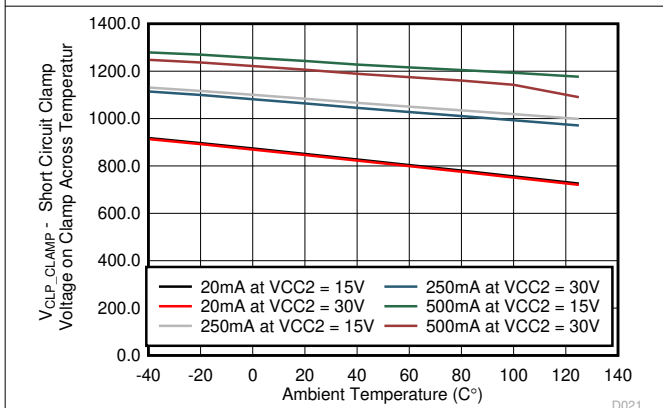


图 7-35.  $V_{CLP\_CLAMP}$  - Short Circuit Clamp Voltage on Clamp Across Temperature

D021

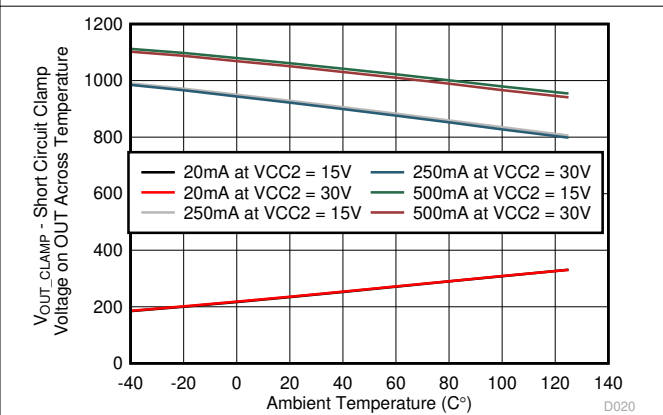
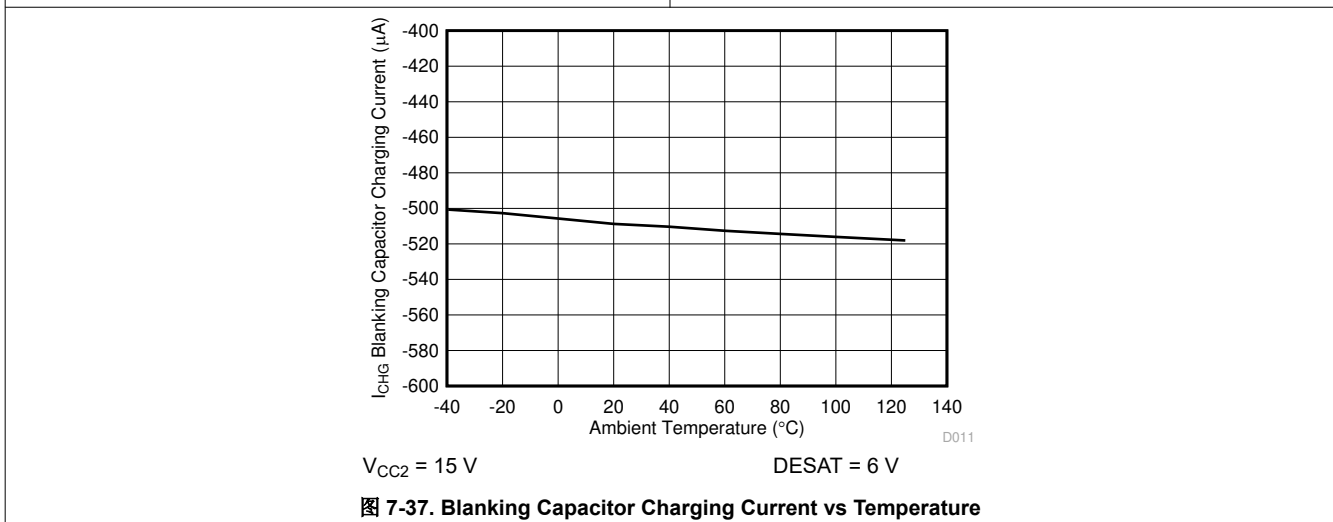


图 7-36.  $V_{OUT\_CLAMP}$  - Short Circuit Clamp Voltage on OUT Across Temperature

D020



$V_{CC2} = 15V$

$DESAT = 6V$

图 7-37. Blanking Capacitor Charging Current vs Temperature

D011

## 8 Parameter Measurement Information

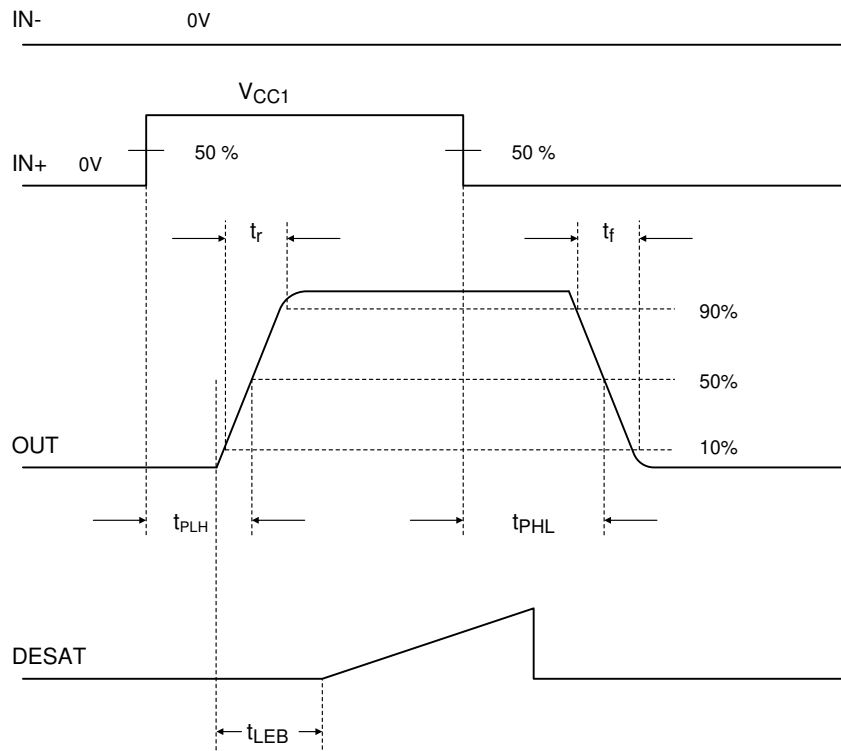


图 8-1. OUT Propagation Delay, Non-Inverting Configuration

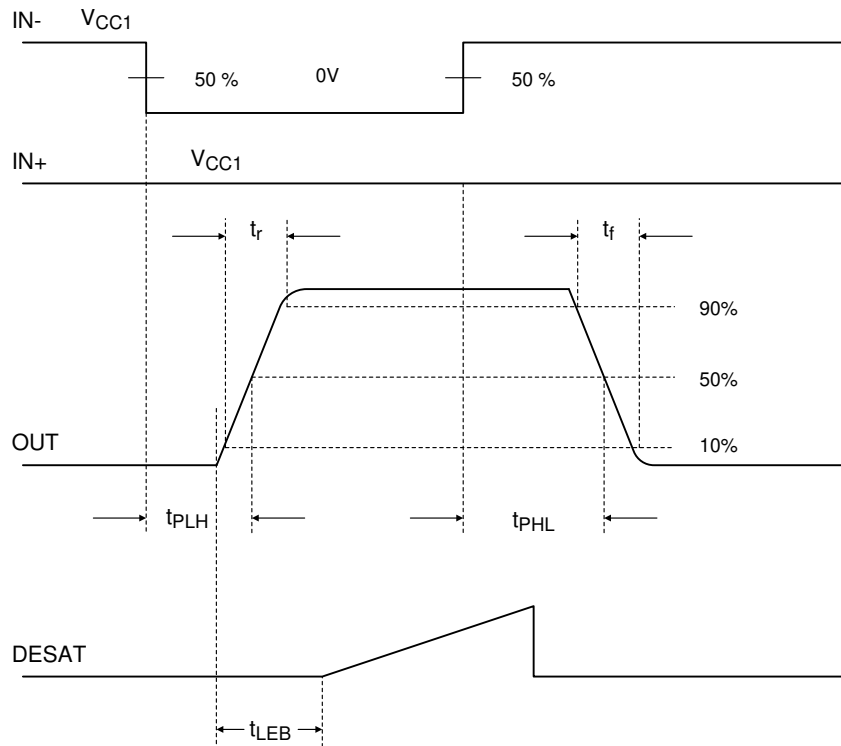


图 8-2. OUT Propagation Delay, Inverting Configuration

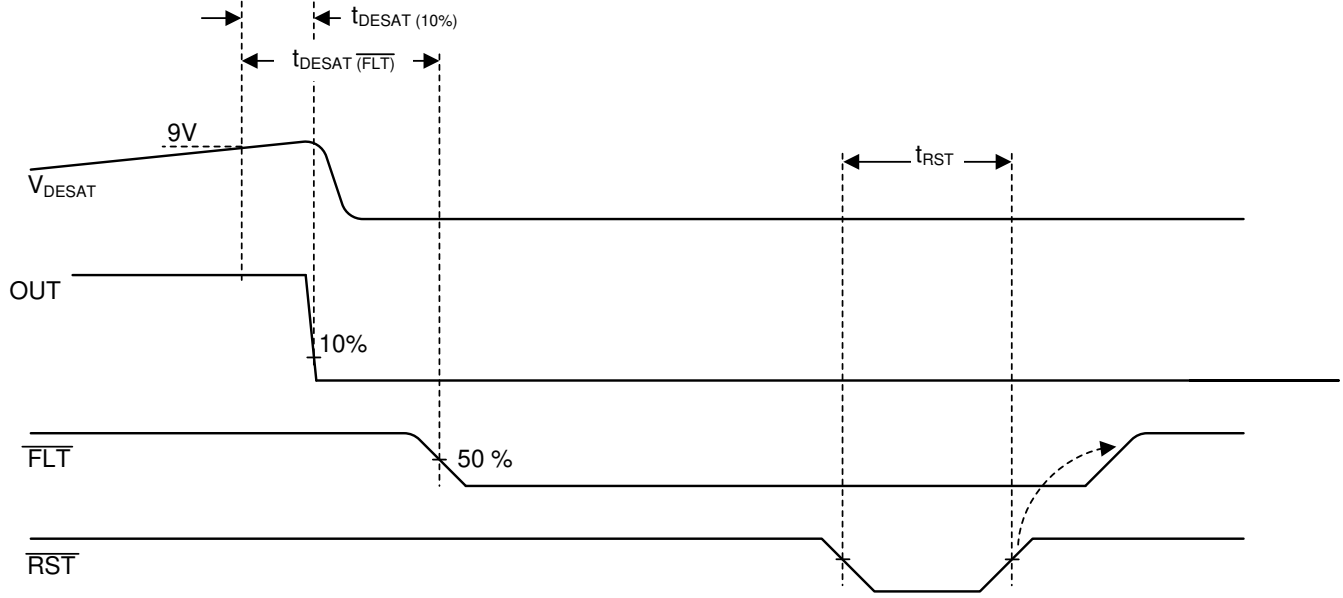
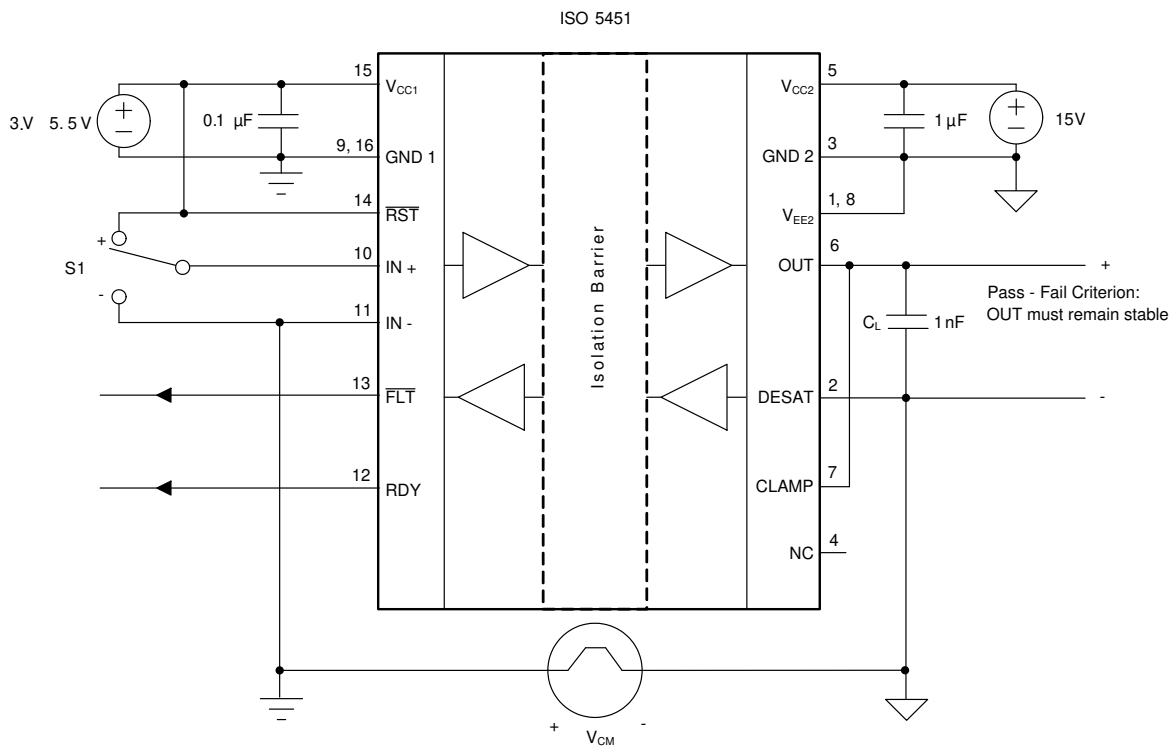


图 8-3. DESAT, OUT,  $\overline{FLT}$ ,  $\overline{RST}$  Delay



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图 8-4. Common-Mode Transient Immunity Test Circuit

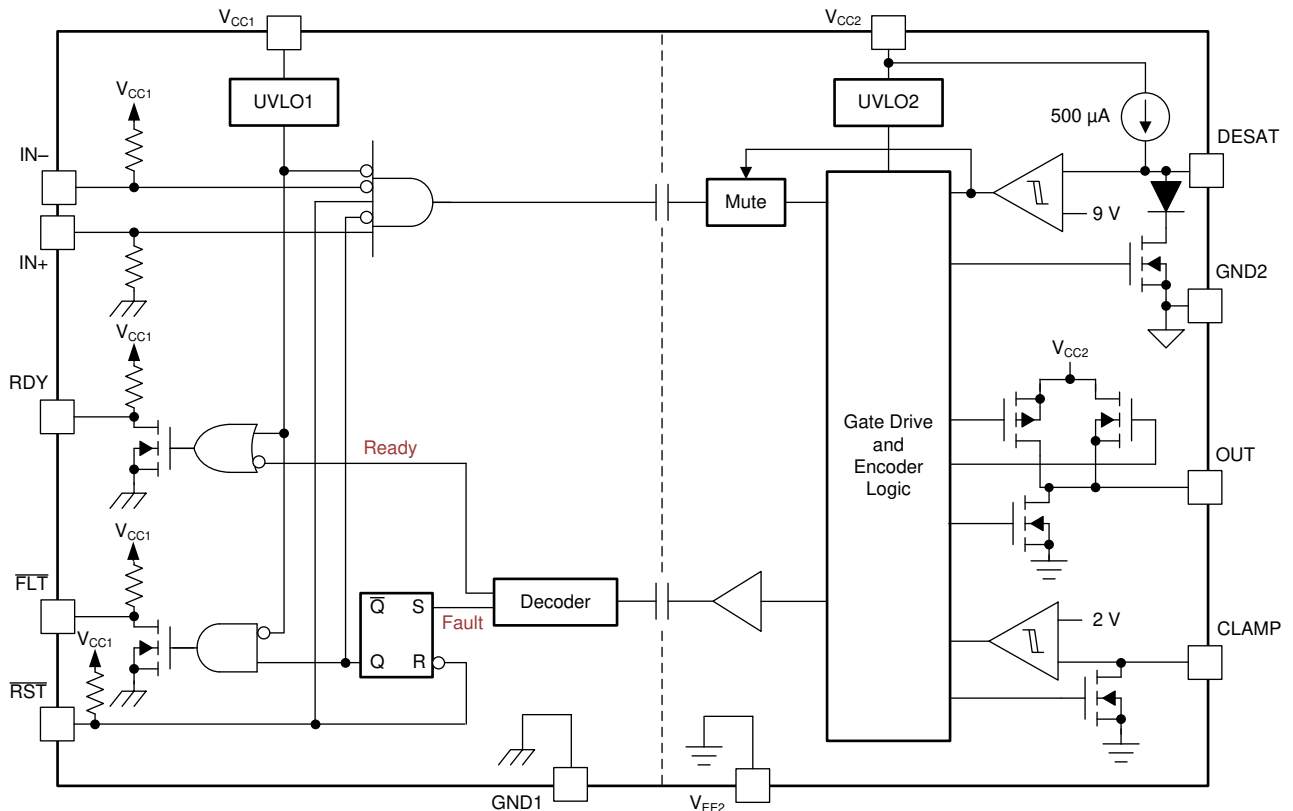
## 9 Detailed Description

### 9.1 Overview

The ISO5451 is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a capacitive, silicon dioxide (SiO<sub>2</sub>), isolation barrier.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and RESET ( $\overline{\text{RST}}$ ) inputs, READY (RDY) and FAULT ( $\overline{\text{FLT}}$ ) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5451 also contains undervoltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5451 also has an active Miller clamp function which can be used to prevent parasitic turnon of the external power transistor, because of Miller effect, for unipolar supply operation.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Supply and Active Miller Clamp

The ISO5451 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of  $V_{CC2}$  and  $V_{EE2}$  for bipolar operation are 15 V and -8 V with respect to GND2.

For operation with unipolar supply, typically,  $V_{CC2}$  is connected to 15 V with respect to GND2, and  $V_{EE2}$  is connected to GND2. In this use case, the IGBT can turn-on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected to IGBT gate and Miller current is sunk through a low impedance CLAMP transistor.

Miller CLAMP is designed for miller current up to 2 A. When the IGBT is turned-off and the gate voltage transitions below 2 V the CLAMP current output is activated.

### 9.3.2 Active Output Pull-down

The Active output pulldown feature ensures that the IGBT gate OUT is clamped to  $V_{EE2}$  to ensure safe IGBT off-state when the output side is not connected to the power supply.

### 9.3.3 Undervoltage Lockout (UVLO) with Ready (RDY) Pin Indication Output

Undervoltage Lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned-off, if the supply  $V_{CC1}$  drops below  $V_{IT-(UVLO1)}$ , irrespective of IN+, IN - and RST input till  $V_{CC1}$  goes above  $V_{IT+(UVLO1)}$ .

In similar manner, the IGBT is turned-off, if the supply  $V_{CC2}$  drops below  $V_{IT-(UVLO2)}$ , irrespective of IN+, IN - and RST input till  $V_{CC2}$  goes above  $V_{IT+(UVLO2)}$ .

Ready (RDY) pin indicates status of input and output side Under Voltage Lock-Out (UVLO) internal protection feature. If either side of device have insufficient supply ( $V_{CC1}$  or  $V_{CC2}$ ), the RDY pin output goes low; otherwise, RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

### 9.3.4 Fault (FLT) and Reset (RST)

During IGBT overload condition, to report desaturation error  $\overline{FLT}$  goes low. If  $\overline{RST}$  is held low for the specified duration,  $\overline{FLT}$  is cleared at rising edge of  $\overline{RST}$ .  $\overline{RST}$  has an internal filter to reject noise and glitches. By asserting  $\overline{RST}$  for at-least the specified minimum duration, device input logic can be enabled or disabled.

### 9.3.5 Short Circuit Clamp

Under short circuit events it is possible that currents are induced back into the gate-driver OUT and CLAMP pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUT and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

## 9.4 Device Functional Modes

For ISO5451 OUT to follow IN+ in normal functional mode,  $\overline{\text{RST}}$  and RDY must be in high state.

**表 9-1. Function Table<sup>(1)</sup>**

V <sub>CC1</sub>	V <sub>CC2</sub>	IN+	IN -	$\overline{\text{RST}}$	RDY	OUT
PU	PD	X	X	X	Low	Low
PD	PU	X	X	X	Low	Low
PU	PU	X	X	Low	High	Low
PU	Open	X	X	X	Low	Low
PU	PU	Low	X	X	High	Low
PU	PU	X	High	X	High	Low
PU	PU	High	Low	High	High	High

(1) PU: Power Up ( $V_{CC1} \geq 2.25\text{ V}$ ,  $V_{CC2} \geq 13\text{ V}$ ), PD: Power Down ( $V_{CC1} \leq 1.7\text{ V}$ ,  $V_{CC2} \leq 9.5\text{ V}$ ), X: Irrelevant

## 10 Application and Implementation

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### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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### 10.1 Application Information

The ISO5451 is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. It is intended for use in applications such as motor control, industrial inverters and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a micro controller, and are at low voltage levels such as 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 30 V (using unipolar output supply) to 15 V (using bipolar output supply), and need high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive needs to be applied with reference to the Emitter of the IGBT (source for MOSFET), and by construction, the Emitter node in a gate drive system may swing between 0 to the DC bus voltage, that can be several hundreds of volts in magnitude.

The ISO5451 is thus used to level shift the incoming 3.3-V and 5-V control signals from the microcontroller to the 30-V (using unipolar output supply) to 15-V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

### 10.2 Typical Applications

图 10-1 shows the typical application of a three-phase inverter using six ISO5451 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high power applications such as High-Voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one ISO5451. The switches are driven on and off at high switching frequency with specific patterns that to converter dc bus voltage to three-phase AC voltages.



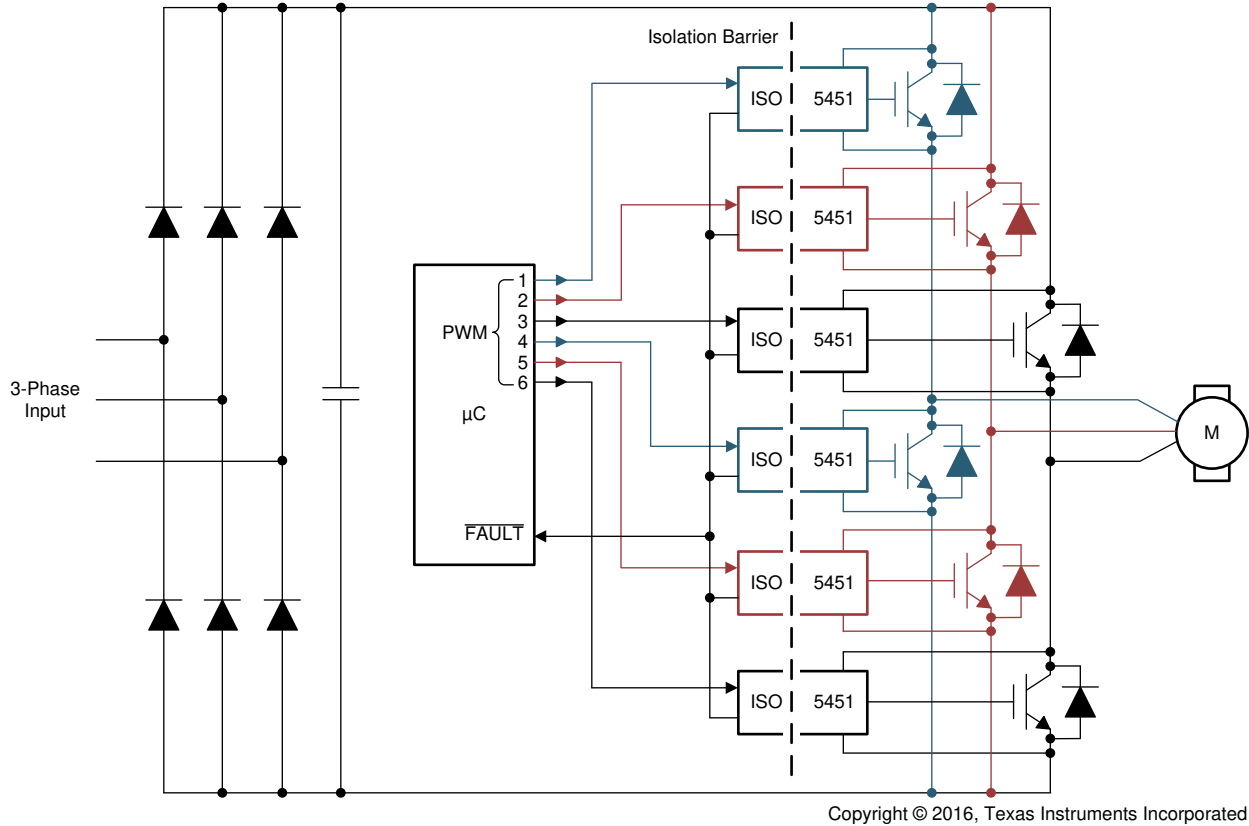


图 10-1. Typical Motor Drive Application

### 10.2.1 Design Requirements

Unlike optocoupler based gate drivers which need external current drivers and biasing circuitry to provide the input control signals, the input control to the device is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain FLT output signal and RST input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. 表 10-1 shows the allowed range for Input and Output supply voltage, and the typical current output available from the gate-driver.

表 10-1. Design Parameters

PARAMETER	VALUE
Input supply voltage	3-V to 5.5-V
Unipolar output supply voltage ( $V_{CC2} - GND2 = V_{CC2} - V_{EE2}$ )	15-V to 30-V
Bipolar output supply voltage ( $V_{CC2} - V_{EE2}$ )	15-V to 30-V
Bipolar output supply voltage ( $GND2 - V_{EE2}$ )	0-V to 15-V
Output current	2.5-A

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Recommended ISO5451 Application Circuit

The ISO5451 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications. The recommended application circuit in 图 10-2 shows a typical gate driver implementation with Unipolar Output Supply and 图 10-3 shows a typical gate driver implementation with Bipolar Output Supply using the ISO5451.

A 0.1- $\mu$ F bypass capacitor, recommended at input supply pin  $V_{CC1}$  and 1- $\mu$ F bypass capacitor, recommended at output supply pin  $V_{CC2}$ , provide the large transient currents necessary during a switching transition to ensure reliable operation. The 220 pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode ( $D_{DST}$ ) and its 1-k $\Omega$  series resistor are external protection components. The  $R_G$  gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain  $\overline{FLT}$  output and RDY output has a passive 10-k $\Omega$  pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

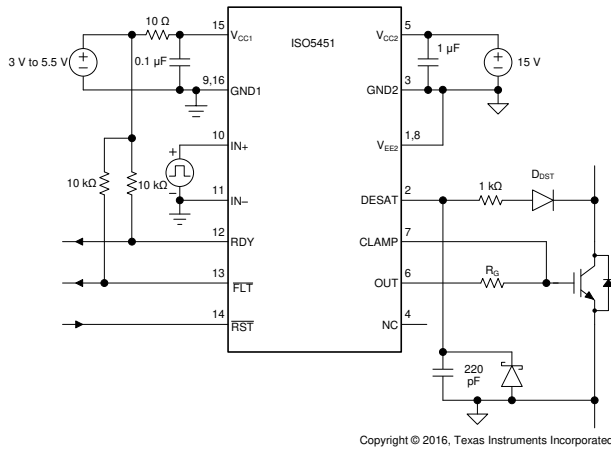


图 10-2. Unipolar Output Supply

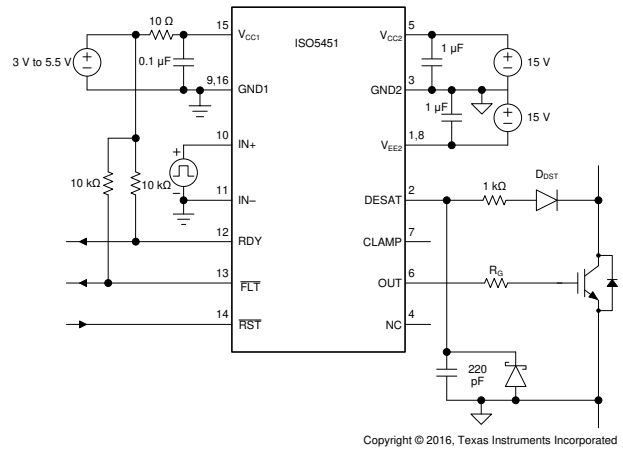


图 10-3. Bipolar Output Supply

### 10.2.2.2 $\overline{FLT}$ and RDY Pin Circuitry

There is 50k pullup resistor internally on  $\overline{FLT}$  and RDY pins. The  $\overline{FLT}$  and RDY pin is an open-drain output. A 10-k $\Omega$  pullup resistor can be used to make it faster rise and to provide logic high when  $\overline{FLT}$  and RDY is inactive, as shown in 图 10-4.

Fast common mode transients can inject noise and glitches on  $\overline{FLT}$  and RDY pins due to parasitic coupling. This is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the  $\overline{FLT}$  and RDY pins.

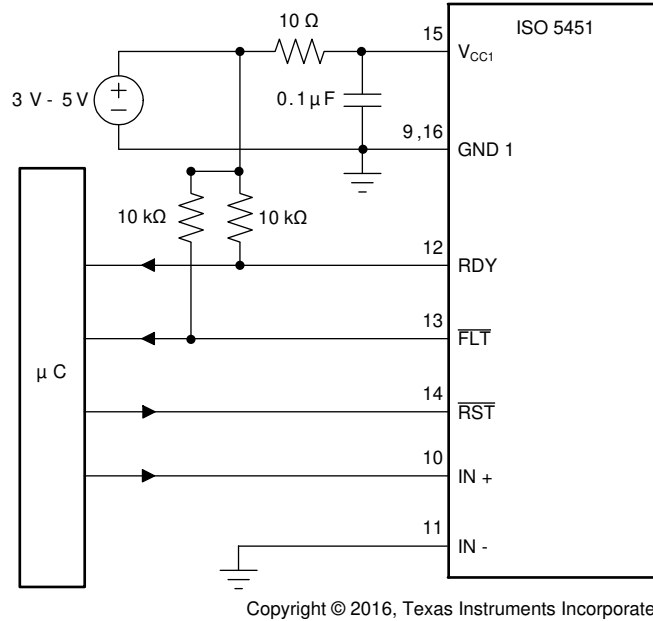


图 10-4.  $\overline{\text{FLT}}$  and RDY Pin Circuitry for High CMTI

### 10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5451. For maximum CMTI performance, the digital control inputs, IN+ and IN- , must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5451 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. There is a 20 ns glitch filter which can filter a glitch up to 20 ns on IN+ or IN- .

### 10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the  $\overline{\text{FLT}}$  output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

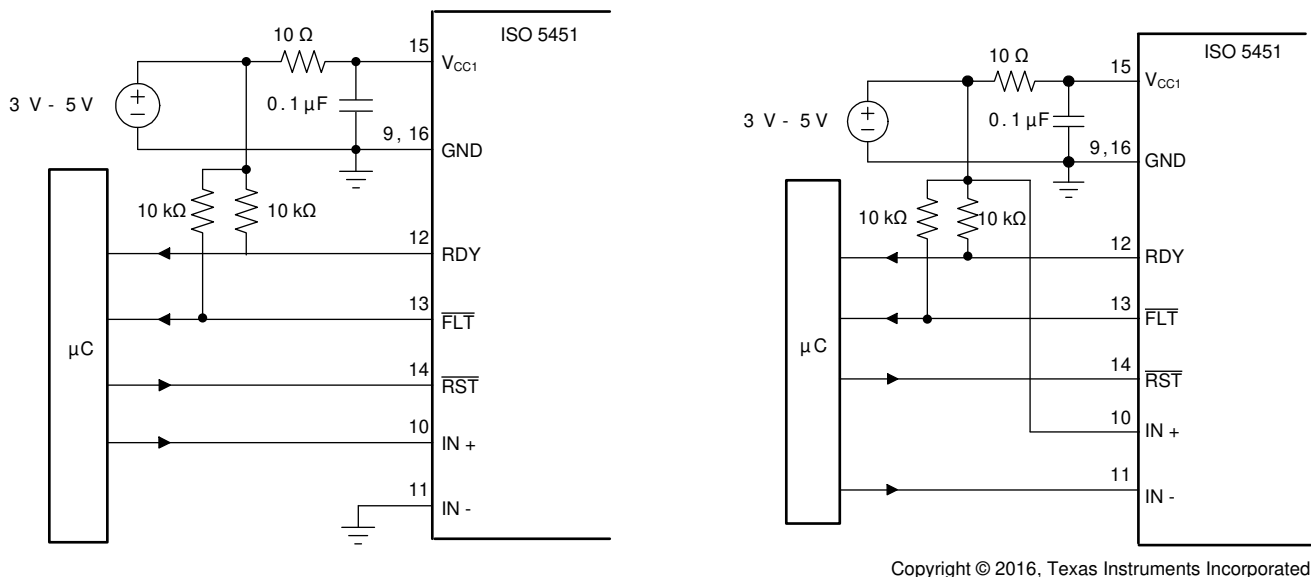
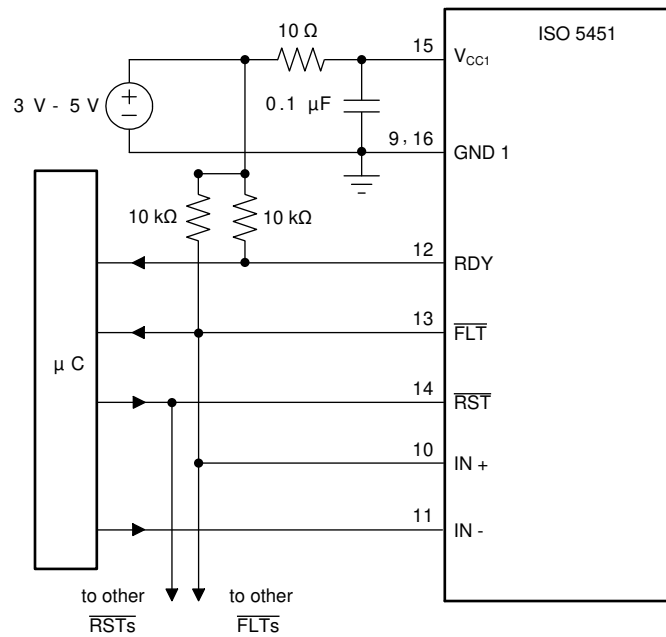


图 10-5. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)

### 10.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5451 can be configured to shutdown automatically in the event of a fault condition by tying the  $\overline{\text{FLT}}$  output to  $\text{IN}+$ . For high reliability drives, the open drain  $\overline{\text{FLT}}$  outputs of multiple ISO5451 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low  $\overline{\text{FLT}}$  output disables all six gate drivers simultaneously.



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图 10-6. Global Shutdown With Inverting Input Configuration

### 10.2.2.6 Auto-Reset

In this case, the gate control signal at  $\text{IN}+$  is also applied to the  $\overline{\text{RST}}$  input to reset the fault latch every switching cycle. Incorrect  $\overline{\text{RST}}$  makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the *gate low* state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before  $\text{IN}+$  goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next 'on' cycle.

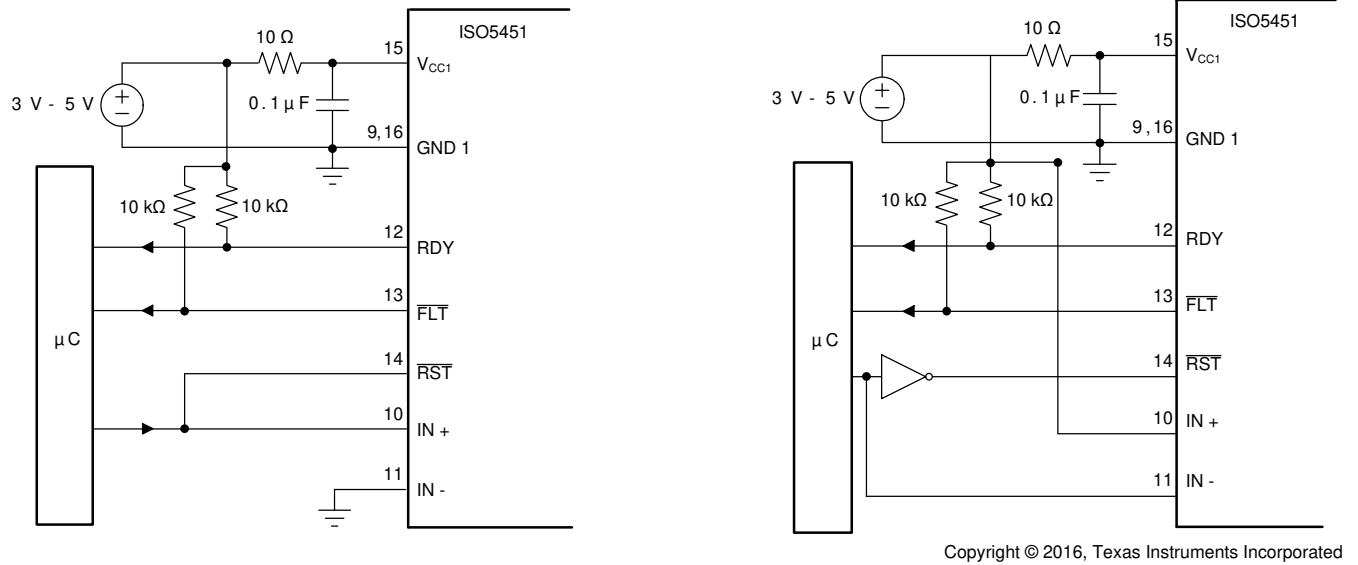


图 10-7. Auto Reset for Noninverting and Inverting Input Configuration

### 10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to GND2 potential at low voltage levels.

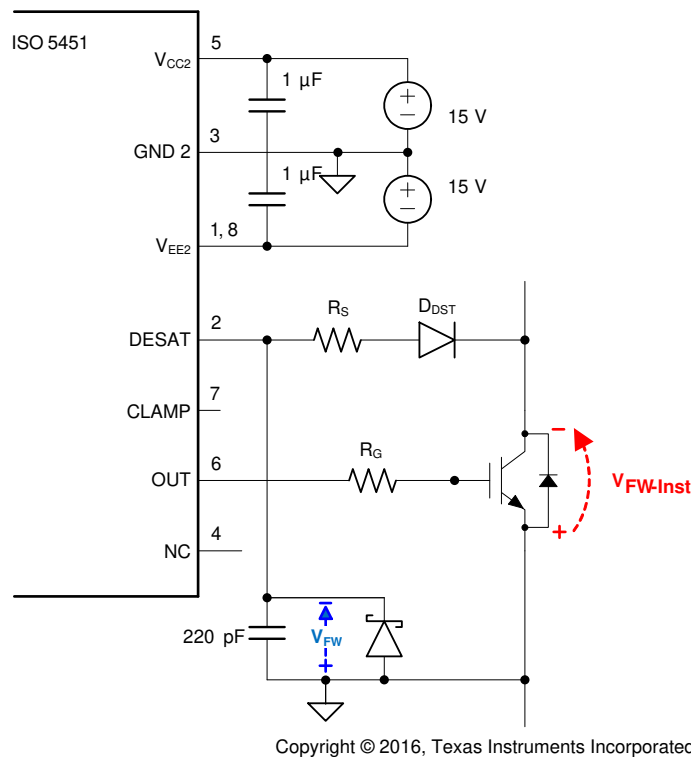


图 10-8. DESAT Pin Protection with Series Resistor and Schottky Diode

### 10.2.2.8 DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage,  $V_{(CESAT)}$ , (when the IGBT is *on*) and to block high voltages (when the IGBT is *off*). During the short transition time when the IGBT is switching, there is commonly a high  $dV_{CE}/dt$  voltage ramp rate across the IGBT. This results in a charging current  $I_{(CHARGE)} = C_{(D-DESAT)} \times dV_{CE}/dt$ , charging the blanking capacitor.  $C_{(D-DESAT)}$  is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of  $1 + C_{(BLANK)} / C_{(D-DESAT)}$ .

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin,  $V_F + V_{CE} = V_{(DESAT)}$ , the  $V_{CE}$  level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series:  $V_{CE-FAULT(TH)} = 9V - n \times V_F$  (where  $n$  is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

### 10.2.2.9 Determining the Maximum Available, Dynamic Output Power, $P_{OD-max}$

The ISO5451 maximum allowed total power consumption of  $P_D = 251$  mW consists of the total input power,  $P_{ID}$ , the total output power,  $P_{OD}$ , and the output power under load,  $P_{OL}$ :

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (1)$$

With:

$$P_{ID} = V_{CC1-max} \times I_{CC1-max} = 5.5 \text{ V} \times 4.5 \text{ mA} = 24.75 \text{ mW} \quad (2)$$

and:

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{CC2-max} = (15\text{V} - (-8\text{V})) \times 6 \text{ mA} = 138 \text{ mW} \quad (3)$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251 \text{ mW} - 24.75 \text{ mW} - 138 \text{ mW} = 88.25 \text{ mW} \quad (4)$$

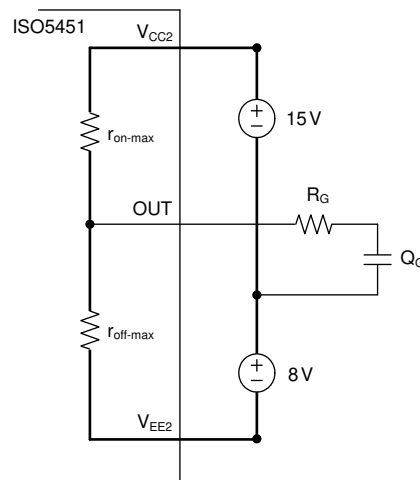
In comparison to  $P_{OL}$ , the actual dynamic output power under worst case condition,  $P_{OL-WC}$ , depends on a variety of parameters:

$$P_{OL-WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left( \frac{r_{on-max}}{r_{on-max} + R_G} + \frac{r_{off-max}}{r_{off-max} + R_G} \right) \quad (5)$$

where

- $f_{INP}$  = signal frequency at the control input IN+
- $Q_G$  = power device gate charge
- $V_{CC2}$  = positive output supply with respect to GND2
- $V_{EE2}$  = negative output supply with respect to GND2
- $r_{on-max}$  = worst case output resistance in the on-state:  $4 \Omega$
- $r_{off-max}$  = worst case output resistance in the off-state:  $2.5 \Omega$
- $R_G$  = gate resistor

Once  $R_G$  is determined, 方程式 5 is to be used to verify whether  $P_{OL-WC} < P_{OL}$ . 图 10-9 shows a simplified output stage model for calculating  $P_{OL-WC}$ .



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图 10-9. Simplified Output Model for Calculating  $P_{OL-WC}$

### 10.2.2.10 Example

This example considers an IGBT drive with the following parameters:

$$I_{ON-PK} = 2 \text{ A}, Q_G = 650 \text{ nC}, f_{INP} = 20 \text{ kHz}, V_{CC2} = 15\text{V}, V_{EE2} = -8 \text{ V} \quad (6)$$

Apply the value of the gate resistor  $R_G = 10 \Omega$ .

Then, calculating the worst-case output power consumption as a function of  $R_G$ , using 方程式 5  $r_{on-max}$  = worst case output resistance in the on-state:  $4 \Omega$ ,  $r_{off-max}$  = worst case output resistance in the off-state:  $2.5 \Omega$ ,  $R_G$  = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20 \text{ kHz} \times 650 \text{ nC} \times (15 \text{ V} - (-8 \text{ V})) \times \left( \frac{4 \Omega}{4 \Omega + 10 \Omega} + \frac{2.5 \Omega}{2.5 \Omega + 10 \Omega} \right) = 72.61 \text{ mW} \quad (7)$$

Because  $P_{OL-WC} = 72.61 \text{ mW}$  is below the calculated maximum of  $P_{OL} = 88.25 \text{ mW}$ , the resistor value of  $R_G = 10 \Omega$  is suitable for this application.

### 10.2.2.11 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/npn buffer shown in 图 10-10) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/D45VH10 pair for up to 15 A maximum.

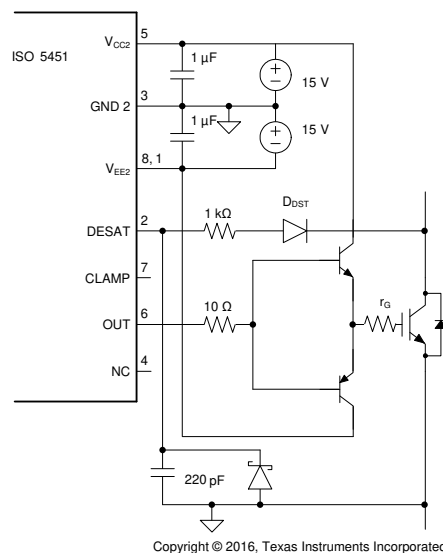
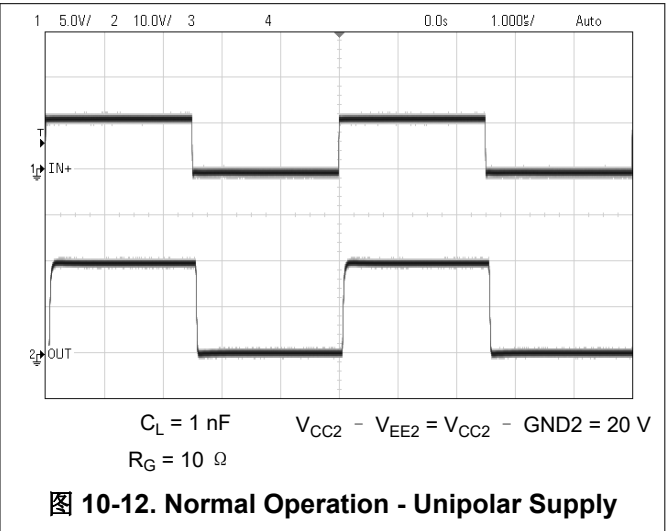
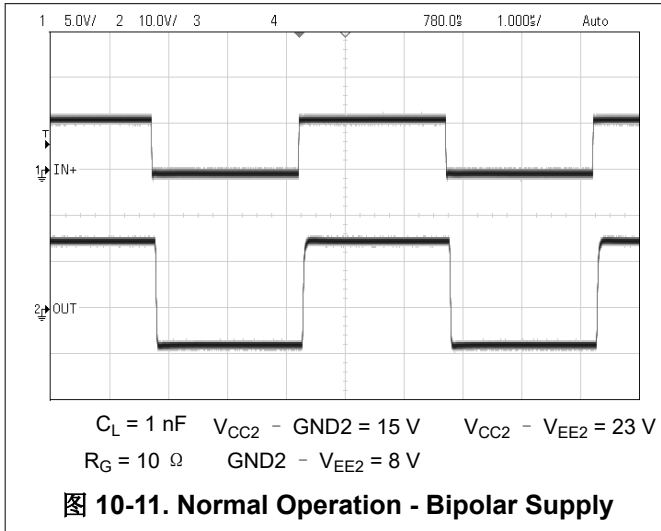


图 10-10. Current Buffer for Increased Drive Current



### 10.2.3 Application Curves



## 11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at input supply pin  $V_{CC1}$  and 1- $\mu$ F bypass capacitor is recommended at output supply pin  $V_{CC2}$ . The capacitors should be placed as close to the supply pins as possible. The recommended placement of capacitors is 2-mm maximum from input and output power supply pin ( $V_{CC1}$  and  $V_{CC2}$ ).

## 12 Layout

### 12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [图 12-1](#)). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output OUT and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch<sup>2</sup>. On the gate-driver  $V_{EE2}$  and  $V_{CC2}$  can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For detailed layout recommendations, see the [Digital Isolator Design Guide](#) (SLLA284).

### 12.2 Layout Example

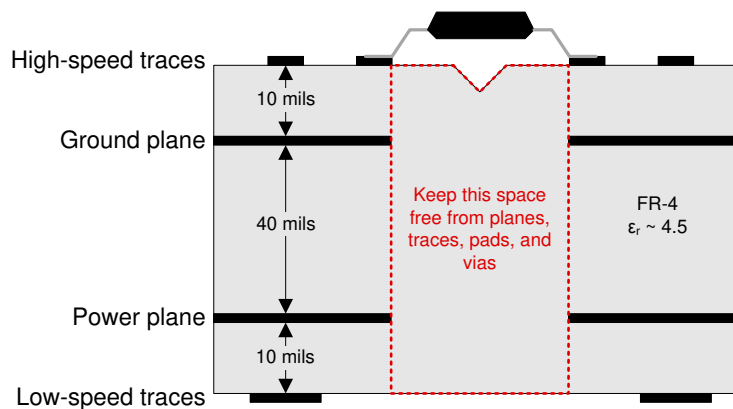


图 12-1. Recommended Layer Stack

### 12.3 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 13 Device and Documentation Support

### 13.1 Device Support

#### 13.1.1 第三方产品免责声明

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### 13.2 Documentation Support

#### 13.2.1 Related Documentation

For related documentation see the following:

- [Isolation Glossary](#)
- [ISO5851 Evaluation Module \(EVM\) User's Guide](#)
- [Digital Isolator Design Guide](#)

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO5451DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5451	
ISO5451DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5451	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF ISO5451 :**

- Automotive : [ISO5451-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO5451DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO5451DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO5451DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO5451DWR	SOIC	DW	16	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ISO5451DW	DW	SOIC	16	40	507	12.83	5080	6.6
ISO5451DW	DW	SOIC	16	40	506.98	12.7	4826	6.6

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