

INA134 INA2134

AUDIO DIFFERENTIAL LINE RECEIVERS 0dB (G = 1)

FEATURES

- SINGLE AND DUAL VERSIONS
- LOW DISTORTION: 0.0005% at $f = 1\text{kHz}$
- HIGH SLEW RATE: $14\text{V}/\mu\text{s}$
- FAST SETTLING TIME: $3\mu\text{s}$ to 0.01%
- WIDE SUPPLY RANGE: $\pm 4\text{V}$ to $\pm 18\text{V}$
- LOW QUIESCENT CURRENT: 2.9mA max
- HIGH CMRR: 90dB
- FIXED GAIN = 0dB (1V/V)
- PACKAGES—SINGLE: 8-PIN DIP, SO-8

DUAL: 14-PIN DIP, SO-14

DESCRIPTION

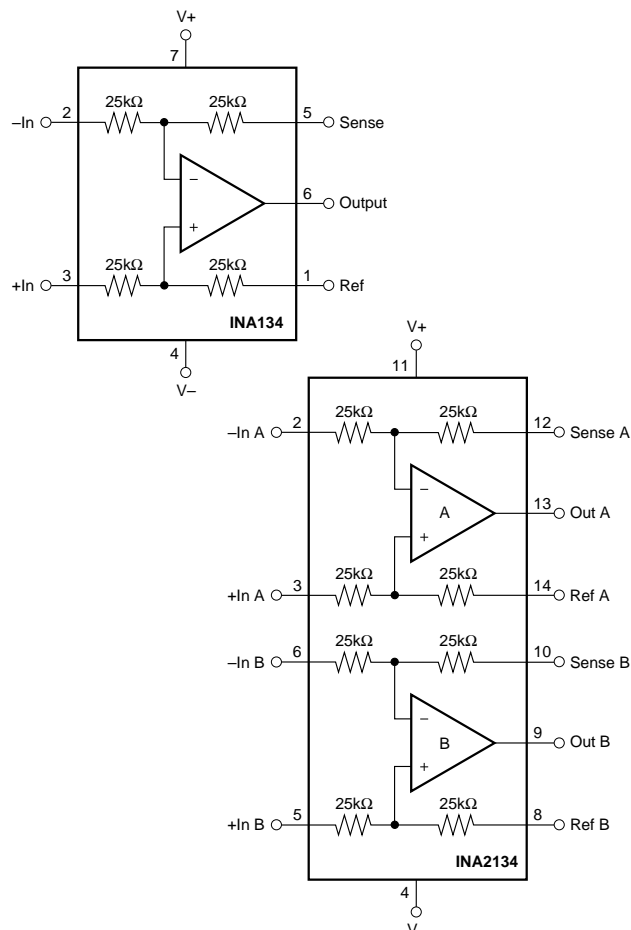
The INA134 and INA2134 are differential line receivers consisting of high performance op amps with on-chip precision resistors. They are fully specified for high performance audio applications and have excellent ac specifications, including low distortion (0.0005% at 1kHz) and high slew rate ($14\text{V}/\mu\text{s}$), assuring good dynamic response. In addition, wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. The dual version features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The INA134 and INA2134 on-chip resistors are laser trimmed for accurate gain and optimum common-mode rejection. Furthermore, excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. Operation is guaranteed from $\pm 4\text{V}$ to $\pm 18\text{V}$ (8V to 36V total supply).

The INA134 is available in 8-pin DIP and SO-8 surface-mount packages. The INA2134 comes in 14-pin DIP and SO-14 surface-mount packages. Both are specified for operation over the extended industrial temperature range, -40°C to $+85^\circ\text{C}$.

APPLICATIONS

- AUDIO DIFFERENTIAL LINE RECEIVER
- SUMMING AMPLIFIER
- UNITY-GAIN INVERTING AMPLIFIER
- PSUEDOGROUND GENERATOR
- INSTRUMENTATION BUILDING BLOCK
- CURRENT SHUNT MONITOR
- VOLTAGE-CONTROLLED CURRENT SOURCE
- GROUND LOOP ELIMINATOR



SPECIFICATIONS: $V_S = \pm 18V$

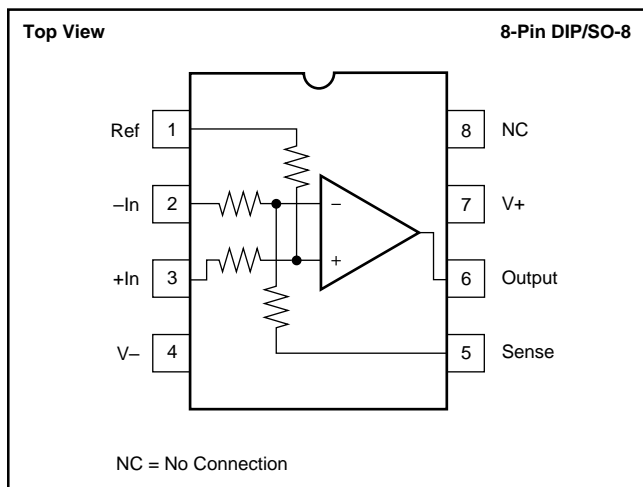
At $T_A = +25^\circ C$, $V_S = \pm 18V$, $R_L = 2k\Omega$, and Ref Pin connected to Ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA134PA, UA INA2134PA, UA			UNITS
		MIN	TYP	MAX	
AUDIO PERFORMANCE Total Harmonic Distortion + Noise, $f = 1kHz$ Noise Floor ⁽¹⁾ Headroom ⁽¹⁾	$V_{IN} = 10V_{rms}$ 20kHz BW THD+N < 1%		0.0005 -100 +23		% dBu dBu
FREQUENCY RESPONSE Small-Signal Bandwidth Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Channel Separation (dual), $f = 1kHz$	10V Step, $C_L = 100pF$ 10V Step, $C_L = 100pF$ 50% Overdrive		3.1 14 2 3 3 117		MHz V/ μs μs μs μs dB
OUTPUT NOISE VOLTAGE ⁽²⁾ $f = 20Hz$ to 20kHz $f = 1kHz$			7 52		μV_{rms} nV/ \sqrt{Hz}
OFFSET VOLTAGE ⁽³⁾ Input Offset Voltage vs Temperature vs Power Supply	$V_{CM} = 0V$ Specified Temperature Range $V_S = \pm 4V$ to $\pm 18V$		± 100 ± 2 ± 5	± 1000 ± 60	μV $\mu V/^\circ C$ $\mu V/V$
INPUT Common-Mode Voltage Range: Positive Negative Differential Voltage Range Common-Mode Rejection Impedance ⁽⁴⁾ Differential Common-Mode	$V_O = 0V$ $V_O = 0V$ $V_{CM} = \pm 31V$, $R_S = 0\Omega$	2(V+)-5 2(V-)+5 74	2(V+)-4 2(V-)+2 See Typical Curve 90 50 50		V V dB k Ω k Ω
GAIN Initial Error vs Temperature Nonlinearity	$V_O = -16V$ to 16V $V_O = -16V$ to 16V		1 ± 0.02 ± 1 0.0001	± 0.1 ± 10	V/V % ppm/ $^\circ C$ %
OUTPUT Voltage Output, Positive Negative Current Limit, Continuous to Common Capacitive Load (Stable Operation)		(V+)-2 (V-)+2	(V+)-1.8 (V-)+1.6 ± 60 500		V V mA pF
POWER SUPPLY Rated Voltage Voltage Range Quiescent Current (per Amplifier)	 $I_O = 0$	± 4	± 18 ± 2.4	± 18 ± 2.9	V V mA
TEMPERATURE RANGE Specification Range Operation Range Storage Range Thermal Resistance, θ_{JA} 8-Pin DIP SO-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount		-40 -55 -55	 100 150 80 100	85 125 125	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

NOTES: (1) dBu = $20\log (V_{rms}/0.7746)$. (2) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (3) Includes effects of amplifier's input bias and offset currents. (4) 25k Ω resistors are ratio matched but have $\pm 25\%$ absolute value.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

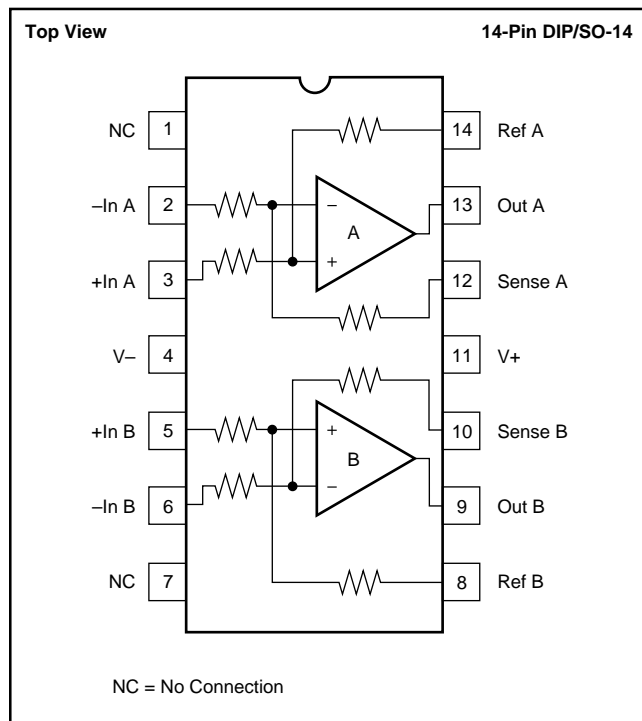
Supply Voltage, V+ to V-	40V
Input Voltage Range	±80V
Output Short-Circuit (to ground) ⁽²⁾	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage.
(2) One channel per package.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFICATION TEMPERATURE RANGE
Single			
INA134PA	8-Pin DIP	006	-40°C to +85°C
INA134UA	SO-8 Surface-Mount	182	-40°C to +85°C
Dual			
INA2134PA	14-Pin DIP	010	-40°C to +85°C
INA2134UA	SO-14 Surface-Mount	235	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



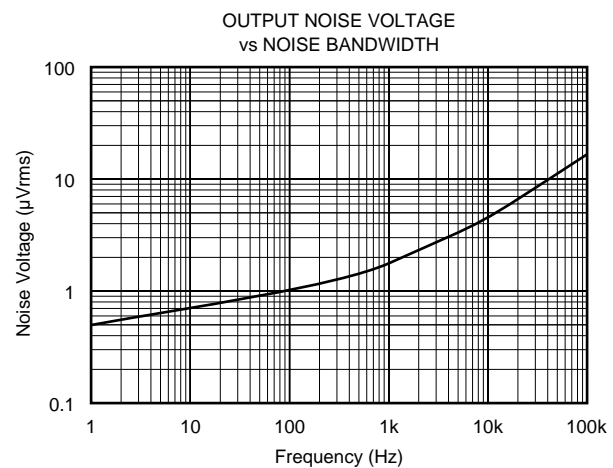
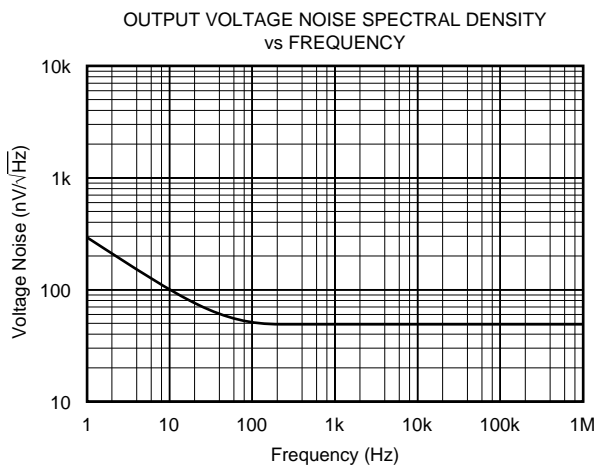
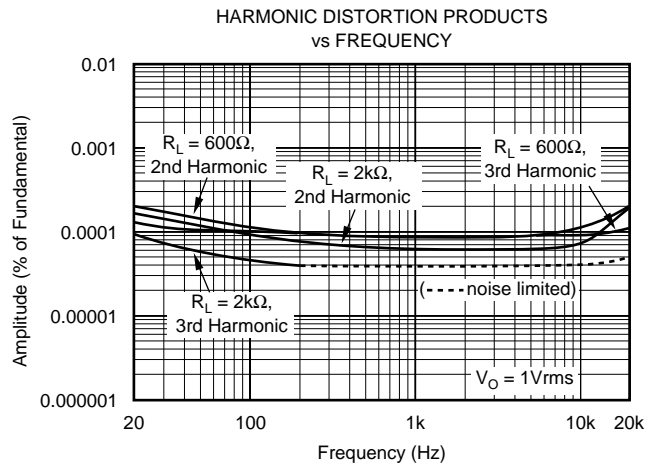
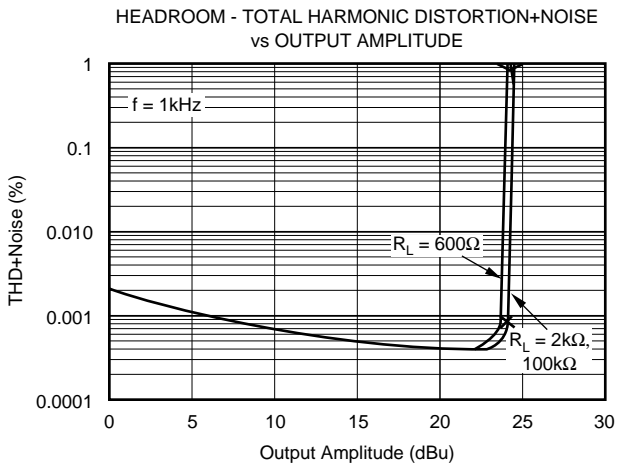
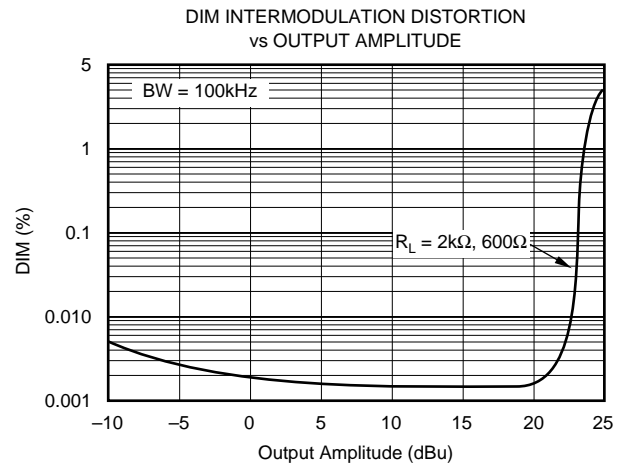
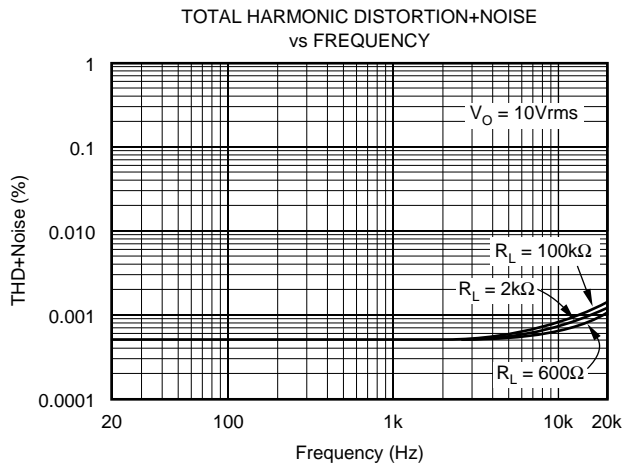
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

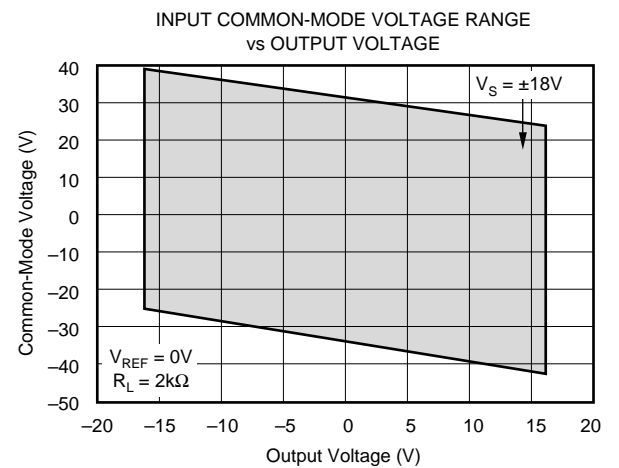
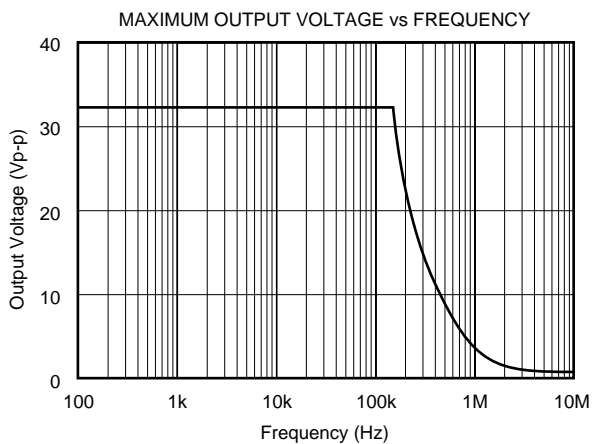
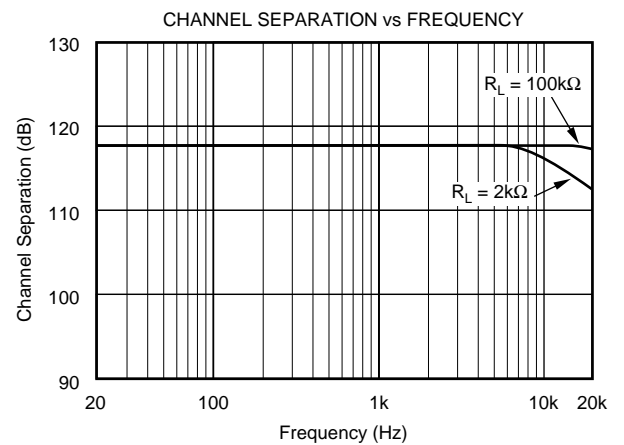
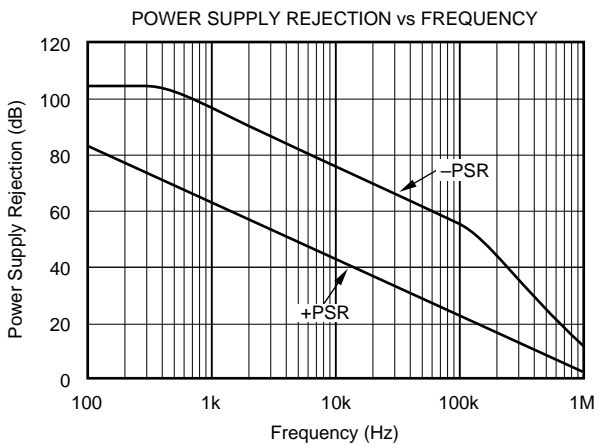
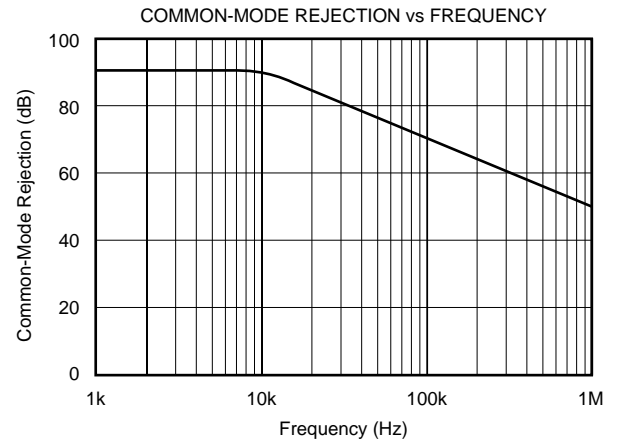
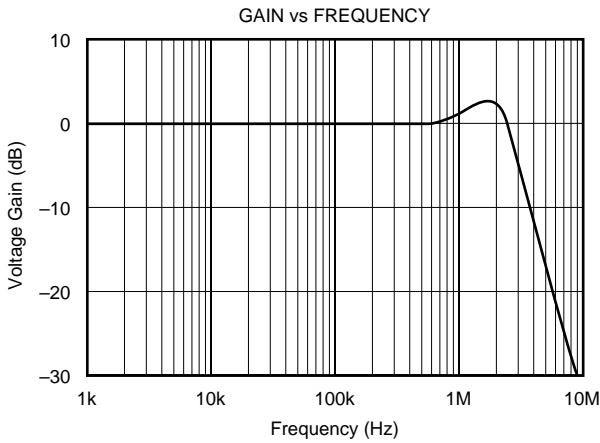
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, unless otherwise noted.



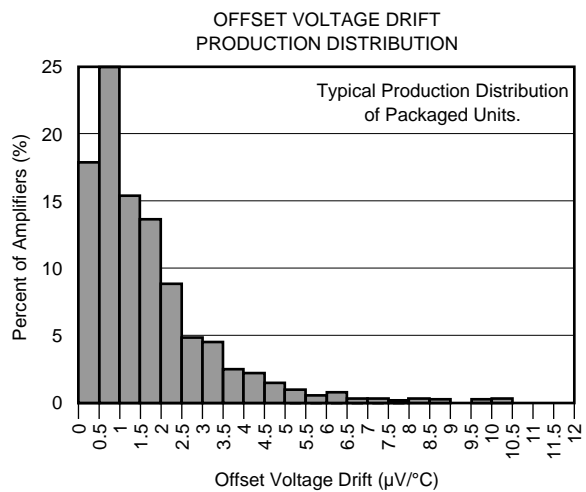
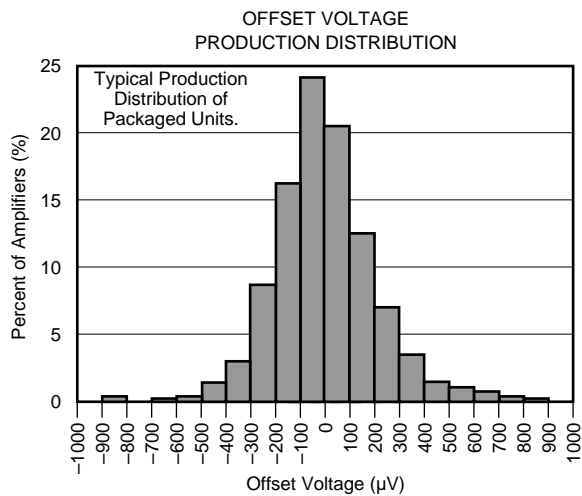
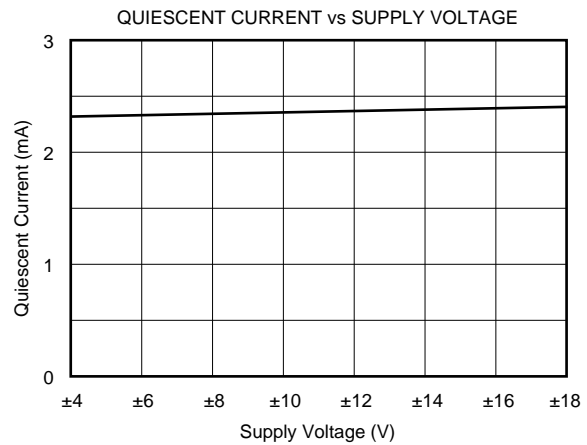
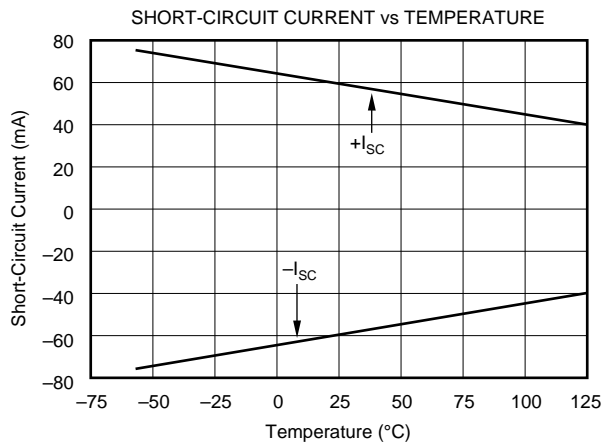
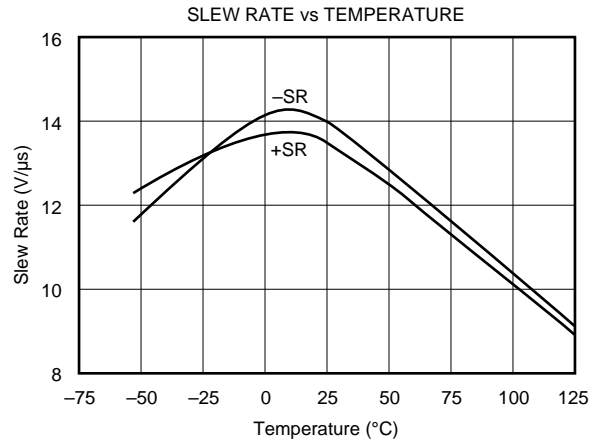
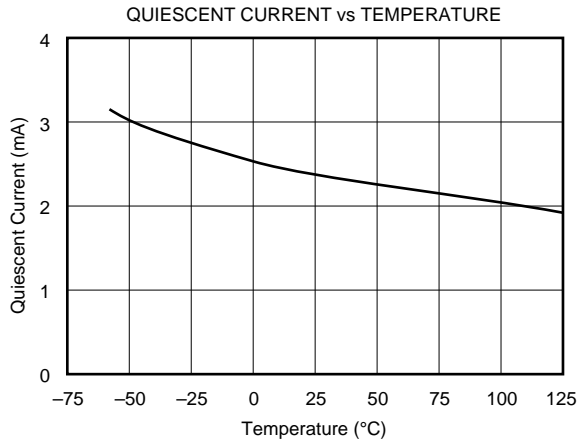
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, unless otherwise noted.



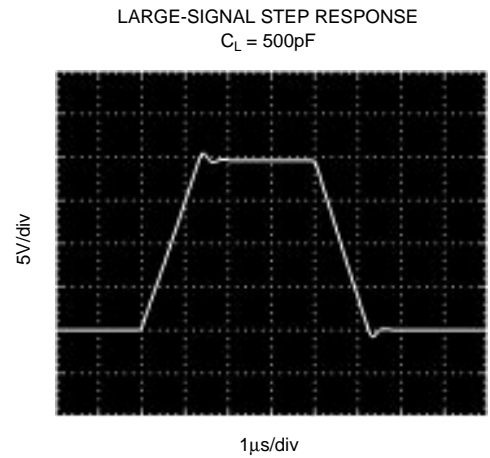
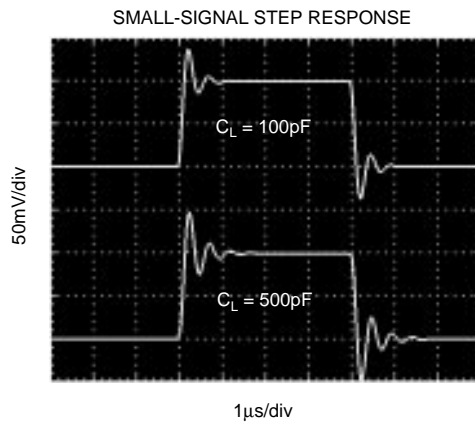
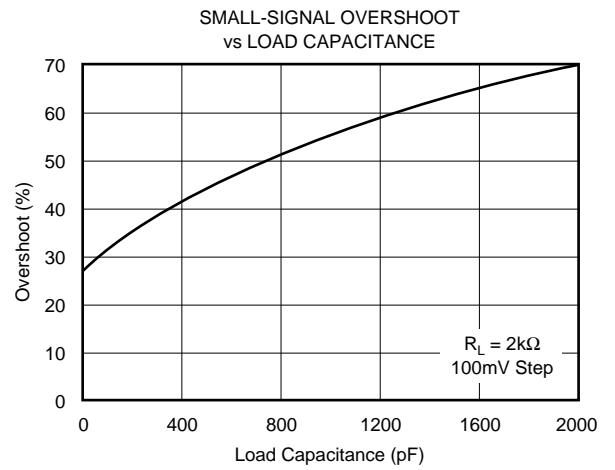
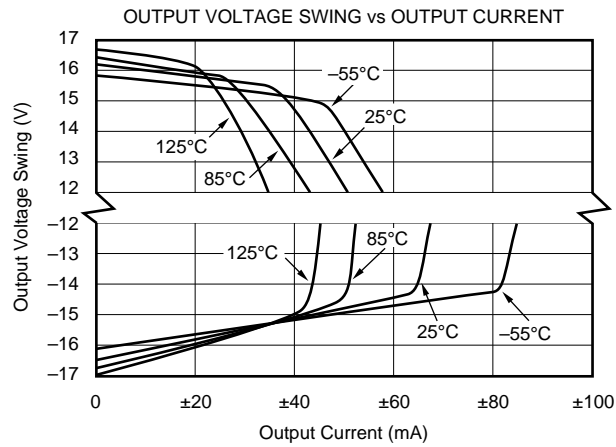
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA134. Decoupling capacitors are strongly recommended in applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 1. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 1, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 10Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 74dB. If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

AUDIO PERFORMANCE

The INA134 and INA2134 were designed for enhanced ac performance. Very low distortion, low noise, and wide bandwidth provide superior performance in high quality audio applications. Laser-trimmed matched resistors provide optimum common-mode rejection (typically 90dB), especially when compared to circuits implemented with an op amp and discrete precision resistors. In addition, high slew rate ($14\text{V}/\mu\text{s}$) and fast settling time ($3\mu\text{s}$ to 0.01%) ensure good dynamic performance.

The INA134 and INA2134 have excellent distortion characteristics. THD+Noise is below 0.002% throughout the audio frequency range. Up to approximately 10kHz distortion is below the measurement limit of commonly used test equipment. Furthermore, distortion remains relatively flat over its wide output voltage swing range (approximately 1.7V from either supply).

OFFSET VOLTAGE TRIM

The INA134 and INA2134 are laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

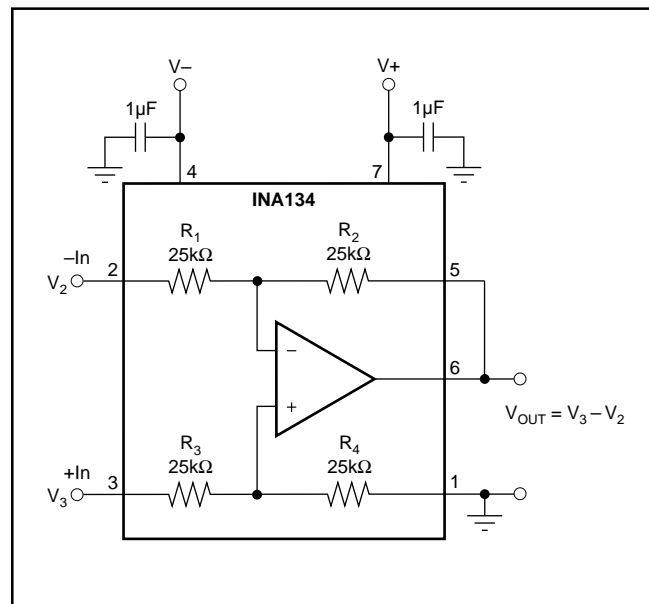


FIGURE 1. Precision Difference Amplifier (Basic Power Supply and Signal Connections).

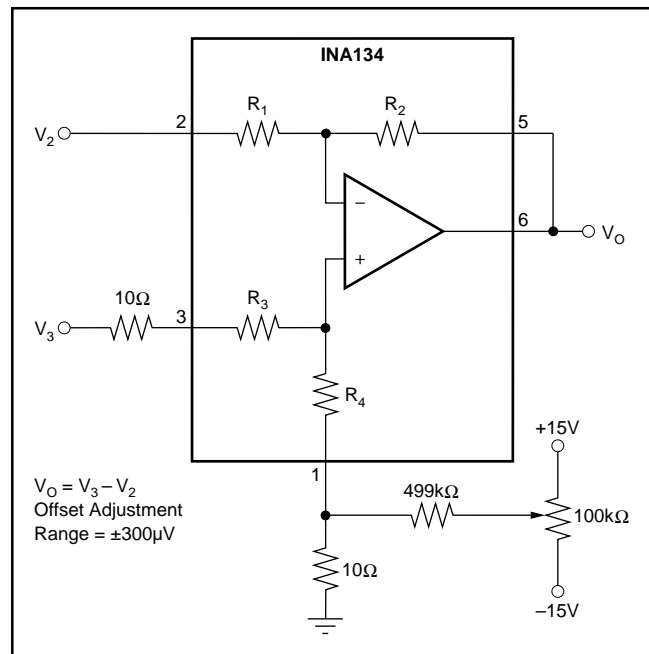


FIGURE 2. Offset Adjustment.

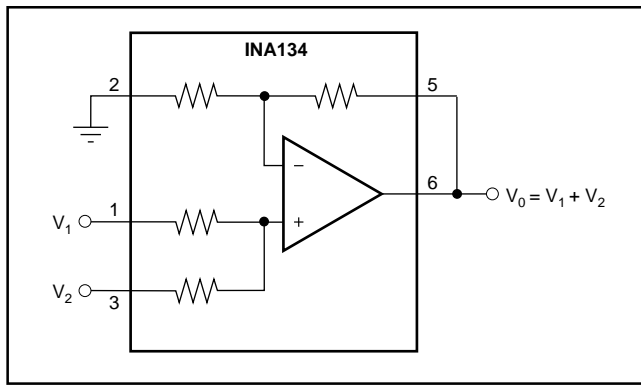


FIGURE 3. Precision Summing Amplifier.

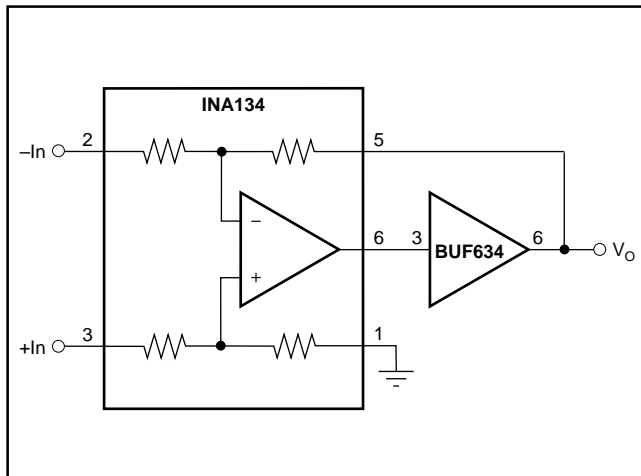


FIGURE 4. Boosting Output Current.

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- $\pm 10\text{V}$ Precision Voltage Reference
- $\pm 5\text{V}$ Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision $G = 2$ Amplifier
- Precision Summing Amplifier
- Precision $G = 1/2$ Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator

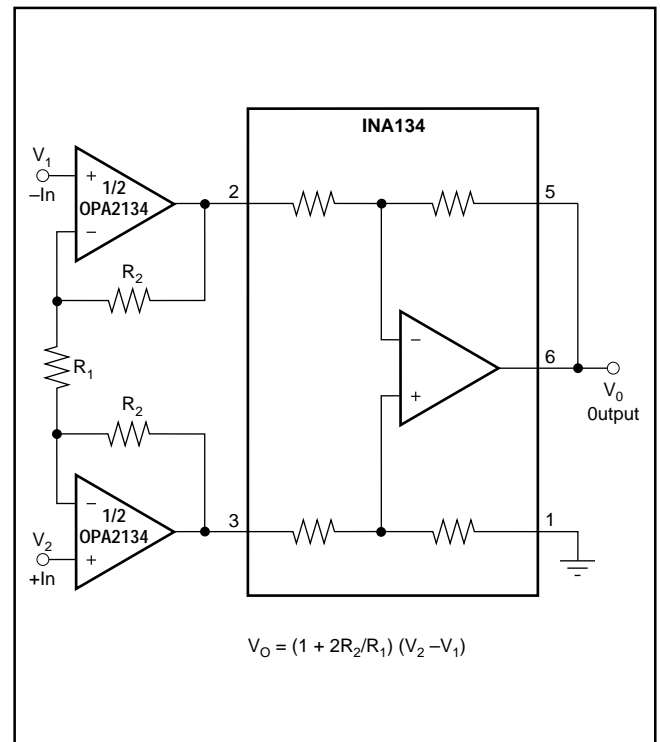


FIGURE 5. High Input Impedance Instrumentation Amplifier.

- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low I_{OUT}
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ± 1 Amplifier

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA134PA	Obsolete	Production	PDIP (P) 8	-	-	Call TI	Call TI	-40 to 85	INA134PA
INA134UA	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 134UA
INA134UA.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 134UA
INA134UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 134UA
INA134UA/2K5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 134UA
INA2134PA	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	INA2134PA
INA2134PA.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	INA2134PA
INA2134UA	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2134UA
INA2134UA.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2134UA
INA2134UA/2K5	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2134UA
INA2134UA/2K5.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2134UA

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA2134 :

- Enhanced Product : [INA2134-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2134UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA134UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA2134UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA134UA	D	SOIC	8	75	506.6	8	3940	4.32
INA134UA.A	D	SOIC	8	75	506.6	8	3940	4.32
INA2134PA	N	PDIP	14	25	506	13.97	11230	4.32
INA2134PA.A	N	PDIP	14	25	506	13.97	11230	4.32
INA2134UA	D	SOIC	14	50	506.6	8	3940	4.32
INA2134UA.A	D	SOIC	14	50	506.6	8	3940	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025