具有 I/O 电平自适应和低功率模式电源优化的 5V 控制器局域网 (CAN) 收发器

查询样品: HVDA551-Q1, HVDA553-Q1

特性

- 符合汽车应用要求
- 符合或超过 **ISO 11898-2** 和 **ISO 11898-5** 的要求
- **GIFT/ICT** 兼容
- 总线引脚上的静电放电 **(ESD)** 保护高达 **±12kV**（人体模型）
- **I/O** 电压电平自适应
  - **HVDA551**：自适应 **I/O** 电压范围 **(V_{IO})** 从 **3V** 至 **5.33V**
- 分离式电压源
  - **HVDA553**：共模总线稳定
- 运行模式：
  - 正常模式
  - 具有 **RXD** 唤醒请求的低功率待机模式
- 高电磁兼容性 **(EMC)**
- 支持 **CAN** 灵活数据速率 **(FD)**
- 保护
  - **V_{IO}**和 **V_{CC}**上的欠压保护
  - **-27V** 至 **40V** 的总线故障保护
  - **TXD** 主状态超时
  - **CAN** 总线阻塞主故障时的 **RXD** 唤醒请求闭锁 **(HVDA551)**
  - 数字输入与 **5V** 微处理器兼容 **(HVDA553)**
  - 热关断保护
  - 加电和断电无毛刺脉冲总线 **I/O**
  - 未加电时（无总线负载）时高总线输入阻抗

应用范围

- 针对汽车应用的 **SAE J2284** 高速 **CAN**
- **SAE J1939** 标准数据总线接口
- **GMW3122** 双线制 **CAN** 物理层
- **ISO 11783** 标准数据总线接口
- **NMEA 2000** 标准数据总线

说明

此器件被设计成在汽车应用中使用，满足汽车应用的要求，并且符合或超过 ISO 11898 高速 CAN（控制器局域网）物理层标准（收发器）的技术规格。

FUNCTIONAL BLOCK DIAGRAMS

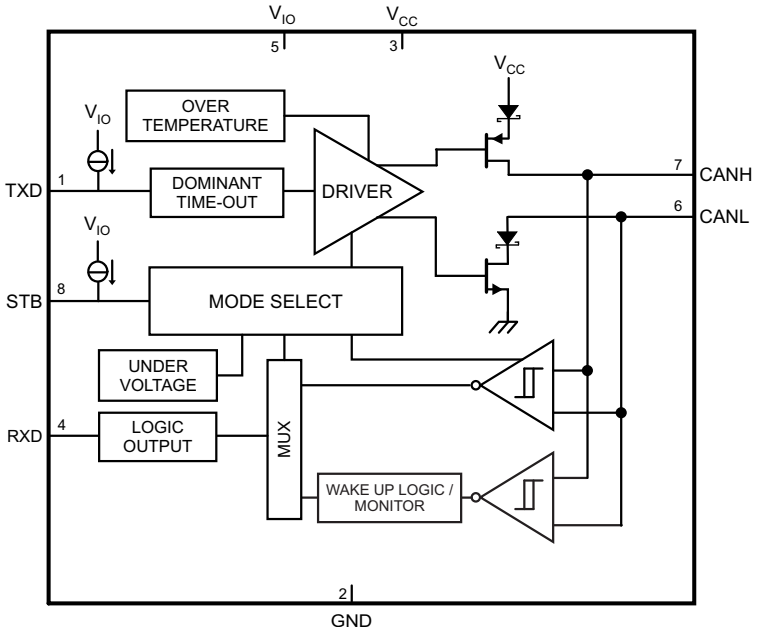


Figure 1. HVDA551

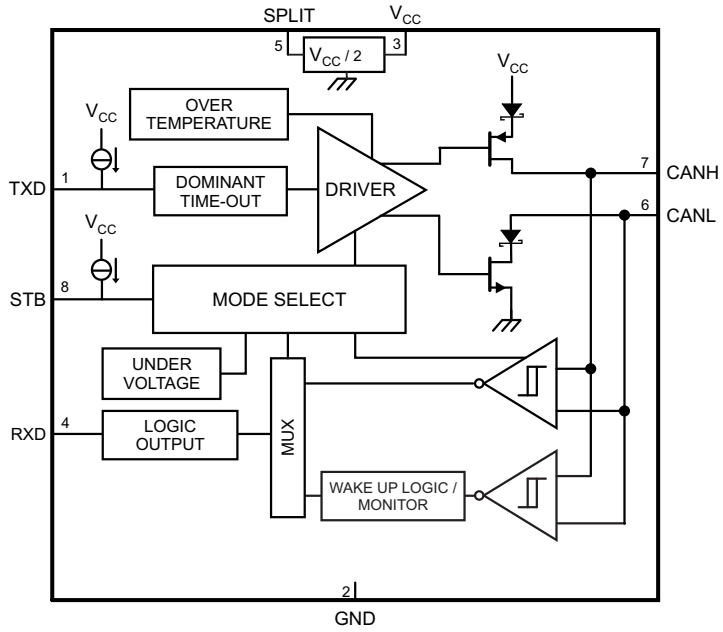


Figure 2. HVDA553

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

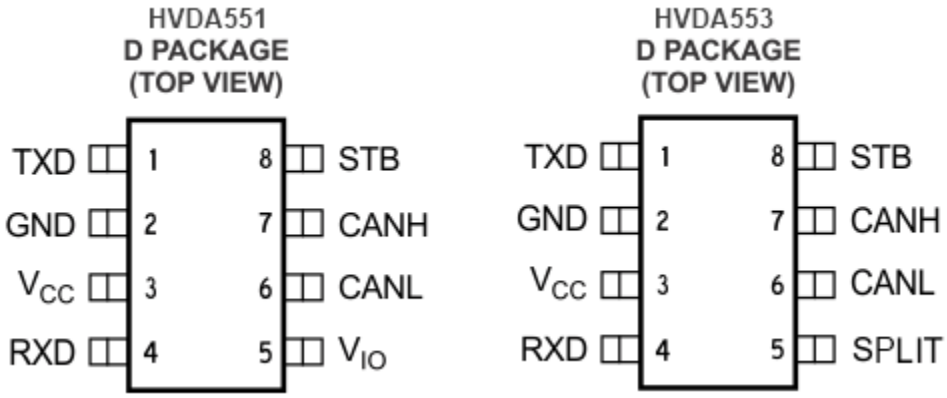


Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	D Package (SOIC) NO.		
CANH	7	I/O	High level CAN bus line
CANL	6	I/O	Low level CAN bus line
GND	2	GND	Ground connection
RXD	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
STB	8	I	Standby mode select pin (active high)
TXD	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
V_{CC}	3	Supply	Transceiver 5V supply voltage
V_{IO} / SPLIT	5	Supply / O	V_{IO} (HVDA551): Transceiver logic level (IO) supply voltage SPLIT (HVDA553): Common mode stabilization output

Table 2. ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	HVDA551QDRQ1	H551Q
			HVDA553QDRQ1	H553Q

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL DESCRIPTION

General Description

The device meets or exceeds the specifications of the ISO 11898 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver). This device provides CAN transceiver functions: differential transmit capability to the bus and differential receive capability at data rates up to 1 megabit per second (Mbps). The device includes many protection features providing device and CAN network robustness.

Operating Modes

These devices have two main operating modes: normal mode and standby mode. Operating mode selection is made via the STB input pin.

Table 3. Operating Modes

DEVICE	STB	MODE	DRIVER	RECEIVER	RXD Pin
All Devices	LOW	Normal Mode	Enabled (On)	Enabled (On)	Mirrors bus state(1)
	HIGH	Standby mode (RXD wake-up request)	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled	Mirrors bus state via wake-up filter(2)

(1) Mirrors bus state: LOW if CAN bus is dominant, HIGH if CAN bus is recessive.
(2) See Figure 5 and Figure 6 for operation of the low-power wake-up receiver and bus monitor for RXD wake-up request behavior and Table 5 for the wake -up receiver threshold levels.

Bus States by Mode

The CAN bus has three valid states during powered operation, depending on the mode of the device. In normal mode the bus may be dominant (logic LOW), where the bus lines are driven differentially apart, or recessive (logic HIGH), where the bus lines are biased to V_{CC} / 2 via the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low-power standby mode where the bus lines are biased to GND via the high-ohmic internal input resistors R_{IN} of the receiver.

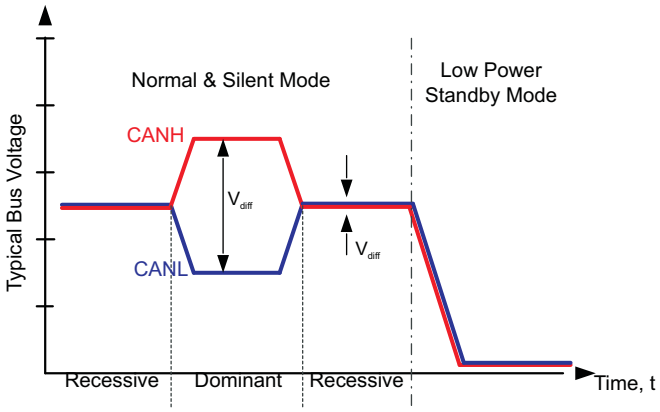


Figure 3. Bus States (Physical Bit Representation)

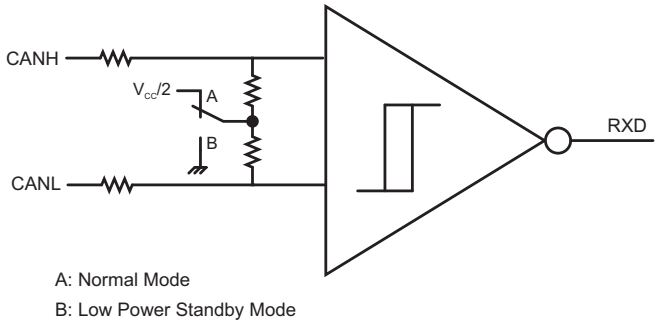


Figure 4. Simplified Common-Mode Bias and Receiver Implementation

Normal Mode

This is the normal operating mode of the device. Normal mode is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state, the CAN bus pins (CANH and CANL) are biased to 0.5 × V_{CC}. In dominant state, the bus pins are driven differentially apart. Logic high is equivalent to recessive on the bus, and logic low is equivalent to a dominant (differential) signal on the bus.

Standby Mode With RXD Wake-Up Request

This is the low-power mode of the device. Standby mode is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor, both supplied via the V_{IO} supply, are enabled to allow for RXD wake-up requests via the CAN bus. The V_{CC} (5-V) supply may be turned off for additional power savings at the system level. A wake-up request is output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake-up request. The 5-V (V_{CC}) supply must be reactivated by the local protocol controller to resume normal mode if it has been turned off for low-power standby operation. The CAN bus pins are weakly pulled to GND, see Figure 3 and Figure 4.

RXD Wake-Up Request Lockout for Bus-Stuck Dominant Fault (HVDA551)

If the bus has a fault condition where it is stuck dominant while the HVDA551 is placed into standby mode via the STB pin, the device locks out the RXD wake-up request until the fault has been removed to prevent false wake-up signals in the system.

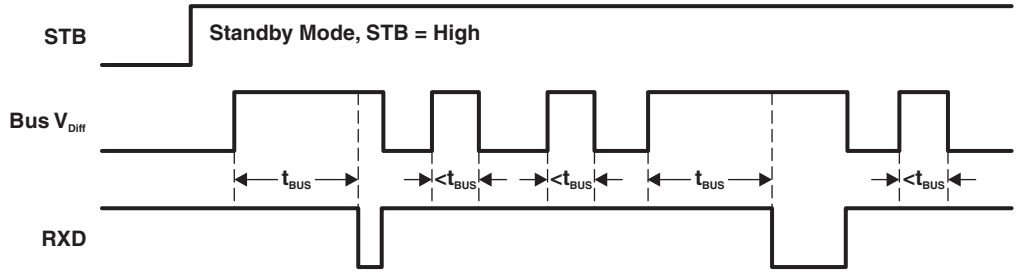


Figure 5. HVDA551 RXD Wake-Up Request With No Bus Fault Condition

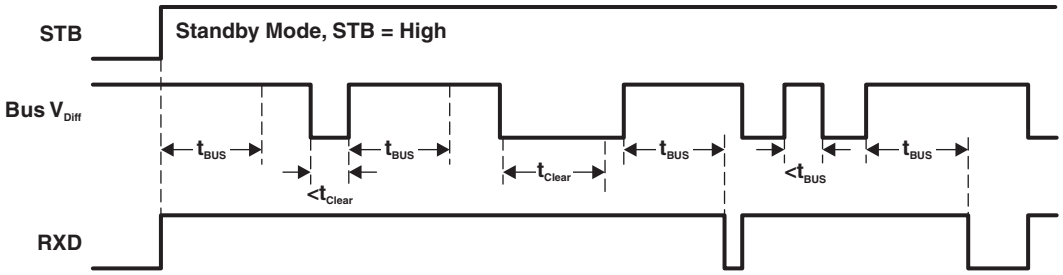


Figure 6. HVDA551 RXD Wake-Up Request Lockout During Bus Dominant Fault Condition

Driver and Receiver Function Tables

Table 4. Driver Function Table

	INPUTS		OUTPUTS		DRIVEN BUS STATE
DEVICE	STB / S(1)	TXD(1)	CANH(1)	CANL(1)	
Both Devices	L	L	H	L	Dominant
	L	H	Z	Z	Recessive
	L	Open	Z	Z	Recessive
HVDA551, HVDA553(2)	H	X	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = common-mode bias to GND, Z = common mode bias to V_{CC} / 2. See Figure 3 and Figure 4 for common mode bias information.
(2) HVDA551 and HVDA553 have internal pullup to V_{IO} on the STB pin. If the STB pin is open, the pin is pulled high and the device is in standby mode.

Table 5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	BUS STATE	RXD PIN(1)
Standby with RXD wake-up request (HVDA551, HVDA553)(2)	$V_{ID} \geq 1.15$ V	DOMINANT	L
	0.4 V < V_{ID} < 1.15 V	?	?
	$V_{ID} \leq 0.4$ V	RECESSIVE	H
NORMAL	$V_{ID} \geq 0.9$ V	DOMINANT	L
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	RECESSIVE	H
ANY	Open	N/A	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate.
(2) While STB is high (standby mode) the RXD output of the HVDA551 functions according to the levels above and the wake-up conditions shown in Figure 5 and Figure 6.

Digital Inputs and Outputs

The HVDA551 device has an I/O supply voltage input pin (V_{IO}) to ratiometrically level shift the digital logic input and output levels with respect to V_{IO} for compatibility with protocol controllers having I/O supply voltages between 3 V and 5.33 V.

The HVDA553 devices have a single V_{CC} supply (5 V). The digital logic input and output levels for these devices are with respect to V_{CC} for compatibility with protocol controllers having I/O supply voltages between 4.68 V and 5.33 V.

Using the HVDA553 With Split Termination

The SPLIT pin voltage output provides 0.5 × V_{CC} in normal mode. The circuit may be used by the application to stabilize the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 7 and Figure 20). This pin provides a stabilizing recessive voltage drive to offset leakage currents of unpowered transceivers or other bias imbalances that might bring the network common-mode voltage away from 0.5 × V_{CC}. Using this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

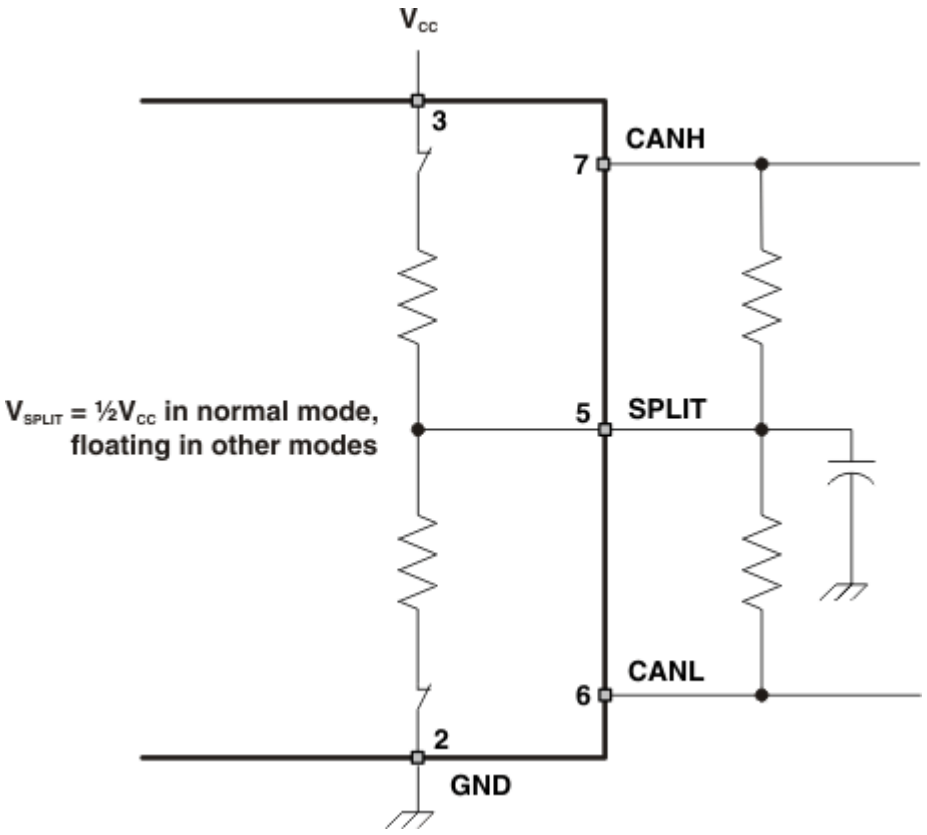


Figure 7. SPLIT Pin Circuitry and Application

Protection Features

TXD Dominant State Time Out

During normal mode, the only mode where the CAN driver is active, the TXD dominant time-out circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period $t_{(DOM)}$. The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires ($t_{(DOM)}$) the CAN bus driver is disabled, freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the dominant-state time-out. The CAN bus pins are biased to the recessive level during a TXD dominant-state time-out.

APPLICATION NOTE: The maximum dominant TXD time allowed by the TXD dominant-state time-out limits the minimum possible data rate of the devices. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(DOM)}$.

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits. This condition is cleared once the temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are biased to the recessive level during a thermal shutdown.

Undervoltage Lockout or Unpowered Device

Both of the supply pins have undervoltage detection, which places the device in forced standby mode to protect the bus during an undervoltage event on either the V_{CC} or V_{IO} supply pins. If V_{IO} is undervoltage, the RXD pin is forced to the high-impedance state and the device does not pass any wake-up signals from the bus to the RXD pin. Because the device is placed into forced standby mode, the CAN bus pins have a common-mode bias to ground, protecting the CAN network; see Figure 3 and Figure 4.

The device is designed to be an *ideal passive* load to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they do not load down the bus but rather be a no-load. This is critical, especially if some nodes of the network are unpowered while the rest of the network remains in operation.

APPLICATION NOTE: Once an undervoltage condition is cleared and V_{CC} and V_{IO} have returned to valid levels, the device typically requires 300 µs to transition to normal operation.

Table 6. Undervoltage Protection

DEVICE	V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD
Both devices	Bad	Good	Forced Standby Mode	Common mode bias to GND(1)	Mirrors bus state via wake-up filter(2)
	Good	Bad	Forced Standby Mode(3)	Common mode bias to GND(1)	High Z
	Unpowered		Unpowered	No load	High Z

(1) See Figure 3 and Figure 4 for common-mode bias information.
(2) See Figure 5 and Figure 6 for operation of the low-power wake-up receiver and bus monitor for RXD wake-up request behavior and Table 5 for the wake-up receiver threshold levels.
(3) When V_{IO} is undervoltage, the device is forced into standby mode with respect to the CAN bus, because there is not a valid digital reference to determine the digital I/O states or power the wake-up receiver.

Floating Pins

The device has integrated pullups and pulldowns on critical pins to place the device into known states if the pins float. The TXD and STB pins on the HVDA551 are pulled up to V_{IO}. This forces a recessive input level on TXD in the case of a floating TXD pin and prevents the device from entering into the low-power standby mode if the STB pin floats. In the case of the HVDA553 both the TXD and STB pins are pulled up to V_{CC}, which has the same effect.

CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver-current limiting (dominant and recessive) and TXD dominant-state time-out to prevent continuously driving dominant. During CAN communication, the bus switches between dominant and recessive states; thus, the short-circuit current may be viewed either as the current during each bus state or as a dc average current. For system current and power considerations in termination resistance and common-mode choke ratings, the average short-circuit current should be used. The device has TXD dominant-state time-out, which prevents permanently having the higher short-circuit current of dominant state. The CAN protocol also has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

APPLICATION NOTE: The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}]$$

where $I_{OS(AVG)}$ is the average short-circuit current, %Transmit is the percentage the node is transmitting CAN messages, %Receive is the percentage the node is receiving CAN messages, %REC_Bits is the percentage of recessive bits in the transmitted CAN messages, %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages, $I_{OS(SS)\_REC}$ is the recessive steady-state short-circuit current and $I_{OS(SS)\_DOM}$ is the dominant steady-state short-circuit current.

ABSOLUTE MAXIMUM RATINGS(1) (2)

1.1	V_{CC}	Supply voltage range	–0.3 V to 6 V	
1.2	V_{IO}	I/O supply voltage range	–0.3 V to 6 V	
1.3		Voltage range at bus terminals (CANH, CANL)	–27 V to 40 V	
1.4	I_O	Receiver output current (RXD)	20 mA	
1.5	V_I	Voltage input range (TXD, STB, S)	HVDA55x	–0.3 V to 6 V and $V_I \le V_{IO}$ + 0.3 V
			HVDA553	–0.3 V to 6 V
1.6	T_J	Operating virtual-junction temperature range	–40°C to 150°C	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the ground terminal.

ELECTROSTATIC DISCHARGE AND TRANSIENT PROTECTION(1)

	PARAMETER	TEST CONDITIONS		VALUE
2.1	Electrostatic discharge	Human-body model(2)	CANH and CANL(3)	±12 kV
2.2			All pins	±4 kV
2.3		Charged-device model(4)	All pins	±1 kV
2.4		IEC 61000-4-2 according to IBEE CAN EMC Test Specification(5)	CANH and CANL pins to GND	±7 kV
2.5	ISO 7637 transients	ISO7637 transients according to IBEE CAN EMC Test Specification(6)	Pulse 1	–100 V
2.6			Pulse 2a	75 V
2.7			Pulse 3a	–150 V
2.8			Pulse 3b	100 V

(1) Stresses beyond those listed under *Electrostatic Discharge and Transient Protection* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) HBM tested in accordance with AEC-Q100-002.
(3) HBM test method based on AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(4) CDM tested in accordance with AEC-Q100-011.
(5) IEC 61000-4-2 is a system-level ESD test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system-level configurations lead to different results.
(6) ISO 7637 is a system level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations lead to different results.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
3.1	V_{CC}	Supply voltage		4.68	5.33	V
3.2	V_{IO}	I/O supply voltage		3	5.33	V
3.3	V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
3.4	V_{IH}	High-level input voltage	TXD, STB (for HVD553: $V_{IO} = V_{CC}$)	0.7 × V_{IO}	V_{IO}	V
3.5	V_{IL}	Low-level input voltage	TXD, STB (for HVD553: $V_{IO} = V_{CC}$)	0	0.3 × V_{IO}	V
3.6	V_{ID}	Differential input voltage, bus	Between CANH and CANL	–6	6	V
3.7	I_{OH}	High-level output current	RXD	–2		mA
3.8	I_{OL}	Low-level output current	RXD		2	mA
3.9	T_A	Operating ambient free-air temperature	See *Thermal Characteristics* table	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA553 V_{IO} = V_{CC}

PARAMETER				TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Supply Characteristics (HVDA551)								
4.1	I_{CC}	5-V supply current	Standby mode (HVDA551 only)	STB at V_{IO}, V_{CC} = 5.33 V, V_{IO} = 3 V, TXD at V_{IO} (2)			5	µA
4.2			Normal mode (dominant)	TXD at 0 V, 60-Ω load, STB at 0 V		50	70	mA
4.3			Normal mode (recessive)	TXD at V_{IO}, no load, STB at 0 V		6.75	10	
4.4								
4.5	I_{IO}	I/O supply current	Standby mode (HVDA551 Only)	STB at V_{IO} , V_{CC} = 5.33 V or 0 V, RXD floating, TXD at V_{IO} T_A = -40°C, 25°C, 125°C (3)		6.5	15	µA
4.6			Normal mode (dominant)	V_{CC} = 5.33V, RXD floating, TXD at 0 V		85	300	
			Normal mode (recessive)	V_{CC} = 5.33V, RXD floating, TXD at V_{IO}		70	300	
4.7	UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.2	3.6	4	V
4.8	$V_{HYS(UVVCC)}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode				200		mV
4.9	UV_{VIO}	Undervoltage detection on V_{IO} for forced standby mode			1.9	2.45	2.95	V
4.10	$V_{HYS(UVVIO)}$	Hysteresis voltage for undervoltage detection on UV_{VIO} for forced standby mode				130		mV
Supply Characteristics (HVDA553)								
4.1-5	I_{CC}	5-V supply current	Standby mode (HVDA553 only)	STB at V_{CC}, V_{CC} = 5.33 V, TXD at V_{CC} (2)			12	µA
4.2-5			Normal mode (dominant)	TXD at 0 V, 60-Ω load, STB at 0 V		50	70	mA
4.3-5			Normal mode (recessive)	TXD at V_{CC}, No load, STB at 0 V		6.75	10	
4.4-5								
4.7-5	UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.2	3.6	4	V
4.8-5	$V_{HYS(UVVCC)}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode				200		mV

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 3.3 V.
(2) The V_{CC} supply is not needed during standby mode so in the application I_{CC} in standby mode may be zero. If the V_{CC} supply remains, then I_{CC} is per specification with V_{CC}.
(3) See HVDA55x Errata, Literature number SLLZ073.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA553 V_{IO} = V_{CC}

	PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Device Switching Characteristics: Propagation Time (Loop Time TXD to RXD)								
5.1	$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant		Figure 15, STB at 0 V	70		230	ns
5.2	$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive		Figure 15, STB at 0 V	70		230	ns
Driver Electrical Characteristics								
6.1	$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 8 and Figure 3	2.9		4.5	V
6.2	$V_{O(D)}$	Bus output voltage (dominant)	CANL	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 8 and Figure 3	0.8		1.75	V
6.3	$V_{O(R)}$	Bus output voltage (recessive)		V_I = V_{IO}, V_{IO} = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 8 and Figure 3	2	2.5	3	V
6.4	$V_{O(STBY)}$	Bus output voltage, standby mode (HVDA551 only)		STB at V_{IO}, R_L = 60 Ω, See Figure 8 and Figure 3	–0.1		0.1	V
6.5	$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 8, Figure 3, and Figure 9	1.5		3	V
6.6	$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 8, Figure 3, and Figure 9	1.4		3	V
6.7	$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 8 and Figure 3	–0.012		0.012	V
6.8	$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, No load	–0.5		0.05	V
6.9	V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 18	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
6.10	$V_{OC(SS)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 14	2	2.5	3	V
6.11	$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 14		50		mV
6.12	$I_{OS(SS)\_DOM}$	Short-circuit steady-state output current, dominant		V_{CANH} = 0 V, CANL open, TXD = low, See Figure 17	–100			mA
6.13	$I_{OS(SS)\_DOM}$	Short-circuit steady-state output current, dominant		V_{CANL} = 32 V, CANH open, TXD = low, See Figure 17			100	mA
6.14	$I_{OS(SS)\_REC}$	Short-circuit steady-state output current, recessive		–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 17	–10		10	mA
6.15	$I_{OS(SS)\_REC}$	Short-circuit steady-state output current, recessive		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 17	–10		10	mA
6.16	C_O	Output capacitance		See receiver input capacitance				

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA553 V_{IO} = V_{CC}

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Driver Switching Characteristics							
7.1	t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, See Figure 10		65		ns
7.2	t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, See Figure 10		50		ns
7.3	t_R	Differential output signal rise time	STB at 0 V, See Figure 10		25		ns
7.4	t_F	Differential output signal fall time	STB at 0 V, See Figure 10		55		ns
7.5	t_{EN}	Enable time from standby or silent mode to normal mode, dominant	See Figure 13			30	µs
7.6	$t_{(DOM)}$ (4)	Dominant time-out	See Figure 16	1200	2000	2800	µs
Receiver Electrical Characteristics							
8.1	V_{IT+}	Positive-going input threshold voltage, normal mode	STB at 0 V, See Table 7		800	900	mV
8.2	$V_{IT–}$	Negative-going input threshold voltage, normal mode	STB at 0 V, See Table 7	500	650		mV
8.3	V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)			125		mV
8.4	$V_{IT(STBY)}$	Input threshold voltage, standby mode (HVDA551 only)	STB at V_{IO}	400		1150	mV
8.5	$I_{I(OFF\_LKG)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} at 0 V, V_{IO} at 0 V, TXD at 0 V			3	µA
8.6	C_I	Input capacitance to ground (CANH or CANL)	HVDA551: TXD at V_{IO}, V_{IO} at 3.3 V. HVDA553: TXD at V_{CC} V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
8.7	C_{ID}	Differential input capacitance	HVDA551: TXD at V_{IO}, V_{IO} at 3.3 V. HVDA553: TXD at V_{CC} V_I = 0.4 sin(4E6πt)		5		pF
8.8	R_{ID}	Differential input resistance	HVDA551: TXD at V_{IO}, V_{IO} = 3.3 V, STB at 0 V HVDA553: TXD at V_{CC}, STB at 0 V	29		80	kΩ
8.9	R_{IN}	Input resistance (CANH or CANL)		14.5	25	40	kΩ
8.10	$R_{I(M)}$	Input resistance matching [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$	–3%	0%	3%	
Receiver Switching Characteristics							
9.1	t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , See Figure 12		95		ns
9.2	t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V , See Figure 12		60		ns
9.3	t_R	Output signal rise time	STB at 0 V , See Figure 12		13		ns
9.4	t_F	Output signal fall time	STB at 0 V , See Figure 12		10		ns
9.5	t_{BUS}	Dominant time required on bus for wake-up from standby (HVDA551 only)	STB at V_{IO}, See Figure 5 and Figure 6	1.5		5	µs
9.6	t_{CLEAR}	Recessive time on the bus to clear the standby mode receiver output (RXD) if standby mode is entered while bus is dominant (HVDA551 only)		1.5		5	µs

(4) The TXD dominant time out ($t_{(DOM)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(DOM)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(DOM)}$ = 11 bits / 300 µs = 37 kbps

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA553 $V_{IO} = V_{CC}$

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TXD Pin Characteristics							
10.1	V_{IH}	High-level input voltage	HVD553: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
10.2	V_{IL}	Low-level input voltage	HVD553: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
10.3	I_{IH}	High-level input current	HVDA551: TXD at V_{IO} HVDA553: TXD at V_{CC}	-2		2	µA
10.4	I_{IL}	Low-level input current	TXD at 0 V	–100		-7	µA
RXD Pin Characteristics							
11.1	V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 12 HVD553: $V_{IO} = V_{CC}$	0.8 × V_{IO}			V
11.2	V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 12 HVD553: $V_{IO} = V_{CC}$			0.2 × V_{IO}	V
STB Pin Characteristics							
12.1	V_{IH}	High-level input voltage	HVD553: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
12.2	V_{IL}	Low-level input voltage	HVD553: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
12.3	I_{IH}	High-level input current	HVDA551: STB at V_{IO} HVDA553: STB at V_{CC}	–2		2	µA
12.4	I_{IL}	Low-level input current	STB at 0 V	–20			µA
SPLIT Pin (HVDA553 Only)							
14.1	V_O	Output Voltage	–500 µA < I_O < 500 µA	0.3 V_{CC}	0.5 V_{CC}	0.7 VCC	V
14.2	$I_{O(STB)}$	Leakage current, standby mode	STB at V_{CC}, –12 V ≤ I_O ≤ 12 V	–5		5	µA

THERMAL CHARACTERISTICS

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), HVDA553 V_{IO} = V_{CC}

THERMAL METRIC(1)(2)			TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL METRIC - SOIC D PACKAGE							
14.1-D	θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance (3)		140		°C/W
14.2-D			High-K thermal resistance (4)		112		
14.3-D	θ_{JB}	Junction-to-board thermal resistance(5)			50		
14.4-D	$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(6)			56		
14.5-D	$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(7)			N/A		
14.6-D	Ψ_{JT}	Junction-to-top characterization parameter(8)			13		
14.7-D	Ψ_{JB}	Junction-to-board characterization parameter(9)			55		
AVERAGE POWER DISSIPATION AND THERMAL SHUTDOWN							
14.8	P_D	Average power dissipation	V_{CC} = 5 V, V_{IO} = V_{CC}, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		140		mW
14.9			V_{CC} = 5.33 V, V_{IO} = V_{CC}, T_J = 130°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			215	
14.10		Thermal shutdown temperature			185		°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times \theta_{JA})$. $\theta_{JA}$is PCB-dependent; both JEDEC-standard low-K and high-K values are given as reference points to standardized reference boards.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold-plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-case (top) thermal resistance is obtained by simulating a cold-plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold-plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(8) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

PARAMETER MEASUREMENT INFORMATION

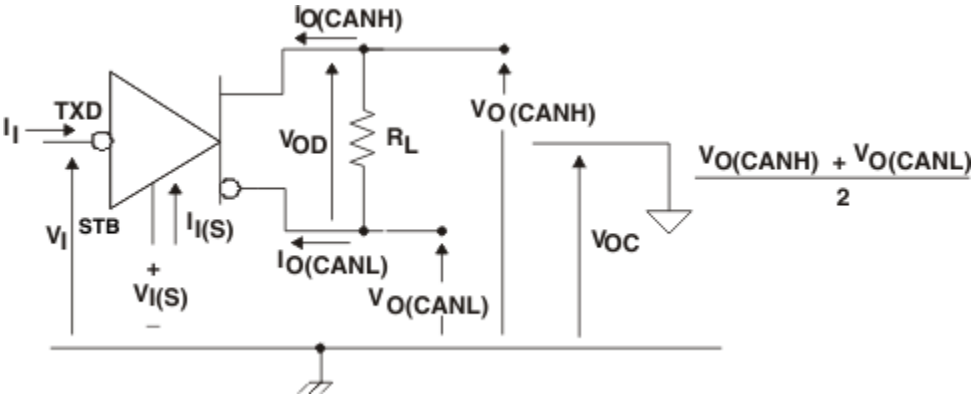


Figure 8. Driver Voltage, Current, and Test Definition

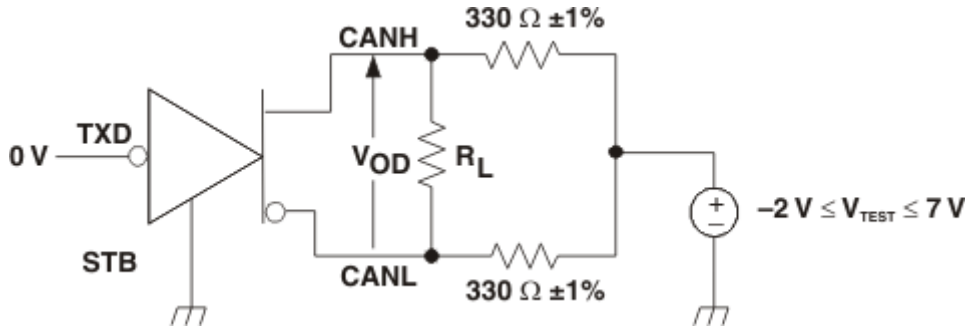
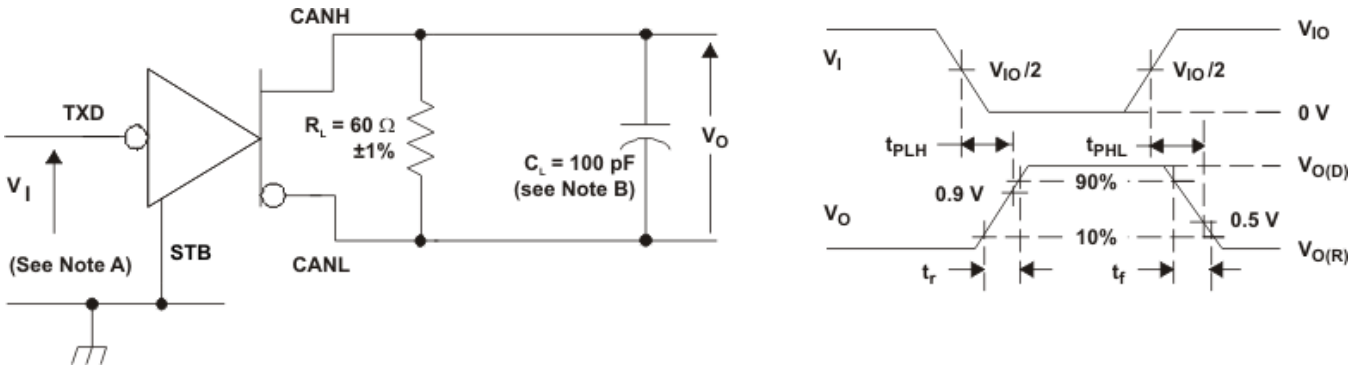


Figure 9. Driver V_{OD} Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 10. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

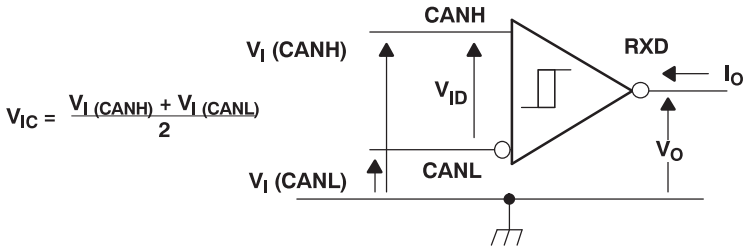
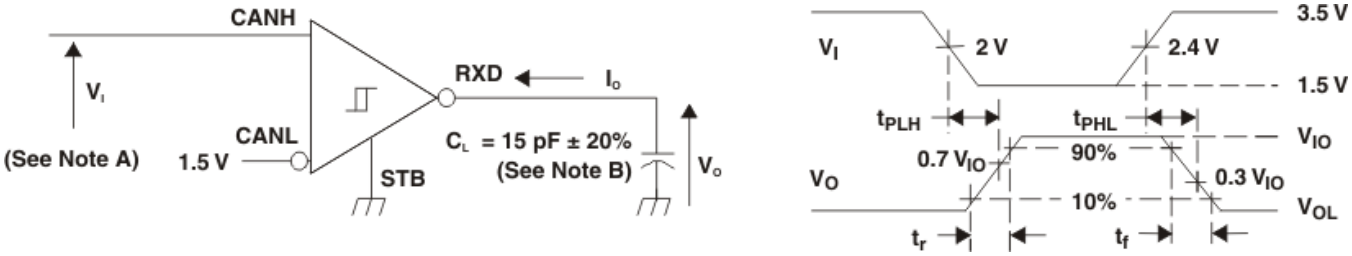


Figure 11. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

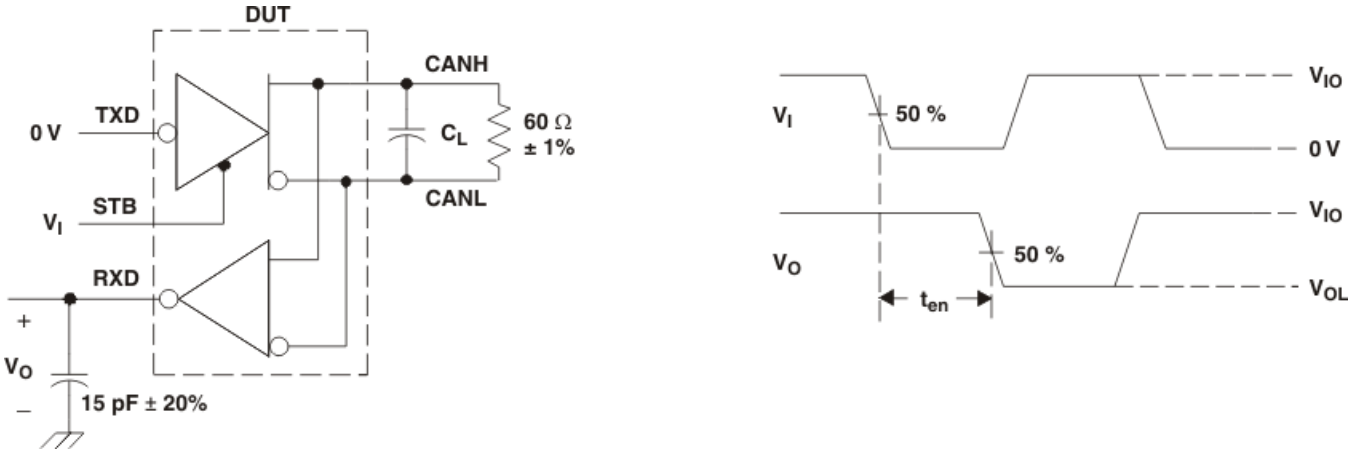
B. C_L includes instrumentation and fixture capacitance within ±20%.

C. C. For HVDA553 device versions $V_{IO} = V_{CC}$.

Figure 12. Receiver Test Circuit and Voltage Waveforms

Table 7. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

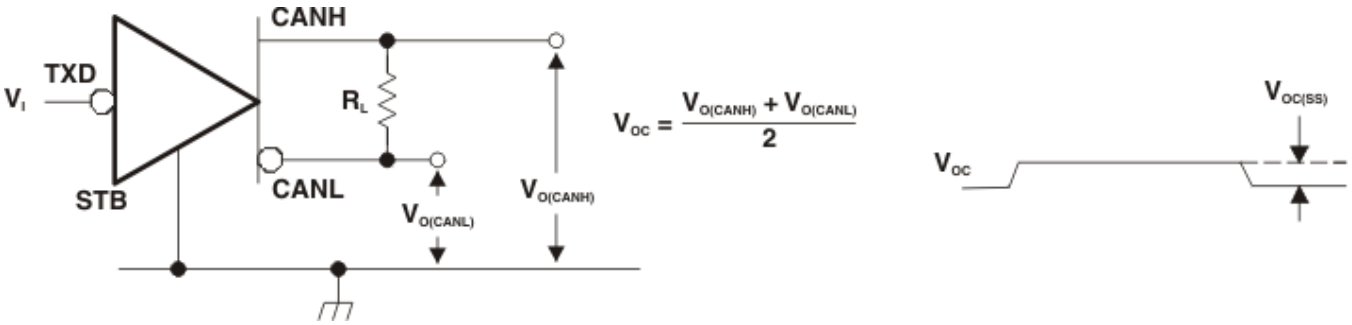


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 25 kHz, 50% duty cycle.

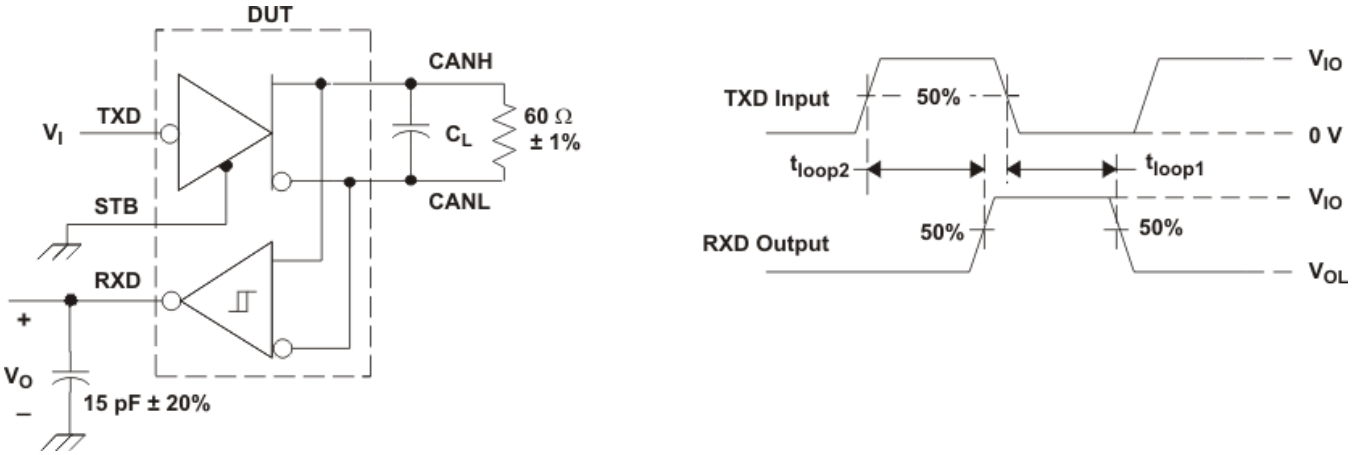
C. C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 13. t_{EN} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 14. Common-Mode Output Voltage Test and Waveforms

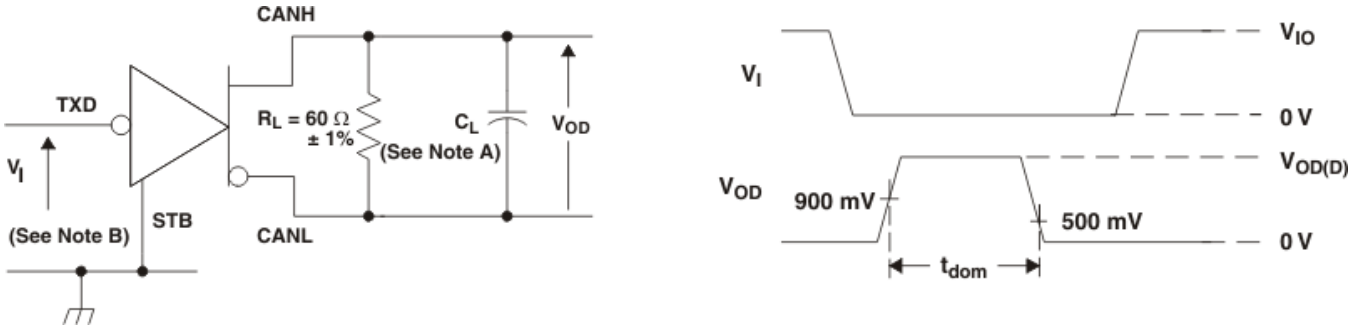


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 15. $t_{PROP(LOOP)}$ Test Circuit and Waveform

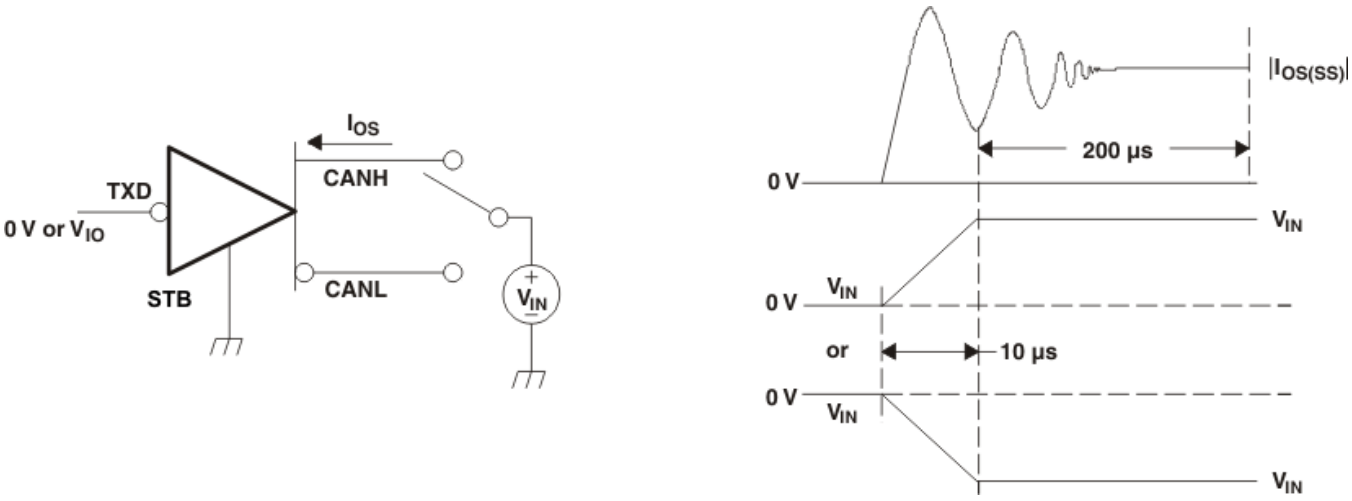


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

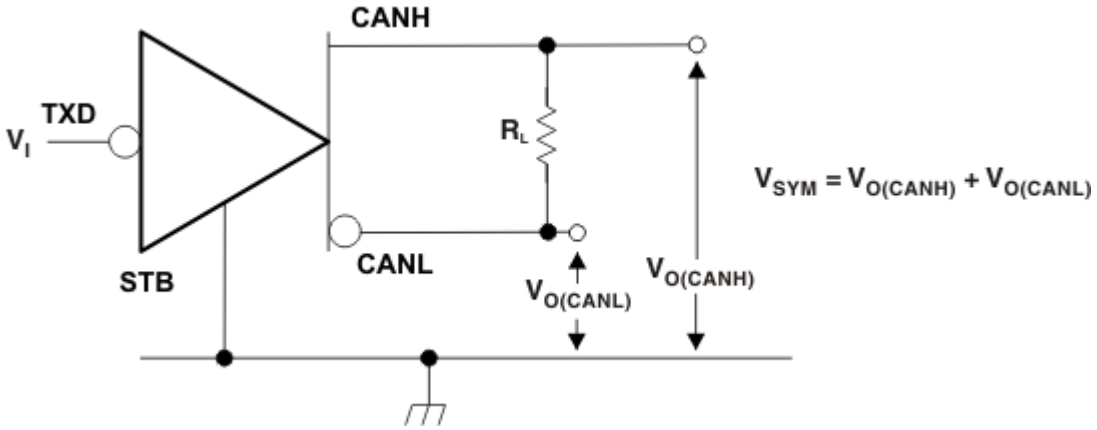
C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 16. TXD Dominant Time-Out Test Circuit and Waveforms



A. For HVDA553 device versions $V_{IO} = V_{CC}$.

Figure 17. Driver Short-Circuit Current Test and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r and $t_f \leq 6$ ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

Figure 18. Driver Output Symmetry Test Circuit

APPLICATION INFORMATION

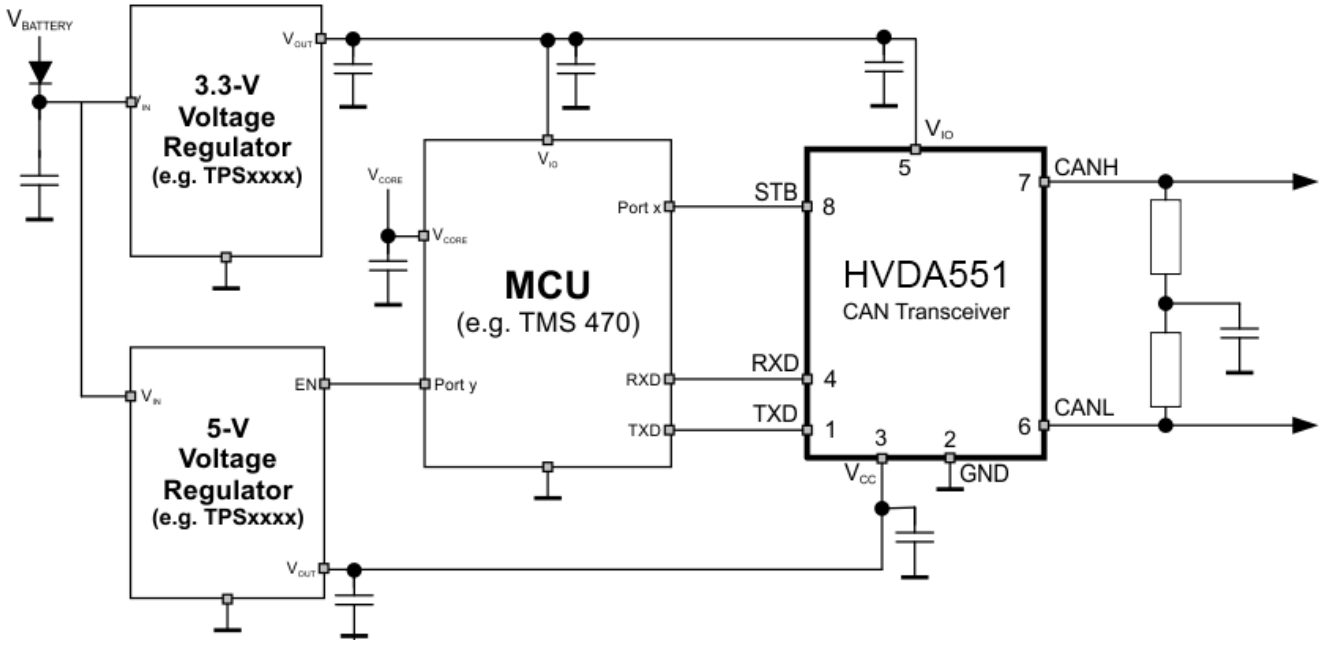


Figure 19. Typical Application Using the HVDA551 With 3.3-V I/O Voltage Level in Low-Power Mode (5-V V_{CC} Not Needed in Low-Power Mode)

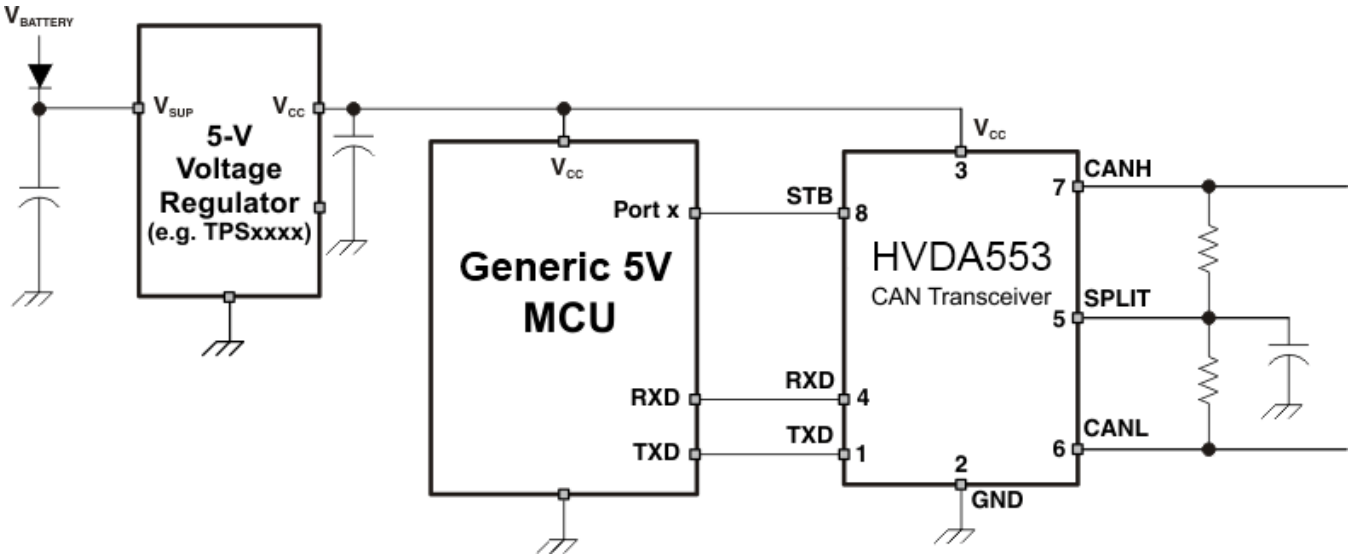


Figure 20. Typical Application Using the HVDA553 With SPLIT Termination

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HVDA551QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H551Q
HVDA551QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H551Q
HVDA553QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H553Q
HVDA553QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H553Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

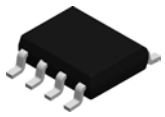
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

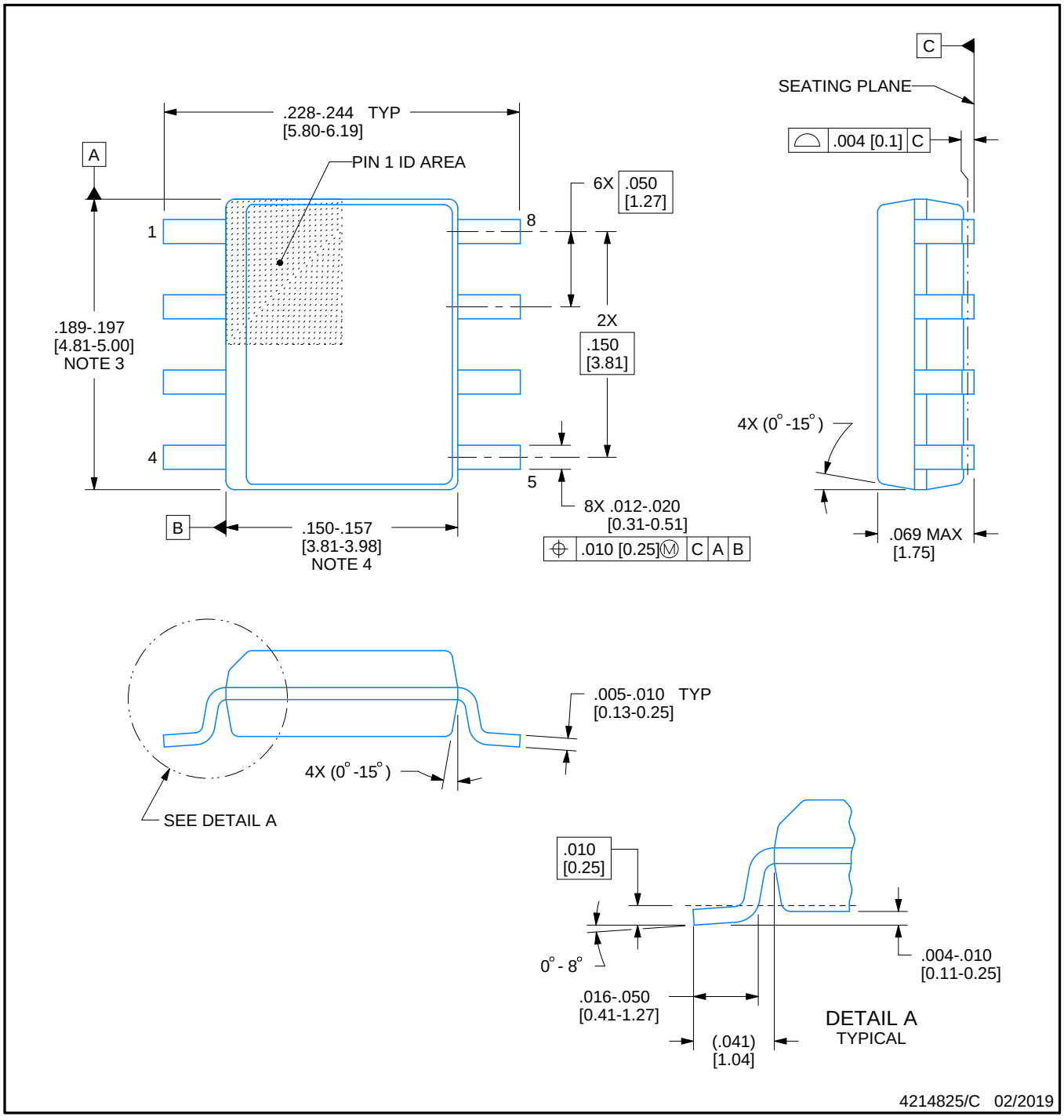


PACKAGE OUTLINE

D0008A

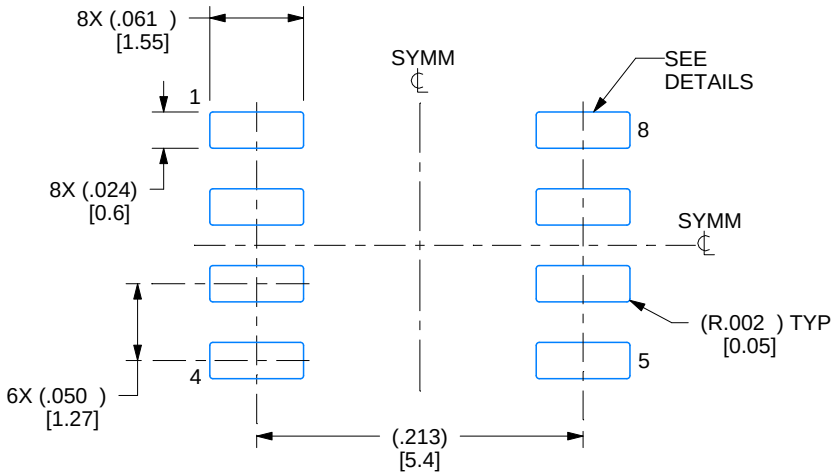
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

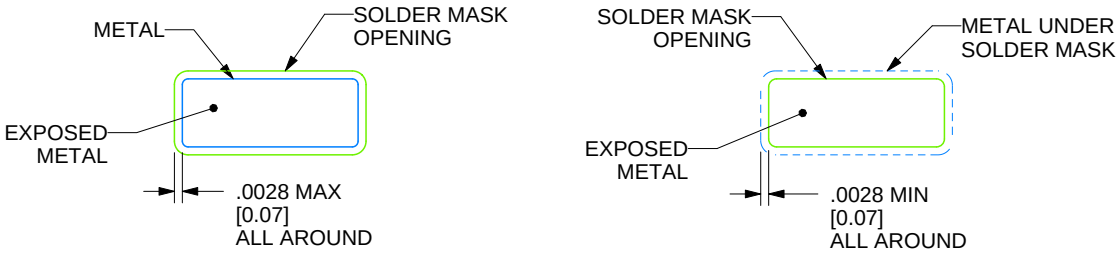


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

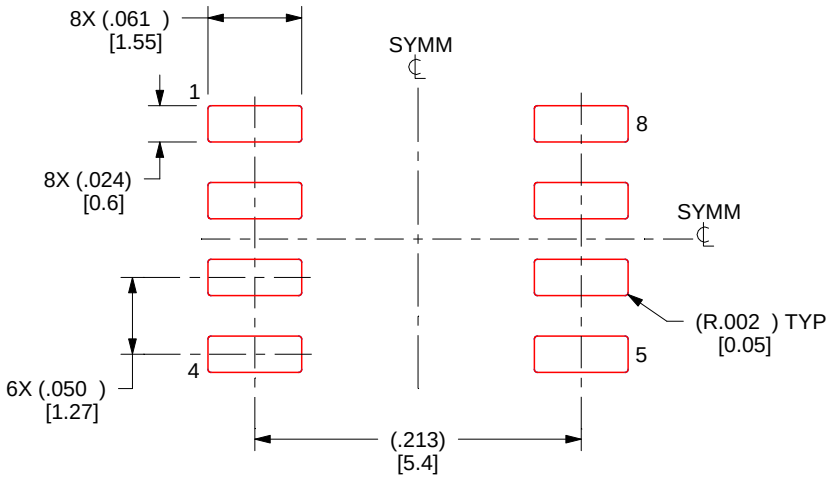
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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