HD3SS2522 具有 DFP 控制器的 USB Type-C SS MUX

1 特性

- 符合 USB Type-C 规范 1.0
- 模式配置
  - 仅主机 - 下行端口 (DFP)
- 通道配置 (CC)
  - USB 端口连接检测
  - 电缆方向检测
  - Type-C 电流模式（默认、中等和高）
- 电源电压：3.3V ± 10%
- 用于 USB 3.1 信号传输的 2:1 复用器 (Mux) 解决方案
- 运行速率高达 10Gbps，-3dB 带宽 (BW) 宽达 8GHz
- 出色动态特性（2.5GHz 时）
  - 串扰 = -39dB
  - 断开隔离 = -22dB
  - 插入损耗 = –1.2dB
  - 输入回波损耗 = –12dB
- 低功耗：激活模式为 2mW；待机模式为 50μW

2 应用

- 台式机和笔记本电脑
- USB Type-C DFP 应用
- 主板

3 说明

HD3SS2522 是一款配有 DFP CC 逻辑的 2:1 USB 复用器。 根据 USB Type-C 规范，HD3SS2522 用作 DFP。 CC 逻辑块通过监视 CC1 和 CC2 引脚的电压来确定何时连接了 USB 端口。 连接 USB 端口后，CC 逻辑还将确定电缆方向并相应地配置 USB SS 复用器。

HD3SS2522 通过 VBUS_EN 信号来控制传统电源开关，从而为 VBUS 提供 5V 电压。 此外，该器件还可提供相应的控制信号，从而为生态系统实现 USB Type-C 提供 5V VCONN 电源。

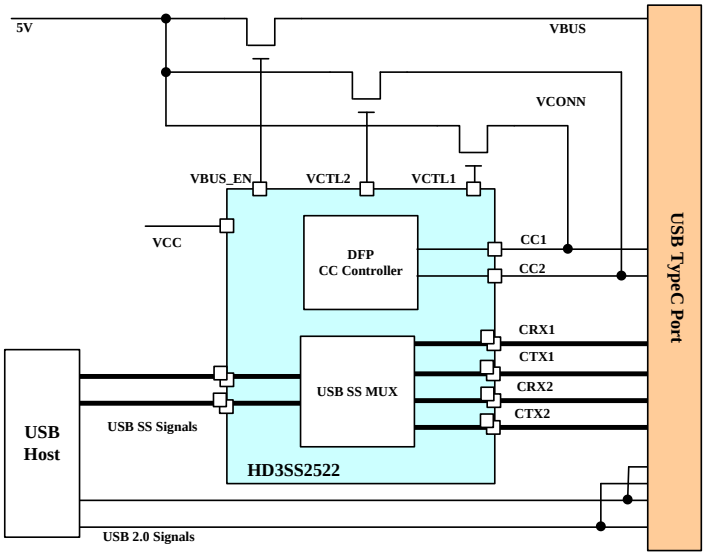
该器件具有出色的动态特性，可在信号眼图衰减最小的情况下实现高速转换，并且附加抖动极少。 此外，该器件在待机模式下具有较低的电流消耗。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
HD3SS2522	WQFN (56)	11.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



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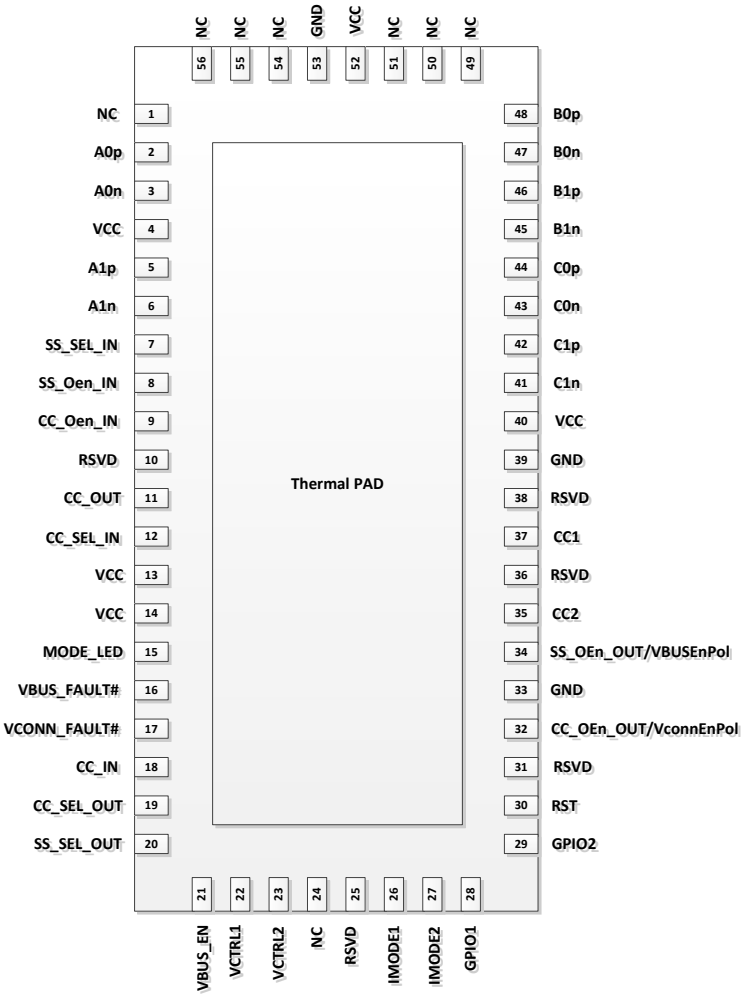
5 修订历史记录

日期	修订版本	注释
2015 年 4 月	*	首次发布。

6 Pin Configuration and Functions

RHU Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0p	2	I/O	Port A0, High Speed Positive Signal
A0n	3	I/O	Port A0, High Speed Negative Signal
A1p	5	I/O	Port A1, High Speed Positive Signal
A1n	6	I/O	Port A1, High Speed Negative Signal
B0p	48	I/O	Port B0, High Speed Positive Signal
B0n	47	I/O	Port B0, High Speed Negative Signal
B1p	46	I/O	Port B1, High Speed Positive Signal
B1n	45	I/O	Port B1, High Speed Negative Signal
C0p	44	I/O	Port C0, High Speed Positive Signal
C0n	43	I/O	Port C0, High Speed Negative Signal
C1p	42	I/O	Port C1, High Speed Positive Signal
C1n	41	I/O	Port C1, High Speed Negative Signal
CC_IN	18	I/O	Selected CC signal back to the device as input - connect to CC_OUT pin

Pin Functions (continued)

PIN		I/O	DESCRIPTION		
NAME	NO.				
CC_OUT	11	I/O	Selected CC signal as output - connect to CC_IN pin		
CC_SEL_IN	12	I	CC Signal select pin input – Connect to CC_SEL_OUT		
CC_SEL_OUT	19	O	CC Signal select pin output – Connect to CC_SEL_IN		
CC_OEn_IN	9	I	Active Low CC MUX Enable input – connect to CC_OEn_OUT		
CC_OEn_OUT / VconnEnPol	32	I/O	Active Low CC MUX Enable output – connect to CC_OEn. The pin is also sampled upon reset to set the polarity of the VCTRL1 and VCTRL2. 0 = VCTRL1/2 polarity is active high. 1 = VCTRL1/2 polarity is active low.		
CC1	37	I/O	USB Type-C configuration channel for position 1		
CC2	35	I/O	USB Type-C configuration channel for position 2		
GND	33 , 39, 53	G	Ground		
GPIO1	28	I/O	GPIO or SCL for FW update		
GPIO2	29	I/O	GPIO or SDA for FW update		
IMODE1 IMODE2	26 27	I	IMODE1	IMODE2	Current Mode
			Low	Low	Default
			Low	High	Mid (1.5 A)
			High	Low	Reserved
			High	High	High (3A)
MODE_LED	15	O	High when UFP attach detected		
NC	1, 24, 49, 50, 51, 54, 55, 56		Not connected		
RST	30	I	CC Controller Reset		
RSVD	10, 25, 31, 36, 38	I/O	Reserved		
SS_OEn_IN	8	I	Active Low SS MUX Enable input – connect to SS_OEn_OUT		
SS_OEn_OUT / VBUSEnPol	34	I/O	Active Low SS MUX Enable output – connect to SS_OEn_IN. The pin is also sampled upon reset to set the polarity of the VBUS_EN. 0 = VBUS_EN polarity is active high. 1 = VBUS_EN polarity is active low.		
SS_SEL_IN	7	I	SS Port select pin input – Connect to SS_SEL_OUT		
SS_SEL_OUT	20	O	SS Port select pin output – Connect to SS_SEL_IN		
VBUS_EN	21	O	Active low: Low when UFP attach detected. Open drain output. This signal drives VBUS power switch.		
VBUS_FAULT#	16	I	VBUS Fault signal in from VBUS Power switch. Active low.		
VCC	4 , 13, 14, 40, 52	P	3.3V Power		
VCONN_FAULT#	17	I	VCONN Fault signal in from VCONN switches. Active low.		
VCTRL1	22	O	Active low open drain control output for VCONN switch for CC1		
VCTRL2	23	O	Active low open drain control output for VCONN switch for CC1		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply voltage range, V_{CC}		–0.4	4	V
Voltage Range	Differential I/O (High bandwidth signal path, AxP/N, BxP/N, CxP/N)	–0.4	2.4	
	Control Pins and Single Ended I/Os including CC1 and CC2	–0.4	V_{CC} + 0.4	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage	Control/Status pins	2		V_{CC}	V
V_{IL}	Input low voltage	Control/Status pins	–0.1		0.8	V
$V_{I/O(Diff)}$	Differential voltage	Switch I/O diff voltage	0		1.6	V_{PP}
$V_{I/O(CM)}$	Common voltage	Switch I/O common mode voltage	0		2	V
$V_{I/O}$	Input / output voltage	CC_OUT, CC_IN, and selected CC pin for configuration	0		V_{CC}	V
V_{IN}	Input voltage	Selected CC pin for VCONN	0		5.5	V
T_A	Operating free-air temperature	HD3SS2522RHU	0		70	°C

7.4 Thermal Information

THERMAL METRIC (1)		HD3SS2521A RHU 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	8.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 3.6 V, SS_OEn, CC_OEn = GND		0.6	1	mA
$I_{(STANDBY)}$	Standby current	V_{CC} = 3.3 V, SS_OEN, CC_OEn = V_{CC}		15		µA
VBUS_FAULT#, VCONN_FAULT#, IMODE1, IMODE2, RST, RSVD, GPIO1, GPIO2						
V_{IT+}	Positive-going input threshold voltage		0.45 x V_{CC}		0.75 x V_{CC}	V
V_{IT-}	Negative-going input threshold voltage		0.25 x V_{CC}		0.55 x V_{CC}	V
V_{hys}	nput voltage hysteresis (V_{IT+} – $V_{IT–}$)	V_{CC} = 3 V	0.3		1	V
R_{PULL}	Pullup/pulldown resistor	Pullup: V_{IN} = GND, Pulldown: V_{IN} = V_CC, V_{CC} = 3 V	20	35	50	kΩ
C_I	Input capacitance	V_{IN} = GND or V_{CC}		5		pF
I_{LGK}	High-impedance leakage current	V_{IN} = GND or V_{CC}, V_{CC} = 3 V, Pullup/Pulldown disabled			±50	nA
VCTRL1, VCTRL2, VBUS_EN						
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 6 mA (1)		GND + 0.3		V
MODE_LED						
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –6 mA (1)		V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 6 mA (1)		GND + 0.3		V
AxP/N, BxP/N, CxP/N						
I_{LGK}	High-impedance leakage current	V_{CC} = 3.6 V, V_{IN} = 0 V, V_{OUT} = 2 V (I_{LKG} on open outputs Port B and C)			130	µA
		V_{CC} = 3.6 V, V_{IN} = 0 V, V_{OUT} = 2 V (I_{LKG} on open outputs Port A)			4	µA
CC1, CC2						
I_{LGK}	High-impedance leakage current	V_{CC} = 3.6 V, V_{IN} = 0 V, V_{OUT} = 0 V to 4 V			1	µA

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
AxP/N, BxP/N, CxP/N HIGH-BANDWIDTH SIGNAL PATH						
t_{PD}	Switch Propagation Delay	R_{SC} and R_L = 50 Ω			85	ps
t_{ON}	SS_SEL_IN -to-Switch t_{ON}	R_{SC} and R_L = 50 Ω		70	250	ns
t_{OFF}	SS_SEL_IN -to-Switch t_{OFF}			70	250	ns

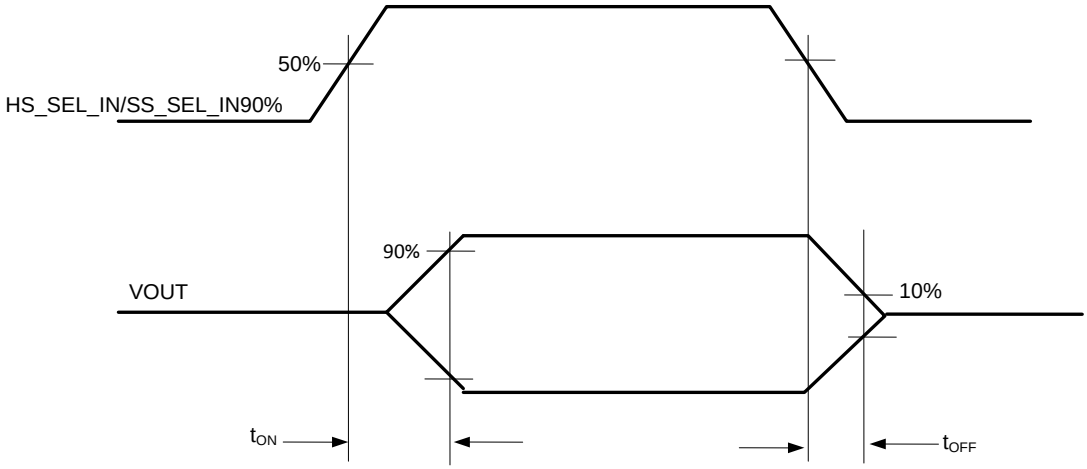
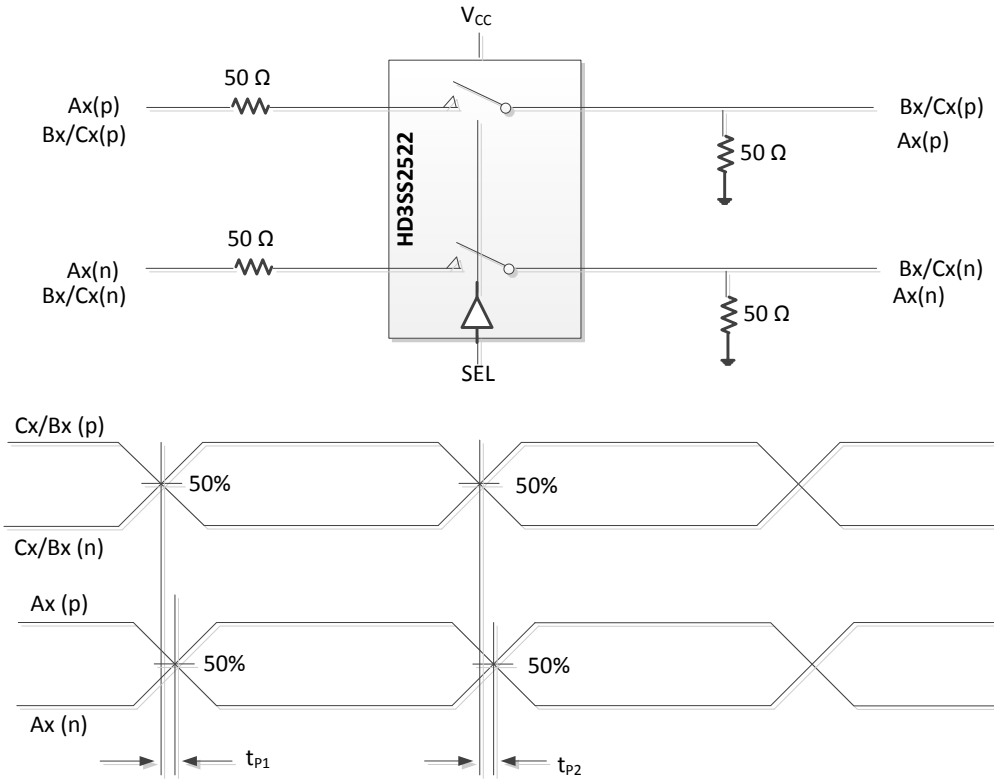


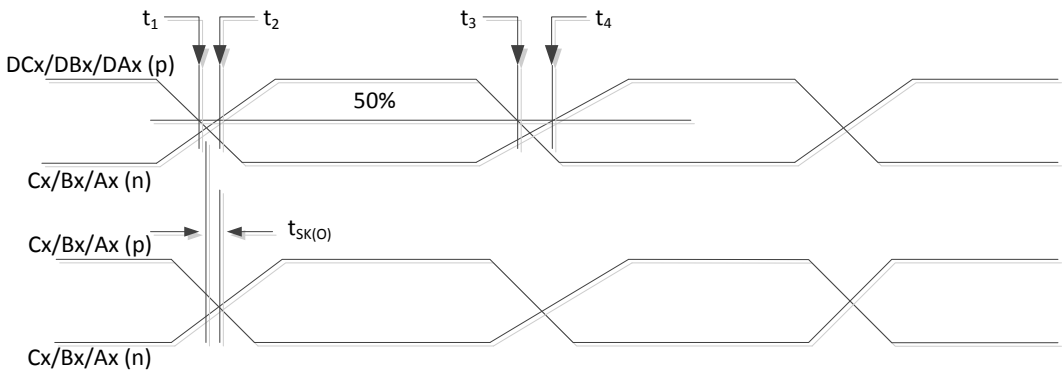
Figure 1. Select to Switch t_{ON} and t_{OFF}



Inter-pair skew

t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs



Intra-pair skew

$t_{SK(b\text{-}b)} = 0.5 \text{ X } |(t_4 - t_3) + (t_1 - t_2)|$

(1) Measurements based on an ideal input with zero intra-pair skew on the input, i.e. the input at A to B/C or the input at B/C to A

(2) Inter-pair skew is measured from lane to lane on the same channel, e.g. C0 to C1

(3) Intra-pair skew is defined as the relative difference from the p and n signals of a single lane

Figure 2. Propagation Delay and Skew

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AxP/N, BxP/N, CxP/N						
$t_{SK(O)}$	Inter-pair output skew (channel-channel)	R_{SC} and R_L = 50 Ω			20	ps
$t_{SK(b-b)}$	Inter-pair output skew (bit-bit)				8	ps
C_{ON}	Outputs ON capacitance	V_{IN} = 0 V, outputs open, switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	V_{IN} = 0 V, outputs open, switch OFF		1		pF
R_{ON}	Output ON resistance	V_{CC} = 3.3 V, V_{CM} = 0.5 V – 1.5 V, I_O = –8 mA		5	8	Ω
ΔR_{ON}	On resistance match between channels	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			2	Ω
	On resistance match between pairs of the same channel				0.7	
$R_{(FLAT\_ON)}$	On resistance flatness [$R_{ON(MAX)}$ – $R_{ON(MIN)}$]	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V			1.15	Ω
R_L	Differential input return loss (V_{CM} = 0 V)	f = 2.5 GHz		–12		dB
		f = 4 GHz		–11		
X_{TALK}	Differential crosstalk (V_{CM} = 0 V)	f = 2.5 GHz		–39		dB
		f = 4 GHz		–35		
O_{IRR}	Differential off-isolation (V_{CM} = 0 V)	f = 2.5 GHz		–22		dB
		f = 4 GHz		–19		
I_L	Differential insertion loss (V_{CM} = 0 V)	f = 2.5 GHz		–1.1		dB
		f = 4 GHz		–1.5		
BW	Bandwidth	At 3 dB		6		GHz

8 Detailed Description

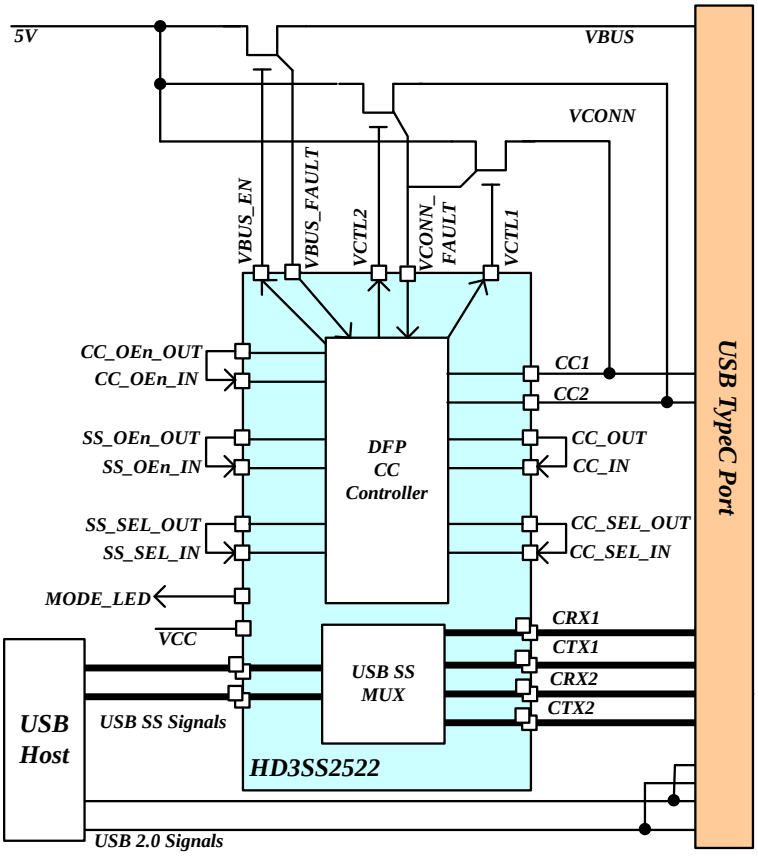
8.1 Overview

HD3SS2522 is a 10-Gbps USB mux with Configuration Channel (CC) logic with DFP support. The HD3SS2522 presents itself as a DFP according to the USB Type-C Spec. The CC logic block monitors the CC1 and CC2 pin voltages to determine when a USB port has been attached. Once a USB port has been attached, the CC logic also determines the orientation of the cable and configures the USB SS mux accordingly.

The device provides an VBUS_EN signal to control legacy power switch to provide 5 V to VBUS. The device also provides IOs needed to support 5 V VCONN sourcing for ecosystems implementing USB Type-C.

Excellent dynamic characteristics of the device allow high speed switching with minimum attenuation to the signal eye diagram and little added jitter. The device also has low current consumption in Standby mode.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adaptive Common Mode Tracking for USB 3.1 MUX

The device provides an integrated USB 3.1 2:1 passive MUX. The MUX provides adaptive common mode tracking allowing RX and TX channels to have different common mode voltage. This feature allows simpler system implementation.

8.3.2 DFP-to-UFP Attach/Detach Detection

The HD3SS2522 monitors the CC lines as a Type-C DFP port. When the device senses that one of the CC has a resistance to GND, it detects that an UFP is attached. The device provides an emulated ID signal (VBUS_EN) in the event of a UFP attach.

The device also monitors specified pull down resistor according to Type-C specifications to determine if an active cable is attached. In the event of active cable detection, HD3SS2522 provides necessary control signals for VCONN switches that provide 5-V VCONN power to appropriate CC pin.

8.3.3 Plug Orientation/Cable Twist Detection

According to USB Type-C specifications plug can be inserted into a receptacle in either one of two orientations. HD3SS2522 monitors for a pull-down resistors from an attached UFP port determining the MUX orientation.

8.3.4 VBUS Fault

HD3SS2522 does not take any action in case of a VBUS fault. VBUS fault needs to be handled by legacy power management implementations.

8.3.5 VCONN Fault

If a VCONN fault is determined by the external power switch and fed into the device through VCONN_FAULT pin, HD3SS2522 will latch it off until the cable is unplugged if there is a fault that does not clear within 5 ms. Which is a sufficient amount of time to charge the 10-µF inrush capacitance.

8.4 Device Functional Modes

8.4.1 Unattached.DFP State

In this state, the HD3SS2522 as a DFP port is waiting to detect the presence of a UFP. The device injects pull-up currents to both of the CC lines.

8.4.2 Attached.DFP State

When HD3SS2522 is in the Attached.DFP state, the port is attached and operating as a DFP. The device continues to monitor the CC pins to make sure the appropriate pin is within vRd range specified by Type-C specification. The device source current on one of the this CC pins and monitor its voltage. The port advertises one of the three levels of VBUS power capability as specified in Type-C spec according to GPIO pins IMODE1 and IMODE2.

The device controls the VCONN power switches to apply VCONN to the unused CC pin if the voltage on the unused CC pin is within the vRa range as specified in Type-C specification.

9 Application and Implementation

NOTE

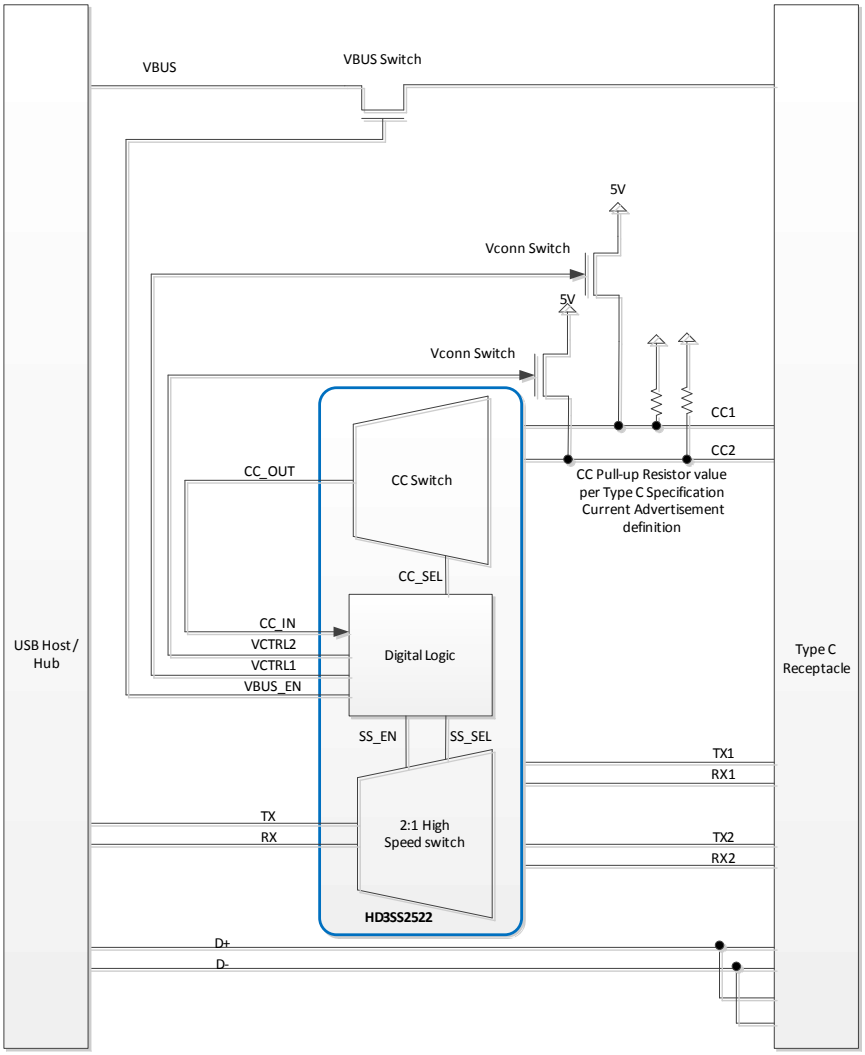
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The HD3SS2522 is a high speed switch with integrated DFP CC controller. The HD3SS2522 can be implemented in any USB Type-C DFP applications in conjunction with VBUS and VCONN switches.

9.2 USB Type-C DFP Typical Application

This section depicts the typical Type-C system with a USB Host or Hub. The Type C receptacle in this system is a DFP only providing VBUS and VCONN upon the connection of UFP device. The HD3SS2522 DFP CC controller determines the UFP attachment and provides VBUS and VCONN based upon the Type-C specification state diagram and timing definition.



This Figure represents high level block diagram of the Type C DFP implementation not a circuit level implementation.

Figure 3. USB Type-C DFP

USB Type-C DFP Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

PARAMETER	VALUE
V_{CC}	3.3 V
AxP/N, BxP/N, CxP/N V_{CM} Voltage	0 V – 2 V
CC_IN, CC_OUT, CC1, CC2	0 V –3.3 V
Control Pin Vmax for Low	0.8 V
Control Pin Vmax for High	2 V

9.2.2 Detailed Design Procedure

9.2.2.1 USB Type-C Current Advertising

HD3SS2522 can be used to advertise USB Type-C current in conjunction with pull up resistors to CC1 and CC2 pins. These pull up resistors must meet the Type C spec requirements. The IMODE1 and IMODE2 setting must match the CC resistor configuration for the current mode: default, mid or high.

9.2.2.2 VCONN and VBUS Power Switch Control

VCTRL1# and VCTRL2# are outputs from the HD3SS2522 CC controller to enable or disable the VCONN switch based upon the orientation detection, audio accessory termination Ra detection, and/or fault condition.

VBUS_EN is an output from the HD3SS2522 CC controller to enable VBUS switch. Upon detection of UFP attachment, the VBUS_EN is asserted to enable VBUS switch.

9.2.2.3 Firmware Upgradability

If necessary, the CC controller firmware (FW) can be updated via GPIO1, GPIO2 and SYS_COM_REQ. Contact Texas Instruments for further assistance with upgrading the FW.

9.2.3 USB Type-C DFP Circuit Schematics with a Type C Receptacle

The schematics below depicts the circuit level implementation of the Type C system with HD3SS2522 and a DFP only Type C connector. The system should select a power switch that complies with the Type C specification and application requirements. The power switch can be controlled by the HD3SS2522. See the *Detailed Design Procedure* section of the datasheet for design details.

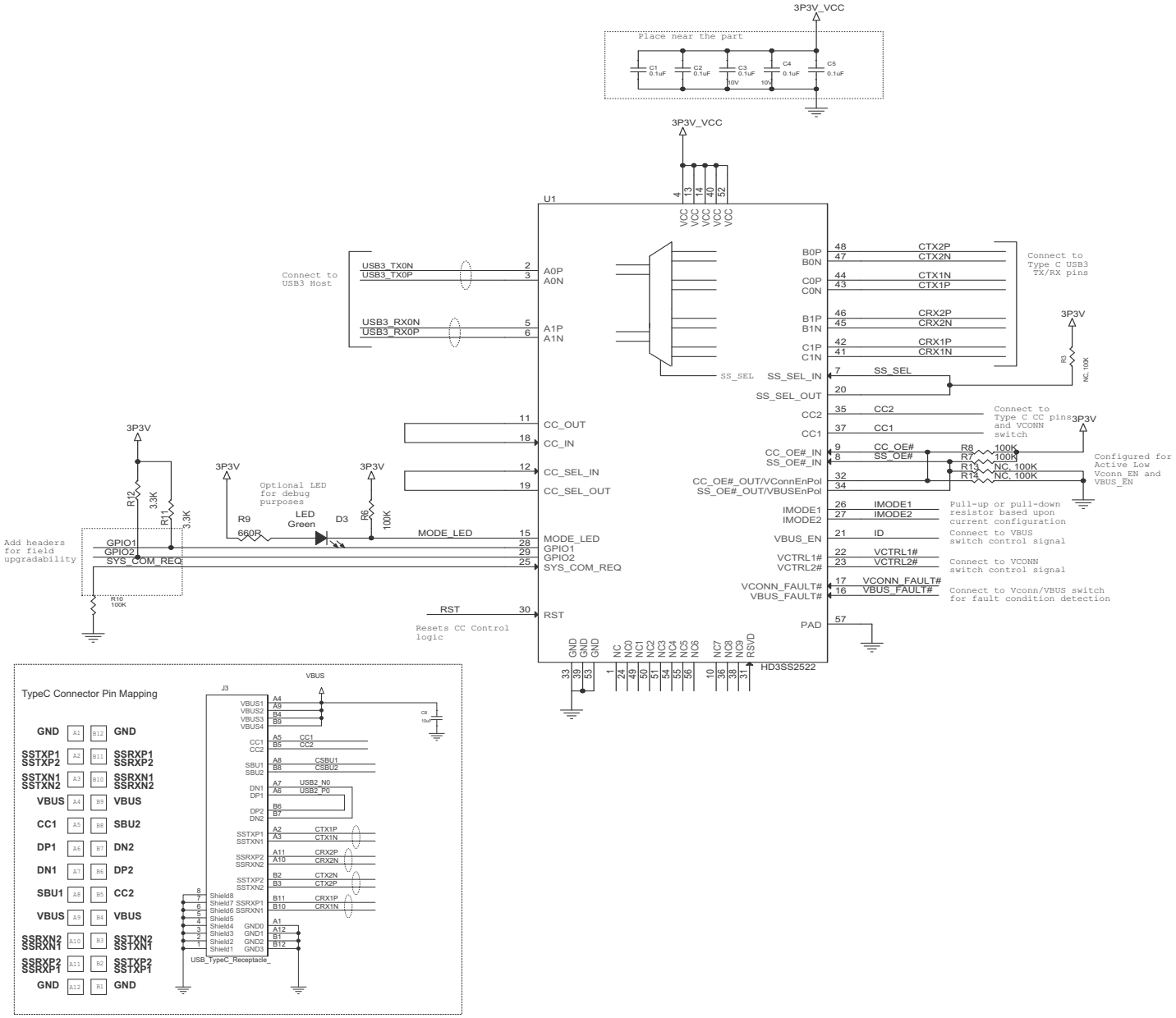


Figure 4. Example Schematics With a Type-C Receptacle

10 Power Supply Recommendations

The HD3SS2522 does not have any special requirement for power supply as long as it is within the recommended range. The device also does not have any special reset requirement.

11 Layout

11.1 Layout Guidelines

11.1.1 Critical Routes

The high speed differential signals must be routed with great care to minimize signal quality degradation between the connector and the source or sink of the high speed signals by following the guidelines provided in this document. Depending on the configuration schemes, the speed of each differential pair can reach a maximum speed of 10 Gbps. These signals are to be routed first before other signals with highest priority.

- Each differential pair should be routed together with controlled differential impedance of 85 to 90-Ω and 50-Ω common mode impedance. Keep away from other high speed signals. The number of vias should be kept to minimum. Each pair should be separated from adjacent pairs by at least 3 times the signal trace width. Route all differential pairs on the same group of layers (Outer layers or inner layers) if not on the same layer. No 90 degree turns on any of the differential pairs. If bends are used on high speed differential pairs, the angle of the bend should be greater than 135 degrees.
- Length matching:
  - Keep high speed differential pairs lengths within 5 mil of each other to keep the intra-pair skew minimum. The inter-pair matching of the differential pairs is not as critical as intra-pair matching. The SSTX and SSRX pairs do not have to match while they need to be routed as short as possible.
- Keep high speed differential pair traces adjacent to ground plane.
- Do not route differential pairs over any plane split.
- ESD components on the high speed differential lanes should be placed nearest to the connector in a pass through manner without stubs on the differential path.
- For ease of routing, the P and N connection of the USB3.1 differential pairs to the HD3SS2522 pins can be swapped.

11.1.2 General Routing/Placement Rules

- Route all high-speed signals first on un-routed PCB. The stub on USB2 D+ and D- pairs should not exceed 3.5 mm.
- Follow 20H rule (H is the distance to ref-plane) for separation of the high speed trace from the edge of the plane
- Minimize parallelism of high speed clocks and other periodic signal traces to high speed lines
- All differential pairs should be routed on the top or bottom layer (microstrip traces) if possible or on the same group of layers. Vias should only be used in the breakout region of the device to route from the top to bottom layer when necessary. Avoid using vias in the main region of the board at all cost. Use a ground reference via next to signal via. Distance between ground reference via and signal need to be calculated to have similar impedance as traces.
- All differential signals should not be routed over plane split. Changing signal layers is preferable to crossing plane splits.
- Use of and proper placement of stitching caps when split plane crossing is unavoidable to account for high-frequency return current path
- Route differential traces over a continuous plane with no interruptions.
- Do not route differential traces under power connectors or other interface connectors, crystals, oscillators, or any magnetic source.
- Route traces away from etching areas like pads, vias, and other signal traces. Try to maintain a 20 mil keep-out distance where possible.
- Decoupling caps should be placed next to each power terminal on the HD3SS2522. Care should be taken to minimize the stub length of the trace connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps.

Layout Guidelines (continued)

- Place vias as close as possible to the decoupling cap solder pad.
- Widen VCC/GND planes to reduce effect of static and dynamic IR drop.
- The VBUS traces/planes must be wide enough to carry max current for the application.

11.2 Layout Example

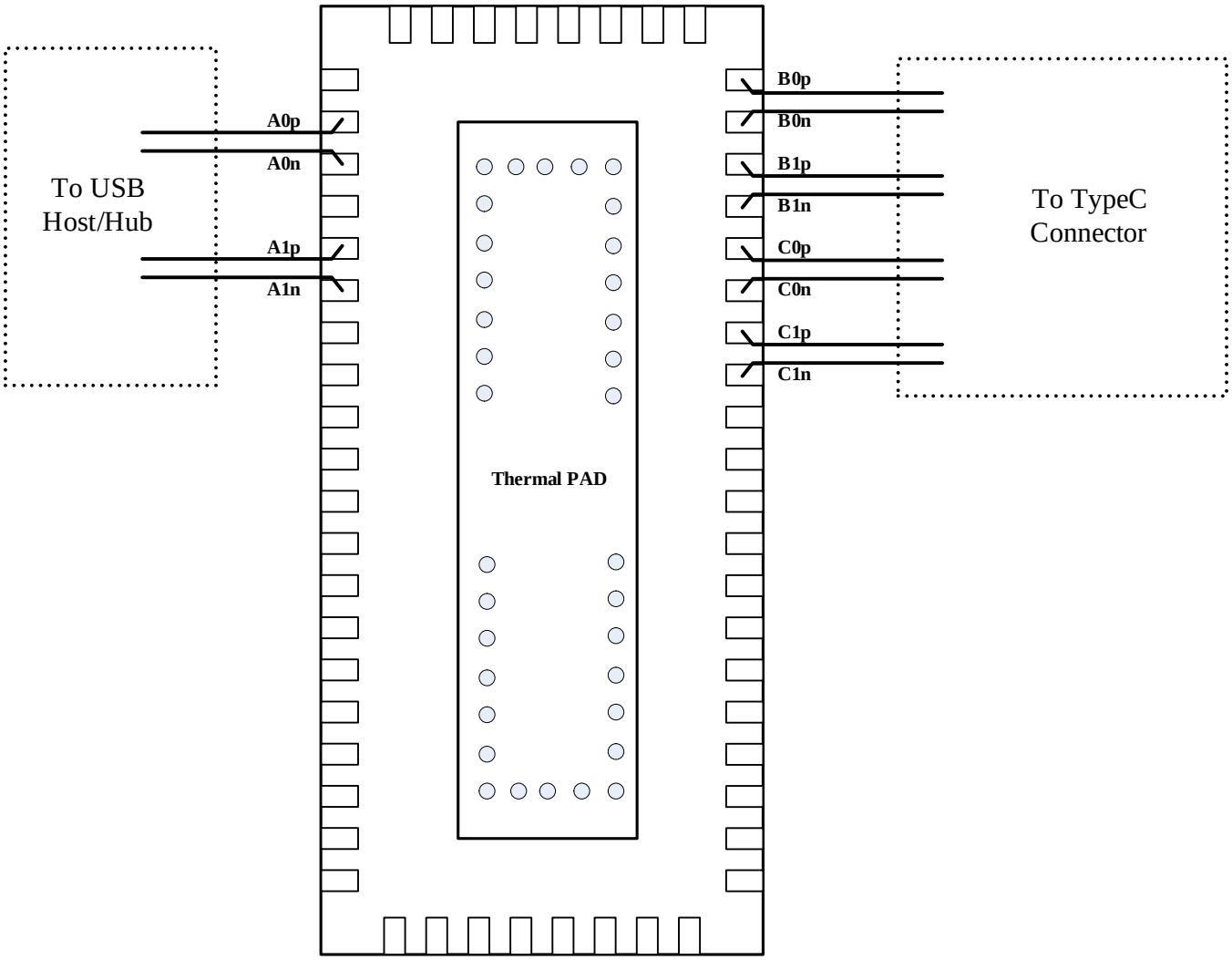


Figure 5. Layout

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HD3SS2522RHU	Preview	Production	WQFN (RHU) | 56	250 | null	-	Call TI	Call TI	0 to 70	
HD3SS2522RHUR	Active	Production	WQFN (RHU) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	HD3S2522
HD3SS2522RHUR.A	Active	Production	WQFN (RHU) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	HD3S2522
HD3SS2522RHUR.B	Active	Production	WQFN (RHU) | 56	2000 | LARGE T&R	-	Call TI	Call TI	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

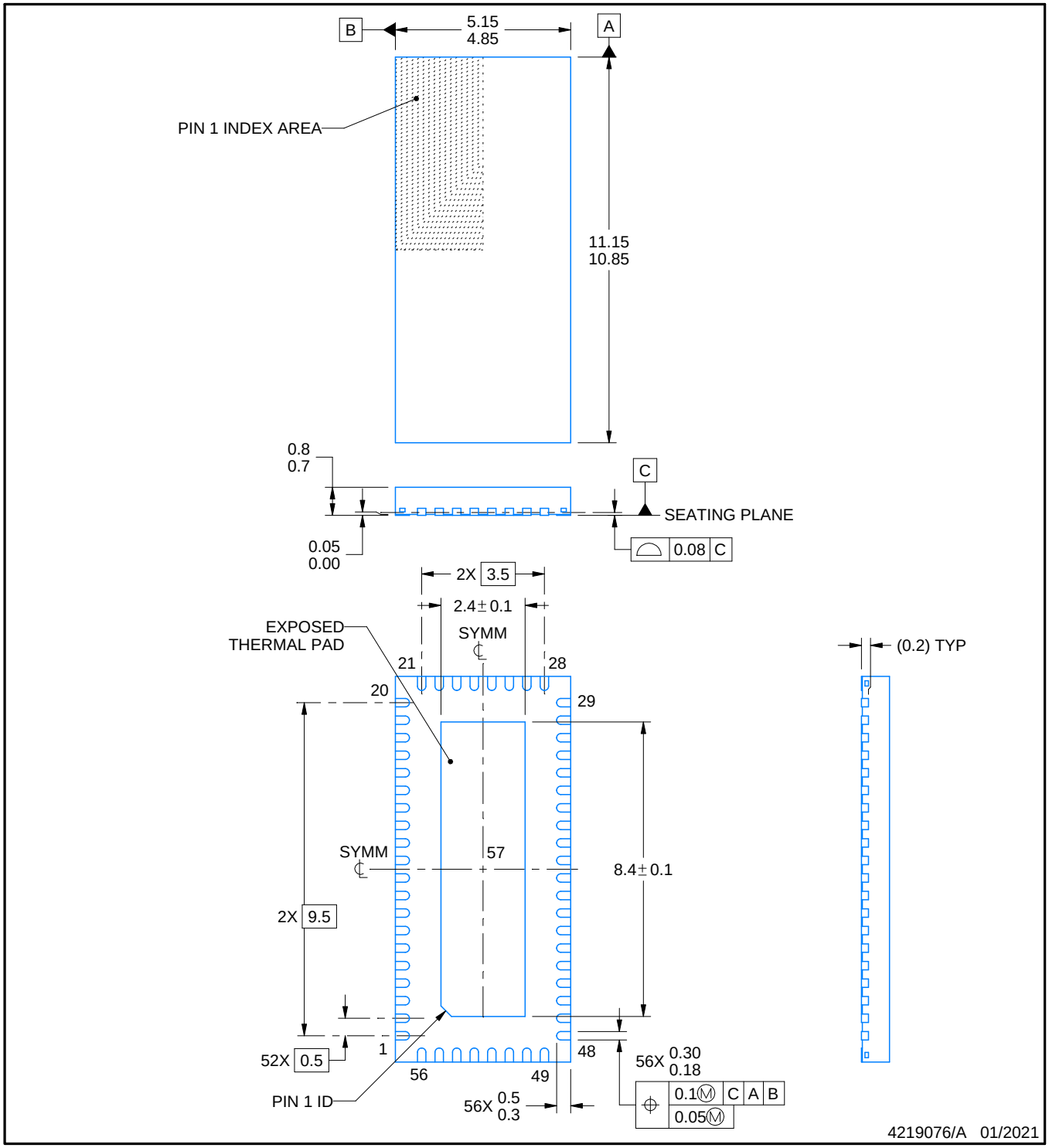
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RHU0056A

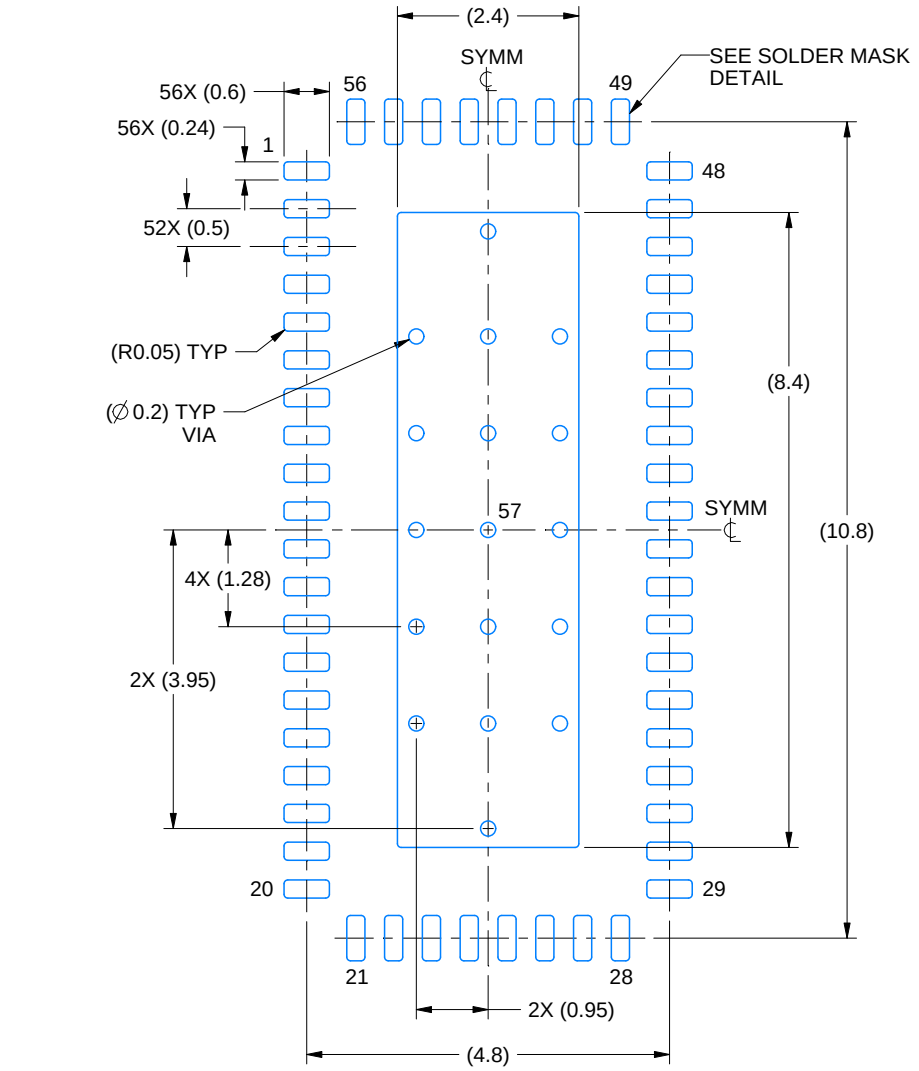
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

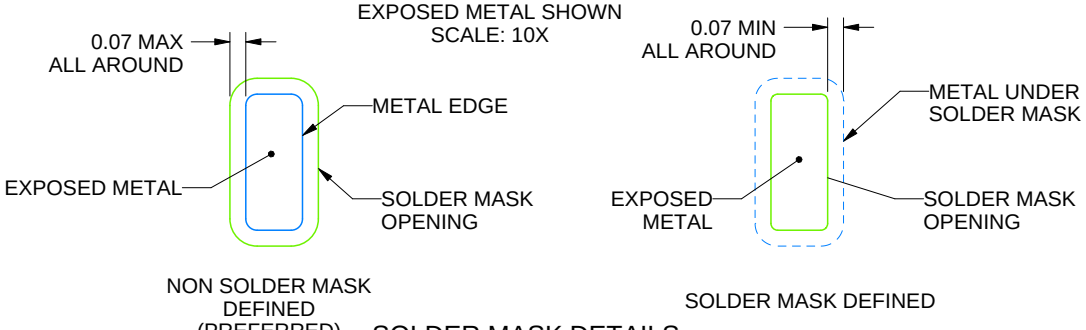
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 10X



SOLDER MASK DETAILS

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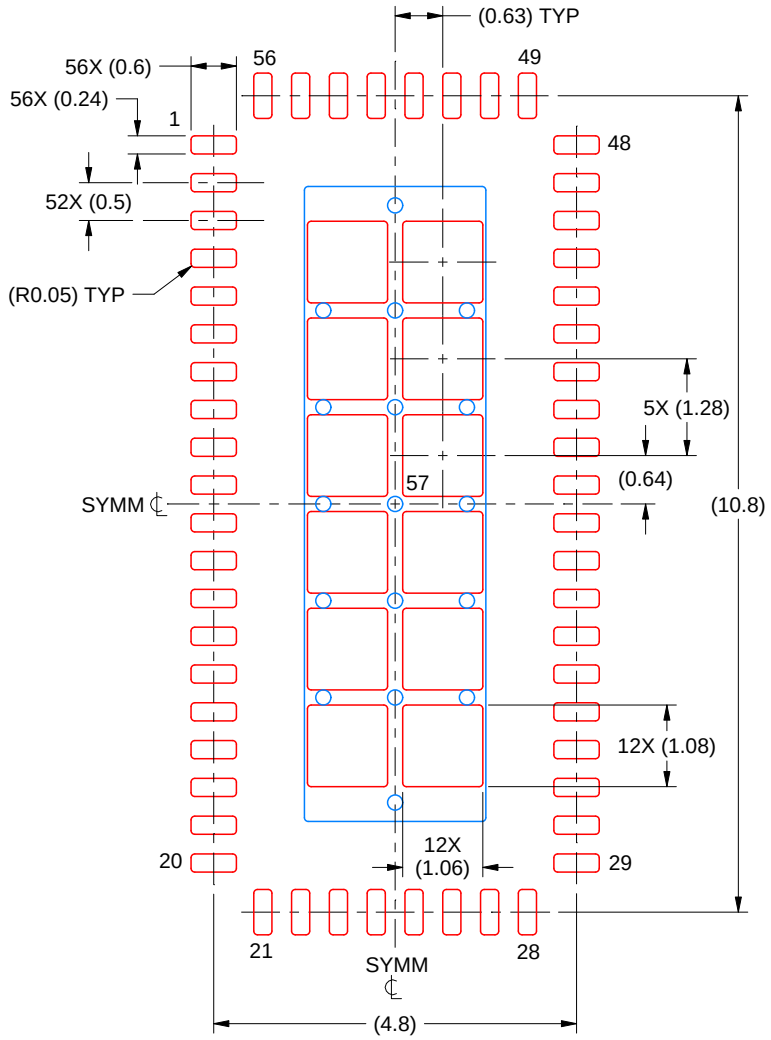
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月