DS91D180/DS91C180 100 MHz M-LVDS Line Driver/Receiver Pair

Check for Samples: DS91C180, DS91D180

FEATURES

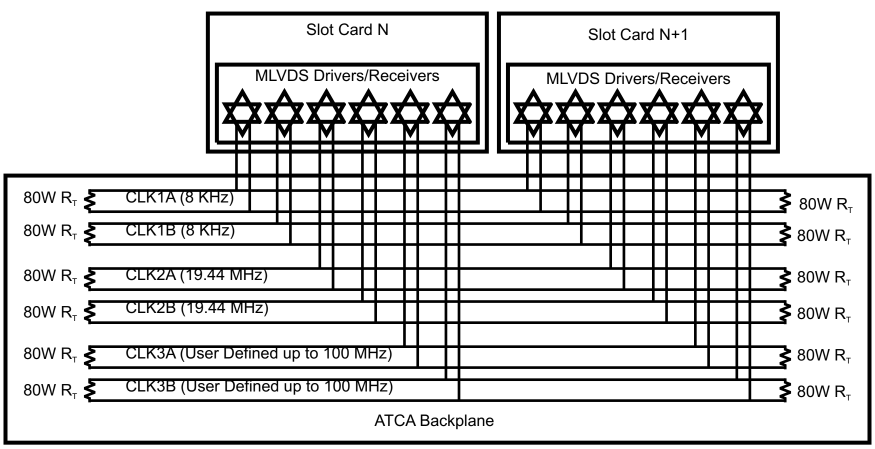
- **DC to 100+ MHz / 200+ Mbps Low Power, Low EMI Operation**
- **Optimal for ATCA, uTCA Clock Distribution Networks**
- **Meets or Exceeds TIA/EIA-899 M-LVDS Standard**
- **Wide Input Common Mode Voltage for Increased Noise Immunity**
- **DS91D180 has Type 1 Receiver Input**
- **DS91C180 has Type 2 Receiver Input for Fail-Safe Functionality**
- **Industrial Temperature Range**
- **Space Saving SOIC-14 Package (JEDEC MS-012)**

DESCRIPTION

The DS91D180 and DS91C180 are 100 MHz M-LVDS (Multipoint Low Voltage Differential Signaling) line driver/receiver pairs designed for applications that utilize multipoint networks (e.g. clock distribution in ATCA and uTCA based systems). M-LVDS is a bus interface standard (TIA/EIA-899) optimized for multidrop networks. Controlled edge rates, tight input receiver thresholds and increased drive strength are sone of the key enhancments that make M-LVDS devices an ideal choice for distributing signals via multipoint networks.

The DS91D180/DS91C180 driver input accepts LVTTL/LVCMOS signals and converts them to differential M-LVDS signal levels. The DS91D180/DS91C180 receiver accepts low voltage differential signals (LVDS, B-LVDS, M-LVDS, LV-PECL and CML) and converts them to 3V LVCMOS signals. The DS91D180 device has a M-LVDS type 1 receiver input with no offset.The DS91C180 device has a type 2 receiver input which enable failsafe functionality.

Typical Application in an ATCA Clock Distribution Network



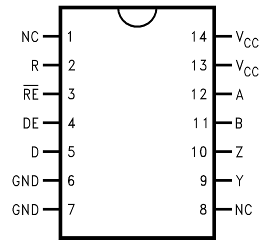
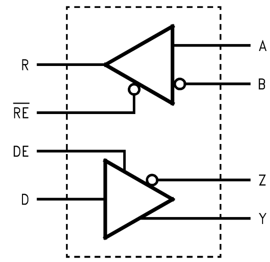


Figure 1. Connection Diagram
Top View
See Package Number D0014A

Logic Diagram



M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater than $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

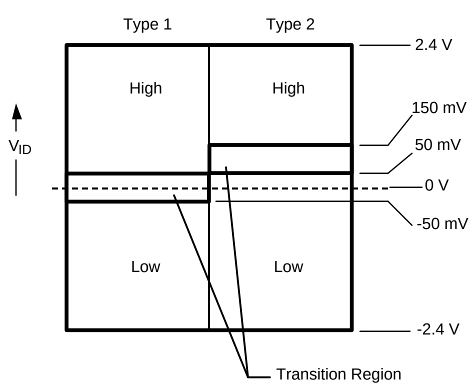


Figure 2. M-LVDS Receiver Input Thresholds

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

Supply Voltage, V_{CC}		−0.3V to +4V
Control Input Voltages		−0.3V to (V_{CC} + 0.3V)
Driver Input Voltage		−0.3V to (V_{CC} + 0.3V)
Driver Output Voltages		−1.8V to +4.1V
Receiver Input Voltages		−1.8V to +4.1V
Receiver Output Voltage		−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation at +25°C	SOIC Package	1.1 W
	Derate SOIC Package	8.8 mW/°C above +25°C
Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	θ_{JA}	113.7 °C/W
	θ_{JC}	36.9 °C/W
Maximum Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		260°C
ESD Ratings:	(HBM 1.5kΩ, 100pF)	≥ 5 kV
	(EIAJ 0Ω, 200pF)	≥ 250 V
	(CDM 0Ω, 0pF)	≥ 1000 V

(1) “Absolute Maximum Ratings” are those beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	−1.4		+3.8	V
Differential Input Voltage V_{ID}			2.4	V
High Level Input Voltage V_{IH}	2.0		V_{CC}	V
Low Level Input Voltage V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. [1][2][3][4]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
M-LVDS Driver						
$\lvert V_{YZ}\rvert$	Differential output voltage magnitude	R_L = 50Ω, C_L = 5pF Figure 3 and Figure 5	480		650	mV
ΔV_{YZ}	Change in differential output voltage magnitude between logic states		−50	0	+50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	R_L = 50Ω, C_L = 5pF Figure 3 and Figure 4	0.3	1.8	2.1	V
$\lvert\Delta V_{OS(SS)}\rvert$	Change in steady-state common-mode output voltage between logic states		0		+50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage	($V_{OS(pp)}$ @ 500KHz clock)		143		mV
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	Figure 6	0		2.4	V
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	R_L = 50Ω, C_L = 5pF, C_D = 0.5pF Figure 8 and Figure 9 [5]			1.2V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		−0.2V_{SS}			V
I_{IH}	High-level input current (LVTTL inputs)	V_{IH} = 2.0V	-15		15	μA

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
(2) All typicals are given for V_{CC} = 3.3V and T_A = 25°C.
(3) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this datasheet.
(4) C_L includes fixture capacitance and C_D includes probe capacitance.
(5) Not production tested. Ensured by a statistical analysis on a sample basis at the time of characterization.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)(4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Low-level input current (LVTTL inputs)	V_{IL} = 0.8V		-15		15	µA
V_{IKL}	Input Clamp Voltage (LVTTL inputs)	I_{IN} = -18 mA		-1.5			V
I_{OS}	Differential short-circuit output current	Figure 7		-43		43	mA
M-LVDS Receiver							
V_{IT+}	Positive-going differential input voltage threshold	See Function Tables	Type 1		20	50	mV
			Type 2		94	150	mV
V_{IT-}	Negative-going differential input voltage threshold	See Function Tables	Type 1	−50	20		mV
			Type 2	50	94		mV
V_{OH}	High-level output voltage	I_{OH} = −8mA		2.4	2.7		V
V_{OL}	Low-level output voltage	I_{OL} = 8mA			0.28	0.4	V
I_{OZ}	TRI-STATE output current	V_O = 0V or 3.6V		−10		10	µA
I_{OSR}	Short circuit Rrceiver output current (LVTTL Output)	V_O = 0V		-90	-48		mA
M-LVDS Bus (Input and Output) Pins							
I_A, I_Y	Receiver input or driver high-impedance output current	$V_{A,Y}$ = 3.8V, $V_{B,Z}$ = 1.2V, DE = GND				32	µA
		$V_{A,Y}$ = 0V or 2.4V, $V_{B,Z}$ = 1.2V, DE = GND		−20		+20	µA
		$V_{A,Y}$ = −1.4V, $V_{B,Z}$ = 1.2V, DE = GND		−32			µA
I_B, I_Z	Receiver input or driver high-impedance output current	$V_{B,Z}$ = 3.8V, $V_{A,Y}$ = 1.2V, DE = GND				32	µA
		$V_{B,Z}$ = 0V or 2.4V, $V_{A,Y}$ = 1.2V, DE = GND		−20		+20	µA
		$V_{B,Z}$ = −1.4V, $V_{A,Y}$ = 1.2V, DE = GND		−32			µA
I_{AB}, I_{YZ}	Receiver input or driver high-impedance output differential current ($I_A − I_B$ or $I_Y − I_Z$)	$V_{A,Y}$ = $V_{B,Z}$, −1.4V ≤ V ≤ 3.8V, DE = GND		−4		+4	µA
$I_{A(OFF)}$, $I_{Y(OFF)}$	Receiver input or driver high-impedance output power-off current	$V_{A,Y}$ = 3.8V, $V_{B,Z}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V				32	µA
		$V_{A,Y}$ = 0V or 2.4V, $V_{B,Z}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V		−20		+20	µA
		$V_{A,Y}$ = −1.4V, $V_{B,Z}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V		−32			µA
$I_{B(OFF)}$, $I_{Z(OFF)}$	Receiver input or driver high-impedance output power-off current	$V_{B,Z}$ = 3.8V, $V_{A,Y}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V				32	µA
		$V_{B,Z}$ = 0V or 2.4V, $V_{A,Y}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V		−20		+20	µA
		$V_{B,Z}$ = −1.4V, $V_{A,Y}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V		−32			µA
$I_{AB(OFF)}$, $I_{YZ(OFF)}$	Receiver input or driver high-impedance output power-off differential current ($I_{A(OFF)} − I_{B(OFF)}$ or $I_{Y(OFF)} − I_{Z(OFF)}$)	$V_{A,Y}$ = $V_{B,Z}$, −1.4V ≤ V ≤ 3.8V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V		−4		+4	µA
C_A, C_B	Receiver input capacitance	V_{CC} = OPEN			5.1		pF
C_Y, C_Z	Driver output capacitance				8.5		pF
C_{AB}	Receiver input differential capacitance				2.5		pF
C_{YZ}	Driver output differential capacitance				5.5		pF

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{A/B}$, $C_{Y/Z}$	Receiver input or driver output capacitance balance (C_A/C_B or C_Y/C_Z)			1.0		
SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	R_L = 50Ω, DE = V_{CC}, $\overline{RE}$ = V_{CC}		17	29.5	mA
I_{CCZ}	TRI-STATE Supply Current	DE = GND, $\overline{RE}$ = V_{CC}		7	9.0	mA
I_{CCR}	Receiver Supply Current	DE = GND, $\overline{RE}$ = GND		14	18.5	mA
I_{CCB}	Supply Current, Driver and Receiver Enabled	DE = V_{CC}, $\overline{RE}$ = GND		20	29.5	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATION						
t_{PLH}	Differential Propagation Delay Low to High	R_L = 50Ω, C_L = 5 pF,	1.0	3.4	5.5	ns
t_{PHL}	Differential Propagation Delay High to Low	C_D = 0.5 pF	1.0	3.1	5.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$ (3) (4)	Figure 8 and Figure 9		300	420	ps
t_{SKD3}	Part-to-Part Skew (5) (4)				1.9	ns
t_{TLH} (t_r)	Rise Time (4)		1.0	1.8	3.0	ns
t_{THL} (t_f)	Fall Time (4)		1.0	1.8	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 50Ω, C_L = 5 pF,			8	ns
t_{PZL}	Enable Time (Z to Active Low)	C_D = 0.5 pF			8	ns
t_{PLZ}	Disable Time (Active Low to Z)	Figure 10 and Figure 11			8	ns
t_{PHZ}	Disable Time (Active High to Z)				8	ns
t_{JIT}	Random Jitter, RJ (4)	100MHz clock pattern (6)		2.5	5.5	psrms
f_{MAX}	Maximum Data Rate		200			Mbps
RECEIVER AC SPECIFICATION						
t_{PLH}	Propagation Delay Low to High	C_L = 15 pF	2.0	4.7	7.5	ns
t_{PHL}	Propagation Delay High to Low	Figure 12 Figure 13 and Figure 14	2.0	5.3	7.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$ (3)(4)			0.6	1.9	ns
t_{SKD3}	Part-to-Part Skew (5)(4)				1.5	ns
t_{TLH} (t_r)	Rise Time (4)		0.5	1.2	3.0	ns
t_{THL} (t_f)	Fall Time (4)		0.5	1.2	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 500Ω, C_L = 15 pF			10	ns
t_{PZL}	Enable Time (Z to Active Low)	Figure 15 and Figure 16			10	ns
t_{PLZ}	Disable Time (Active Low to Z)				10	ns
t_{PHZ}	Disable Time (Active High to Z)				10	ns
f_{MAX}	Maximum Data Rate		200			Mbps

(1) All typicals are given for V = 3.3V and T_A = 25°C.
(2) C_L includes fixture capacitance and C_D includes probe capacitance.
(3) t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(4) Not production tested. Ensured by a statistical analysis on a sample basis at the time of characterization.
(5) t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(6) Stimulus and fixture jitter has been subtracted.

Test Circuits and Waveforms

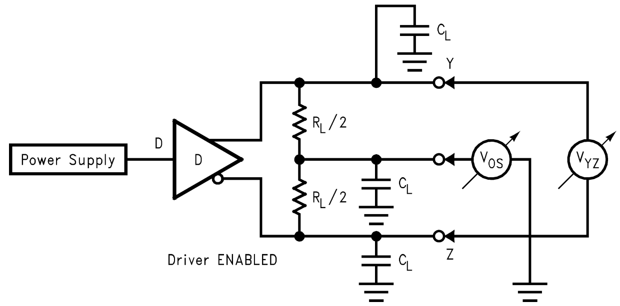


Figure 3. Differential Driver Test Circuit

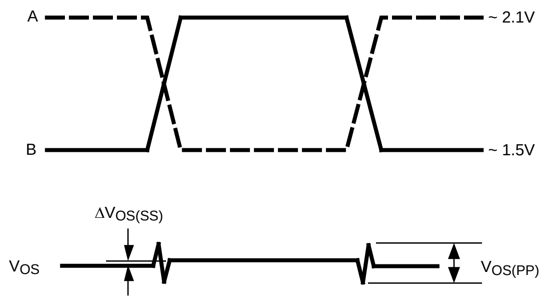


Figure 4. Differential Driver Waveforms

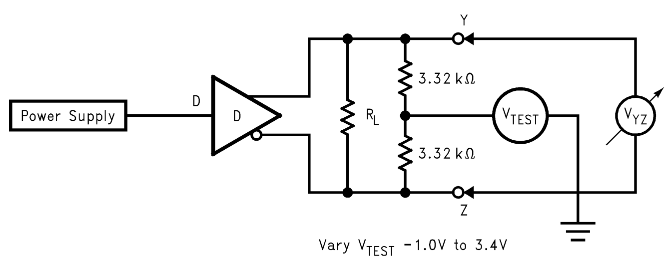


Figure 5. Differential Driver Full Load Test Circuit

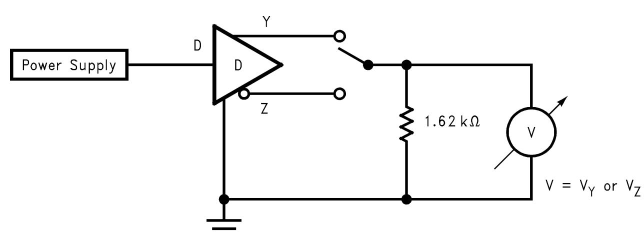


Figure 6. Differential Driver DC Open Test Circuit

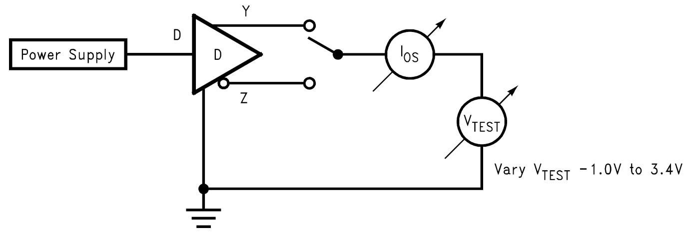


Figure 7. Differential Driver Short-Circuit Test Circuit

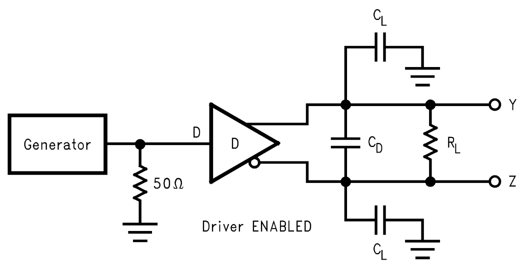


Figure 8. Driver Propagation Delay and Transition Time Test Circuit

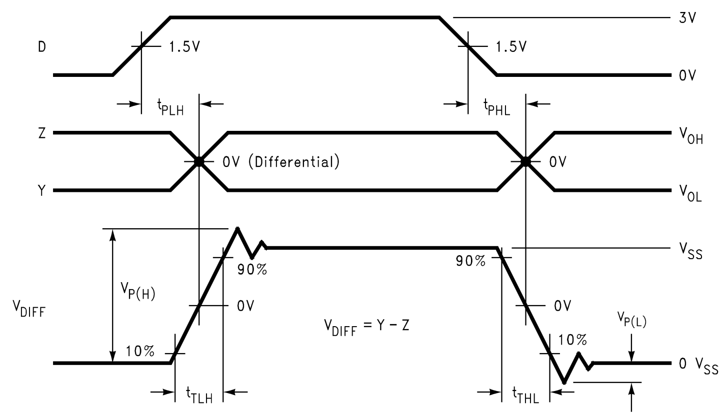


Figure 9. Driver Propagation Delays and Transition Time Waveforms

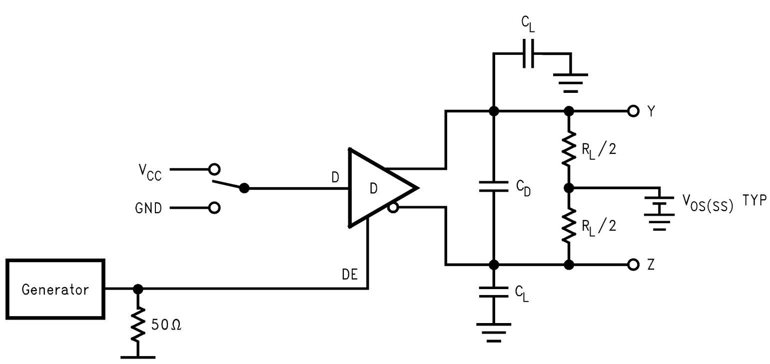


Figure 10. Driver TRI-STATE Delay Test Circuit

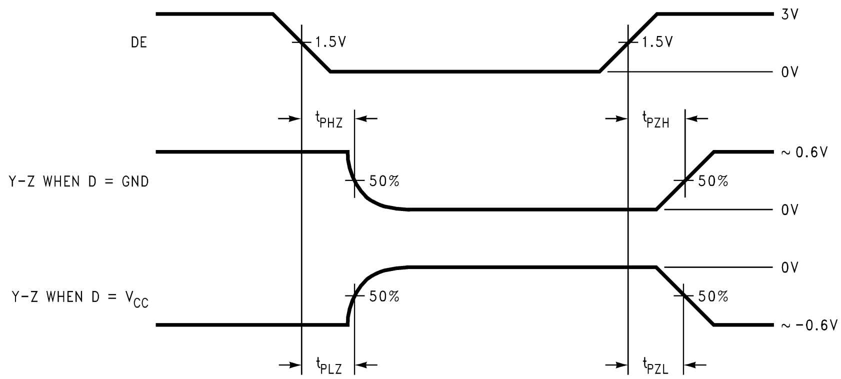


Figure 11. Driver TRI-STATE Delay Waveforms

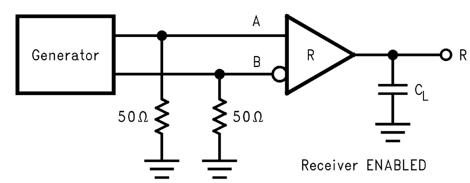


Figure 12. Receiver Propagation Delay and Transition Time Test Circuit

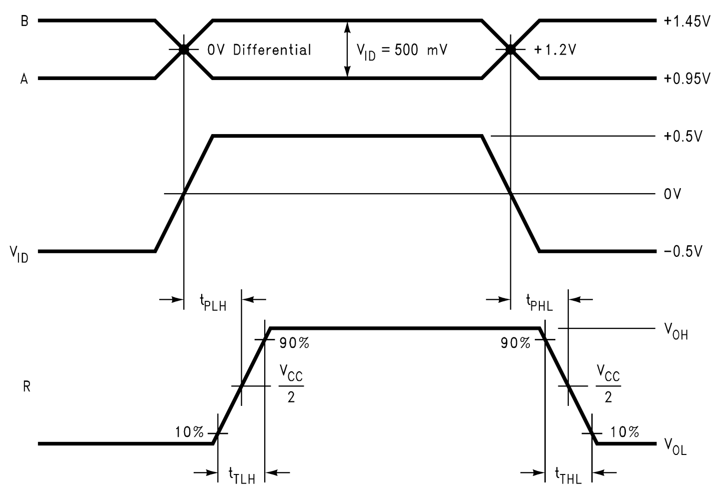


Figure 13. Type 1 Receiver Propagation Delay and Transition Time Waveforms

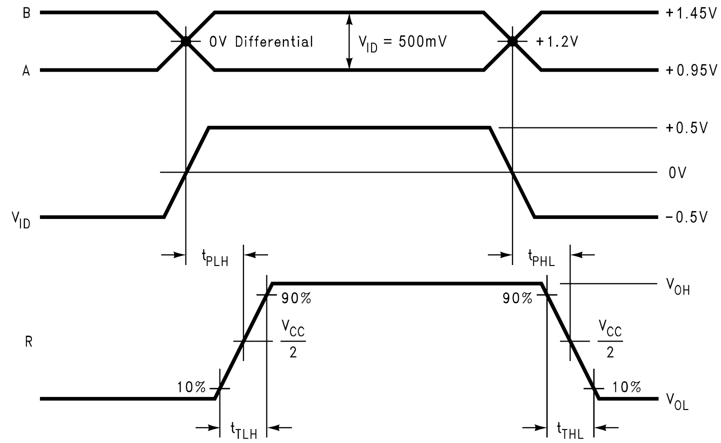


Figure 14. Type 2 Receiver Propagation Delay and Transition Time Waveforms

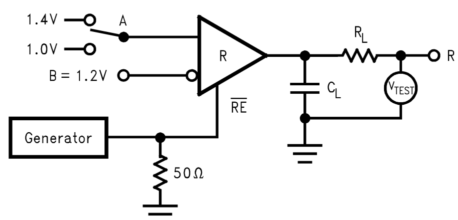


Figure 15. Receiver TRI-STATE Delay Test Circuit

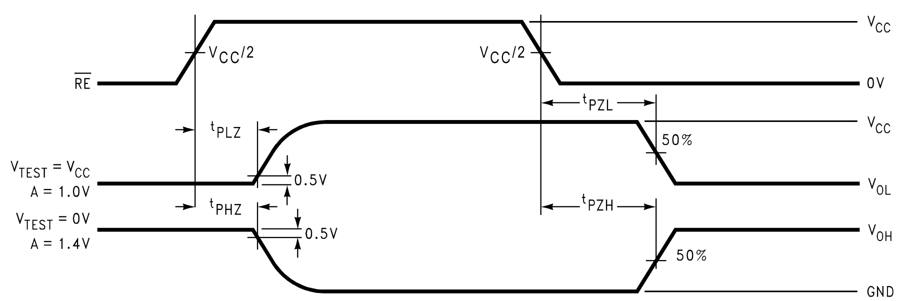


Figure 16. Receiver TRI-STATE Delay Waveforms

FUNCTION TABLES

Table 1. DS91D180/DS91C180 Transmitting(1)

Inputs		Outputs	
DE	D	Z	Y
2.0V	2.0V	L	H
2.0V	0.8V	H	L
0.8V	X	Z	Z

(1) X — Don't care condition
Z — High impedance state

Table 2. DS91D180 Receiving(1)

Inputs		Output
$\overline{RE}$	A − B	R
0.8V	≥ +0.05V	H
0.8V	≤ −0.05V	L
0.8V	0V	X
2.0V	X	Z

(1) X — Don't care condition
Z — High impedance state

Table 3. DS91C180 Receiving(1)

Inputs		Output
$\overline{RE}$	A − B	R
0.8V	≥ +0.15V	H
0.8V	≤ +0.05V	L
0.8V	0V	L
2.0V	X	Z

(1) X — Don't care condition
Z — High impedance state

Table 4. DS91D180 Receiver Input Threshold Test Voltages(1)

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	H
3.750V	3.800V	−0.050V	3.775V	L
−1.400V	−1.350V	−0.050V	−1.375V	H
−1.350V	−1.400V	0.050V	−1.375V	L

(1) H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

Table 5. DS91C180 Receiver Input Threshold Test Voltages(1)

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	H
3.800V	3.750V	0.050V	3.775V	L
−1.250V	−1.400V	0.150V	−1.325V	H
−1.350V	−1.400V	0.050V	−1.375V	L

(1) H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

PIN DESCRIPTIONS

Pin No.	Name	Description
1, 8	NC	No connect.
2	R	Receiver output pin
3	$\overline{RE}$	Receiver enable pin: When $\overline{RE}$ is high, the receiver is disabled. When $\overline{RE}$ is low or open, the receiver is enabled.
4	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled.
5	D	Driver input pin
6, 7	GND	Ground pin
9	Y	Non-inverting driver output pin
10	Z	Inverting driver output pin
11	B	Inverting receiver input pin
12	A	Non-inverting receiver input pin
13, 14	V_{CC}	Power supply pin, +3.3V ± 0.3V

REVISION HISTORY

Changes from Revision L (April 2013) to Revision M	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS91C180TMA/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91C180 TMA
DS91C180TMA/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91C180 TMA
DS91C180TMAX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91C180 TMA
DS91C180TMAX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91C180 TMA
DS91D180TMA/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91D180 TMA
DS91D180TMA/NOPB.A	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91D180 TMA
DS91D180TMAX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91D180 TMA
DS91D180TMAX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS91D180 TMA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

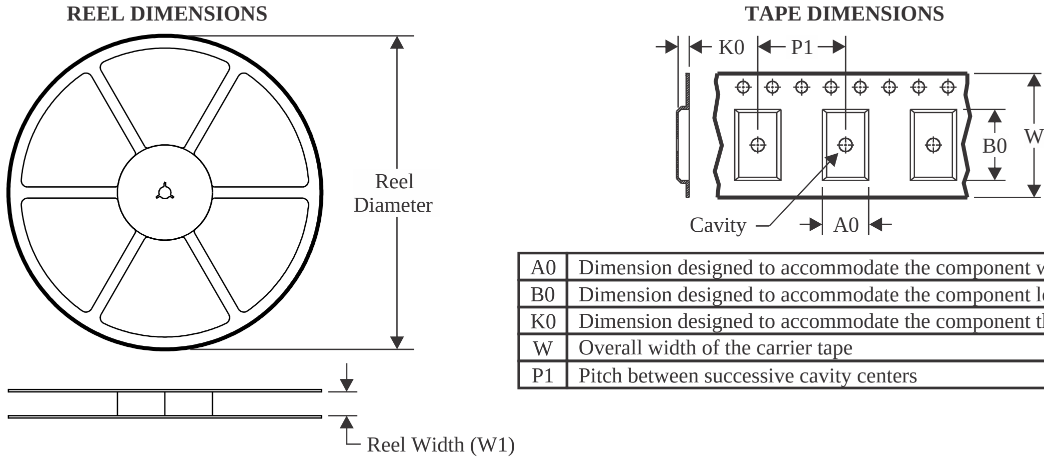
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

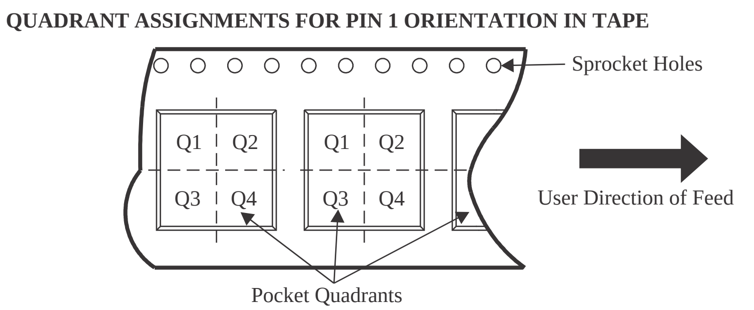
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



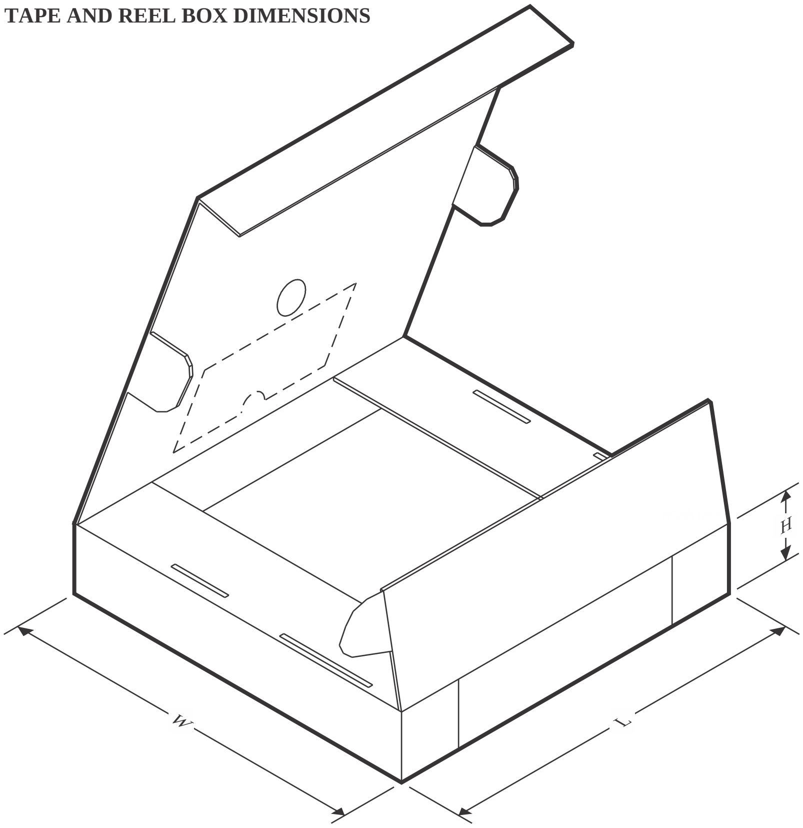
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91C180TMAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
DS91D180TMAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

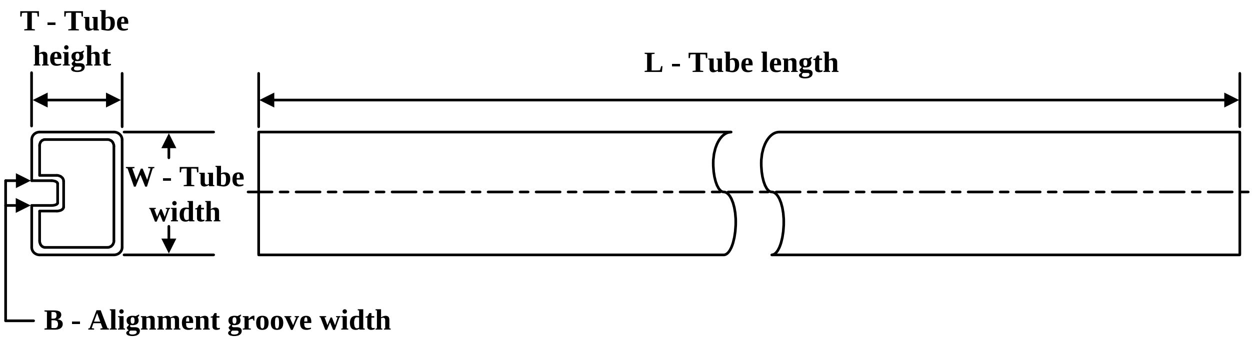
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

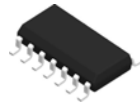
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91C180TMAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
DS91D180TMAX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS91C180TMA/NOPB	D	SOIC	14	55	495	8	4064	3.05
DS91C180TMA/NOPB.A	D	SOIC	14	55	495	8	4064	3.05
DS91D180TMA/NOPB	D	SOIC	14	55	495	8	4064	3.05
DS91D180TMA/NOPB.A	D	SOIC	14	55	495	8	4064	3.05

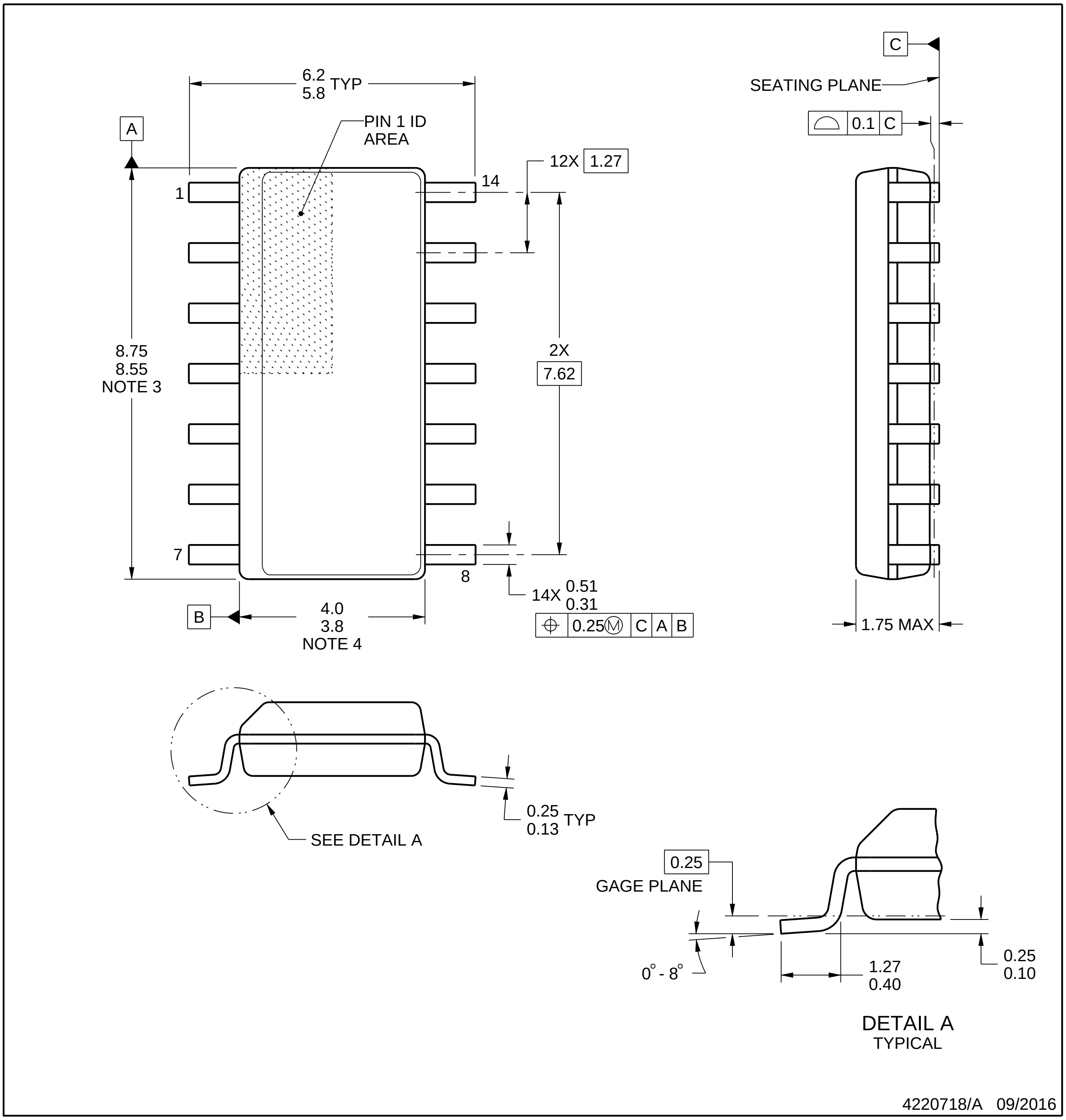


PACKAGE OUTLINE

D0014A

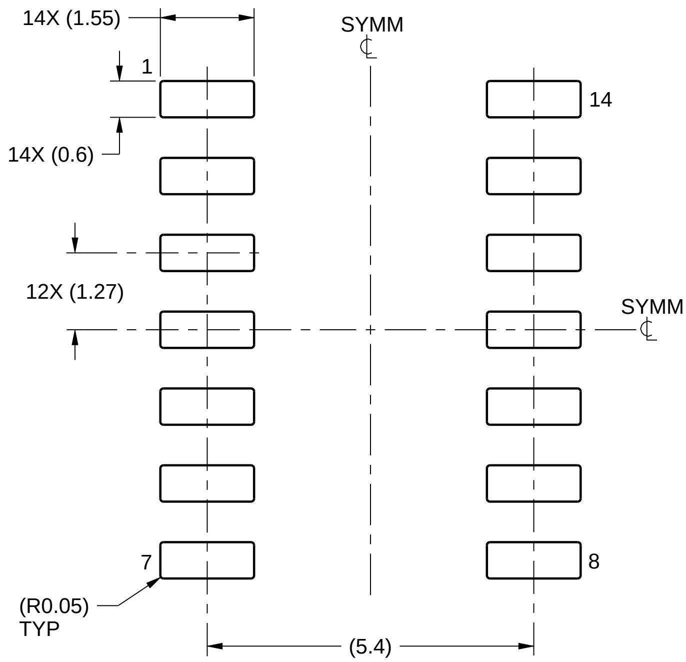
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

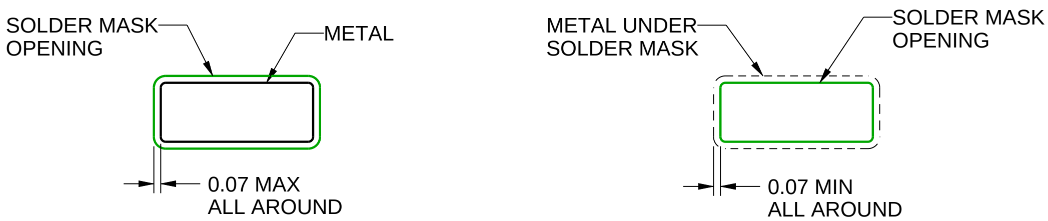


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED

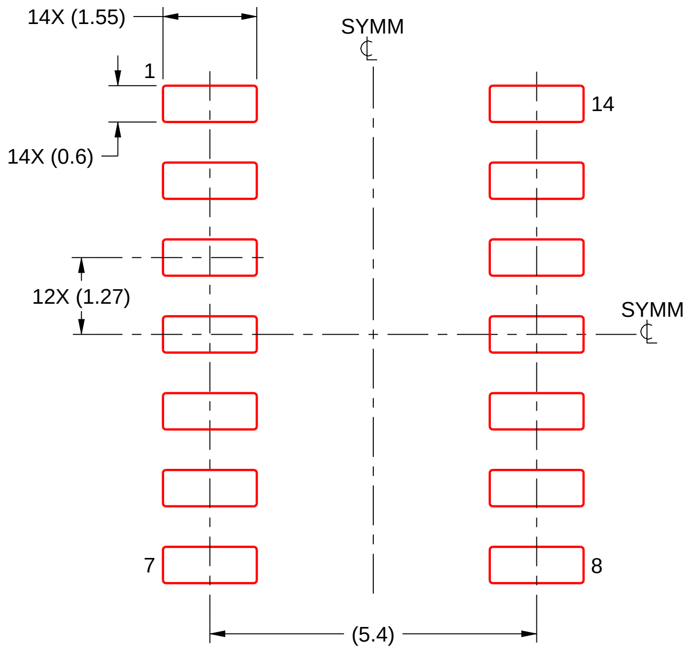
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.