DS90LV031AQML 3V LVDS Quad CMOS Differential Line Driver

Check for Samples: DS90LV031AQML

FEATURES

- **High impedance LVDS outputs with power-off**
- **Low differential skew**
- **Low propagation delay**
- **3.3V power supply design**
- **±350 mV differential signaling**
- **Low power dissipation**
- **Interoperable with existing 5V LVDS devices**
- **Compatible with IEEE 1596.3 SCI LVDS standard**
- **Compatible with proposed TIA/EIA-644 LVDS standard**
- **Pin compatible with DS26C31**
- **Typical Rise/Fall times of 800pS.**
- **Typical Tri-State Enable/Disable delays of less than 5nS.**

DESCRIPTION

The DS90LV031A is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Connection Diagram

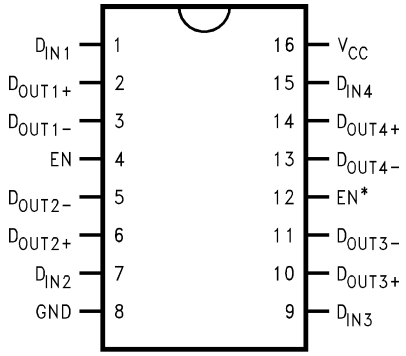


Figure 1. Dual-In-Line
See Package Number NAC0016A or NAD0016A

Functional Diagram

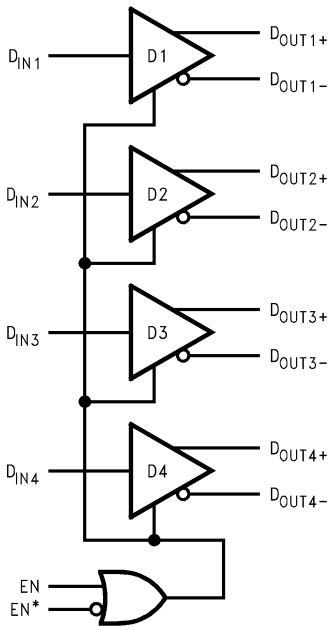


Figure 2.

Truth Table – Driver

Enables		Input	Outputs	
En	**En***	**D_I**	**D_{O+}**	**D_{O-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (D_I)	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (En, En*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_O+, D_O−)	−0.3V to +3.9V
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Lead Temperature Range (Soldering 4 sec.)	+260°C
Maximum Junction Temperature	+150°C
Maximum Power Dissipation @ +25°C (2)	
16LD CLGA (NAC and NAD)	845mW
Thermal Resistance	
θ_{JA}	
16LD CLGA (NAC and NAD)	148°C/W
θ_{JC}	
16LD CLGA (NAC and NAD)	22°C/W
ESD Rating (3)	6KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Derate (NAD & NAC packages) at 6.8mW/°C for temperatures above +25°C.
(3) Human body model, 1.5 kΩ in series with 100 pF

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{CC})	+3.0V	+3.3V	+3.6V
Operating Free Air Temperature (T_A)	-55°C	+25°C	+125°C

Table 1. Quality Conformance InspectionMil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS90LV031A Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = 3.0/3.6V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{OD1}	Differential Ouput Voltage	R_L = 100Ω	Figure 3	250	450	mV	1, 2, 3
ΔV_{OD1}	Δ in magnitude of V_{OD1} for complementary output States	R_L = 100Ω	Figure 3		50	mV	1, 2, 3
V_{OS}	Offset Voltage	R_L = 100Ω	Figure 3	1.125	1.625	V	1, 2, 3
ΔV_{OS}	Δ in Magnitude of V_{OS} for Complementary Output States	R_L = 100Ω	Figure 3		50	mV	1, 2, 3
V_{OH}	Output Voltage High	R_L = 100Ω	Figure 3		1.85	V	1, 2, 3
V_{OL}	Output Voltage Low	R_L = 100Ω	Figure 3	0.9		V	1, 2, 3
V_{IH}	Input Voltage High		(1)	2.0	V_{CC}	V	1, 2, 3
V_{IL}	Input Voltage Low		(1)	Gnd	0.8	V	1, 2, 3
I_{IH}	Input Current	V_I = V_{CC} or 2.5V, V_{CC} = 3.6V			±10	µA	1, 2, 3
I_{IL}	Input Current	V_I = Gnd or 0.4V, V_{CC} = 3.6V			±10	µA	1, 2, 3
V_{CI}	Input Clamp Voltage	I_{CI} = -8mA, V_{CC} = 3.0V			-1.5	V	1, 2, 3
I_{OS}	Output Short Circuit Current	Enabled, D_I = V_{CC}, D_O+ = 0V or D_I = Gnd, D_O- = 0V		-9.0		mA	1, 2, 3
I_{Off}	Power-off Leakage	V_O = 0V or 3.6V V_{CC} = 0V or V_{CC} = Open			±20	µA	1, 2, 3
I_{OZ}	Output TRI-STATE Current	En = 0.8V and En* = 2.0V V_O = 0V or V_{CC}, V_{CC} = 3.6V			±10	µA	1, 2, 3
I_{CC}	No Load Drivers Enabled Supply Current	D_I = V_{CC} or Gnd			18	mA	1, 2, 3
I_{CCL}	Loaded Drivers Enabled Supply Current	R_L = 100Ω All Channels, D_I = V_{CC} or Gnd (all inputs)			35	mA	1, 2, 3
I_{CCZ}	Loaded or No Load Drivers Disabled Supply Current	D_I = V_{CC} or Gnd, En = Gnd, En* = V_{CC}			12	mA	1, 2, 3

(1) Tested during V_{OH}/V_{OL} tests.

DS90LV031A Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = 3.0/3.3/3.6V, R_L = 100Ω, C_L = 20pF.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHLD}	Differential Propagation Delay High to Low		Figure 4 and Figure 5	0.3	3.5	ns	9, 10, 11
t_{PLHD}	Differential Propagation Delay Low to High		Figure 4 and Figure 5	0.3	3.5	ns	9, 10, 11
t_{SkD}	Differential Skew t_{PHLD} - t_{PLHD}				1.5	ns	9, 10, 11
t_{Sk1}	Channel to Channel Skew		(1)		1.75	ns	9, 10, 11
t_{Sk2}	Chip to Chip Skew		(2)		3.2	ns	9, 10, 11

(1) Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

(2) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

PARAMETER MEASUREMENT INFORMATION

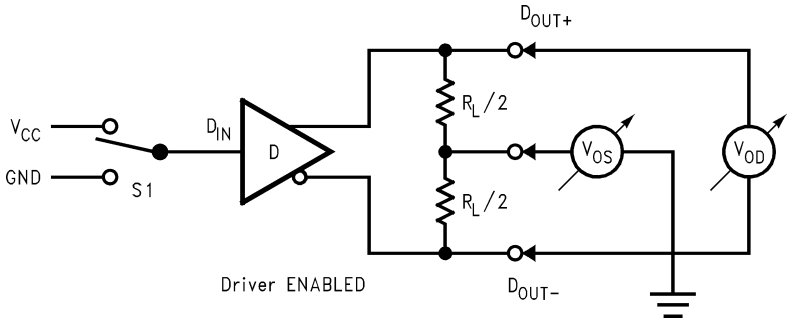


Figure 3. Driver V_{OD} and V_{OS} Test Circuit

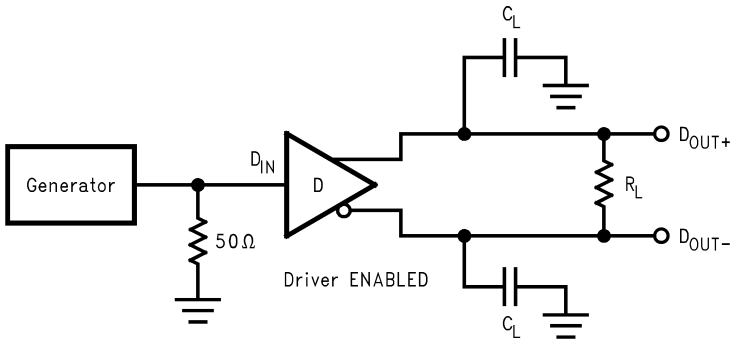


Figure 4. Driver Propagation Delay and Transition Time Test Circuit

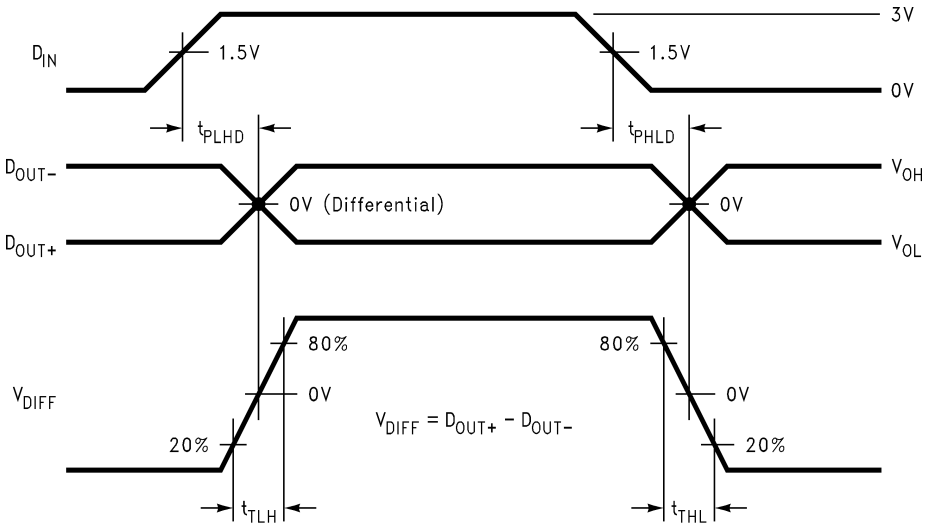


Figure 5. Driver Propagation Delay and Transition Time Waveforms

TYPICAL APPLICATION

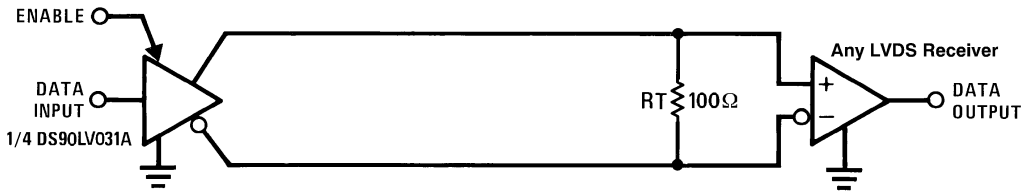


Figure 6. Point-to-Point Application

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the LVDS Owner's Manual at http://www.ti.com/ww/en/analog/interface/lvds.shtml.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 6. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV031A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.5 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 6. AC or unterminated configurations are not allowed. The 3.5 mA loop current will develop a differential voltage of 350 mV across the 100Ω termination resistor which the receiver detects with a 250 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV – 100 mV = 250 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 7. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90LV031A is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver and is a step down replacement for the 5V DS90C031 Quad Driver.

Power Decoupling Recommendations

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is greater with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination

Use a resistor which best matches the differential impedance of your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Fail-safe Feature

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV032A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

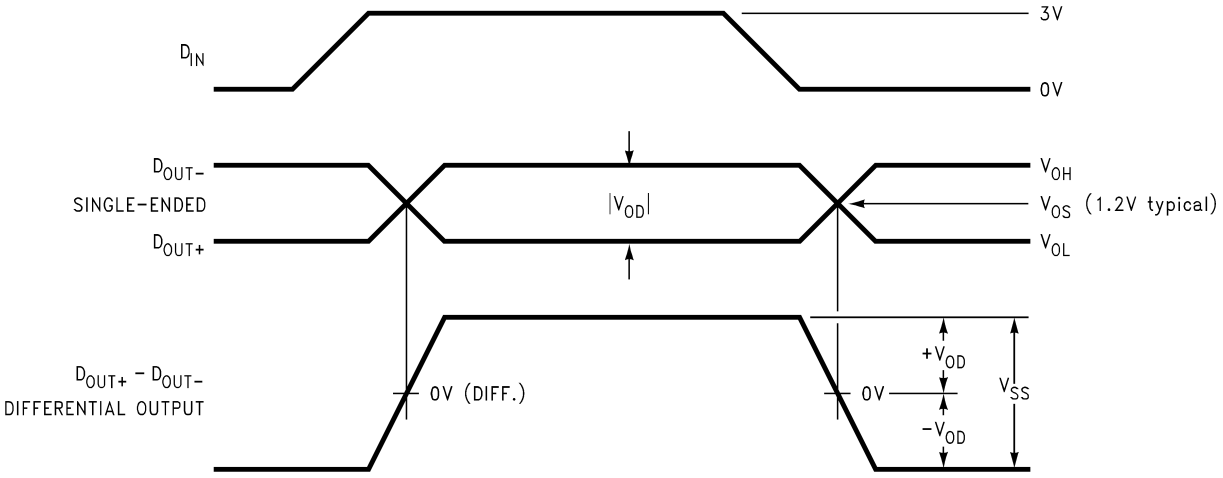


Figure 7. Driver Output Levels

Pin Descriptions

Pin No.	Name	Description
1, 7, 9, 15	D_I	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_O+	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_O−	Inverting driver output pin, LVDS levels
4	En	Active high enable pin, OR-ed with En*
12	En*	Active low enable pin, OR-ed with En
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	Gnd	Ground pin

Typical Performance Curves

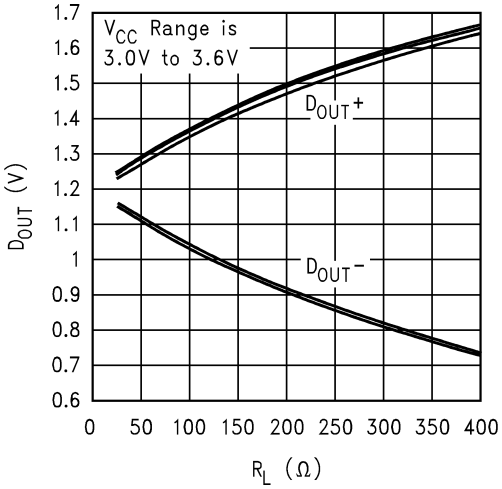


Figure 8. Typical DS90LV031, T_A = 25°C D_O (single ended) vs R_L

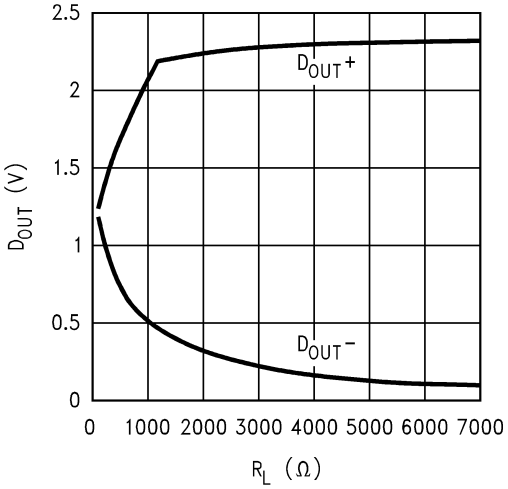


Figure 9. Typical DS90LV031, D_O vs R_L, V_{CC} = 3.3V, T_A = 25°C

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9865101QFA	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90LV031AW -QML Q 5962-98651 01QFA ACO 01QFA >T
DS90LV031AW-QML	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90LV031AW -QML Q 5962-98651 01QFA ACO 01QFA >T
DS90LV031AWGMLS	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DS90LV031AWG MLS ACO MLS >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

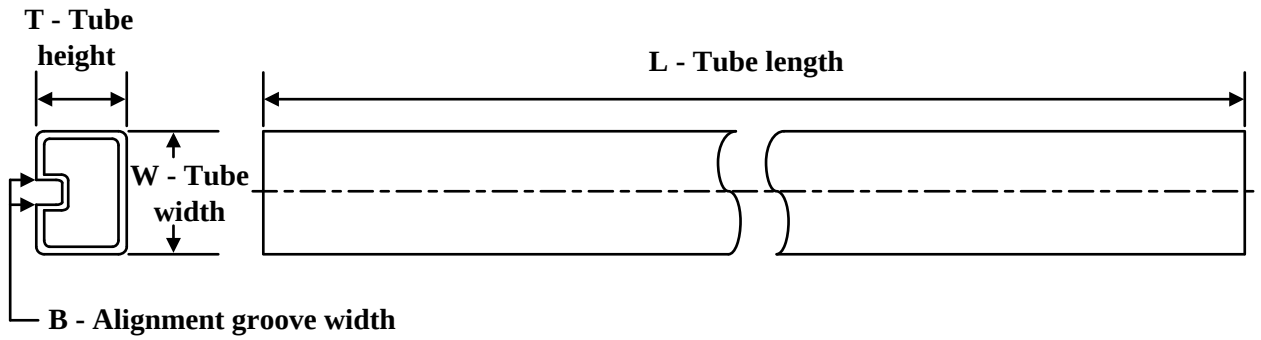
OTHER QUALIFIED VERSIONS OF DS90LV031AQML, DS90LV031AQML-SP :

- Military : DS90LV031AQML
- Space : DS90LV031AQML-SP

NOTE: Qualified Version Definitions:

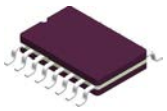
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9865101QFA	NAD	CFP	16	19	502	23	9398	9.78
DS90LV031AW-QML	NAD	CFP	16	19	502	23	9398	9.78

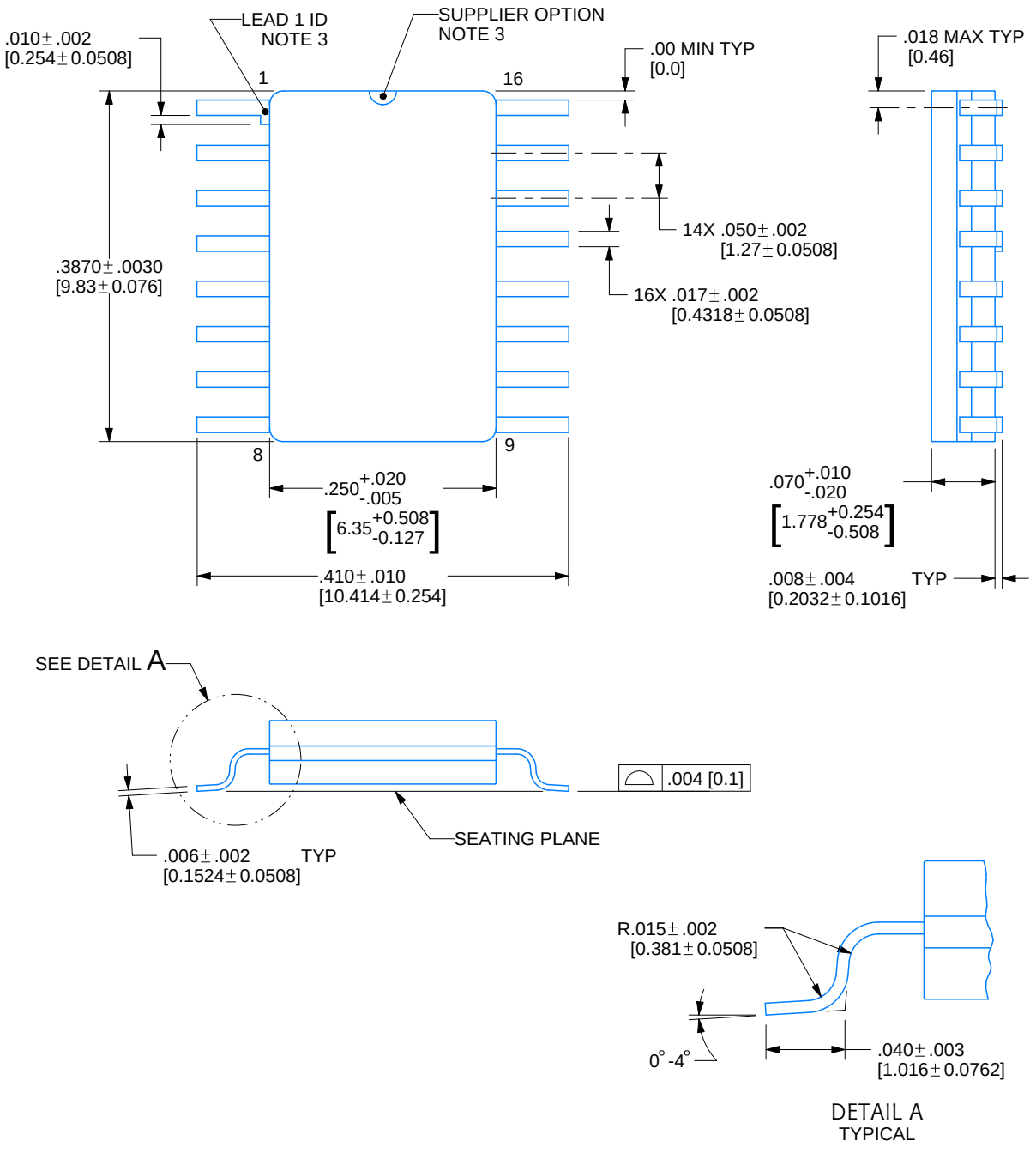


PACKAGE OUTLINE

NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



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NOTES:

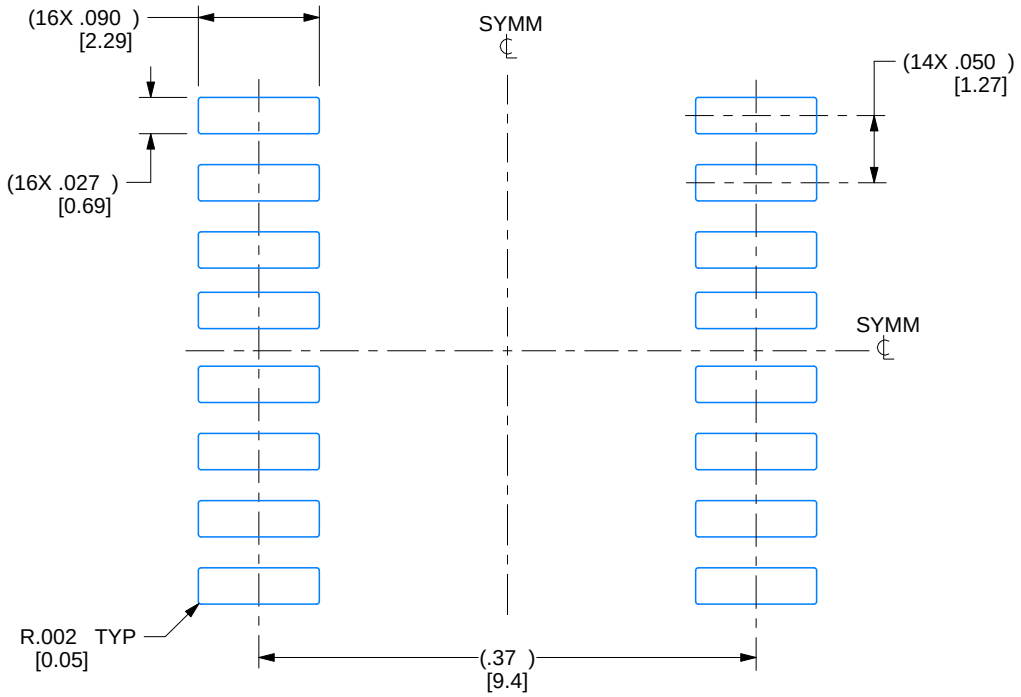
1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

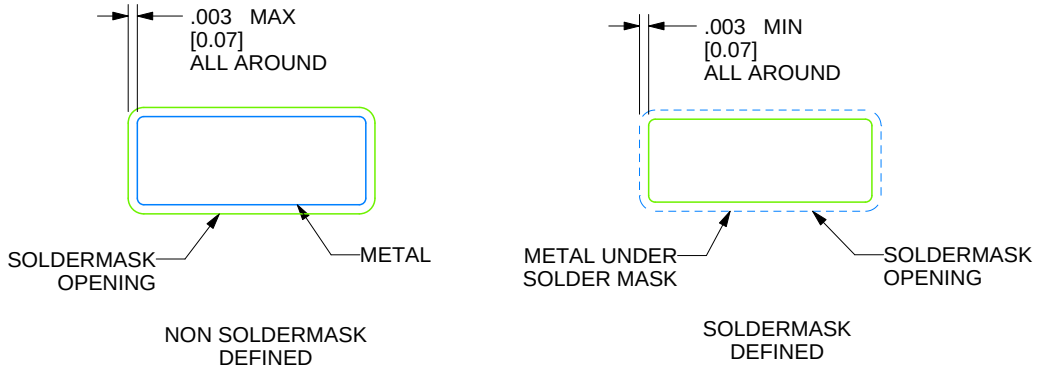
NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



RECOMMENDED LAND PATTERN



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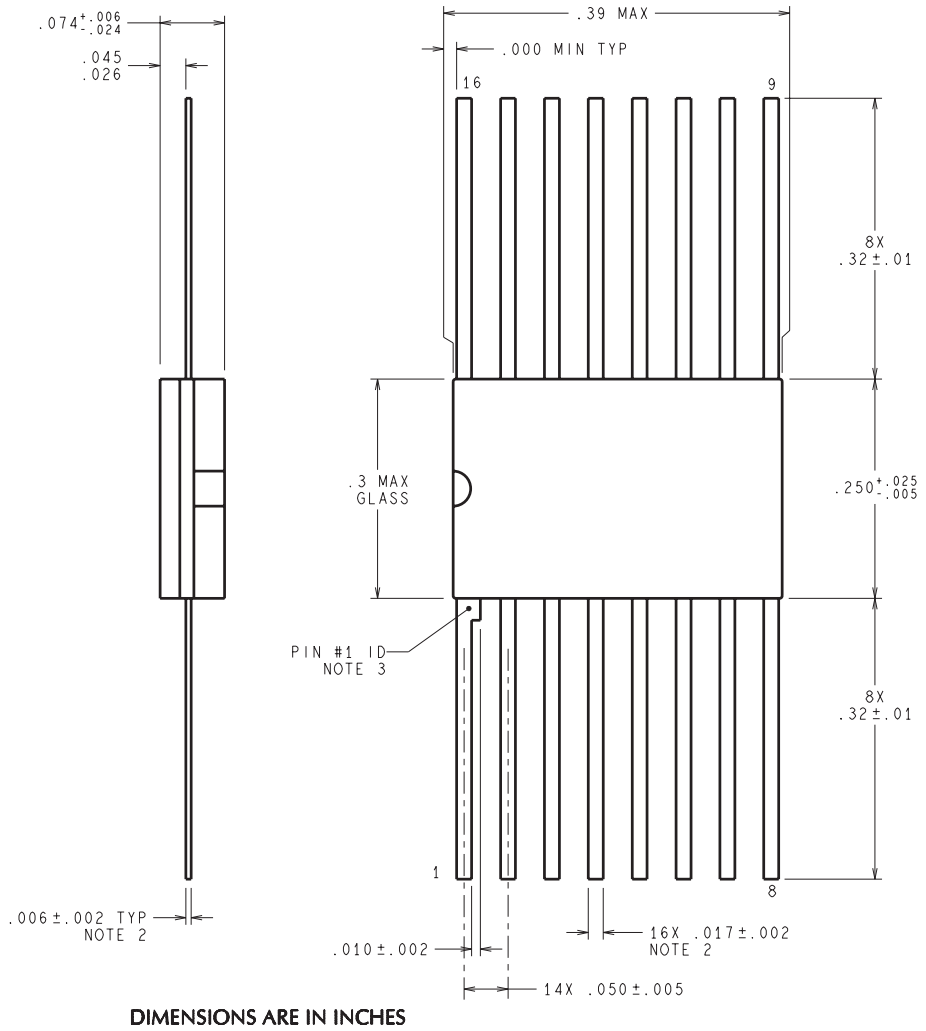
REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197879	12/30/2021	TINA TRAN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198832	02/15/2022	K. SINCERBOX
C	.387± .003 WAS .39000± .00012;	2200917	08/08/2022	D. CHIN / K. SINCERBOX

NAD0016A



DIMENSIONS ARE IN INCHES

W16A (Rev T)

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Last updated 10/2025