DS320PR810 八通道线性转接驱动器，用于 PCIe 5.0、CXL 1.1

1 特性

- 八通道线性转接驱动器支持速率高达 32 Gbps 的 PCIe 5.0、CXL 2.0 和 UPI 2.0
- 支持大多数交流耦合接口，包括 DP、SAS、SATA、XFI
- CTLE 在 16GHz 下可升至 22dB
- 100 ps 的超低延迟
- PRBS 数据的 75 fs 低附加随机抖动
- 16GHz 时 -10dB 的极低回波损耗
- 3.3V 单电源
- 内部稳压器具有抗电源噪声能力
- 160mW/通道的低有功功率
- 无需散热器
- 引脚搭接、SMBus 或 EEPROM 编程
- 针对 PCIe 用例的自动接收器检测
- 与协议无关的线性转接驱动器可无缝支持 PCIe 链接训练
- 通过一个或多个 DS320PR810 支持 x4、x8、x16、x24 总线宽度
- 温度范围为 -40 °C 至 85°C
- 5.5mm × 10mm、64 引脚 WQFN 封装

2 应用

- 机架式服务器、微服务器和塔式服务器
- 高性能计算
- 硬件加速器
- 网络连接存储
- 存储区域网络 (SAN) 和主机总线适配器 (HBA) 卡
- 网络接口卡 (NIC)
- 台式计算机/主板

3 说明

DS320PR810 是一款八通道低功耗高性能线性中继器或转接驱动器，专为支持 PCIe 5.0、CXL 2.0、UPI 2.0 和其他速率高达 32 Gbps 的接口而设计。

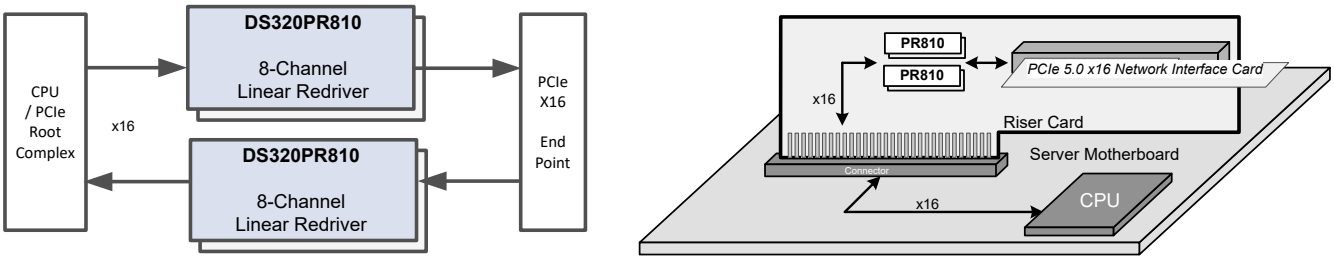
DS320PR810 接收器部署了连续时间线性均衡器 (CTLE)，用以提供可编程高频增强功能。均衡器可以打开由于 PCB 布线等互连介质引起的码间串扰 (ISI) 而完全关闭的输入眼图。CTLE 接收器后跟一个线性输出驱动器。DS320PR810 的线性数据路径保留了发射预设信号的特性。线性转接驱动器成为无源通道的一部分，该通道作为一个整体进行链路训练，可获得更优发送和接收均衡设置。对这种链路训练协议进行透明管理可实现更优的电气链路和尽可能低的延迟。该器件具有低通道间串扰、低附加抖动和极低的回波损耗，因此在链路中几乎可用作无源元件，而又具有实用的均衡功能。该器件的数据路径使用内部稳压电源轨，可高度抵抗板上的各种电源噪声。

此器件还具有低交流和直流增益变化，可在各种平台部署中提供一致的均衡功能。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
DS320PR810	WQFN（NJX，64）	5.50mm × 10.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



典型应用

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4 Revision History

DATE	REVISION	NOTES
August 2022	*	Initial Release

5 Pin Configuration and Functions

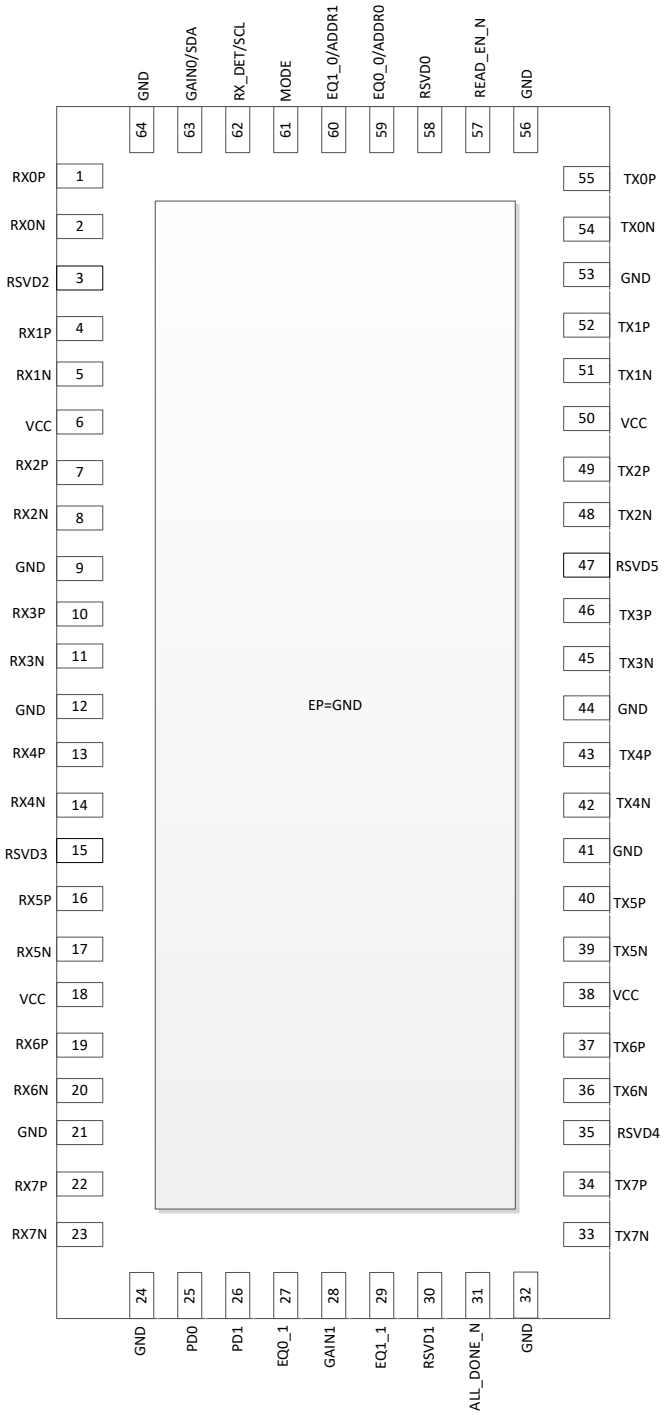


图 5-1. NJX Package, 64-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ALL_DONE_N	31	O, 3.3 V open drain	In **SMBus/I²C Primary mode**: Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7 kΩ required for operation. High: External EEPROM load failed or incomplete Low: External EEPROM load successful and complete In **SMBus/I²C Secondary/Pin mode**: This output is High-Z. The pin can be left floating.
MODE	61	I, 5-level	Sets device control configuration modes. 5-level IO pin as provided in 表 7-4. The pin can be exercised at device power up or in normal operation mode. L0: **Pin mode** – device control configuration is done solely by strap pins. L1: **SMBus/I²C Primary mode** – device control configuration is read from external EEPROM. When the DS320PR810 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C secondary operation is available in this mode before, during or after EEPROM reading. Note: during EEPROM reading if the external SMBus/I²C primary wants to access DS320PR810 registers it must support arbitration. L2: **SMBus/I²C Secondary mode** – device control configuration is done by an external controller with SMBus/I²C primary. L3 and L4 (Float): RESERVED – TI internal test modes.
EQ0 / ADDR0	59	I, 5-level	In **Pin mode:** Sets receiver linear equalization (CTLE) boost for channels 0-3 (Bank 0) as provided in 表 7-1. These pins are sampled at device power-up only. In **SMBus/I²C mode:** Sets SMBus / I²C secondary address as provided in 表 7-5. These pins are sampled at device power-up only.
EQ1 / ADDR1	60	I, 5-level	
EQ0_1	27	I, 5-level	Sets receiver linear equalization (CTLE) boost for channels 4-7 (Bank 1) as provided in 表 7-1 in Pin mode. The pin is sampled at device power-up only.
EQ1_1	29	I, 5-level	
GAIN0 / SDA	63	I, 5-level / I/O, 3.3 V LVCMOS, open drain	In **Pin mode:** Flat gain (DC and AC) from the input to the output of the device for channels 0-3 (Bank 0). The pin is sampled at device power-up only. In **SMBus/I²C mode:** 3.3 V SMBus/I²C data. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I²C interface standard.
GAIN1	28	I, 5-level	Flat gain (DC and AC) from the input to the output of the device for channels 4-7 (Bank 1) in Pin mode. The pin is sampled at device power-up only.
GND	EP, 9, 12, 21, 24, 32, 41, 44, 53, 56, 64	P	Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
PD0	25	I, 3.3 V LVCMOS	2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1-MΩ weak pull-down resistor. The pin triggers PCIe Rx detect state machine when toggled. High: power down for channels 0-3 Low: power up, normal operation for channels 0-3
PD1	26	I, 3.3 V LVCMOS	2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1-MΩ weak pull-down resistor. The pin triggers PCIe Rx detect state machine when toggled. High: power down for channels 4-7 Low: power up, normal operation for channels 4-7
READ_EN_N	57	I, 3.3 V LVCMOS	In **SMBus/I²C Primary mode**: After device power up, when the pin is low, it initiates the SMBus / I²C Primary mode EEPROM read function. When EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. During the EEPROM load process the device’s signal path is disabled. In **SMBus/I²C Secondary and Pin modes:** In these modes the pin is not used. The pin can be left floating. The pin has internal 1-MΩ weak pull-down resistor.

表 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RSVD0	58	—	Reserved use for TI. The pin must be left floating (NC).
RSVD1	30	—	Reserved use for TI. The pin must be left floating (NC).
RX_DET / SCL	62	I, 5-level / I/O, 3.3 V LVCMOS, open drain	In **Pin mode:** Sets receiver detect state machine options as provided in 表 7-3. The pin is sampled at device power-up only. In **SMBus/I²C mode:** 3.3V SMBus/I²C clock. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I²C interface standard.
RX0N	2	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 0.
RX0P	1	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 0.
RX1N	5	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 1.
RX1P	4	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 1.
RX2N	8	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 2.
RX2P	7	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 2.
RX3N	11	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 3.
RX3P	10	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 3.
RX4N	14	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 4.
RX4P	13	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 4.
RX5N	17	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 5.
RX5P	16	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 5.
RX6N	20	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 6.
RX6P	19	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 6.
RX7N	23	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 7.
RX7P	22	I	Non-inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 7.
TX0N	54	O	Inverting pin for 100 Ω differential driver output. Channel 0.
TX0P	55	O	Non-inverting pin for 100 Ω differential driver output. Channel 0.
TX1N	51	O	Inverting pin for 100 Ω differential driver output. Channel 1.
TX1P	52	O	Non-inverting pin for 100 Ω differential driver output. Channel 1.
TX2N	48	O	Inverting pin for 100 Ω differential driver output. Channel 2.
TX2P	49	O	Non-inverting pin for 100 Ω differential driver output. Channel 2.
TX3N	45	O	Inverting pin for 100 Ω differential driver output. Channel 3.
TX3P	46	O	Non-inverting pin for 100 Ω differential driver output. Channel 3.
TX4N	42	O	Inverting pin for 100 Ω differential driver output. Channel 4.

表 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
TX4P	43	O	Non-inverting pin for 100 Ω differential driver output. Channel 4.
TX5N	39	O	Inverting pin for 100 Ω differential driver output. Channel 5.
TX5P	40	O	Non-inverting pin for 100 Ω differential driver output. Channel 5.
TX6N	36	O	Inverting pin for 100 Ω differential driver output. Channel 6.
TX6P	37	O	Non-inverting pin for 100 Ω differential driver output. Channel 6.
TX7N	33	O	Inverting pin for 100 Ω differential driver output. Channel 7.
TX7P	34	O	Non-inverting pin for 100 Ω differential driver output. Channel 7.
VCC	6, 18, 38, 50	P	Power supply pins. VCC = 3.3 V ±10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane. Install a decoupling capacitor to GND near each VCC pin.
RSVD2, 3, 4, 5	3, 15, 35, 47	—	Reserved pins – for best signal integrity performance connect the pins to GND. Alternate option would be 0 Ω resistors from pins to GND.

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply Voltage (VCC)	– 0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and Open Drain I/O voltage	– 0.5	4.0	V
$VIO_{5LVL,ABSMAX}$	5-level Input I/O voltage	– 0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	– 0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	– 0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance	DC to <50 Hz, sinusoidal[1]			250	mVpp
		50 Hz to 500 kHz, sinusoidal[1]			100	mVpp
		500 kHz to 2.5 MHz, sinusoidal[1]			33	mVpp
		Supply noise, >2.5 MHz, sinusoidal[1]			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_A	Operating ambient temperature		−40		85	°C
T_J	Operating junction temperature	All device modes			125	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD1/0, and READ_EN_N	200			µs
VCC_{SMBUS}	SMBus/I²C SDA and SCL Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in SMBus secondary mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate		1		32	Gbps

6.4 Thermal Information

THERMAL METRIC(1)		DS320PR810 NJX, 64 Pins	UNIT
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	22.9	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.6	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	℃/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	℃/W
ψ_{JB}	Junction-to-board characterization parameter	7.1	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	℃/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{ACT}	Device active power	8 channels active, EQ = 0-2		1.15	1.42	W
		8 channels active, EQ = 5-19		1.41	1.75	W
P_{RXDET}	Device power consumption while waiting for far end receiver terminations	All channels enabled but no far end receiver detected		166		mW
P_{STBY}	Device power consumption in standby power mode	All channels disabled (PD1,0 = H)		23		mW
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PD1, PD0, READ_EN_N pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD1, PD0, READ_EN_N pins			1.08	V
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7 kΩ (SDA, SCL, ALL_DONE_N pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = – 4 mA (SDA, SCL, ALL_DONE_N pins)			0.4	V
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD1, PD0, READ_EN_N pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PD1, PD0, READ_EN_N pins)	−10			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6 V, VCC = 0 V, (SCL, SDA, , PD1, PD0, READ_EN_N pins)			200	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SDA, SCL, PD1, PD0, READ_EN_Npins		1.6		pF
5 Level IOs (MODE, GAIN0, GAIN1, EQ0_0, EQ1_0, EQ0_1, EQ1_1, RX_DET pins)						
I_{IH_5L}	Input high leakage current, 5-level IOs	VIN = 2.5 V			10	µA
I_{IL_5L}	Input low leakage current for all 5-level IOs except MODE.	VIN = GND	−10			µA
$I_{IL\_5L,MODE}$	Input low leakage current for MODE pin	VIN = GND	−200			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC Common Mode Voltage	Device is in active or standby state		1.4		V
$Z_{RX\text{-}DC}$	Rx DC Single-Ended Impedance			50		Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	DC input CM input impedance during Reset or power-down	Inputs are at $V_{RX\text{-}DC\text{-}CM}$ voltage	15			kΩ

6.5 DC Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	Impedance of Tx during active signaling, VID,diff = 1 Vpp		100		Ω
$V_{TX-DC-CM}$	Tx DC common mode Voltage			1.0		V
$I_{TX-SHORT}$	Tx Short Circuit Current	Total current the Tx can supply when shorted to GND		70		mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50 MHz to 1.25 GHz		−22		dB
		1.25 GHz to 2.5 GHz		−19		dB
		2.5 GHz to 4.0 GHz		−16		dB
		4.0 GHz to 8.0 GHz		−12		dB
		8.0 GHz to 16 GHz		−9		dB
RL_{RX-CM}	Input common-mode return loss	50 MHz to 2.5 GHz		−16		dB
		2.5 GHz to 8.0 GHz		−9		dB
		8.0 GHz to 16 GHz		−6		dB
XT_{RX}	Receiver-side pair-to-pair isolation; Port A or Port B	Minimum over 10 MHz to 16 GHz range		−40		dB
Transmitter						
$V_{TX-AC-CM-PP}$	Tx AC Peak-to-Peak Common Mode Voltage	Measured with lowest EQ, GAIN = L4; PRBS-7, 32 Gbps, over at least 10^6 bits using a bandpass-Pass Filter from 30 Khz - 500 Mhz			50	mVpp
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	$V_{TX-CM-DC} = \lvert V_{OUTn+} + V_{OUTn-} \rvert /2$, Measured by taking the absolute difference of $V_{TX-CM-DC}$ during PCIe state L0 and Electrical Idle	0		120	mV
$V_{TX-RCV-DETECT}$	Amount of Voltage change allowed during Receiver Detection	Measured while Tx is sensing whether a low-impedance Receiver is present. No load is connected to the driver output	0		600	mV
$RL_{TX-DIFF}$	Output differential return loss	50 MHz to 1.25 GHz		−22		dB
		1.25 GHz to 2.5 GHz		−21		dB
		2.5 GHz to 4.0 GHz		−19		dB
		4.0 GHz to 8.0 GHz		−14		dB
		8.0 Ghz to 16 Ghz		−10		dB
RL_{TX-CM}	Output Common-mode return loss	50 MHz to 2.5 GHz		−14		dB
		2.5 GHz to 8.0 GHz		−10		dB
		8.0 GHz to 16 GHz		−7		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum over 10 MHz to 16 GHz range		−40		dB
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either Low-to-High or High-to-Low transition.		100	140	ps

6.6 High Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	Between any two lanes within a single transmitter.			20	ps
$T_{RJ-DATA}$	Additive Random Jitter with data	Jitter through redriver minus the calibration trace. 32 Gbps PRBS15. 800 mVpp-diff input swing.		75		fs
$T_{RJ-INTRINSIC}$	Intrinsic additive Random Jitter with clock	Jitter through redriver minus the calibration trace. 16 Ghz CK. 800 mVpp-diff input swing.		40		fs
$JITTER_{TOTAL-DATA}$	Additive Total Jitter with data	Jitter through redriver minus the calibration trace. 32 Gbps PRBS15. 800 mVpp-diff input swing.		1.5		ps
$JITTER_{TOTAL-INTRINSIC}$	Intrinsic additive Total Jitter with clock	Jitter through redriver minus the calibration trace. 16 Ghz CK. 800 mVpp-diff input swing.		1.7		ps
FLAT-GAIN	Broadband DC and AC flat gain - input to output, measured at DC	Minimum EQ, GAIN1/0 = L0		−5.6		dB
		Minimum EQ, GAIN1/0 = L1		−3.8		dB
		Minimum EQ, GAIN1/0 = L2		−1.2		dB
		Minimum EQ, GAIN1/0 = L3		2.6		dB
		Minimum EQ, GAIN1/0 = L4 (Float)		0.6		dB
$EQ-MAX_{16G}$	EQ boost at max setting (EQ INDEX = 19)	AC gain at 16 GHz relative to gain at 100 MHz.		22		dB
$FLAT-GAIN_{VAR}$	Flat gain variation across PVT measured at DC	GAIN1/0 = L4, minimum EQ setting. Max-Min.	−2.5		1.5	dB
$EQ-GAIN_{VAR}$	EQ boost variation across PVT	At 16 Ghz. GAIN1/0 = L4, maximum EQ setting. Max-Min.	−3.0		4.0	dB
LINEARITY-DC	Output DC Linearity	at GAIN1/0 = L4		1700		mVpp
LINEARITY-AC	Output AC Linearity at 32Gbps	at GAIN1/0 = L4		700		mVpp

6.7 SMBUS/I²C Timing Charateristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Secondary Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU-STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD-DAT}	Data hold time		0			µs
T_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		2		ns
t_{SU-STO}	Set-up time for STOP condition		0.6			µs

6.7 SMBUS/I²C Timing Charateristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs
C_b	Capacitive load for each bus line				400	pF
Primary Mode						
f_{SCL-M}	SCL clock frequency			303		kHz
t_{LOW-M}	SCL low period			1.90		µs
T_{HIGH-M}	SCL high period			1.40		µs
$t_{SU-STA-M}$	Set-up time for a repeated START condition			2		µs
$t_{HD-STA-M}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated			1.5		µs
$T_{SU-DAT-M}$	Data setup time			1.4		µs
$t_{HD-DAT-M}$	Data hold time			0.5		µs
t_{R-M}	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		120		ns
T_{F-M}	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		2		ns
$t_{SU-STO-M}$	Stop condition setup time			1.5		µs
EEPROM Timing						
T_{EEPROM}	EEPROM configuration load time	Time to assert ALL_DONE_N after READ_EN_N has been asserted.		7.5		ms
T_{POR}	Time to first SMBus access	Power supply stable after initial ramp. Includes initial power-on reset time.		50		ms

6.8 Typical Characteristics

图 6-1 shows typical EQ gain curves versus frequency for different EQ settings. 图 6-2 shows EQ gain variation over temperature for maximum EQ setting of 19. 图 6-3 shows typical differential return loss for Rx and Tx pins.

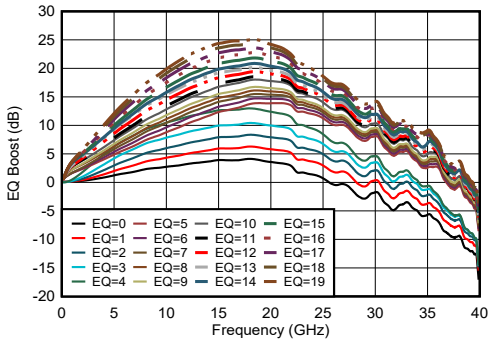


图 6-1. Typical EQ Boost vs Frequency

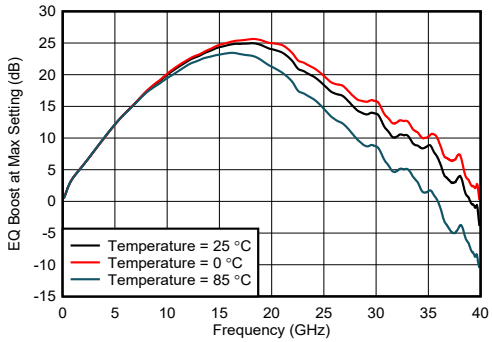


图 6-2. Typical EQ Boost vs Frequency at Different Temperature with EQ=19

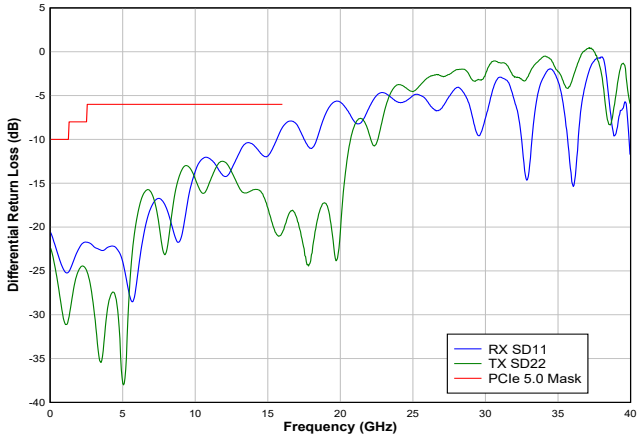


图 6-3. Typical Differential Return Loss

6.9 Typical Jitter Characteristics

图 6-4 , 图 6-5, and 图 6-6 show eye diagrams at BERT source output, through calibration traces, and through 810 respectively. Note: 810 adds little to no random jitter. Residual equalization of ≅4 dB at EQ = 0 setting results in slightly lower deterministic jitter through DUT compared to baseline setup with 7 dB loss.

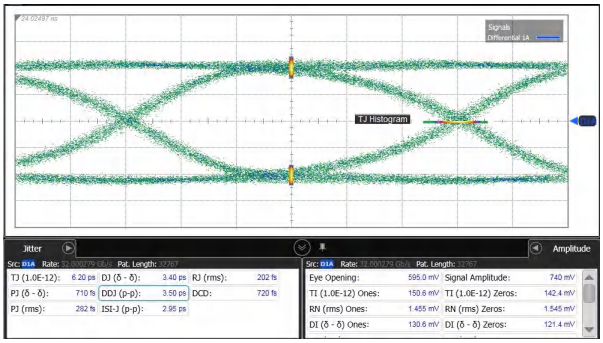


图 6-4. At BERT Source Output (1 dB Loss)

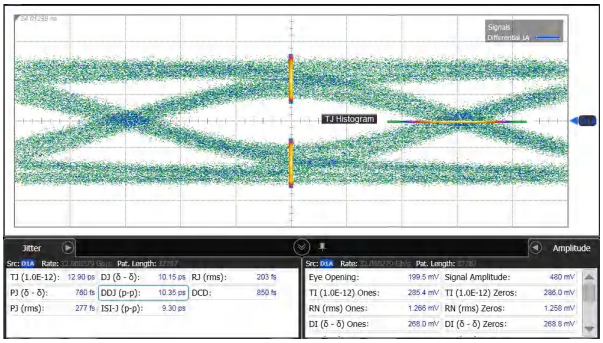


图 6-5. Through Baseline Calibration Trace Setup (7 dB Loss)

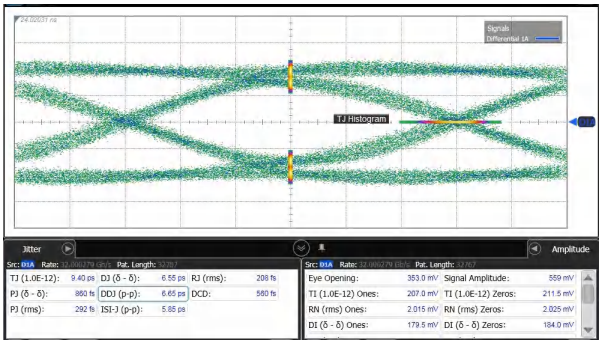


图 6-6. Through DS320PR810 (7 dB Loss and DUT EQ = 0)

7 Detailed Description

7.1 Overview

The DS320PR810 is an eight-channel multi-rate linear repeater with integrated signal conditioning. The device's signal channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

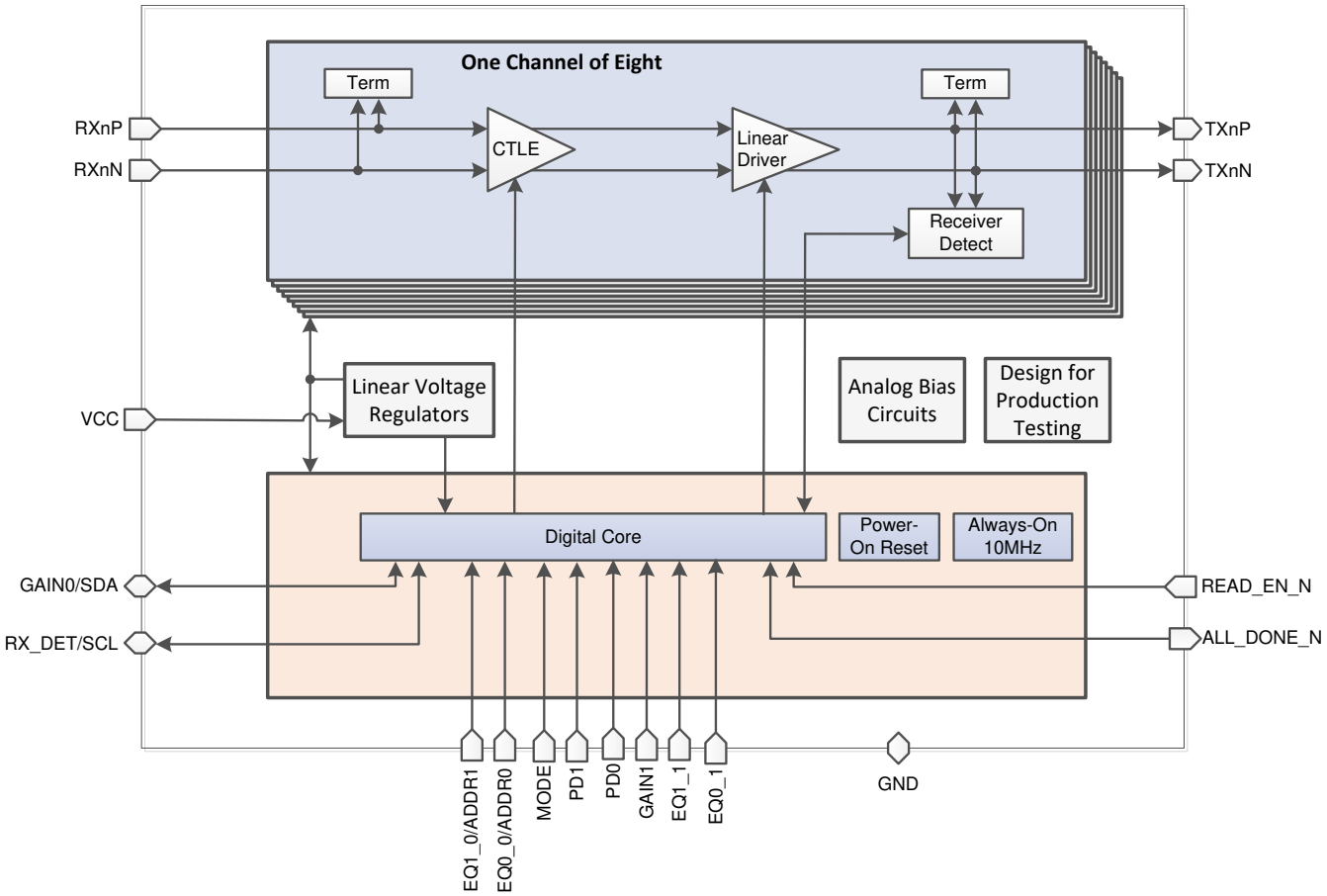
The DS320PR810 can be configured three different ways:

Pin mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I²C Primary mode – device control configuration is read from external EEPROM. When the DS320PR810 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C secondary operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I²C primary wants to access DS320PR810 registers, then it must support arbitration. The mode is preferred when software implementation is not desired.

SMBus/I²C Secondary mode – provides most flexibility. Requires a SMBus/I²C primary device to configure DS320PR810 though writing to its secondary address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Equalization

The DS320PR810 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I^{2}C mode. In Pin mode the settings are optimized for FR4 traces.

表 7-1 provides available equalization boost through EQ control pins or SMBus/I^{2}C registers. In Pin Control mode EQ1_0 and EQ0_0 pins set equalization boost for channels 0-3 (Bank 0) and EQ1_1 and EQ0_1 for channels 4-7 (Bank 1). In I^{2}C mode individual channels can be independently programmed for EQ boost.

表 7-1. Equalization Control Settings

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)	
EQ INDEX	Pin mode		SMBus/I^{2}C Mode					
	EQ1_0/1	EQ0_0/1	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass	at 8 GHz	at 16 GHz
0	L0	L0	0	0	0	1	3.0	4.0
1	L0	L1	1	0	0	1	4.0	6.0
2	L0	L2	3	0	0	1	5.5	8.0
5	L1	L0	0	0	1	0	6.5	10.5
6	L1	L1	1	0	1	0	7.0	11.5
7	L1	L2	2	0	1	0	7.5	12.5
8	L1	L3	3	0	3	0	8.5	13.0
9	L1	L4	4	0	3	0	9.0	14.0
10	L2	L0	5	1	7	0	10.0	15.0
11	L2	L1	6	1	7	0	10.5	15.5
12	L2	L2	8	1	7	0	11.0	16.5
13	L2	L3	10	1	7	0	12.0	17.0
14	L2	L4	10	2	15	0	12.5	18.0
15	L3	L0	11	3	15	0	13.0	19.0
16	L3	L1	12	4	15	0	14.0	19.5
17	L3	L2	13	5	15	0	14.5	20.5
18	L3	L3	14	6	15	0	15.5	21.0
19	L3	L4	15	7	15	0	16.0	22.0

7.3.2 Flat-Gain

The GAIN1 and GAIN0 pins can be used to set the overall data-path flat gain (DC and AC) of the DS320PR810 when the device is in Pin mode. The pin GAIN0 sets the Flat-Gain for channels 0-3 (Bank 0) and GAIN1 sets the same for channels 4-7 (Bank 1). In I^{2}C mode each channel can be independently set. 表 7-2 provides flat gain control configuration settings. In the default recommendation for most systems will be GAIN1,0 = L4 (float) that provides flat gain of 0 dB.

The flat-gain and equalization of the DS320PR810 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

表 7-2. Flat Gain Configuration Settings

Pin mode GAIN0/1	I²C Modeflat_gain_2:0	Flat Gain
L0	0	-6 dB
L1	1	-4 dB
L2	3	-2 dB
L4 (float)	5	0 dB (default recommendation)
L3	7	+2 dB

7.3.3 Receiver Detect State Machine

The DS320PR810 deploys an Rx detect state machine that governs the Rx detection cycle as defined in the PCI express specifications. At power up or after a manual PD0/1 toggle the redriver determines whether or not a valid PCI express termination is present at the far end receiver. The RX_DET pin of DS320PR810 provides additional flexibility for system designers to appropriately set the device in desired mode as provided in 表 7-3. PD0 and PD1 pins impact channel groups 0-3 and 4-7 respectively. If all eight channels of DS320PR810 is used for a same PCI express link, then the PD1 and PD0 pins can be shorted and driven together. For most applications the RX_DET pin can be left floating for default settings. In SMBus/I²C mode each channel can be configured independently.

表 7-3. Receiver Detect State Machine Settings

PD0	PD1	RX_DET	Channels 0-3 Rx Common-mode Impedance	Channels 4-7 Rx Common-mode Impedance	COMMENTS
L	L	L0	Always 50 Ω	Always 50 Ω	PCI Express Rx detection state machine is disabled. Recommended for non PCIe interface use case where the DS320PR810 is used as buffer with equalization.
L	L	L1	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 3 consecutive valid detections
L	L	L2	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Outputs polls until 2 consecutive valid detections
L	L	L3	NA	NA	Reserved
L	L	L4 (Float)	Pre Detect: Hi-Z Post Detect: 50 Ω.	Pre Detect: Hi-Z Post Detect: 50 Ω.	Tx polls every ≅150 µs until valid termination is detected. Rx CM impedance held at Hi-Z until detection Reset by asserting PD0/1 high for 200 µs then low.
H	L	X	Hi-Z	Pre Detect: Hi-Z Post Detect: 50 Ω.	Reset Channels 0-3 signal path and set their Rx impedance to Hi-Z
L	H	X	Pre Detect: Hi-Z Post Detect: 50 Ω.	Hi-Z	Reset Channels 4-7 signal path and set their Rx impedance to Hi-Z.
H	H	X	Hi-Z	Hi-Z	

In PCIe applications PD0/1 pins can be connected to PCIe sideband signals PERST# with inverted polarity or one or more appropriate PRSNTx# signals to achieve desired RX detect functionality.

7.4 Device Functional Modes

7.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled by RX_DET = L1/L2/L4. In this mode PD0 and PD1 pins are driven low in a system (for example, by PCIE connector *PRSNTx#* or fundamental reset *PERST#* signal). In this mode, the DS320PR810 redrives and equalizes PCIe Rx or Tx signals to provide better signal integrity.

7.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled by RX_DET = L0. This mode is recommended for non-PCIe use cases. In this mode the device is working as a buffer to provide linear equalization to improve signal integrity.

7.4.3 Standby Mode

The device is in standby mode invoked by PD1,0 = H. In this mode, the device is in standby mode conserving power.

7.5 Programming

7.5.1 Pin mode

The DS320PR810 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 5-level pins for device control and signal integrity optimum settings.

7.5.1.1 Five-Level Control Inputs

The DS320PR810 has eight (EQ0_0, EQ1_0, EQ0_1, EQ1_1, GAIN0, GAIN1, MODE, and RX_DET) 5-level input pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The EQ0_0, EQ1_0, EQ0_1, EQ1_1, GAIN0, GAIN1, and RX_DET pins are sampled at power-up only. The MODE pin can be exercised at device power up or in normal operation mode.

表 7-4. 5-level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	F (Float)

7.5.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus/I²C Secondary control mode), then the DS320PR810 is configured through a standard I²C or SMBus interface that may operate up to 400 kHz. The secondary address of the DS320PR810 is determined by the pin strap settings on the ADDR1 and ADDR0 pins. Note: secondary addresses to access channels 0-3 (Bank 0) and channels 4-7 (Bank 1) are different. Channel Bank 1 has address which is Channel Bank 0 address +1. The sixteen possible secondary addresses for each channel bank of the DS320PR810 are provided in 表 7-5. In SMBus/I²C modes the SCL and SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

表 7-5. SMBUS/I2C Secondary Address Settings

ADDR1	ADDR0	7-bit Secondary Address Channels 0-3 (Bank 0)	7-bit Secondary Address Channels 4-7 (Bank 1)
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L0	L4	Reserved	Reserved
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27

表 7-5. SMBUS/I2C Secondary Address Settings (continued)

ADDR1	ADDR0	7-bit Secondary Address Channels 0-3 (Bank 0)	7-bit Secondary Address Channels 4-7 (Bank 1)
L1	L4	Reserved	Reserved
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L2	L4	Reserved	Reserved
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37
L3	L4	Reserved	Reserved

The DS320PR810 has two types of registers:

- **Shared Registers:** these registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers:** these registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group through broadcast writes to Bank 0 or Bank 1.

The DS320PR810 features two banks of channels, Bank 0 (Channels 0-3) and Bank 1 (Channels 4-7), each featuring a separate register set and requiring a unique SMBus secondary address.

Channel Registers Base Address	Channel Bank 0 Access	Channel Bank 1 Access
0x00	Channel 0 registers	Channel 4 registers
0x20	Channel 1 registers	Channel 5 registers
0x40	Channel 2 registers	Channel 6 registers
0x60	Channel 3 registers	Channel 7 registers
0x80	Broadcast write channel Bank 0 registers, read channel 0 registers	Broadcast write channel Bank 1 registers, read channel 4 registers
0xA0	Broadcast write channel 0-1 registers, read channel 0 registers	Broadcast write channel 4-5 registers, read channel 4 registers
0xC0	Broadcast write channel 2-3 registers, read channel 2 registers	Broadcast write channel 6-7 registers, read channel 6 registers
0xE0	Bank 0 Share registers	Bank 1 Share registers

7.5.2.1 Shared Registers

表 7-6. General Registers (Offset = 0xE2)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device reset control: Reset all I^2C registers to default values (self-clearing).
5	rst_i2c_mas	R/W/SC	0x0	Reset I^2C Primary (self-clearing).
4-1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM configuration load.

表 7-7. EEPROM_Status Register (Offset = 0xE3)

Bit	Field	Type	Reset	Description
7	eecfg_cmplt	R	0x0	EEPROM load complete.
6	eecfg_fail	R	0x0	EEPROM load failed.
5	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image.
4	eecfg_atmpt_0	R	0x0	see MSB
3	eecfg_cmplt	R	0x0	EEPROM load complete 2.
2	eecfg_fail	R	0x0	EEPROM load failed 2.
1	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image 2.
0	eecfg_atmpt_0	R	0x0	see MSB

表 7-8. DEVICE_ID0 Register (Offset = 0xF0)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011
2	device_id0_2	R	0x1	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

表 7-9. *DEVICE_ID1 Register (Offset = 0xF1)*

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1001: DS320PR810
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x0	see MSB

7.5.2.2 Channel Registers

表 7-10. RX Detect Status Register (Channel register base + Offset = 0x00)

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	0x0	Rx Detect positive data pin status: 0: Not detected 1: Detected – the value is latched
6	rx_det_comp_n	R	0x0	Rx Detect negative data pin status: 0: Not detected 1: Detected – the value is latched
5-0	RESERVED	R	0x0	Reserved

表 7-11. EQ Gain Control Register (Channel register base + Offset = 0x01)

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled

表 7-11. EQ Gain Control Register (Channel register base + Offset = 0x01) (continued)

Bit	Field	Type	Reset	Description
6	eq_stage1_3	R/W	0x0	EQBoost stage 1 control See 表 7-1 for details
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost stage 2 control See 表 7-1 for details
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

表 7-12. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile See 表 7-1 for details
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat gain select: See 表 7-2 for details
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

表 7-13. RX Detect Control Register (Channel register base + Offset = 0x04)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2	mr_rx_det_man	R/W	0x0	Manual override of rx_detect_p/n decision: 0: rx detect state machine is enabled 1: rx detect state machine is overridden – always valid RX termination detected
1	en_rx_det_count	R/W	0x0	Enable additional RX detect polling 0: Additional RX detect polling disabled 1: Additional RX detect polling enabled
0	sel_rx_det_count	R/W	0x0	Select number of valid RX detect polls – gated by en_rx_det_count = 1 0: Device transmitters poll until 2 consecutive valid detections 1: Device transmitters poll until 3 consecutive valid detections

表 7-14. PD Override Register (Channel register base + Offset = 0x05)

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides thorugh SMBus/I^2C 0: Manual override disabled 1: Manual override enabled
6-0	device_en	R/W	0x111111	Manual power down of redriver various blocks – gated by device_en_override = 1 111111: All blocks are enabled 000000: All blocks are disabled

表 7-15. Bias Register (Channel register base + Offset = 0x06)

Bit	Field	Type	Reset	Description
5-3	Bias current	R/W	0x100	Control bias current Set 001 for best performance

表 7-15. Bias Register (Channel register base + Offset = 0x06) (continued)

Bit	Field	Type	Reset	Description
7,6,2-0	Reserved	R/W	0x00000	Reserved

7.5.3 SMBus/I²C Primary Mode Configuration (EEPROM Self Load)

The DS320PR810 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after the device's initial power-up. If the DS320PR810 is configured for SMBus Primary mode, then it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, the DS320PR810 becomes an SMBus primary and attempts to self-configure by reading the device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the DS320PR810 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C secondary operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I²C primary wants to access DS320PR810 registers, then it must support arbitration.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2 kb (256 × 8-bit) is recommended.
- Set MODE = L1, configure for SMBus Primary mode.
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 3.3 V supply
- In SMBus/I²C modes the SCL and SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

图 7-1 shows a use case with four DS320PR810 to implement a PCIe x16 configuration, but the user can cascade any number of DS320PR810 devices in a similar way. Tie the READ_EN_N pin of the first device low to automatically initiate EEPROM read at power up. Alternatively, the READ_EN_N pin of the first device can also be controlled by a micro-controller to initiate the EEPROM read manually. Leave the ALL_DONE_N pin of the final device floating, or connect the pin to a micro-controller input to monitor the completion of the final EEPROM read.

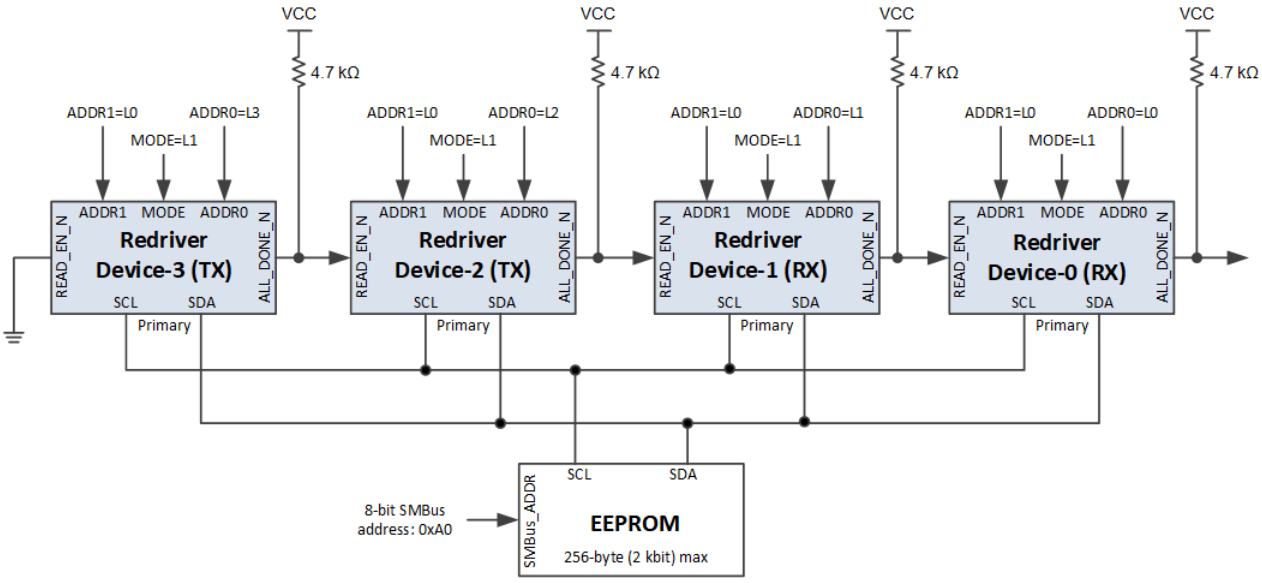


图 7-1. Daisy Chain Four DS320PR810 Devices to Read from Single EEPROM in x16 Configuration

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The DS320PR810 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The DS320PR810 is a PCI Express linear redriver that can also be configured as interface agnostic redriver by disabling its Rx detect feature. The device can be used in wide range of interfaces including:

- PCI Express 1.0, 2.0, 3.0, 4.0, and 5.0
- Ultra Path Interconnect (UPI) 1.0 and 2.0
- DisplayPort 2.0

The DS320PR810 is a protocol agnostic 8-channel 4-lane linear redriver with PCI Express receiver-detect capability. Its protocol agnostic nature allows it to be used in PCI Express x4, x8, and x16 applications. 图 8-1 shows how a number of DS320PR810 devices can be used to obtain signal conditioning for PCI Express buses of varying widths.

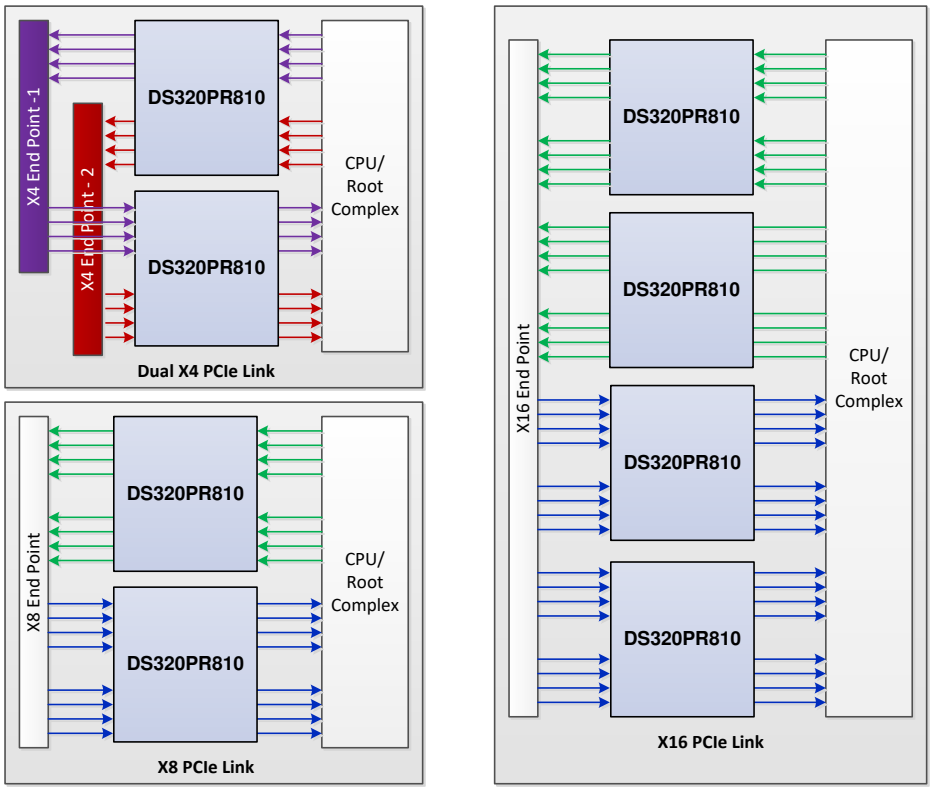


图 8-1. PCI Express x4, x8 and x16 Use Cases Using DS320PR 810

Note: all eight channels of the DS320PR810 flow in same direction. Therefore, if the device is used for dual x4 configuration with two devices, then PD0 of both devices need to be connected together to implement PCIe state machine for the first x4 link while PD1 for the second x4 link.

8.2.1 PCIe Reach Extension – x16 Lane Configuration

The DS320PR810 can be used in server or motherboard applications to boost transmit and receive signals to increase the reach of the host or root complex processor to PCI Express slots or connectors. The following sections outline detailed procedures and design requirements for a typical PCIe x16 lane configuration. However, the design recommendations can be used in any lane configuration.

8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near the receiver end of each channel segment to minimize reflections.
- For PCIe Gen 3.0, 4.0, and 5.0, AC-coupling capacitors of 220 nF are recommended. Set the maximum body size to 0402 and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

In PCIe Gen 3.0, 4.0, and 5.0 applications, the specification requires Rx-Tx (of root-complex and endpoint) link training to establish and optimize signal conditioning settings at 8 Gbps, 16 Gbps, and 32 Gbps, respectively. In link training, the Rx partner requests a series of FIR – preshoot and de-emphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels of CTLE followed by a single tap DFE. The link training would pre-condition the signal, with an equalized link between the root-complex and endpoint resulting an optimized link. Note that there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications.

For operation in Gen 3.0, 4.0, and 5.0 links, the DS320PR810 is designed with linear data-path to pass the Tx Preset signaling (by root complex and end point) onto the Rx (of root complex and end point) for the PCIe Gen 3.0, 4.0, or 5.0 link to train and optimize the equalization settings. The linear redriver DS320PR810 helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream Rx more easily. The device must be placed in between the Tx and Rx (of root complex and end point) such a way that both Rx and Tx signal swing stays within the linearity range of the device. Adjustments to the DS320PR810 EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The available EQ gain settings are provided in 表 7-1. For most PCIe systems the default flat gain setting 0 dB (GAIN = floating) would be sufficient. However, a flat gain attenuation can be utilized to apply extra equalization when needed to keep the data-path linear.

The DS320PR810 can be optimized for a given system utilizing its three configuration modes – Pin mode, SMBus/I^2C Primary mode, and SMBus/I^2C Secondary mode. In SMBus/I^2C modes the SCL and SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

In PCIe applications PD0/1 pins can be connected to PCIe sideband signals PERST# with inverted polarity or one or more appropriate PRSNTx# signals to achieve desired RX detect functionality.

图 8-2 shows a simplified schematic for x16 lane configuration in Pin mode.

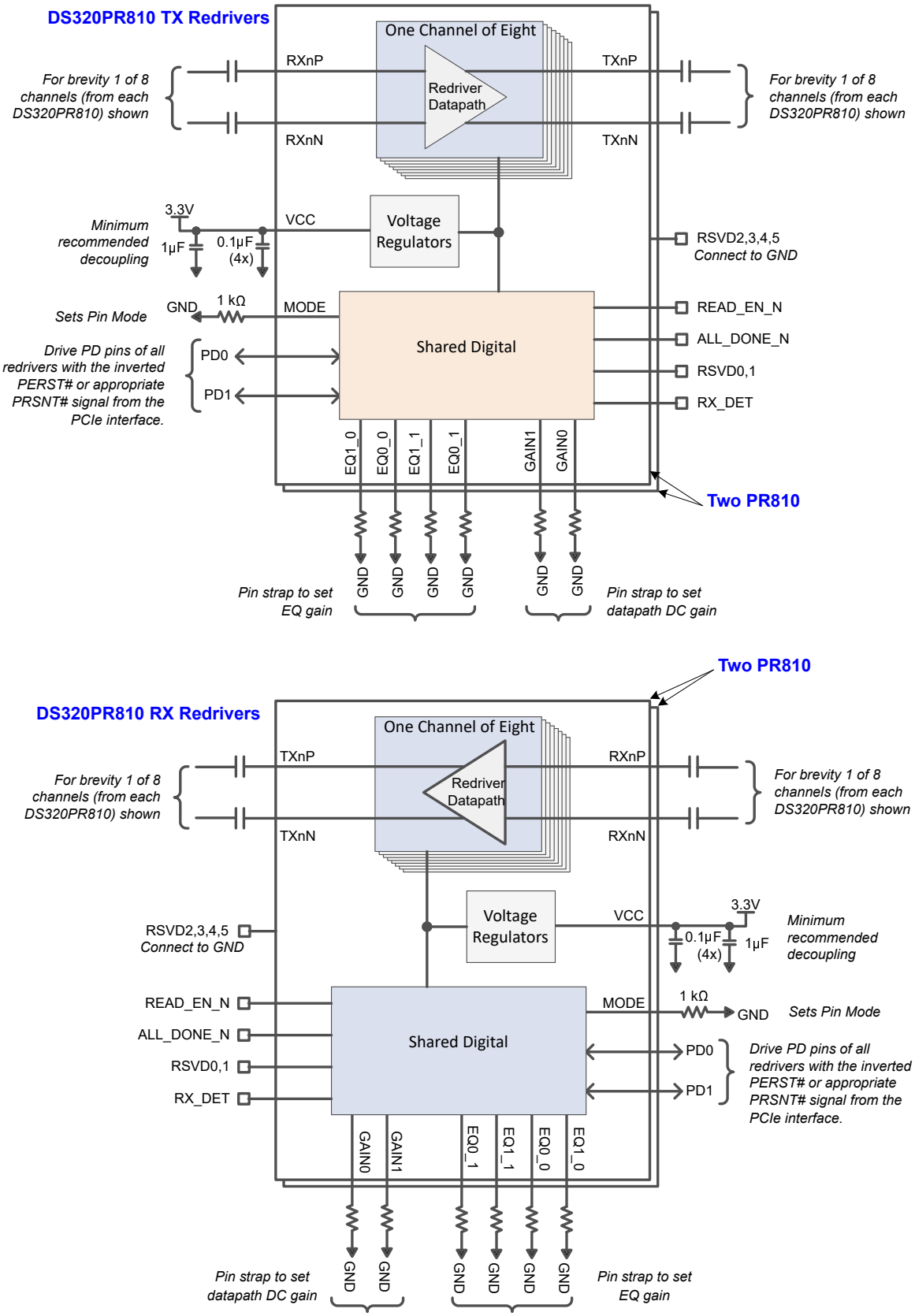


图 8-2. Simplified Schematic for PCIe x16 Lane Configuration in Pin mode

图 8-3 shows a simplified schematic for x16 lane configuration in SMBus/I2C Primary mode.

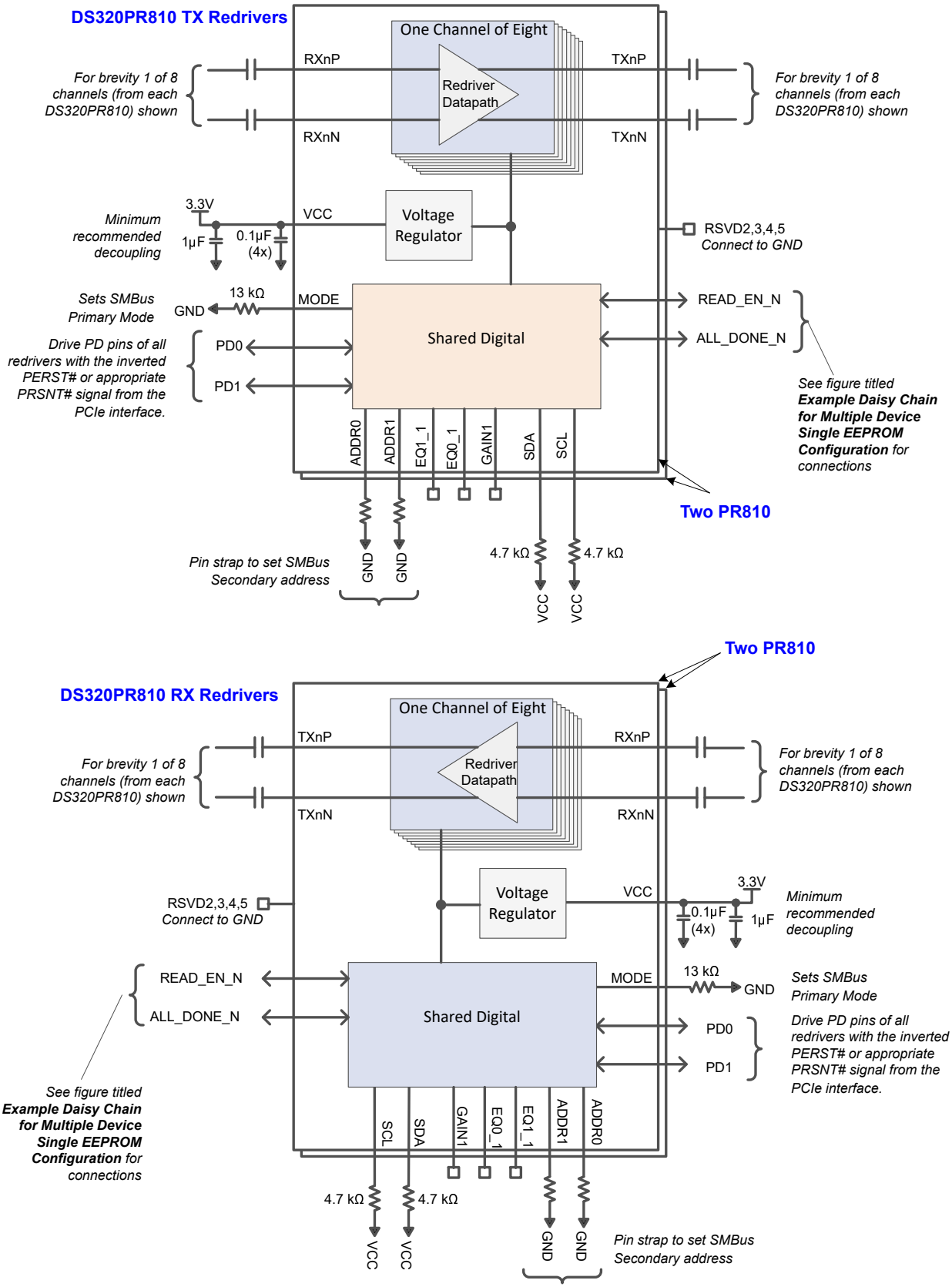


图 8-3. Simplified Schematic for PCIe x16 Lane Configuration in SMBus/I2C Primary mode

图 8-4 shows a simplified schematic for x16 lane configuration in SMBus/I²C Secondary mode.

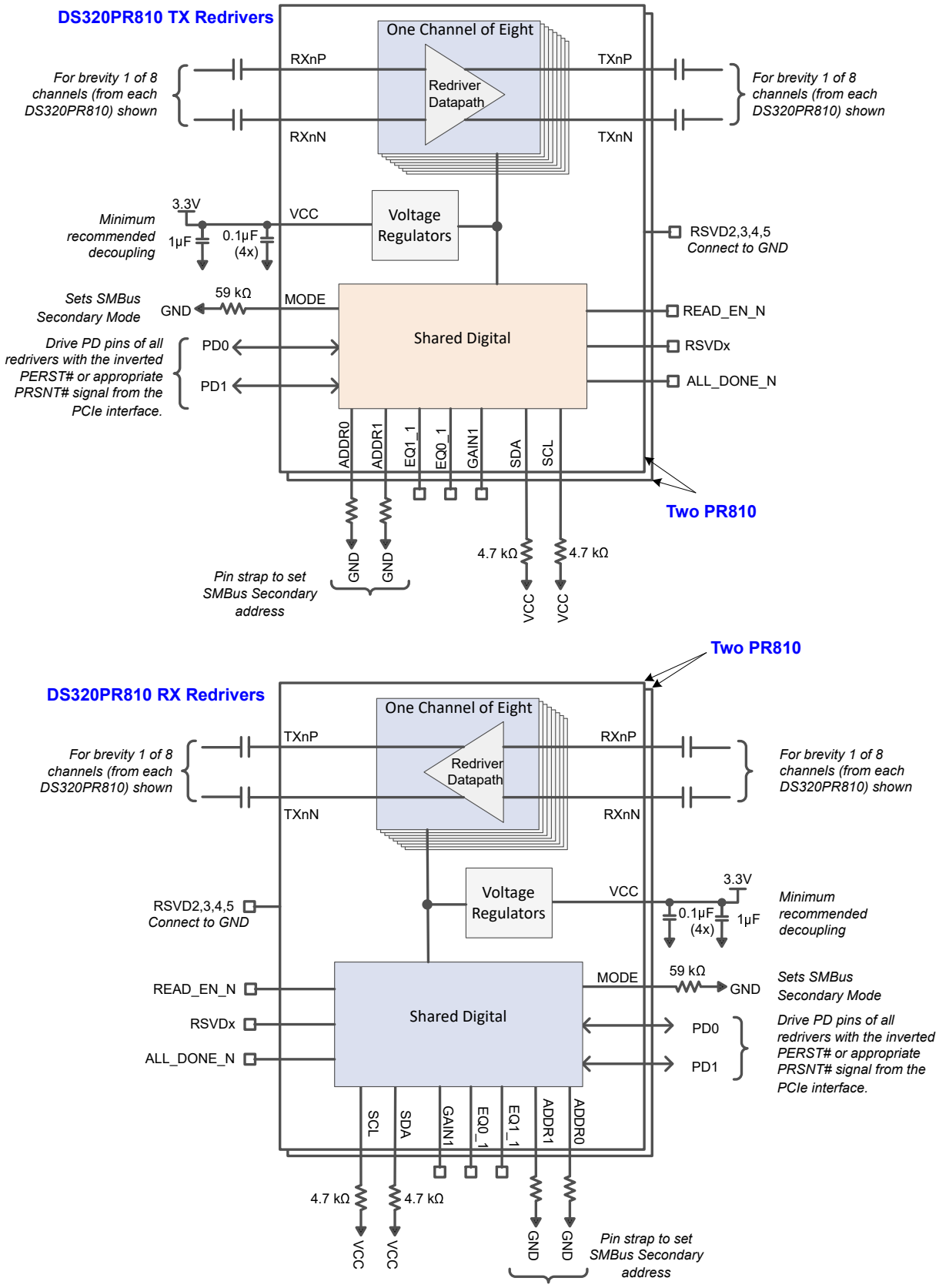


图 8-4. Simplified Schematic for PCIe x16 Lane Configuration in SMBus/I²C Secondary mode

8.2.1.3 Application Curves

The DS320PR810 is a linear redriver that can be used to extend channel reach of a PCIe link. Normally, PCIe-compliant Tx and Rx are equipped with signal-conditioning functions and can handle channel losses of up to 36 dB at 16 GHz. With the DS320PR810, the total channel loss between a PCIe root complex and an end point can be extended up to 58 dB at 16 GHz.

To demonstrate the reach extension capability of the DS320PR810, two comparative setups are constructed. In first setup as shown in 图 8-5 there is no redriver in the PCIe 5.0 link. 图 8-6 shows eye diagram at the end of the link using SigTest. In second setup as shown in 图 8-7, the DS320PR810 is inserted in the middle to extend link reach. 图 8-8 shows SigTest eye diagram.

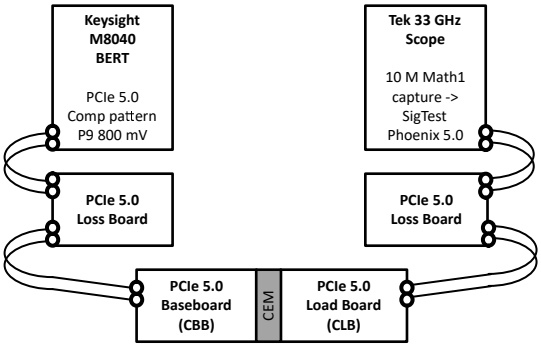


图 8-5. PCIe 5.0 Link Baseline Setup Without Redriver the Link Elements

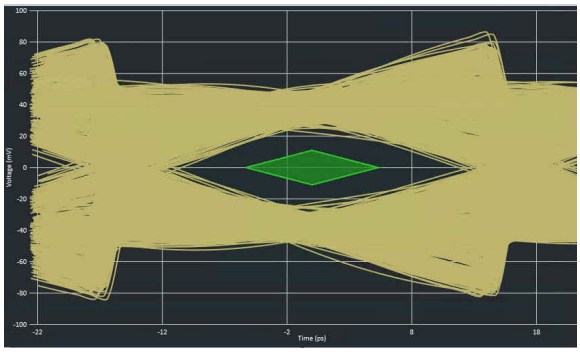


图 8-6. PCIe 5.0 link Baseline Setup Without Redriver Eye Diagram Using SigTest

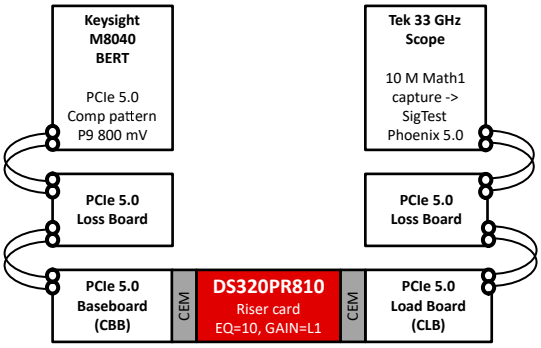


图 8-7. PCIe 5.0 Link Setup with the DS320PR810 the Link Elements

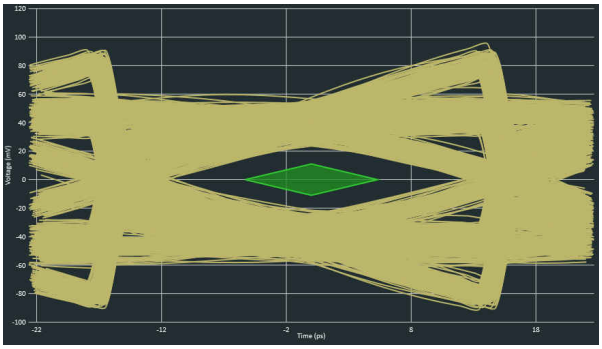


图 8-8. PCIe 5.0 Link Setup with the DS320PR810 Eye Diagram Using SigTest

表 8-1 summarizes the PCIe 5.0 links without and with the DS320PR810. The illustration shows that redriver is capable of ≅22 dB reach extension at PCIe 5.0 speed with EQ = 10 (EQ gain of 16 dB) and GAIN1,2 = L1 (flat gain of −4 dB). Note: actual reach extension depends on various signal integrity factors. It is recommended to run signal intergrity simulations with all the components in the link to get any guidance.

表 8-1. PCIe 5.0 Reach Extension using the DS320PR810

Setup	Pre Channel Loss	Post Channel Loss	Total Loss	Eye at BER 1E-12	SigTest Pass?
Baseline – no DUT	—	—	≅36 dB	14 ps, 41 mV	Pass
With DUT (DS320PR810)	≅29 dB	≅29 dB	≅58 dB	14 ps, 33 mV	Pass

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The DS320PR810 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 µF capacitor per VCC pin, one 1.0 µF bulk capacitor per device, and one 10 µF bulk capacitor per power bus that delivers power to one or more DS320PR810 devices. The local decoupling (0.1 µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the DS320PR810 ground pad.
3. The DS320PR810 voltage regulator output pins require decoupling caps of 0.1 µF near each pin. The regulator is only for internal use. Do not use to provide power to any external component.

10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

10.2 Layout Example

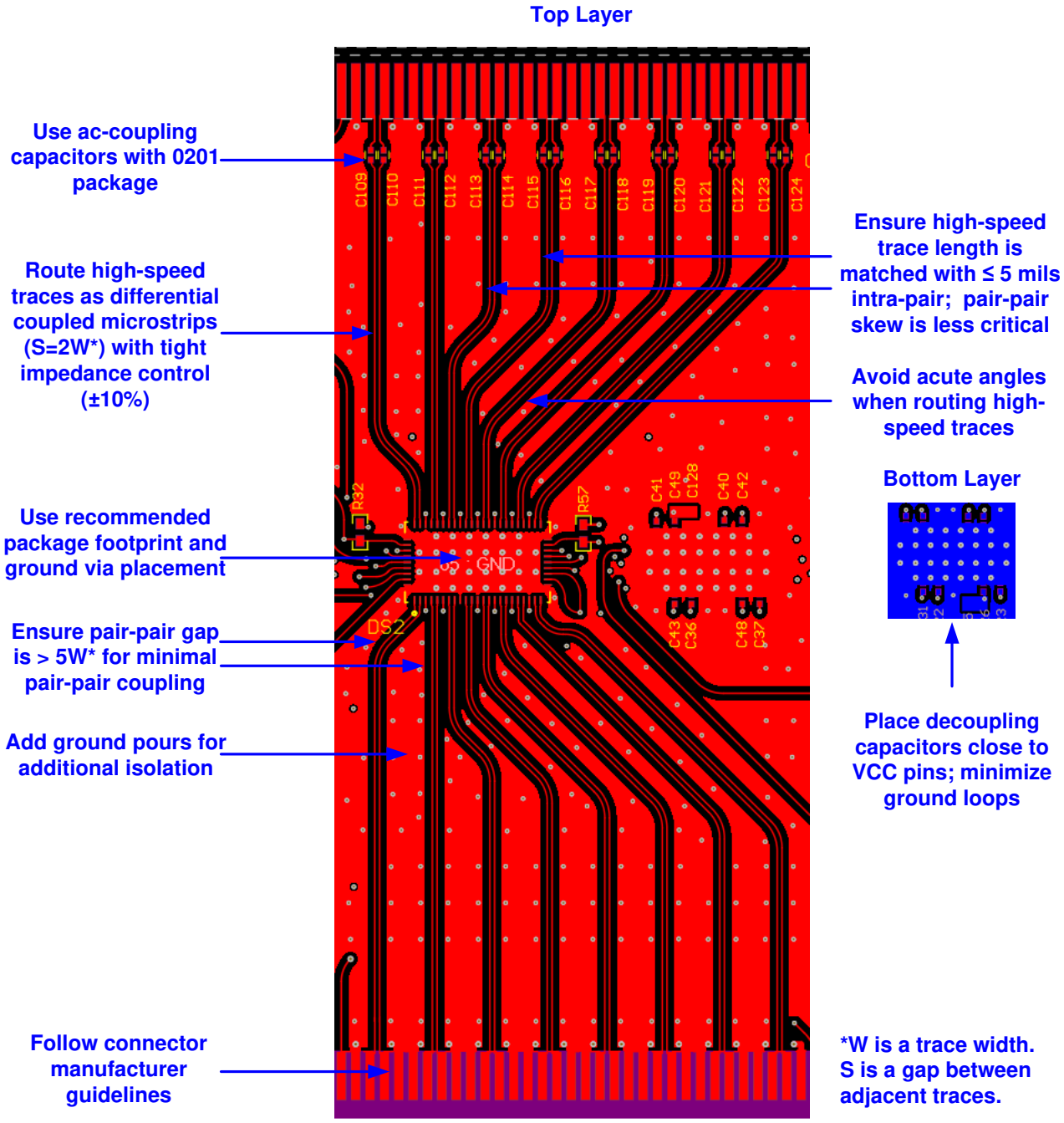


图 10-1. DS320PR810 Layout Example – Sub-Section of a PCIe Riser Card With CEM Connectors

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.3 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS320PR810NJXR	Active	Production	WQFN (NJX) | 64	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	5PR8
DS320PR810NJXT	Active	Production	WQFN (NJX) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	5PR8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

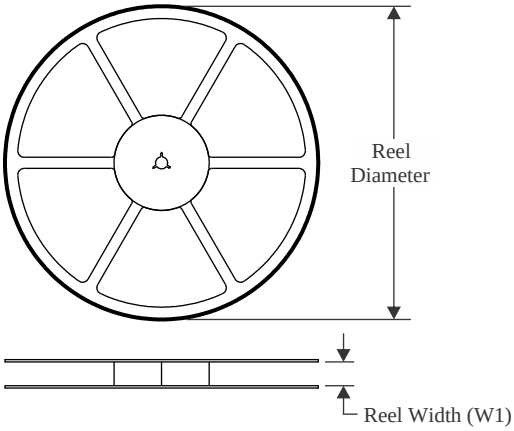
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

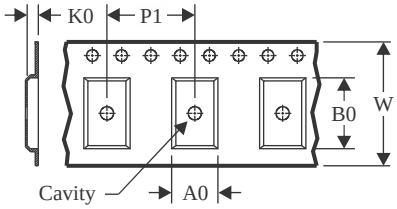
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

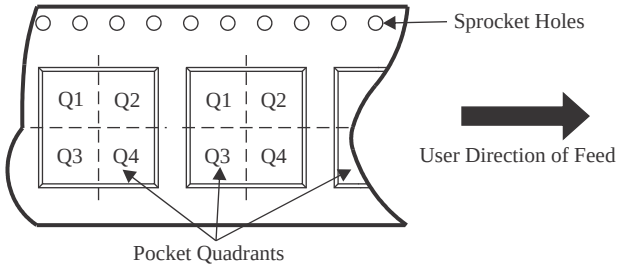


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

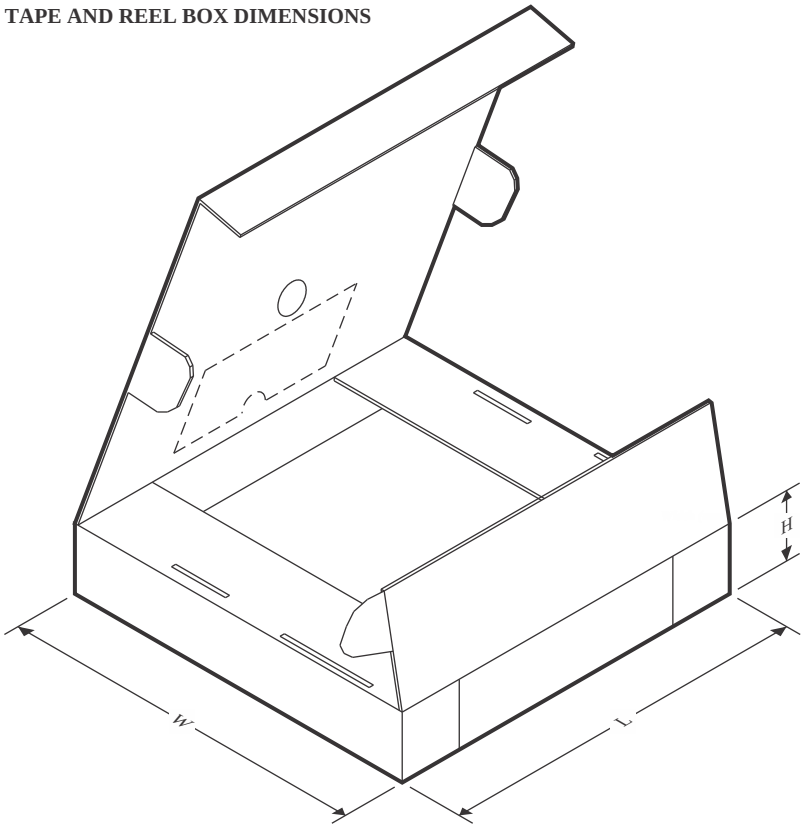
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS320PR810NJXR	WQFN	NJX	64	3000	330.0	16.4	5.8	10.3	1.2	12.0	16.0	Q1
DS320PR810NJXT	WQFN	NJX	64	250	180.0	16.4	5.8	10.3	1.2	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

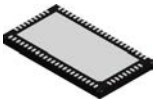


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS320PR810NJXR	WQFN	NJX	64	3000	367.0	367.0	35.0
DS320PR810NJXT	WQFN	NJX	64	250	210.0	185.0	35.0

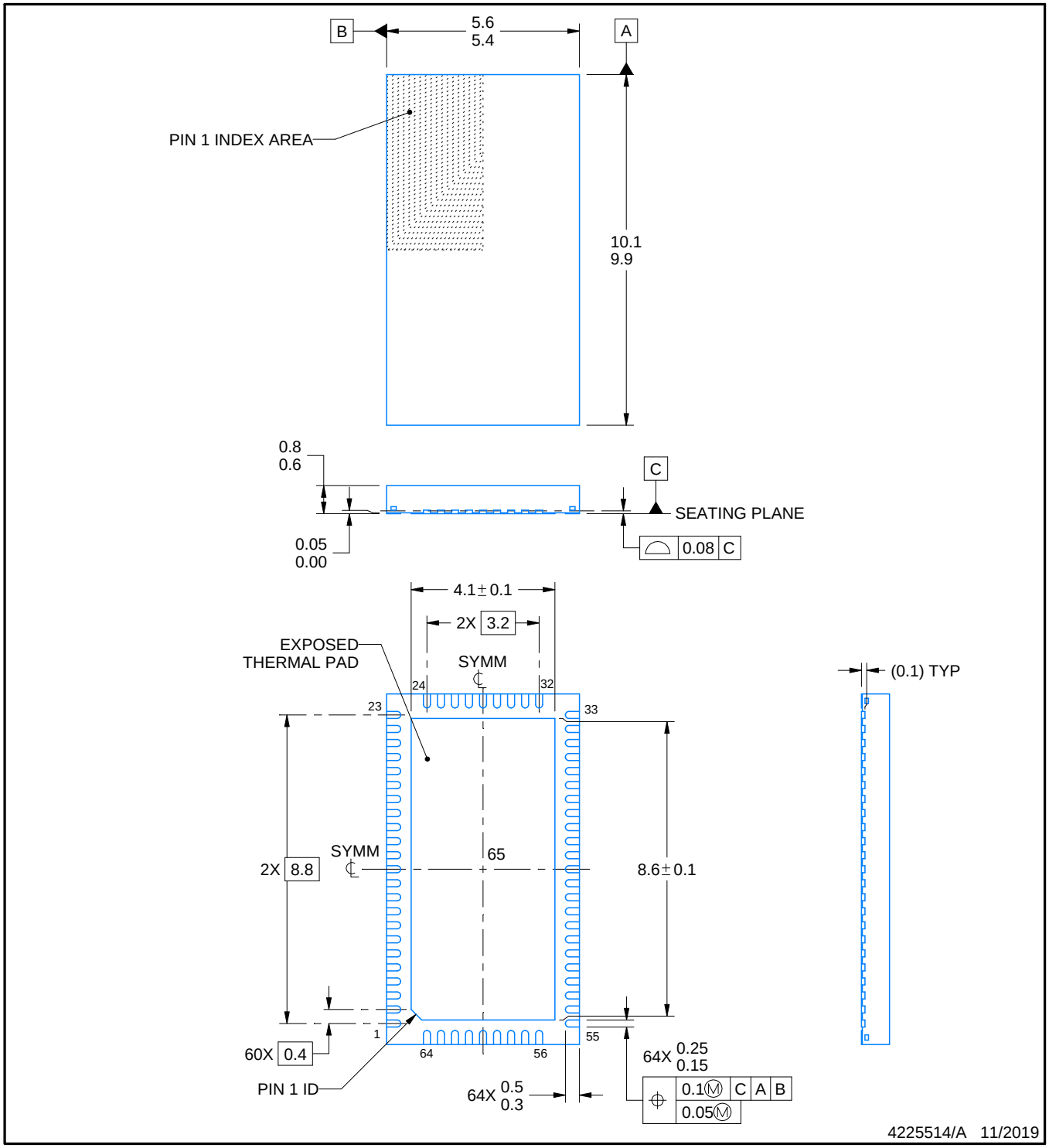
PACKAGE OUTLINE

NJX0064A



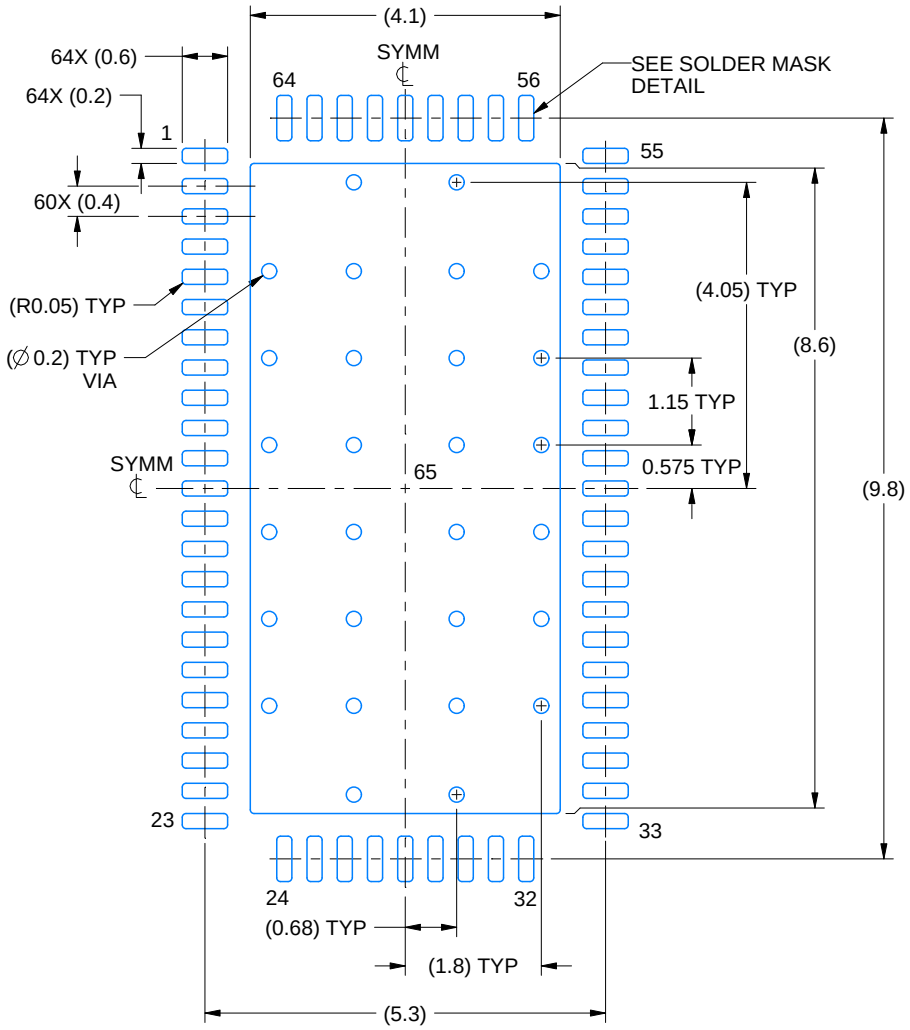
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

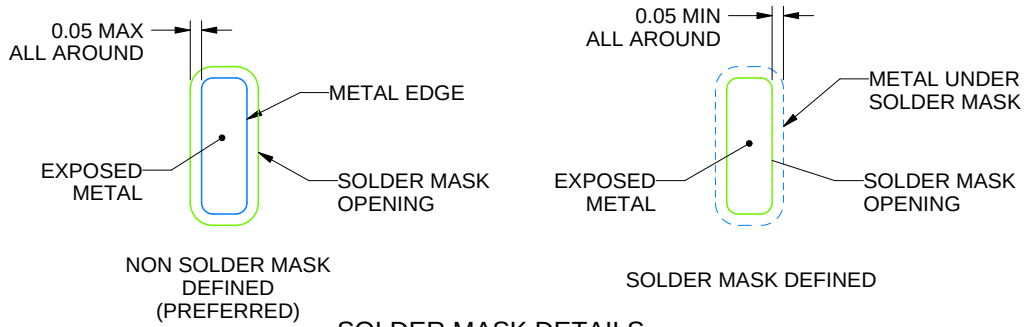


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

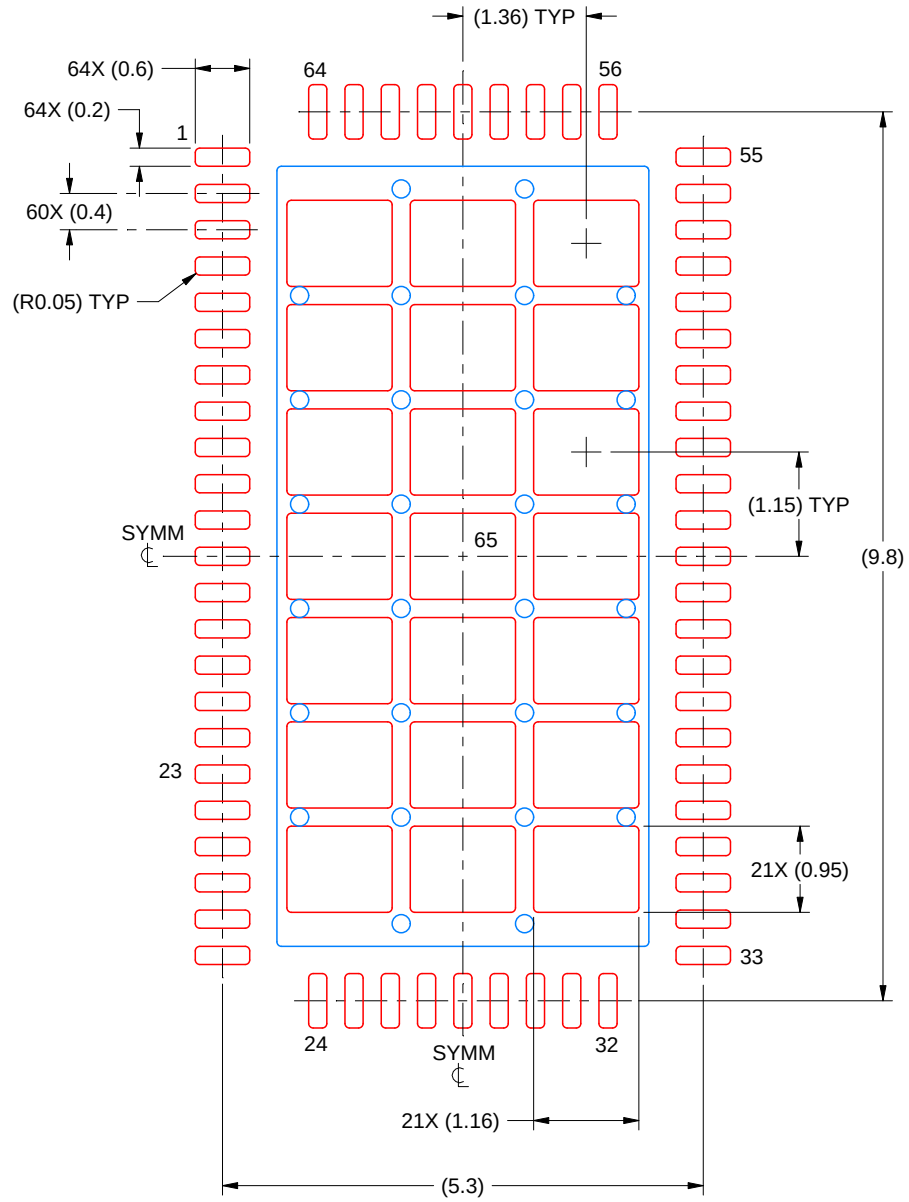


SOLDER MASK DETAILS

4225514/A 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 65
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225514/A 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月