DRV8824-Q1 汽车用电机控制器集成电路 (IC)

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级 1：-40°C 至 +125°C
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件充电器件模型 (CDM) ESD 分类等级 C4B
- 脉宽调制 (PWM) 微步进电机驱动器
  - 内置微步进分度器
  - 5 位绕组电流控制支持高达 32 个电流级
  - 低金属氧化物半导体场效应晶体管 (MOSFET) 导通电阻
- 24V，25°C 时 1.6A 最大驱动电流
- 内置 3.3V 基准输出
- 8.2V 至 45V 宽工作电源电压范围
- 耐热增强型带散热片超薄小外形尺寸 (HTSSOP) 表面贴装封装

2 应用范围

- 汽车制热、通风与空调控制 (HVAC)
- 汽车用阀门
- 车用信息娱乐

3 说明

DRV8824-Q1 为汽车应用提供一个集成电机驱动器解决方案。 此器件具有两个 H 桥驱动器和一个微步进分度器，并且专门用来驱动一个双极步进电机。 每个输出驱动器块包含被配置为全 H 桥的 N 通道功率 MOSFET，以驱动电机绕组。 DRV8824-Q1 能够驱动高达 1.6V 的输出电流（在 24V 和 25°C，具有适当散热时）。

一个简单的步进/方向接口可轻松连接到控制器电路。 端子可实现全步进到 1/32 步进模式的电机配置。 衰减模式可设定。

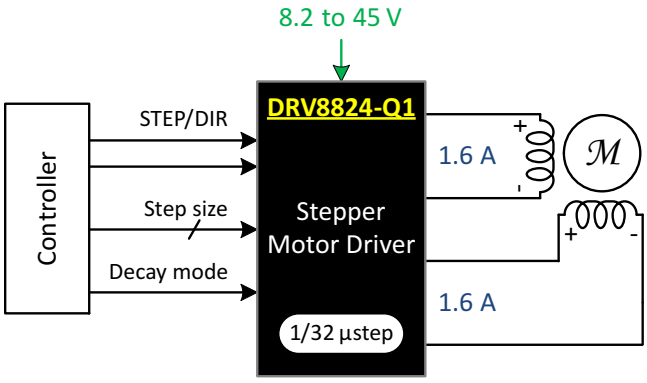
还提供用于过流保护、短路保护、欠压闭锁和过热保护的内部关断功能。

DRV8824-Q1 采用具有 PowerPAD™ 的 28 引脚 HTSSOP 封装（环保型：符合 RoHS 标准且不含铅/溴）。

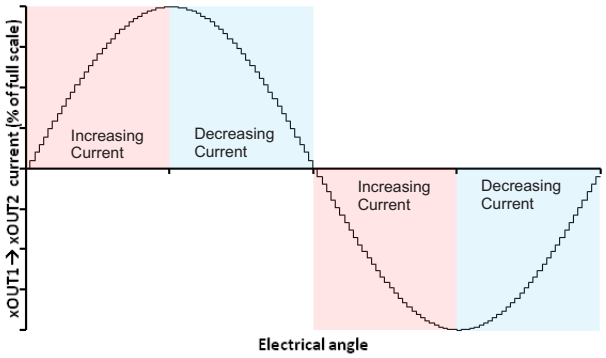
器件信息

订货编号	封装	封装尺寸
DRV8824QPWPRQ1	HTSSOP (28)	9.7mm x 4.4mm

4 简化电路原理图



微步进电流波形



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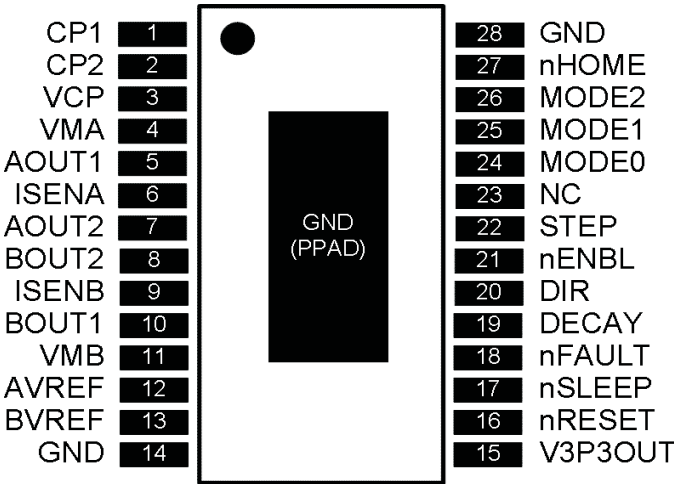
5 修订历史记录

日期	修订版本	注释
2014 年 4 月	*	最初发布。

6 Terminal Configuration and Functions

PWP Package
(Top View)



Terminal Functions

NAME	TERMINAL	I/O	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	14, 28	-	Device ground	
VMA	4	-	Bridge A power supply	Connect to motor supply (8.2 V - 45 V). Both terminals must be connected to same supply.
VMB	11	-	Bridge B power supply	
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor and a 1-MΩ resistor to VM.
CONTROL				
nENBL	21	I	Enable input	Logic high to disable device outputs and indexer operation, logic low to enable. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
STEP	22	I	Step input	Rising edge causes the indexer to move one step. Internal pulldown.
DIR	20	I	Direction input	Level sets the direction of stepping. Internal pulldown.
MODE0	24	I	Microstep mode 0	MODE0 - MODE2 set the step mode - full, 1/2, 1/4, 1/8/ 1/16, or 1/32 step. Internal pulldown.
MODE1	25	I	Microstep mode 1	
MODE2	26	I	Microstep mode 2	
DECAY	19	I	Decay mode	Low = slow decay, open = mixed decay, high = fast decay. Internal pulldown and pullup.
nRESET	16	I	Reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs. Internal pulldown.
AVREF	12	I	Bridge A current set reference input	Reference voltage for winding current set. Normally AVREF and BVREF are connected to the same voltage. Can be connected to V3P3OUT. A 0.01-µF bypass capacitor to GND is recommended.
BVREF	13	I	Bridge B current set reference input	
NC	23		No connect	Leave this terminal unconnected.
STATUS				
nHOME	27	OD	Home position	Logic low when at home state of step table
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)

Terminal Functions (continued)

NAME	TERMINAL	I/O	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
OUTPUT				
ISENA	6	IO	Bridge A ground / Isense	Connect to current sense resistor for bridge A.
ISENB	9	IO	Bridge B ground / Isense	Connect to current sense resistor for bridge B.
AOUT1	5	O	Bridge A output 1	Connect to bipolar stepper motor winding A. Positive current is AOUT1 → AOUT2
AOUT2	7	O	Bridge A output 2	
BOUT1	10	O	Bridge B output 1	Connect to bipolar stepper motor winding B. Positive current is BOUT1 → BOUT2
BOUT2	8	O	Bridge B output 2	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		VALUE	UNIT
VMx	Power supply voltage range	–0.3 to 47	V
	Digital terminal voltage range	–0.5 to 7	V
VREF	Input voltage	–0.3 to 4	V
	ISENSEx terminal voltage	–0.3 to 0.8	V
	Peak motor drive output current, t < 1 µS	Internally limited	A
	Continuous motor drive output current(3)	1.6	A
	Continuous total power dissipation	See Thermal Information table	
T_J	Operating virtual junction temperature range	–40 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–60	150	°C
V_{ESD}	HBD (human body model), AEC-Q100 Classification H2		2000	V
	CDM (charged device model), AEC-Q100 Classification C4B		750	

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage(1)	8.2		45	V
V_{REF}	VREF input voltage(2)	1		3.5	V
I_{V3P3}	V3P3OUT load current			1	mA

(1) All V_M terminals must be connected to the same supply voltage.
(2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

7.4 Thermal Information

THERMAL METRIC		DRV8824-Q1 PWP 28 TERMINAL	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(2)	23.3	
$R_{\theta JB}$	Junction-to-board thermal resistance(3)	21.2	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.8	
ψ_{JB}	Junction-to-board characterization parameter(5)	20.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(6)	2.6	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over operating free-air temperature range of -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		10	20	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		7.8	8.2	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA, V_M = 24 V, T_J = 25°C	3.18	3.30	3.45	V
		IOUT = 0 to 1 mA	3.10	3.30	3.50	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2		5.25	V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Internal pulldown resistance	nENBL, nRESET, DIR, STEP, MODEx		100		kΩ
		nSLEEP		1		MΩ
nHOME, nFAULT OUTPUTS (OPEN-DRAIN OUTPUTS)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay mode			0.8	V
V_{IH}	Input high threshold voltage	For fast decay mode	2			V
I_{IN}	Input current		–100		100	µA
R_{PU}	Internal pullup resistance			130		kΩ
R_{PD}	Internal pulldown resistance			80		kΩ

Electrical Characteristics (continued)

over operating free-air temperature range of -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.63		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.76	0.90	
		V_M = 24 V, I_O = 1 A, T_J = 125°C		0.85	1	
$R_{DS(ON)}$	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.65		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.78	0.90	
		V_M = 24 V, I_O = 1 A, T_J = 125°C		0.85	1	
I_{OFF}	Off-state leakage current		–20		20	µA
MOTOR DRIVER						
f_{PWM}	Internal PWM frequency			50		kHz
t_{BLANK}	Current sense blanking time			3.75		µs
t_R	Rise time	V_M = 24 V	100		360	ns
t_F	Fall time	V_M = 24 V	80		250	ns
t_{DEAD}	Dead time			400		ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.8		5	A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	xVREF input current	xVREF = 3.3 V	–3		3	µA
V_{TRIP}	xISENSE trip voltage	xVREF = 3.3 V, 100% current setting	635	660	685	mV
ΔI_{TRIP}	Current trip accuracy (relative to programmed value)	xVREF = 3.3 V , 5% current setting	–25%		25%	
		xVREF = 3.3 V , 10% - 34% current setting	–15%		15%	
		xVREF = 3.3 V, 38% - 67% current setting	–10%		10%	
		xVREF = 3.3 V, 71% - 100% current setting	–5%		5%	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

7.6 Timing Requirements

			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9		µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9		µs
4	$t_{SU(STEP)}$	Setup time, command to STEP rising	200		ns
5	$t_{H(STEP)}$	Hold time, command to STEP rising	200		ns
6	t_{ENBL}	Enable time, nENBL active to STEP	200		ns
7	t_{WAKE}	Wakeup time, nSLEEP inactive to STEP	1		ms

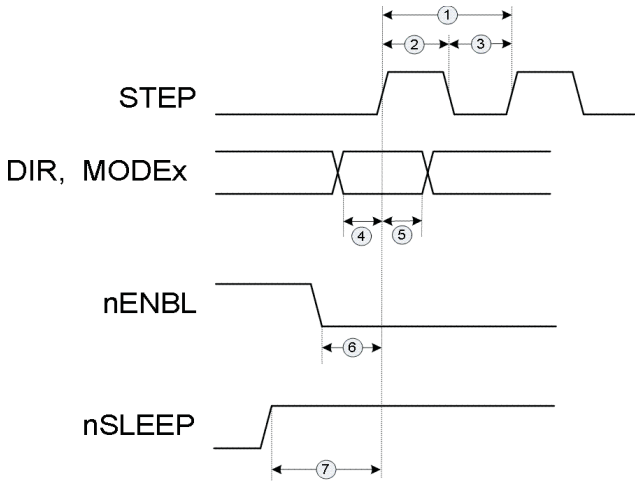


Figure 1. Timing Diagram

7.7 Typical Characteristics

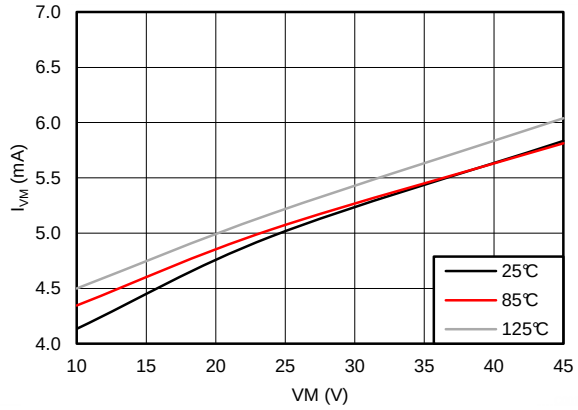


Figure 2. I_{VM} vs VM

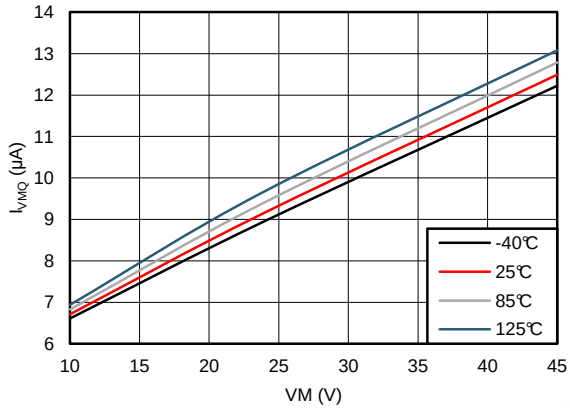


Figure 3. IVMQ vs VM

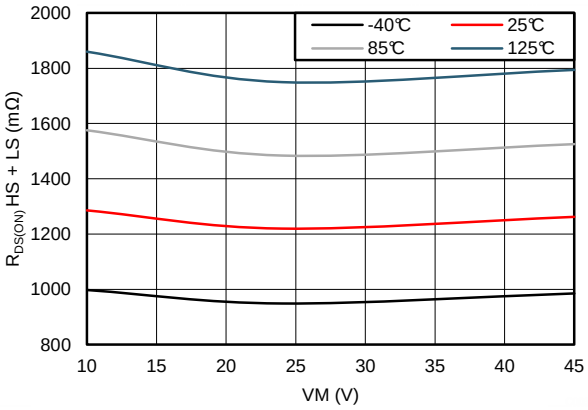


Figure 4. $R_{DS(ON)}$ vs VM

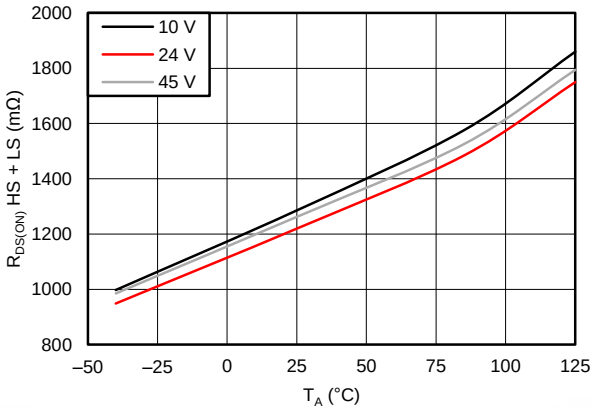


Figure 5. $R_{DS(ON)}$ vs Temperature

8 Detailed Description

8.1 Overview

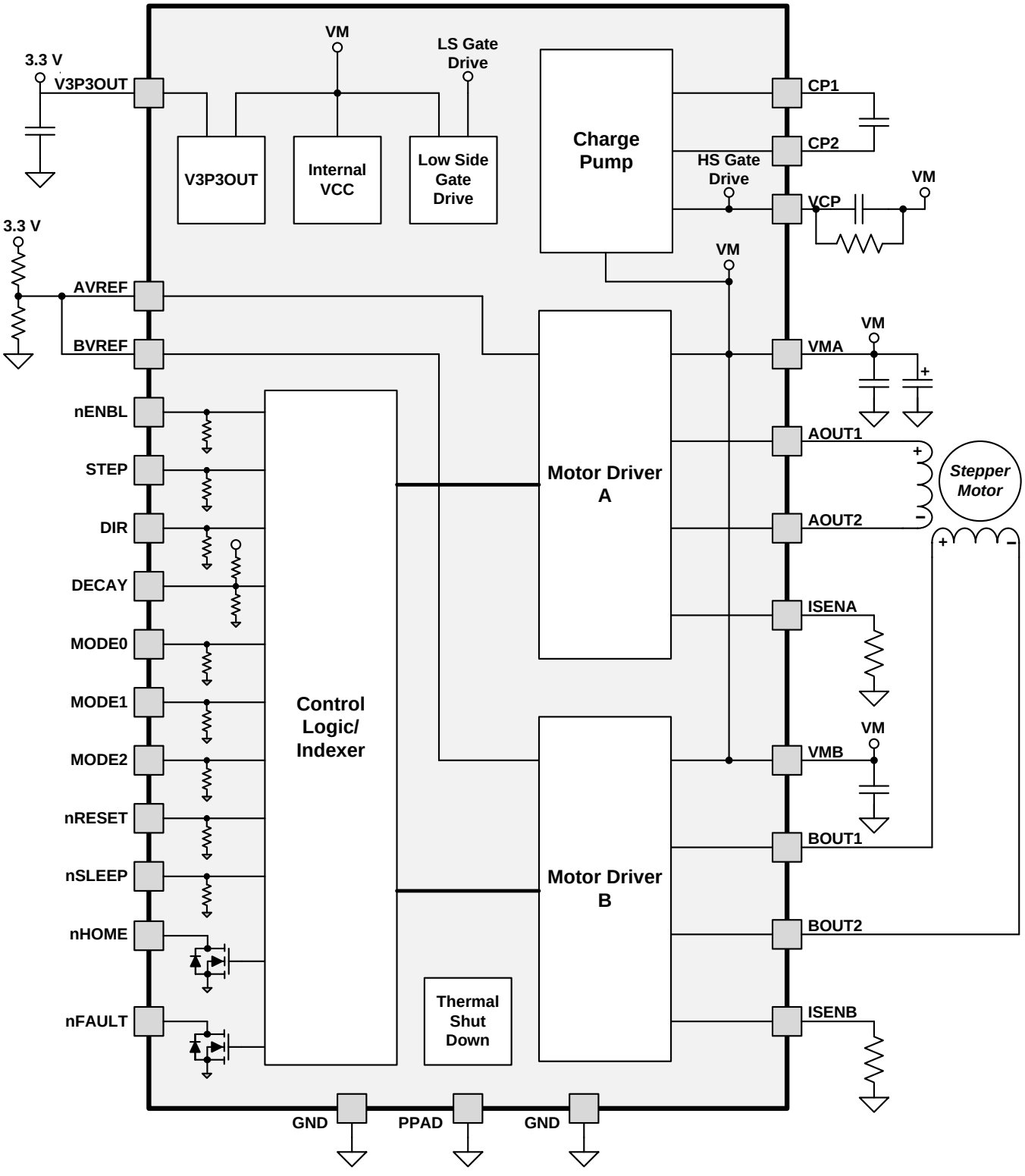
The DRV8824-Q1 is an integrated motor driver solution for bipolar stepper motors. The device integrates two NMOS H-bridges, current sense and regulation circuitry, and a microstepping indexer. The DRV8824-Q1 can be powered with a supply voltage between 8.2 V and 45 V, and is capable of providing an output current up to 1.6 A full-scale or 1.1 A rms.

A simple STEP/DIR interface allows easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level.

The current regulation is highly configurable, with three decay modes of operation. Fast, slow, and mixed decay can be used.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Motor Drivers

The DRV8824-Q1 contains two H-bridge motor drivers with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 6.

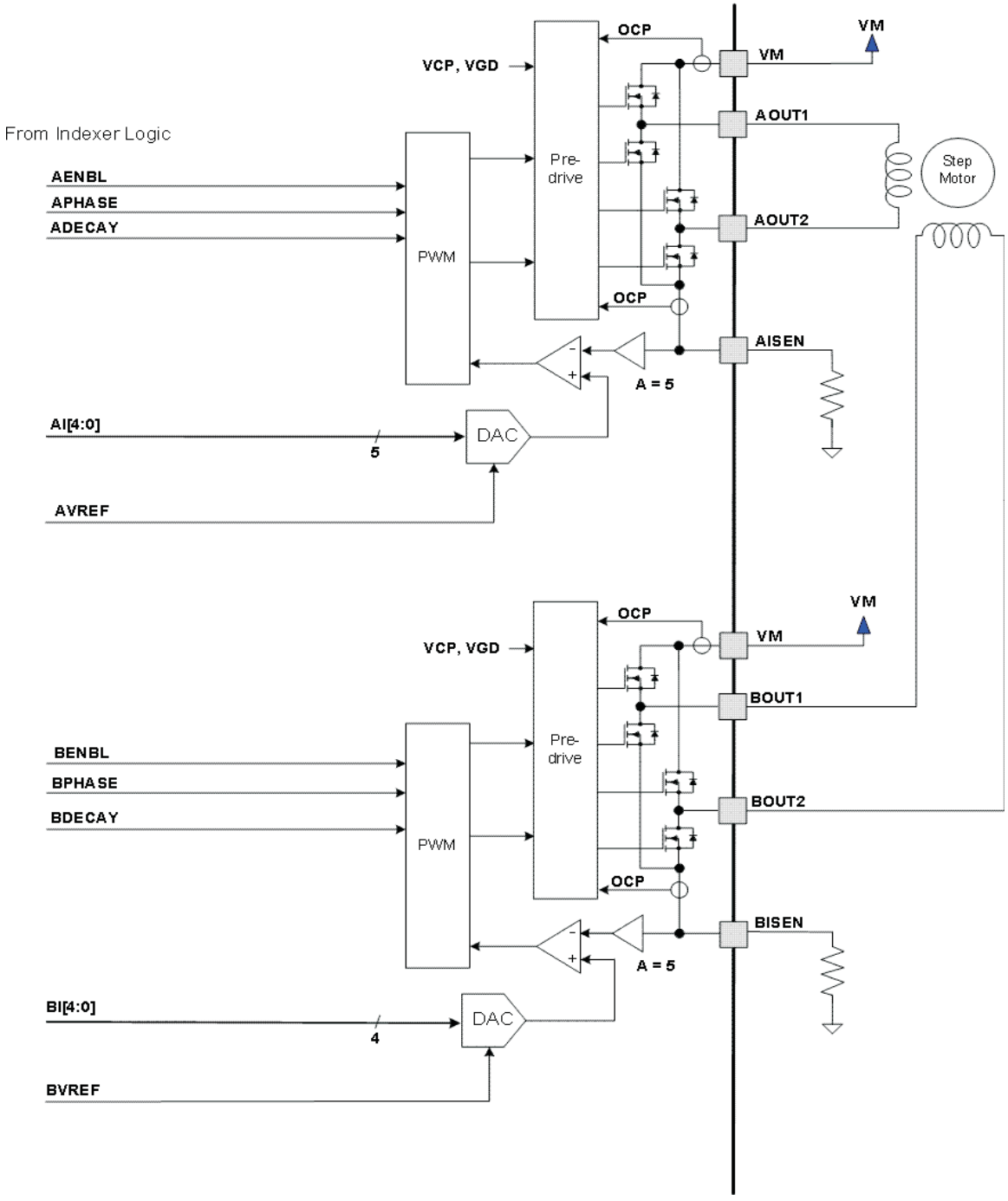


Figure 6. Motor Control Circuitry

Note that there are multiple VM motor power supply terminals. All VM terminals must be connected together to the motor supply voltage.

Feature Description (continued)

8.3.2 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

In stepping motors, current regulation is used to vary the current in the two windings in a semi-sinusoidal fashion to provide smooth motion.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN terminals, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF terminals.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx terminal is 3.3 V, the full-scale (100%) chopping current will be 3.3 V / (5 x 0.5 Ω) = 1.32 A.

The reference voltage is scaled by an internal DAC that allows fractional stepping of a bipolar stepper motor, as described in the microstepping indexer section below.

8.3.3 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN terminal is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

8.3.4 Microstepping Indexer

Built-in indexer logic in the DRV8824-Q1 allows a number of different stepping configurations. The MODE0 - MODE2 terminals are used to configure the stepping format as shown in .

Table 1. Stepping Format

MODE2	MODE1	MODE0	STEP MODE
0	0	0	Full step (2-phase excitation) with 71% current
0	0	1	1/2 step (1-2 phase excitation)
0	1	0	1/4 step (W1-2 phase excitation)
0	1	1	8 microsteps / step
1	0	0	16 microsteps / step
1	0	1	32 microsteps / step
1	1	0	32 microsteps / step
1	1	1	32 microsteps / step

Table 2 shows the relative current and step directions for different settings of MODEx. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR terminal high; if the DIR terminal is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that if the step mode is changed while stepping, the indexer will advance to the next valid state for the new MODEx setting at the rising edge of STEP.

The home state is 45°. This state is entered at power-up or application of nRESET. This is shown in Table 2 by the shaded cells. The logic inputs DIR, STEP, nRESET and MODEx have an internal pulldown resistors of 100 kΩ

Table 2. Relative Current and Step Directions

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
1	1	1	1	1		100%	0%	0
2						100%	5%	3
3	2					100%	10%	6
4						99%	15%	8
5	3	2				98%	20%	11
6						97%	24%	14
7	4					96%	29%	17
8						94%	34%	20
9	5	3	2			92%	38%	23
10						90%	43%	25
11	6					88%	47%	28
12						86%	51%	31
13	7	4				83%	56%	34
14						80%	60%	37
15	8					77%	63%	39
16						74%	67%	42
17	9	5	3	2	1	71%	71%	45
18						67%	74%	48
19	10					63%	77%	51
20						60%	80%	53
21	11	6				56%	83%	56
22						51%	86%	59
23	12					47%	88%	62
24						43%	90%	65
25	13	7	4			38%	92%	68
26						34%	94%	70
27	14					29%	96%	73
28						24%	97%	76
29	15	8				20%	98%	79
30						15%	99%	82
31	16					10%	100%	84
32						5%	100%	87
33	17	9	5	3		0%	100%	90
34						–5%	100%	93
35	18					–10%	100%	96
36						–15%	99%	98
37	19	10				–20%	98%	101
38						–24%	97%	104
39	20					–29%	96%	107
40						–34%	94%	110
41	21	11	6			–38%	92%	113
42						–43%	90%	115
43	22					–47%	88%	118
44						–51%	86%	121
45	23	12				–56%	83%	124
46						–60%	80%	127

Table 2. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
47	24					–63%	77%	129
48						–67%	74%	132
49	25	13	7	4	2	–71%	71%	135
50						–74%	67%	138
51	26					–77%	63%	141
52						–80%	60%	143
53	27	14				–83%	56%	146
54						–86%	51%	149
55	28					–88%	47%	152
56						–90%	43%	155
57	29	15	8			–92%	38%	158
58						–94%	34%	160
59	30					–96%	29%	163
60						–97%	24%	166
61	31	16				–98%	20%	169
62						–99%	15%	172
63	32					–100%	10%	174
64						–100%	5%	177
65	33	17	9	5		–100%	0%	180
66						–100%	–5%	183
67	34					–100%	–10%	186
68						–99%	–15%	188
69	35	18				–98%	–20%	191
70						–97%	–24%	194
71	36					–96%	–29%	197
72						–94%	–34%	200
73	37	19	10			–92%	–38%	203
74						–90%	–43%	205
75	38					–88%	–47%	208
76						–86%	–51%	211
77	39	20				–83%	–56%	214
78						–80%	–60%	217
79	40					–77%	–63%	219
80						–74%	–67%	222
81	41	21	11	6	3	–71%	–71%	225
82						–67%	–74%	228
83	42					–63%	–77%	231
84						–60%	–80%	233
85	43	22				–56%	–83%	236
86						–51%	–86%	239
87	44					–47%	–88%	242
88						–43%	–90%	245
89	45	23	12			–38%	–92%	248
90						–34%	–94%	250
91	46					–29%	–96%	253
92						–24%	–97%	256

Table 2. Relative Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
93	47	24				–20%	–98%	259
94						–15%	–99%	262
95	48					–10%	–100%	264
96						–5%	–100%	267
97	49	25	13	7		0%	–100%	270
98						5%	–100%	273
99	50					10%	–100%	276
100						15%	–99%	278
101	51	26				20%	–98%	281
102						24%	–97%	284
103	52					29%	–96%	287
104						34%	–94%	290
105	53	27	14			38%	–92%	293
106						43%	–90%	295
107	54					47%	–88%	298
108						51%	–86%	301
109	55	28				56%	–83%	304
110						60%	–80%	307
111	56					63%	–77%	309
112						67%	–74%	312
113	57	29	15	8	4	71%	–71%	315
114						74%	–67%	318
115	58					77%	–63%	321
116						80%	–60%	323
117	59	30				83%	–56%	326
118						86%	–51%	329
119	60					88%	–47%	332
120						90%	–43%	335
121	61	31	16			92%	–38%	338
122						94%	–34%	340
123	62					96%	–29%	343
124						97%	–24%	346
125	63	32				98%	–20%	349
126						99%	–15%	352
127	64					100%	–10%	354
128						100%	–5%	357

8.3.5 nRESET, nENBLE and nSLEEP Operation

The nRESET terminal, when driven active low, resets internal logic, and resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while nRESET is active.

The nENBL terminal is used to control the output drivers and enable/disable operation of the indexer. When nENBL is low, the output H-bridges are enabled, and rising edges on the STEP terminal are recognized. When nENBL is high, the H-bridges are disabled, the outputs are in a high-impedance state, and the STEP input is ignored.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before applying a STEP input, to allow the internal circuitry to stabilize.

The nRESET and nENABLE terminals have internal pulldown resistors of 100 kΩ. The nSLEEP terminal has an internal pulldown resistor of 1 MΩ.

8.3.6 Protection Circuits

The DRV8824-Q1 is fully protected against undervoltage, overcurrent and overtemperature events.

8.3.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT terminal will be driven low. The device will remain disabled until either nRESET terminal is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

8.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT terminal will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

8.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM terminals falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

8.3.7 Thermal Information

8.3.7.1 Thermal Protection

The DRV8824-Q1 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.3.7.2 Power Dissipation

Power dissipation in the DRV8824-Q1 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 2.

$$P_{TOT} = 4 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (2)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

8.3.7.3 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, "PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, "PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. It can be seen that the heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

8.4 Device Functional Modes

8.4.1 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7 as case 1. The current flow direction shown indicates positive current flow.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7 as case 3.

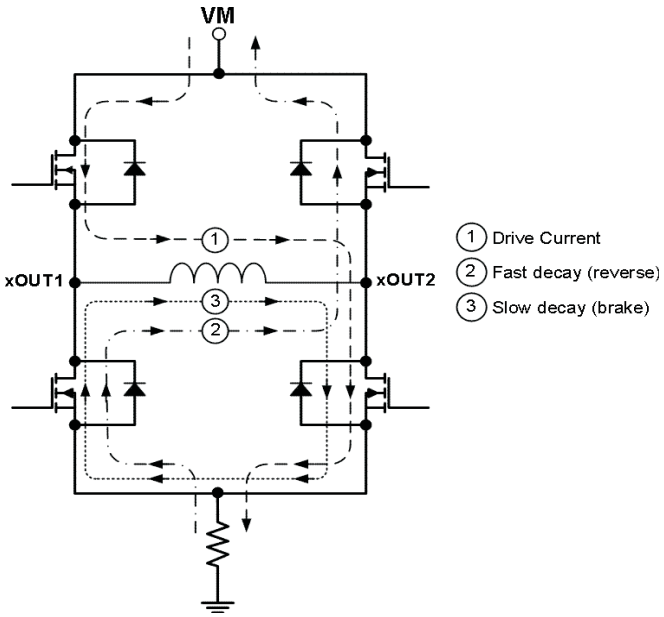


Figure 7. Decay Mode

The DRV8824-Q1 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY terminal - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY terminal has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the terminal is left open or undriven.

Device Functional Modes (continued)

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period. This occurs only if the current through the winding is decreasing (per the indexer step table); if the current is increasing, then slow decay is used.

9 Application and Implementation

9.1 Application Information

The DRV8824-Q1 is used in bipolar stepper control. The following design procedure can be used to configure the DRV8824-Q1.

9.2 Typical Application

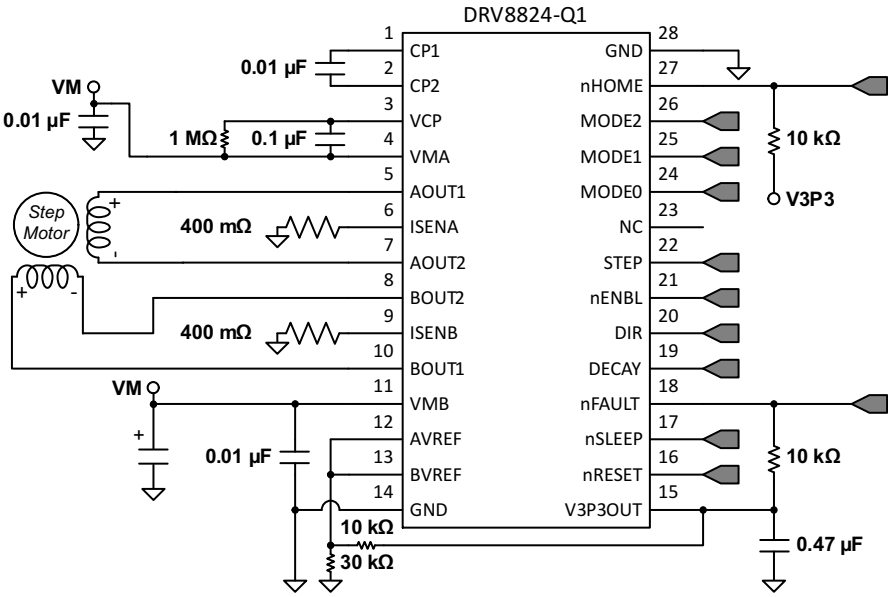


Figure 8. Typical Application Schematic

9.2.1 Design Requirements

Table 3 gives design input parameters for system design.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	1.0 Ω/phase
Motor winding inductance	L_L	3.5 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	8 microsteps per step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	1.25 A

9.2.2 Detailed Design Procedure

9.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8824-Q1 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}(step/sec) = \frac{v(rpm) \bullet n_m(steps) \bullet 6}{\theta_{step}(°/step)} \quad (3)$$

θ_{step} can be found in the stepper motor datasheet or written on the motor itself.

For the DRV8824-Q1, the microstepping level is set by the USM pins and can be any of the settings in . Higher microstepping will mean a smother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

9.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the VREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}(A) = \frac{VREF(V)}{A_v \bullet R_{SENSE}(\Omega)} = \frac{VREF(V)}{5 \bullet R_{SENSE}(\Omega)} \quad (4)$$

I_{FS} is set by a comparator which compares the voltage across R_{SENSE} to a reference voltage. There is a current sense amplifier built in with programmable gain through ISGAIN. Note that I_{FS} must also follow the equation below in order to avoid saturating the motor. VM is the motor supply voltage and R_L is the motor winding resistance.

$$I_{FS}(A) < \frac{VM(V)}{R_L(\Omega) + 2 \bullet R_{DS(ON)}(\Omega) + RSENSE(\Omega)} \quad (5)$$

9.2.2.3 Decay Modes

The DRV8824-Q1 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8824-Q1 will place the winding in one of the three decay modes until the PWM cycle has expired. Afterwards, a new drive phase starts.

The blanking time t_{BLANK} defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

9.2.3 Application Curves

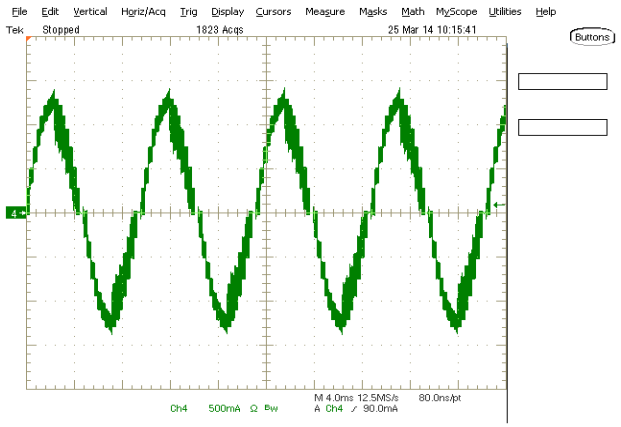


Figure 9. Microstepping Waveform, Phase A, Mixed Decay

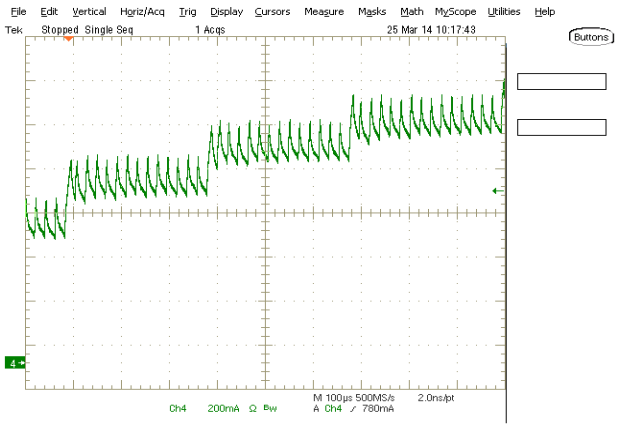


Figure 10. Microstepping Waveform, Slow Decay on Increasing Steps

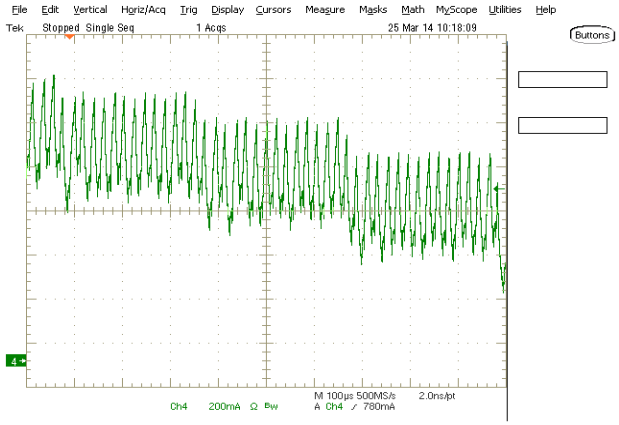


Figure 11. Microstepping Waveform, Mixed Decay on Decreasing Steps

10 Power Supply Recommendations

The DRV8824-Q1 is designed to operate from an input voltage supply (VM) range between 8.2 V and 45 V. Two 0.01-µF ceramic capacitorS rated for VMA and VMB must be placed as close to the DRV8824-Q1 as possible. In addition, a bulk capacitor must be included. If VMA and VMB are connected to the same board net, a single bulk capacitor is sufficient.

11 Layout

11.1 Layout Guidelines

The VMA and VMB terminals should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

The VMA and VMB pins must be bypassed to ground using a bulk capacitor. This component may be an electrolytic. If VMA and VMB are connected to the same board net, a single bulk capacitor is sufficient.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.01 µF rated for VMA and VMB is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. A value of 0.1 µF rated for 16 V is recommended. Place this component as close to the pins as possible. In addition place a 1-MΩ resistor between VCP and VMA.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

11.2 Layout Example

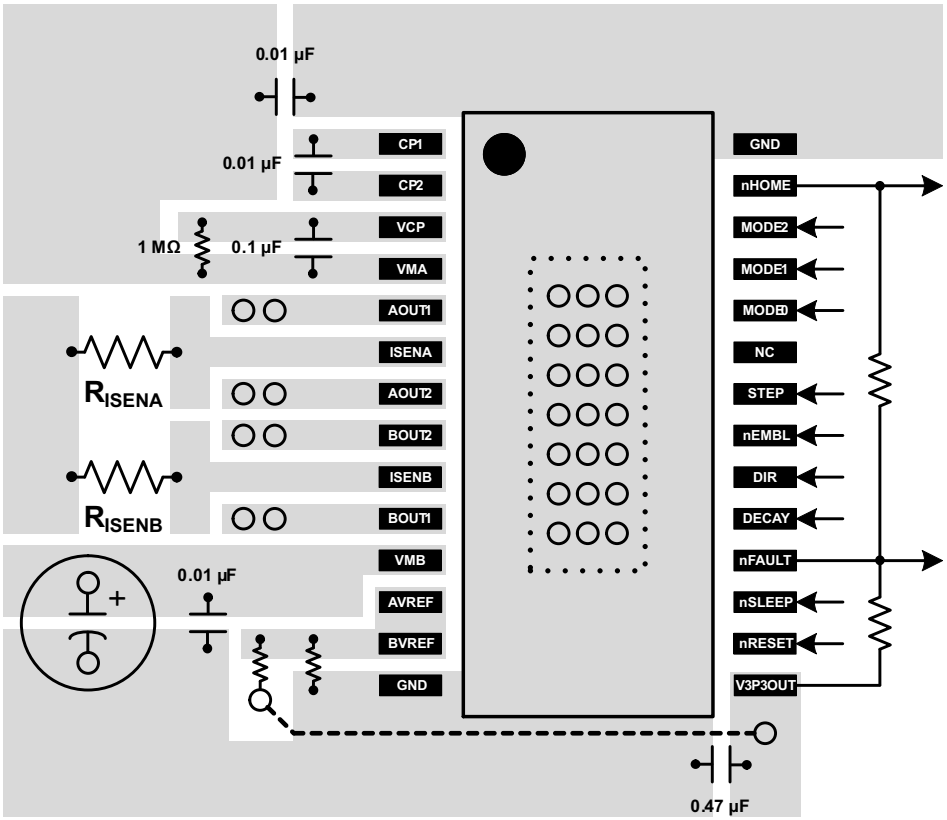


Figure 12. DRV8824-Q1 Board Layout

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8824QPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8824Q1
DRV8824QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8824Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DRV8824-Q1 :

- Catalog : DRV8824

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

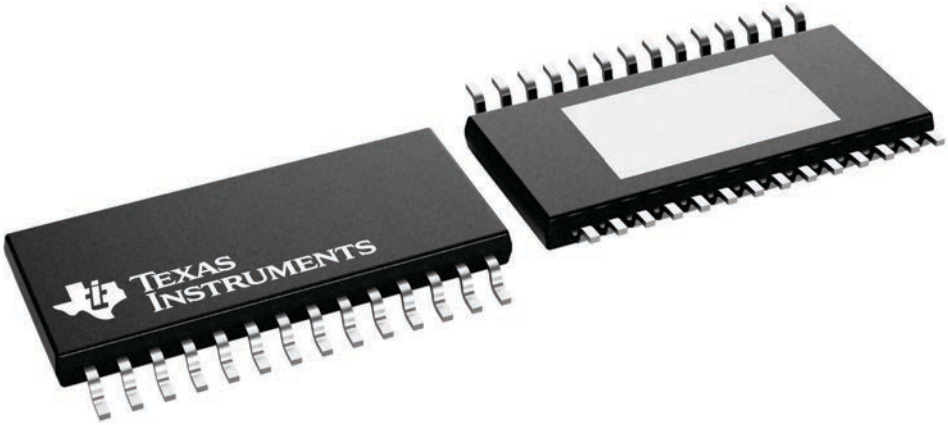
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

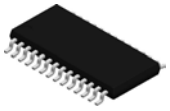
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

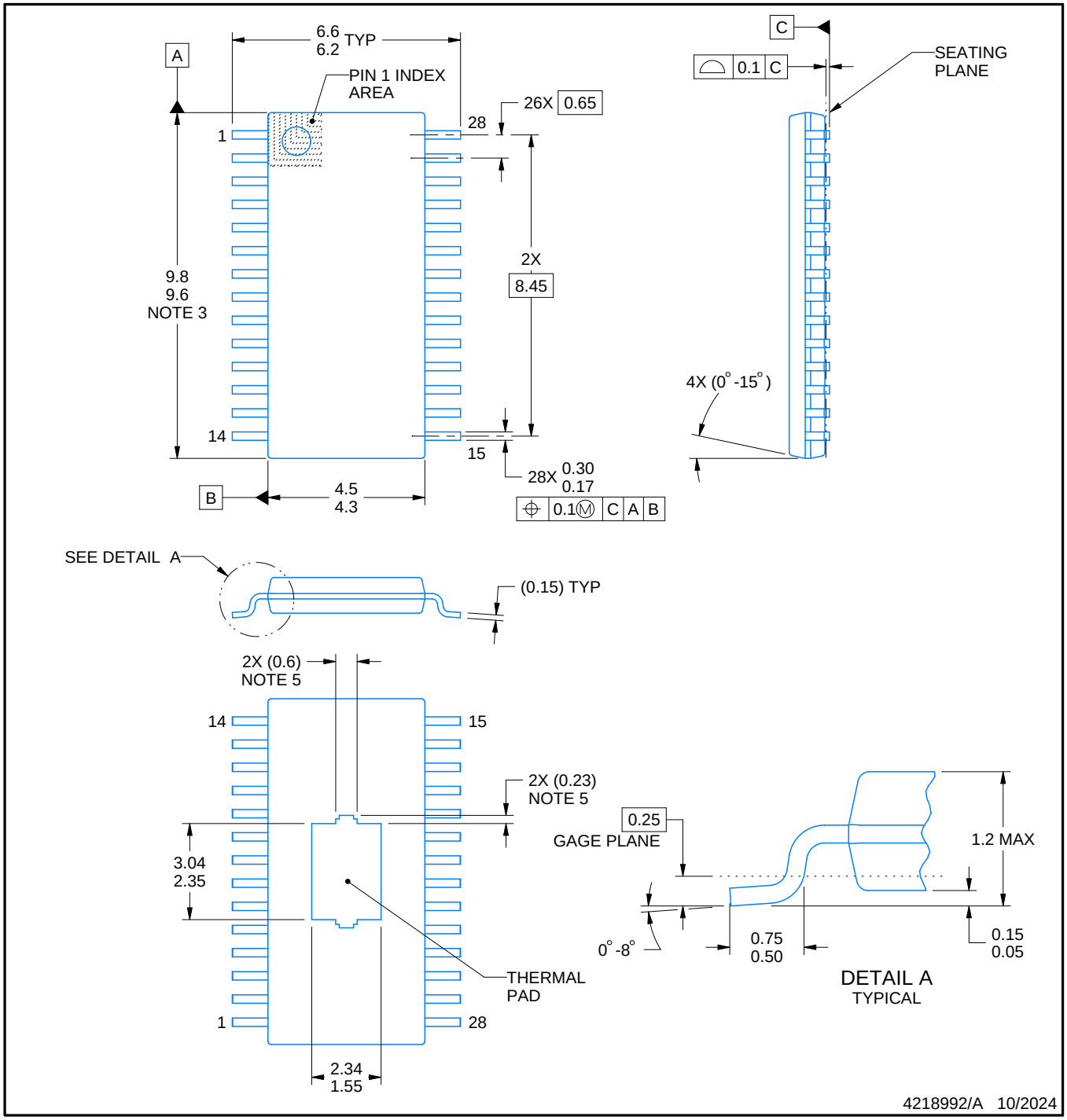
PACKAGE OUTLINE

PWP0028H



PowerPAD™ TSSOP - 1.2 mm max height

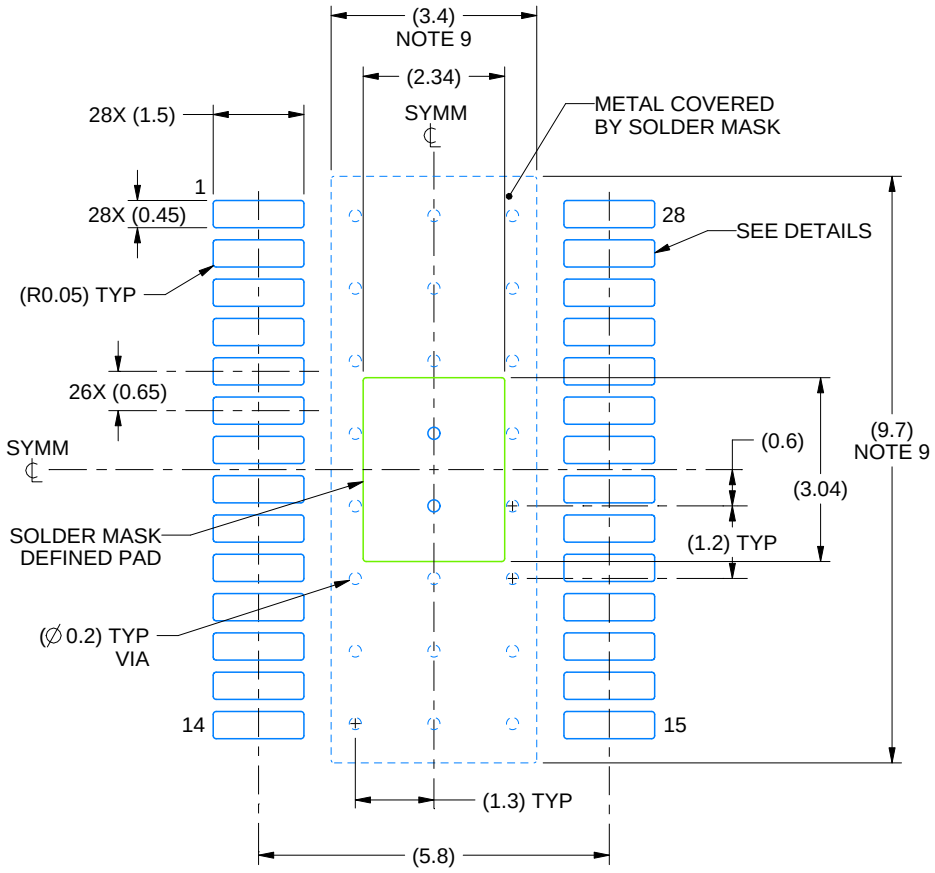
SMALL OUTLINE PACKAGE



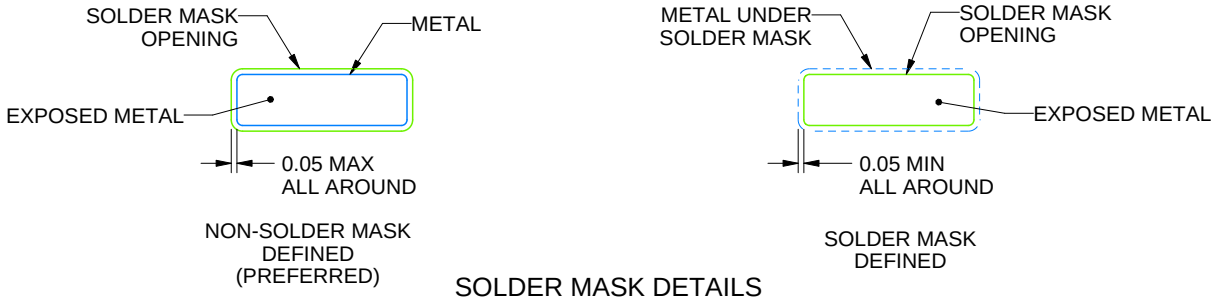
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

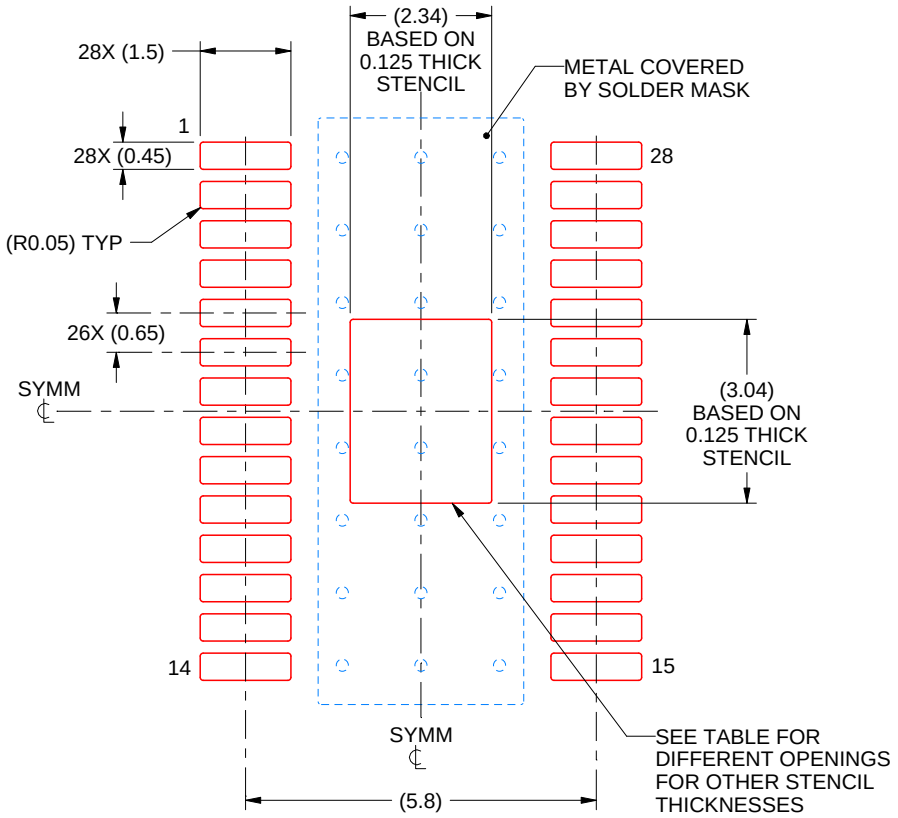


SOLDER MASK DETAILS

4218992/A 10/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

4218992/A 10/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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