

DRV8802 直流电机驱动器 IC

1 特性

- 8.2V 至 45V 宽工作电源电压范围
- 具有电流控制功能的双 H 桥电机驱动器
 - 驱动两个直流电机
 - 制动模式
 - 四级绕组电流控制
- 最大驱动电流为 1.6A (24V 且 T_A 为 25°C)
- 符合行业标准的并行数字控制接口
- 低电流休眠模式
- 内置 3.3V 基准输出
- 小型封装尺寸
- 保护 特性
 - 过流保护 (OCP)
 - 热关断 (TSD)
 - VM 欠压锁定 (UVLO)
 - 故障条件指示引脚 (nFAULT)
- 耐热增强型表面贴装封装

2 应用范围

- 打印机
- 扫描仪
- 办公自动化设备
- 游戏机
- 工厂自动化
- 机器人

3 说明

DRV8802 可为打印机、扫描仪以及其他自动化设备应用提供 集成电机驱动器解决方案。。此器件具有两个 H 桥驱动器，用来驱动直流电机。每个输出驱动模块由 N 沟道功率 MOSFET 组成的 H 桥构成，用以驱动电机绕组。在 24V 工作电压、25°C 工作温度并有适当散热的工作条件下，DRV8802 的每个 H 桥可驱动高达 1.6A 的峰值电流或 1.1A 的 RMS 输出电流。

一个简单的并行数字控制接口与行业标准器件兼容。可对衰减模式进行设定，以便在被禁用时实现电机制动或缓动。

提供针对过流保护、短路保护、欠压闭锁以及过热保护的内部关断功能。

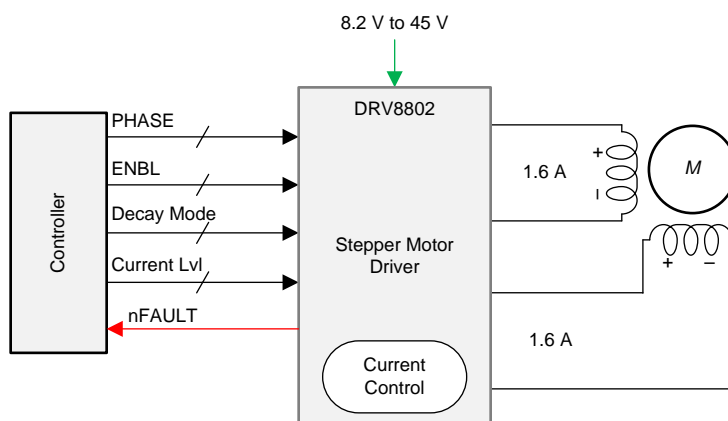
DRV8802 采用带有 PowerPAD™ 的 16 引脚超薄型四方扁平无引线 (WQFN) 封装（环保型：符合 RoHS 标准且不含镉/溴）。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
DRV8802	HTSSOP (28)	9.70mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

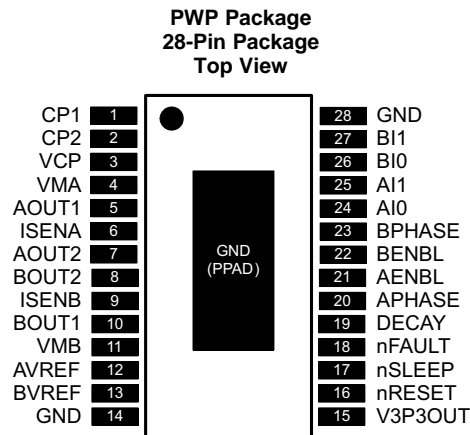
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (August 2013) to Revision D	Page
<ul style="list-style-type: none"> 已添加 ESD 额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	PIN			
POWER AND GROUND				
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01- μ F 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
GND	14, 28	—	Device ground	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1- μ F 16-V ceramic capacitor and a 1-M Ω resistor to VM.
VMA	4	—	Bridge A power supply	Connect to motor supply (8.2 V to 45 V). Both pins must be connected to the same supply, bypassed with a 0.1- μ F capacitor to GND, and connected to appropriate bulk capacitance.
VMB	11	—	Bridge B power supply	
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47- μ F, 6.3-V ceramic capacitor. Can be used to supply VREF.
CONTROL				
AENBL	21	I	Bridge A enable	Logic high to enable bridge A
AI0	24	I	Bridge A current set	Sets bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0
AI1	25	I		
APHASE	20	I	Bridge A phase (direction)	Logic high sets AOUT1 high, AOUT2 low
AVREF	12	I	Bridge A current set reference input	Reference voltage for winding current set. Can be driven individually with an external DAC for microstepping, or tied to a reference (for example, V3P3OUT).
BENBL	22	I	Bridge B enable	Logic high to enable bridge B
BI0	26	I	Bridge B current set	Sets bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0
BI1	27	I		
BPHASE	23	I	Bridge B phase (direction)	Logic high sets BOUT1 high, BOUT2 low
BVREF	13	I	Bridge B current set reference input	Reference voltage for winding current set. Can be driven individually with an external DAC for microstepping, or tied to a reference (for example, V3P3OUT).
DECAY	19	I	Decay (brake) mode	Low = brake (slow decay), high = coast (fast decay)
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	PIN			
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT				
AOUT1	5	O	Bridge A output 1	Connect to motor winding A
AOUT2	7	O	Bridge A output 2	
BOUT1	10	O	Bridge B output 1	Connect to motor winding B
BOUT2	8	O	Bridge B output 2	
ISENA	6	IO	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	9	IO	Bridge B ground / Isense	Connect to current sense resistor for bridge B

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
VMx	Power supply voltage	-0.3	47	V
VM _x	Power supply ramp rate	0	1	V/μs
	Digital pin voltage	-0.5	7	V
VREF	Input voltage	-0.3	4	V
	ISENSEx pin voltage ⁽³⁾	-0.8	0.8	V
	Peak motor drive output current, t < 1 μs	Internally limited		A
	Continuous motor drive output current ⁽⁴⁾	0	1.6	A
	Continuous total power dissipation	See Thermal Information .		
T _J	Operating virtual junction temperature	-40	150	°C
T _A	Operating ambient temperature	-40	85	°C
T _{stg}	Storage temperature	-60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Transients of ±1 V for less than 25 ns are acceptable
- (4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range ⁽¹⁾	8.2		45	V
V_{REF}	VREF input voltage ⁽²⁾	1		3.5	V
I_{V3P3}	V3P3OUT load current			1	mA

- (1) All V_M pins must be connected to the same supply voltage.
 (2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV8802	UNIT
		PWP (HTSSOP)	
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	$V_M = 24\text{ V}$, $f_{PWM} < 50\text{ kHz}$		5	8	mA
I_{VMQ}	VM sleep mode supply current	$V_M = 24\text{ V}$		10	20	μA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		7.8	8.2	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	$I_{OUT} = 0$ to 1 mA, $V_M = 24\text{ V}$, $T_J = 25^\circ\text{C}$	3.18	3.3	3.42	V
		$I_{OUT} = 0$ to 1 mA	3.1	3.3	3.5	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2		5.25	V
V_{HYS}	Input hysteresis			0.45		V
I_{iL}	Input low current	$V_{IN} = 0$	-20		20	μA
I_{iH}	Input high current	$V_{IN} = 3.3\text{ V}$			100	μA
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	$I_O = 5\text{ mA}$			0.5	V
I_{OH}	Output high leakage current	$V_O = 3.3\text{ V}$			1	μA
DECAY INPUT						
V_{iL}	Input low threshold voltage	For slow decay mode	0		0.8	V
V_{iH}	Input high threshold voltage	For fast decay mode	2			V
I_{iN}	Input current				± 40	μA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	$V_M = 24\text{ V}$, $I_O = 1\text{ A}$, $T_J = 25^\circ\text{C}$		0.63		Ω
		$V_M = 24\text{ V}$, $I_O = 1\text{ A}$, $T_J = 85^\circ\text{C}$		0.76	0.9	
$R_{DS(ON)}$	LS FET on resistance	$V_M = 24\text{ V}$, $I_O = 1\text{ A}$, $T_J = 25^\circ\text{C}$		0.65		Ω
		$V_M = 24\text{ V}$, $I_O = 1\text{ A}$, $T_J = 85^\circ\text{C}$		0.78	0.9	
I_{OFF}	Off-state leakage current		-20		20	μA
MOTOR DRIVER						
f_{PWM}	Internal PWM frequency			50		kHz
t_{BLANK}	Current sense blanking time			3.75		μs
t_R	Rise time	$V_M = 24\text{ V}$	100		360	ns
t_F	Fall time	$V_M = 24\text{ V}$	80		250	ns
t_{DEAD}	Dead time			400		ns
t_{DEG}	Input deglitch time		1.3		2.9	μs
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.8		5	A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	$^\circ\text{C}$
CURRENT CONTROL						
I_{REF}	xVREF input current	$xVREF = 3.3\text{ V}$	-3		3	μA
V_{TRIP}	xISENSE trip voltage	$xVREF = 3.3\text{ V}$, 100% current setting	635	660	685	mV
		$xVREF = 3.3\text{ V}$, 71% current setting	445	469	492	
		$xVREF = 3.3\text{ V}$, 38% current setting	225	251	276	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

6.6 Typical Characteristics

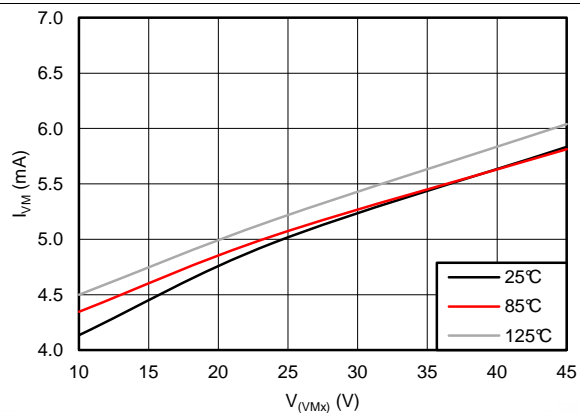


Figure 1. I_{VMX} vs V_{VMX}

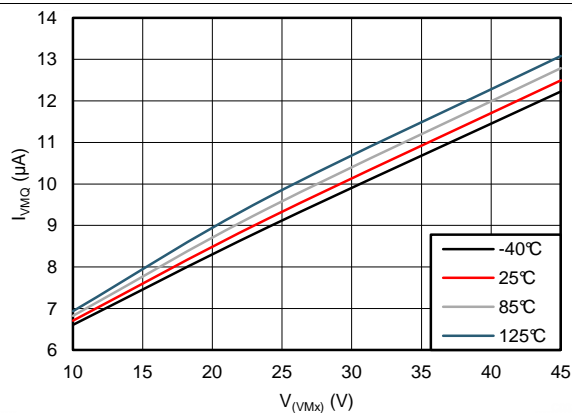


Figure 2. I_{VMXQ} vs V_{VMX}

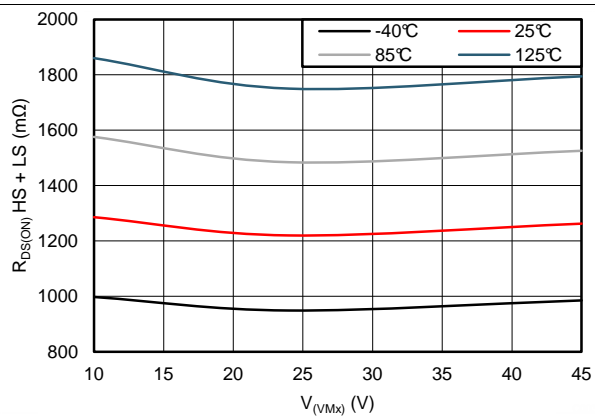


Figure 3. $R_{DS(ON)}$ vs V_{VMX}

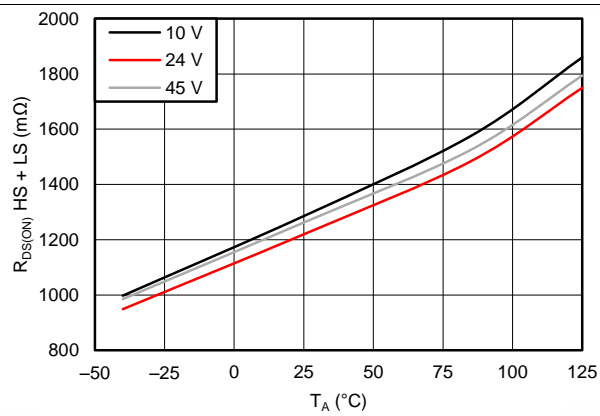


Figure 4. $R_{DS(ON)}$ vs Temperature

7 Detailed Description

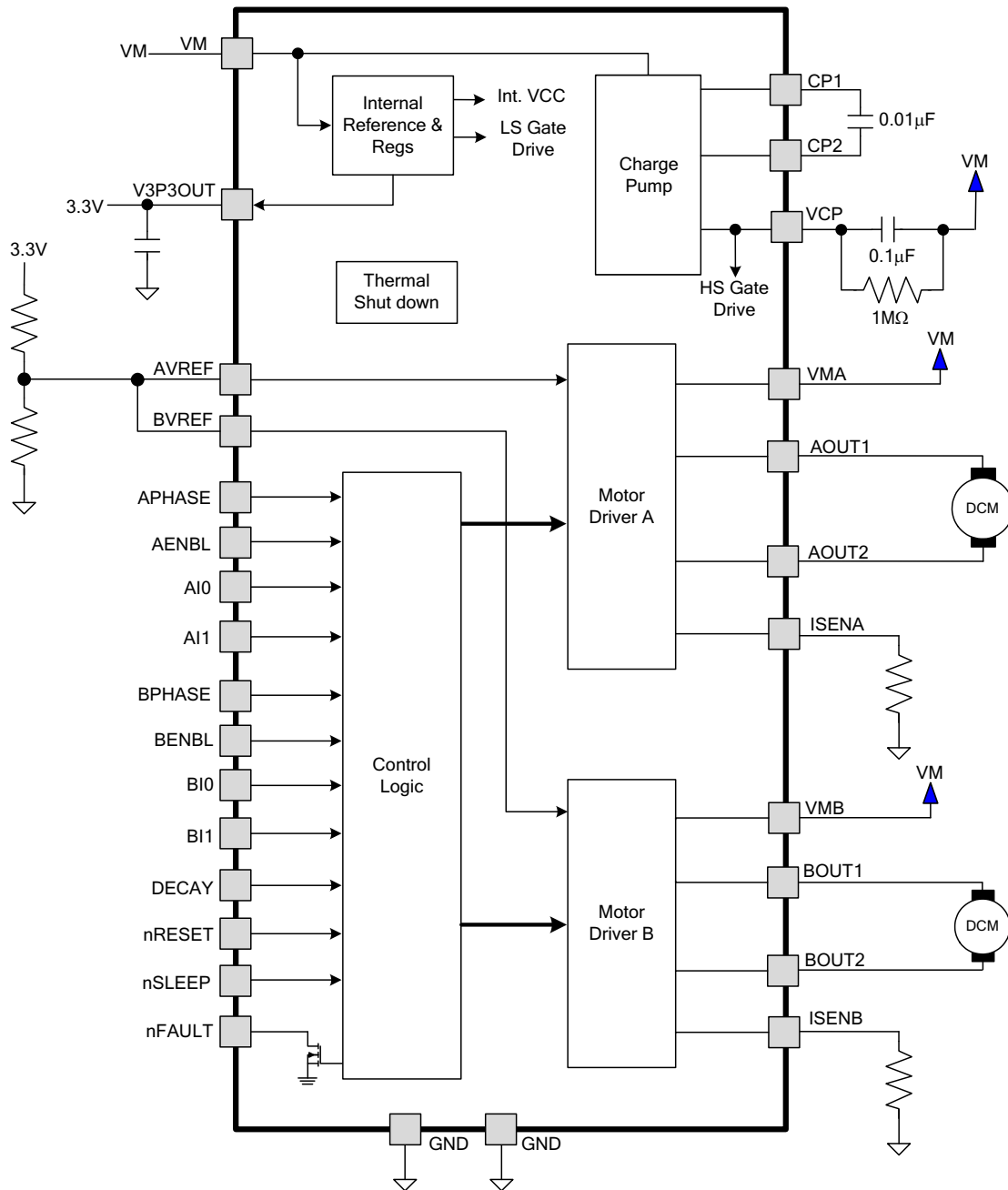
7.1 Overview

The DRV8802 is an integrated motor driver solution for two brushed DC motors. The device integrates two NMOS H-bridges, current sense, regulation circuitry, and detailed fault detection. The DRV8802 can be powered with a supply voltage from 8.2 V to 45 V and is capable of providing an output current up to 1.6-A full-scale.

A PHASE/ENBL interface allows for simple interfacing to the controller circuit. The winding current control allows the external controller to adjust the regulated current that is provided to the motor. The current regulation is highly configurable, with two decay modes of operation. Fast and slow decay can be selected depending on the application requirements.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8802 contains two H-bridge motor drivers with current-control PWM circuitry. Figure 5 shows a block diagram of the motor control circuitry.

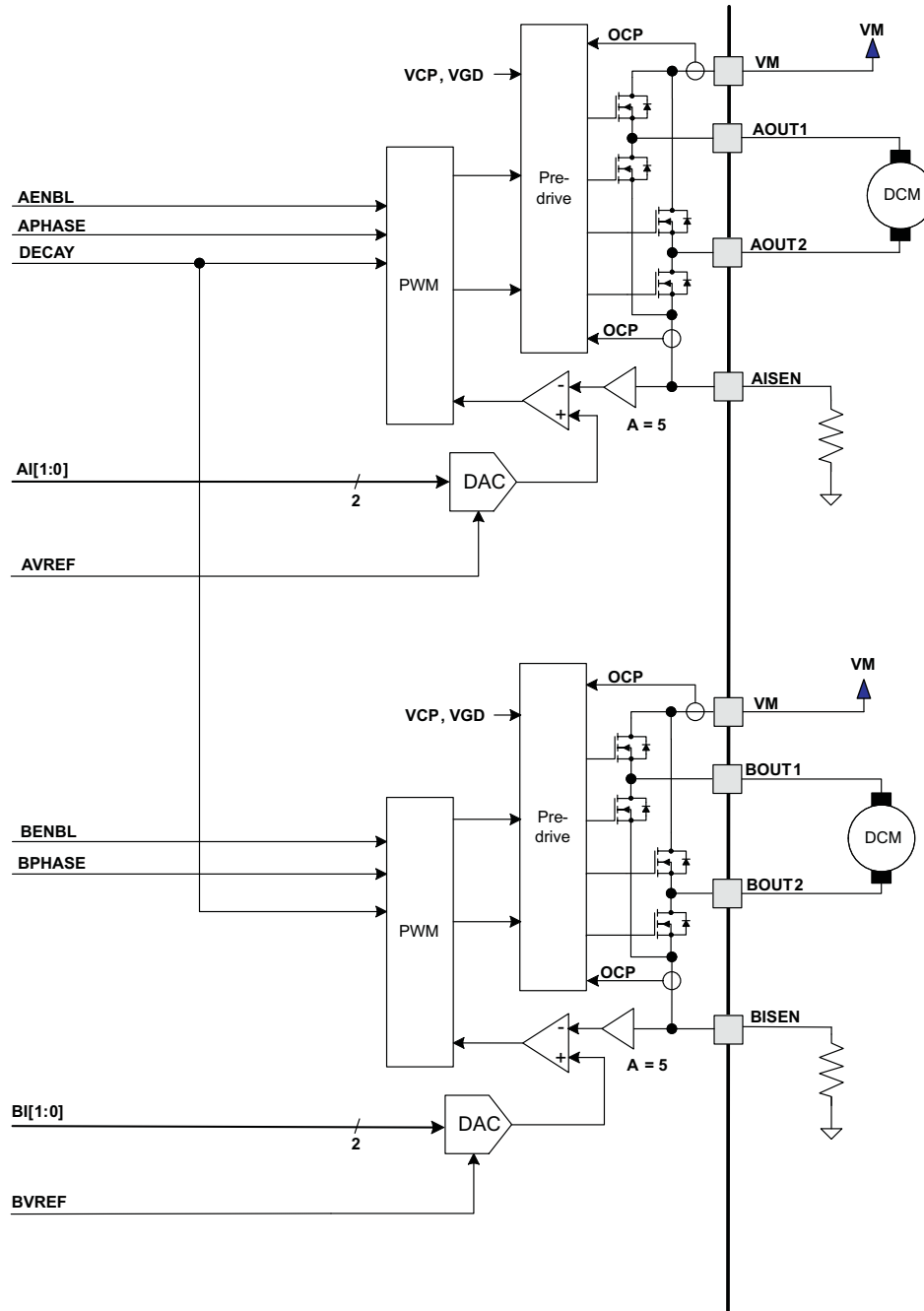


Figure 5. Motor Control Circuitry

Note that there are multiple VM pins. All VM pins must be connected together to the motor supply voltage.

7.3.2 Protection Circuits

The DRV8802 is fully protected against undervoltage, overcurrent, and overtemperature events.

Feature Description (continued)

7.3.2.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge are disabled and the nFAULT pin are driven low. The device remains disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; that is, a short-to-ground, supply, or across the motor winding results in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

7.3.2.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin are driven low. Once the die temperature has fallen to a safe level operation automatically resumes.

7.3.2.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic resets. Operation resumes when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 Bridge Control

The xPHASE input pins control the direction of current flow through each H-bridge, and hence the direction of rotation of a DC motor. The xENBL input pins enable the H-bridge outputs when active high, and can also be used for PWM speed control of the motor. [Table 1](#) shows the logic.

Table 1. H-Bridge Logic

xENBL	xPHASE	xOUT1	xOUT2
0	X	see ⁽¹⁾	see ⁽¹⁾
1	1	H	L
1	0	L	H

(1) Depends on state of the DECAY pin. See [Decay Mode and Braking](#).

7.4.2 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and can changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 2-bit DAC that allows current settings of 100%, 71%, 38% of full-scale, plus zero.

The full-scale (100%) chopping current is calculated in [Equation 1](#).

$$I_{\text{CHOP}} = \frac{V_{\text{REFX}}}{5 \times R_{\text{ISENSE}}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current is 3.3 V / (5 × 0.5 Ω) = 1.32 A.

Two input pins per H-bridge (xI1 and xI0) are used to scale the current in each bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The function of the pins is shown in [Table 2](#).

Table 2. H-Bridge Pin Functions

xI1	xI0	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
1	1	0% (Bridge disabled)
1	0	38%
0	1	71%
0	0	100%

Note that when both xI bits are 1, the H-bridge is disabled and no current flows.

Example:

If a 0.5-Ω sense resistor is used and the VREF pin is 3.3 V, the chopping current is 1.32 A at the 100% setting (xI1, xI0 = 00). At the 71% setting (xI1, xI0 = 01) the current is 1.32 A × 0.71 = 0.937 A, and at the 38% setting (xI1, xI0 = 10) the current is 1.32 A × 0.38 = 0.502 A. If (xI1, xI0 = 11) the bridge is disabled and no current flows.

7.4.3 Decay Mode and Braking

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in [Figure 6](#) as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in [Figure 6](#) as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in [Figure 6](#) as case 3.

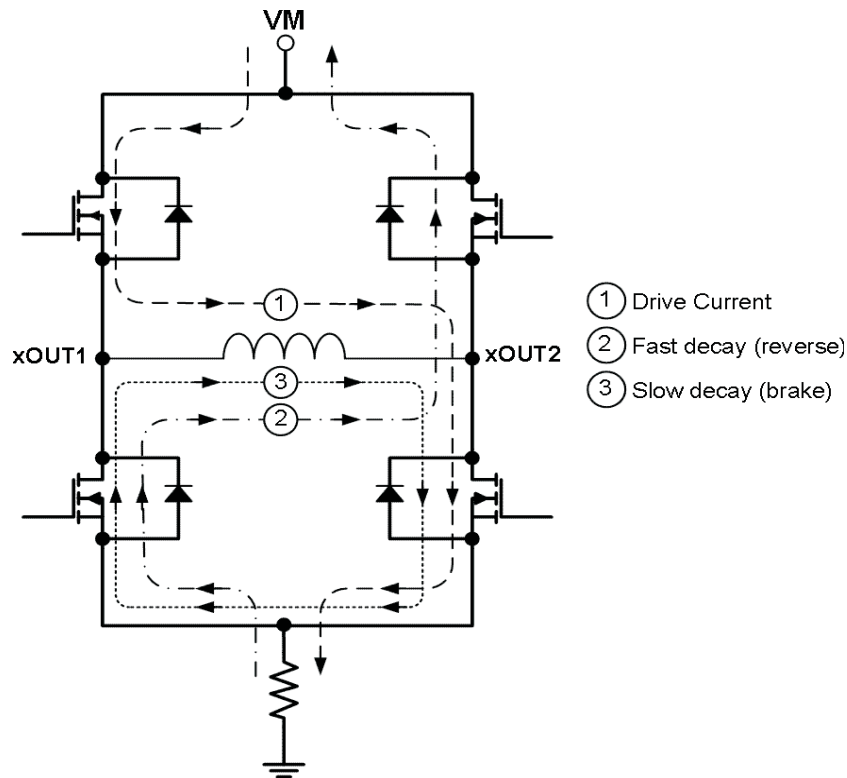


Figure 6. Decay Mode

The DRV8802 supports fast decay and slow decay mode. Slow or fast decay mode is selected by the state of the DECAY pin - logic low selects slow decay, and logic high sets fast decay mode. Note that the DECAY pin sets the decay mode for both H-bridges.

DECAY mode also affects the operation of the bridge when it is disabled (by taking the ENBL pin inactive). This applies if the ENABLE input is being used for PWM speed control of the motor, or if it is simply being used to start and stop motor rotation.

If the DECAY pin is high (fast decay), when the bridge is disabled, all FETs are turned off and decay current flows through the body diodes. This allows the motor to coast to a stop.

If the DECAY pin is low (slow decay), both low-side FETs is turned on when ENBL is made inactive. This essentially shorts out the back EMF of the motor, causing the motor to brake, and stop quickly. The low-side FETs stays in the ON state even after the current reaches zero.

7.4.4 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μ s. Note that the blanking time also sets the minimum on time of the PWM.

7.4.5 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8802 can be used to control two brushed DC motors. The PHASE/ENBL interface controls the outputs and current control can be implemented with the internal current regulation circuitry. Detailed fault reporting is provided with the internal protection circuits and nFAULT pin.

8.2 Typical Application

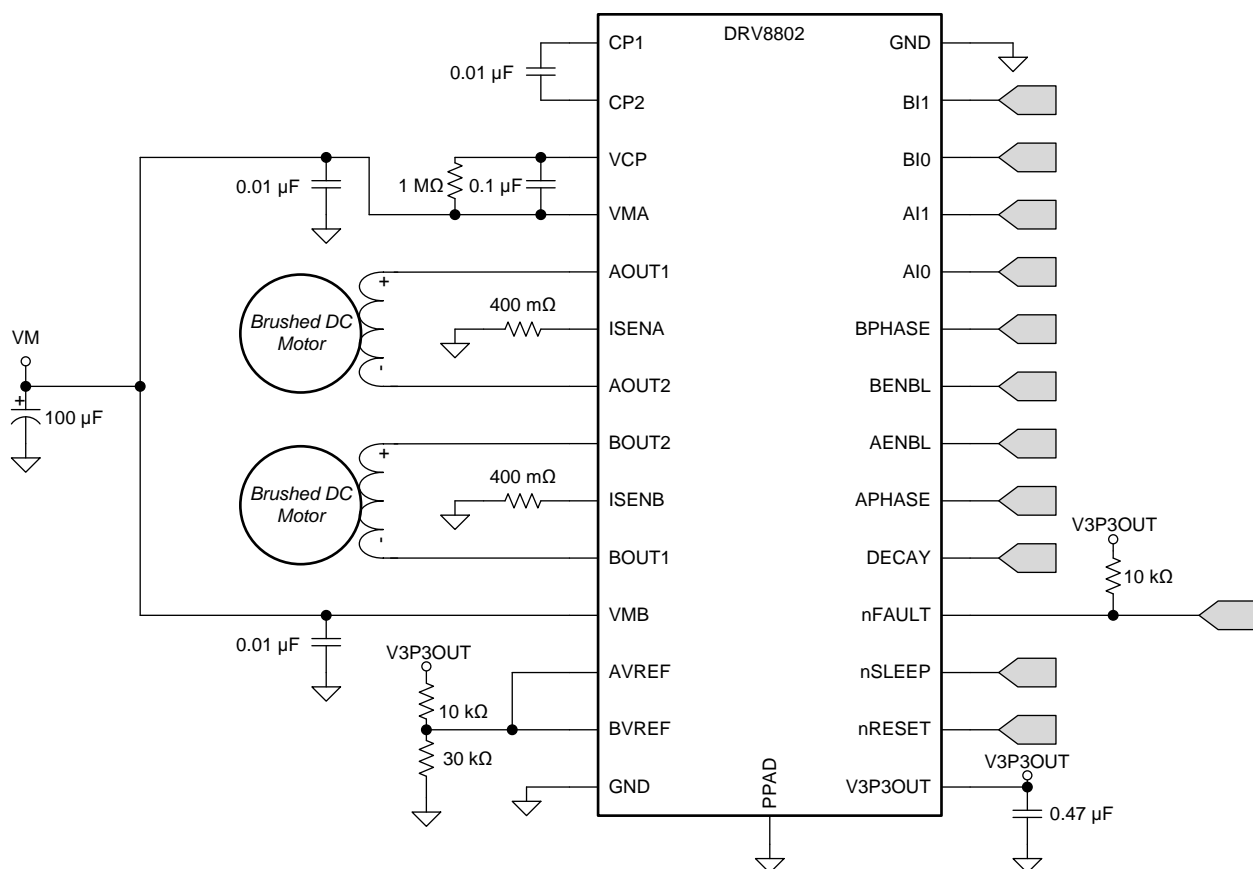


Figure 7. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 3 lists the parameters for this design example.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R _L	3.9 Ω
Motor winding inductance	I _L	2.9 mH
Sense resistor value	R _{SENSE}	400 mΩ
Target full-scale current	I _{FS}	1.25 A

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the xVREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8802 is set for 5 V/V.

$$I_{FS} (A) = \frac{xVREF (V)}{A_v \times R_{SENSE} (\Omega)} = \frac{xVREF (V)}{5 \times R_{SENSE} (\Omega)} \quad (2)$$

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.2 Ω, xVREF must be 1.25 V.

8.2.2.2 Decay Modes

The DRV8802 supports two different decay modes: slow decay and fast decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (ITRIP), the DRV8802 places the winding in one of the two decay modes until the PWM cycle has expired. Afterward, a new drive phase starts. The blanking time, tBLANK, defines the minimum drive time for the current chopping. ITRIP is ignored during tBLANK, so the winding current may overshoot the trip level.

8.2.2.3 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

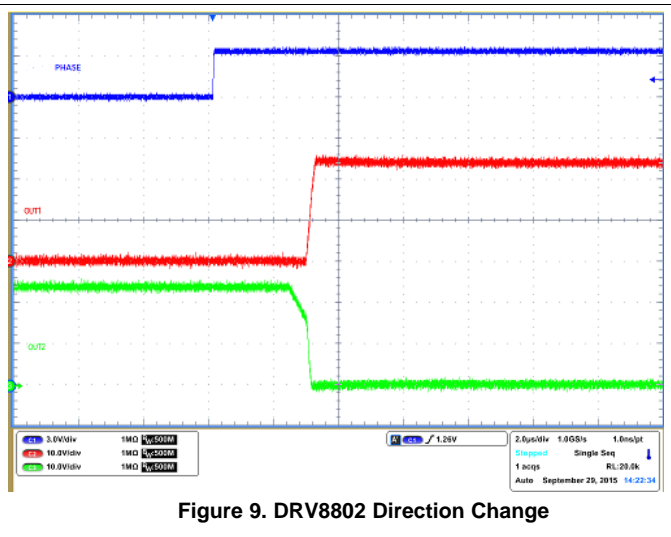
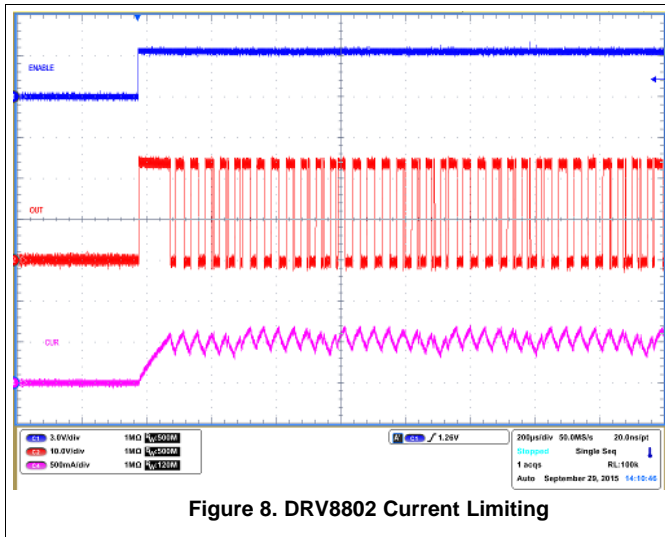
- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals I_{rms}² × R. For example, if the rms motor current is 2-A and a 100-mΩ sense resistor is used, the resistor dissipates 2 A² × 0.1 Ω = 0.4 W. The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin must be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.3 Application Curves



9 Power Supply Recommendations

The DRV8802 is designed to operate from an input voltage supply (VMx) range between 8.2 V and 45 V. Two 0.1- μ F ceramic capacitors rated for VMx must be placed as close as possible to the VMA and VMB pins respectively (one on each pin). In addition to the local decoupling capacitors, additional bulk capacitors is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. You must size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

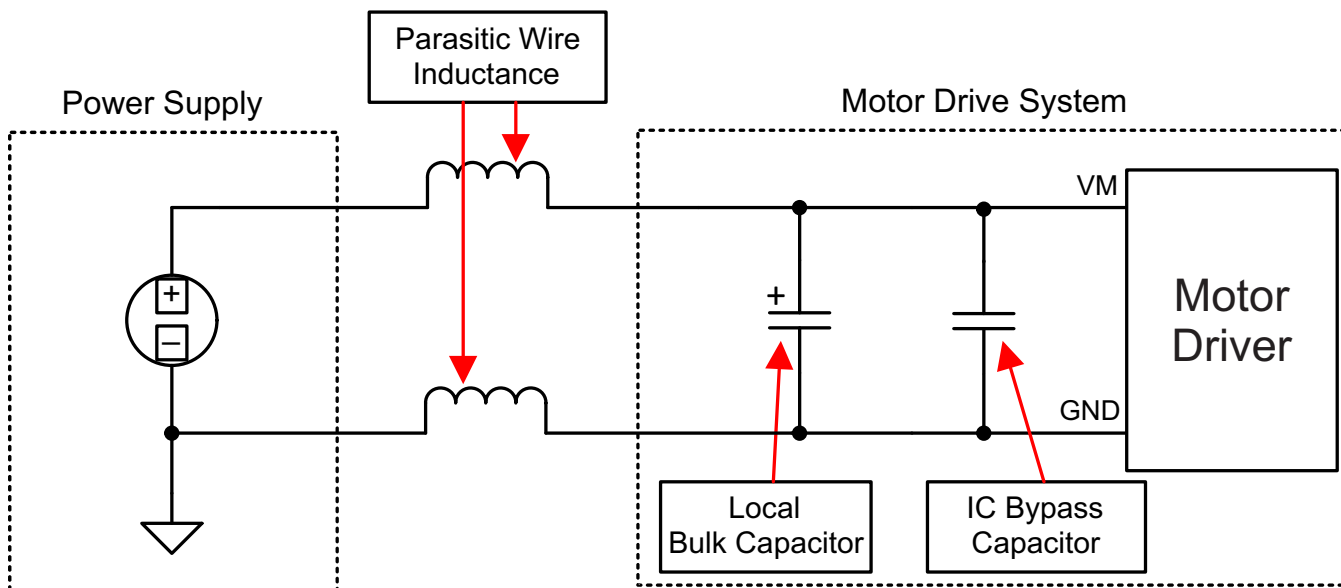


Figure 10. Setup of Motor Drive System With External Power Supply

9.2 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8802. It is okay for digital input signals to be present before VMx is applied. After VMx is applied to the DRV8802, it begins operation based on the status of the control pins.

10 Layout

10.1 Layout Guidelines

The VMA and VMB pins must be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1- μ F rated for VMx. This capacitor must be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and must be located close to the DRV8802.

A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. TI recommends a value of 0.1- μ F rated for 16 V. Place this component as close to the pins as possible. Also, place a 1-M Ω resistor between VCP and VMA.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible

10.2 Layout Example

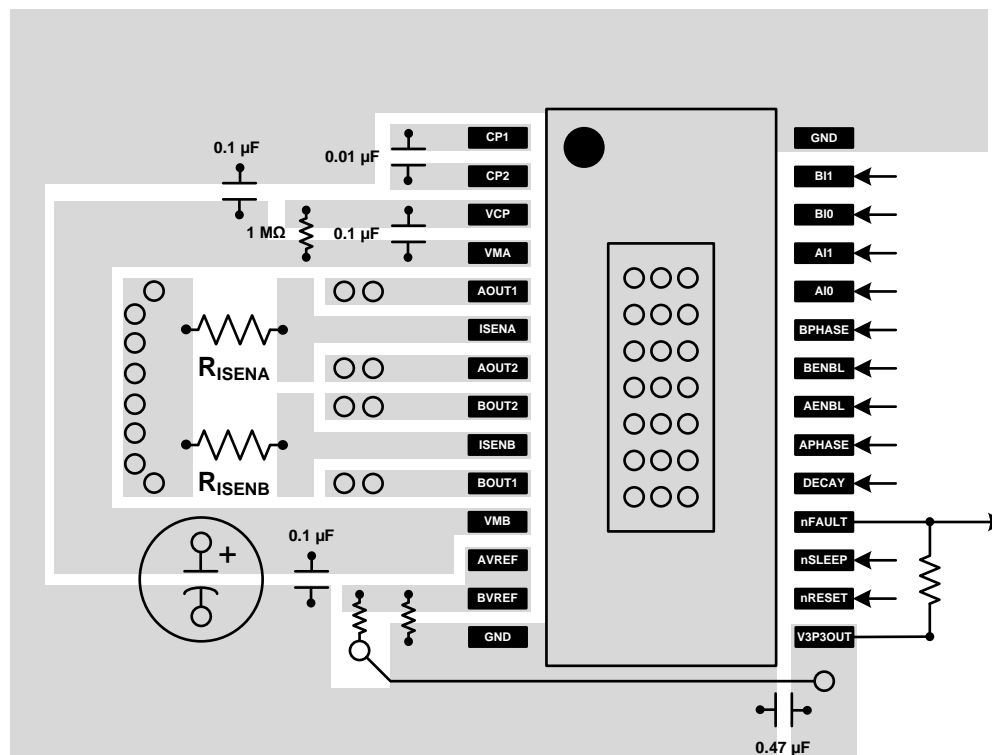


Figure 11. Typical Layout of DRV8802

10.3 Thermal Considerations

The DRV8802 has thermal shutdown (TSD) as described in [Thermal Shutdown \(TSD\)](#). If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8802 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each H-bridge when running a DC motor can be roughly estimated by [Equation 3](#).

Thermal Considerations (continued)

$$P = 2 \times R_{DS(ON)} \times (I_{OUT})^2$$

where

- P is the power dissipation of one H-bridge
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is the RMS output current being applied to each winding
- I_{OUT} is equal to the average current drawn by the DC motor. (3)

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation is the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), and TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

更多详细信息，请参见以下文档：

- TM 《PowerPAD 耐热增强型封装》， [SLMA002](#)
- TM 《PowerPAD 速成》， [SLMA004](#)

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

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11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8802PWP	Obsolete	Production	HTSSOP (PWP) 28	-	-	Call TI	Call TI	-40 to 85	DRV8802
DRV8802PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8802
DRV8802PWPR.A	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8802

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DRV8802 :

- Automotive : [DRV8802-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8802PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8802PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

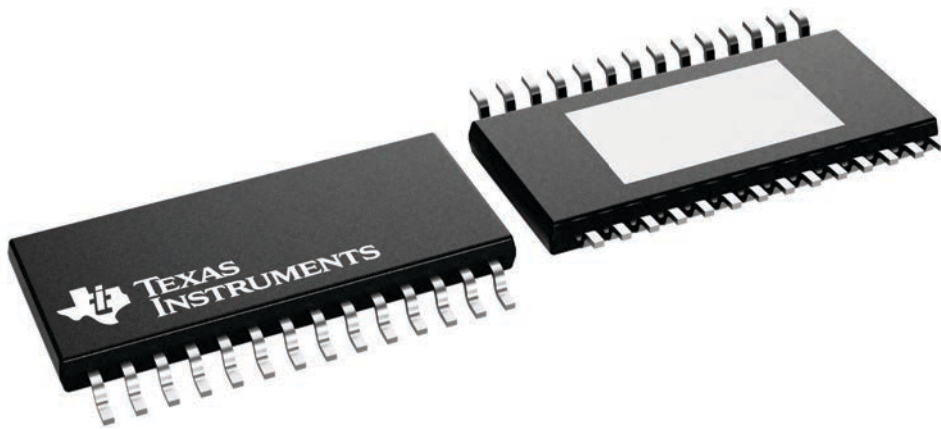
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

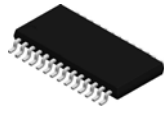
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

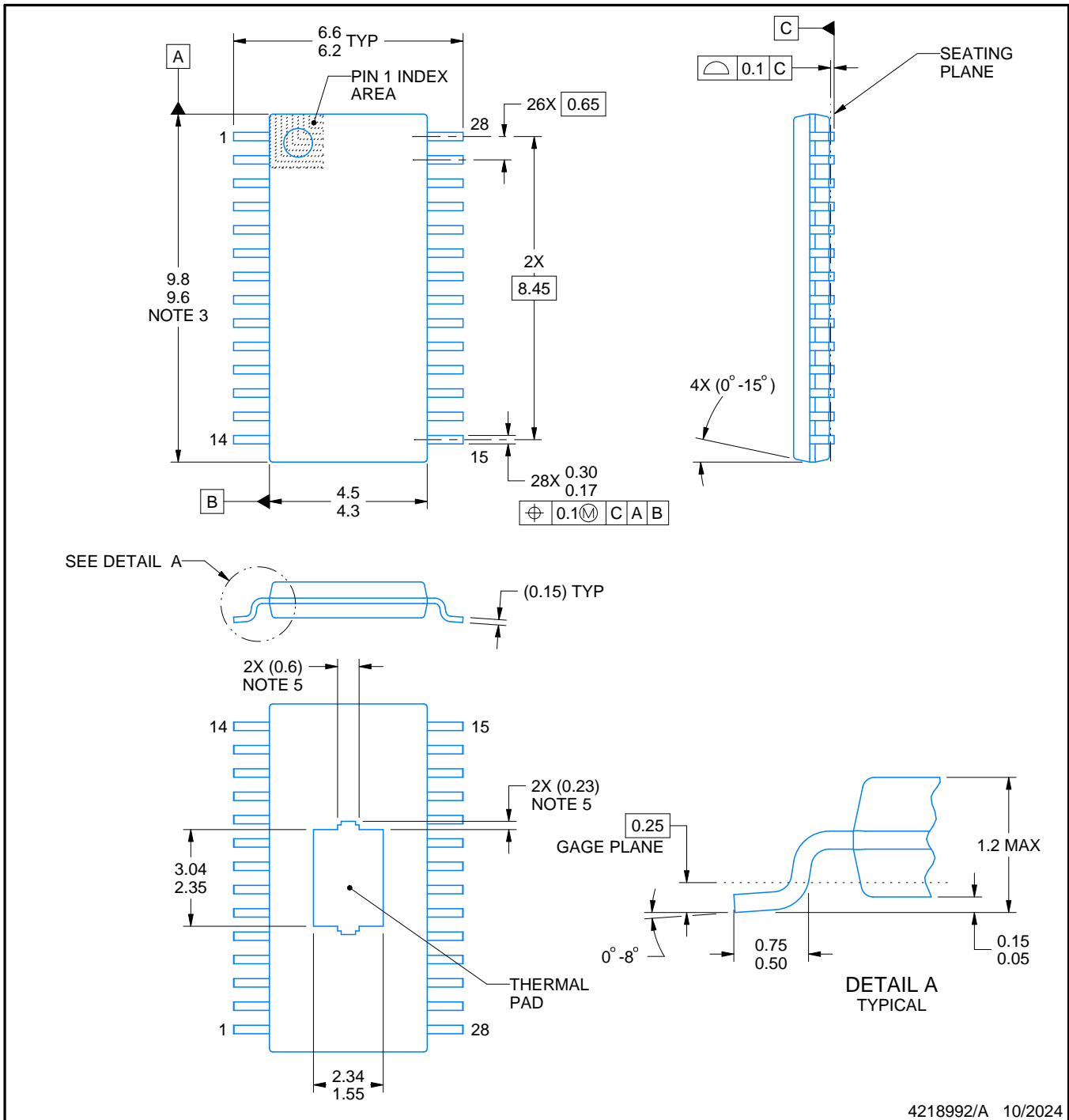
PWP0028H



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4218992/A 10/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

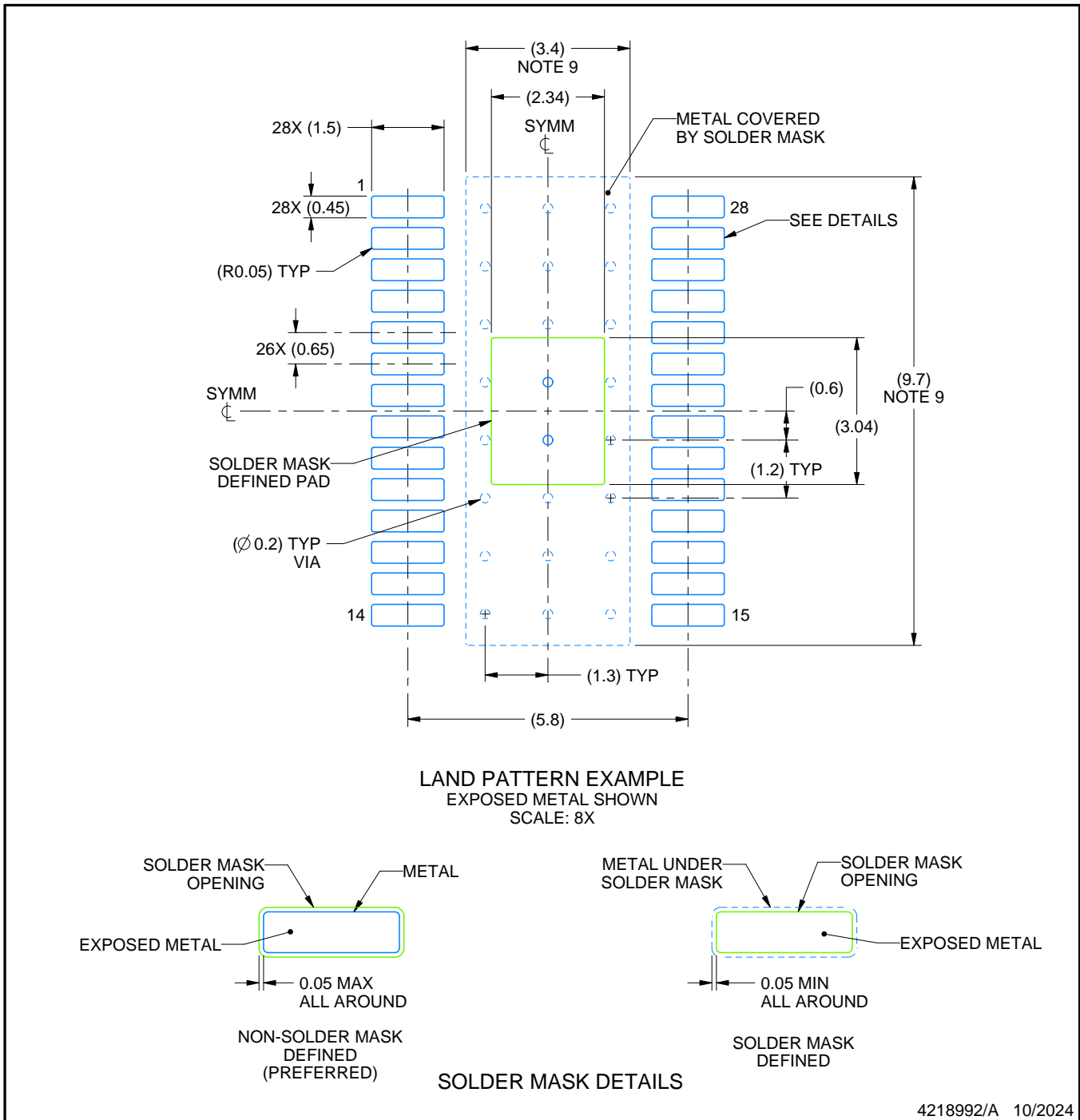
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028H

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

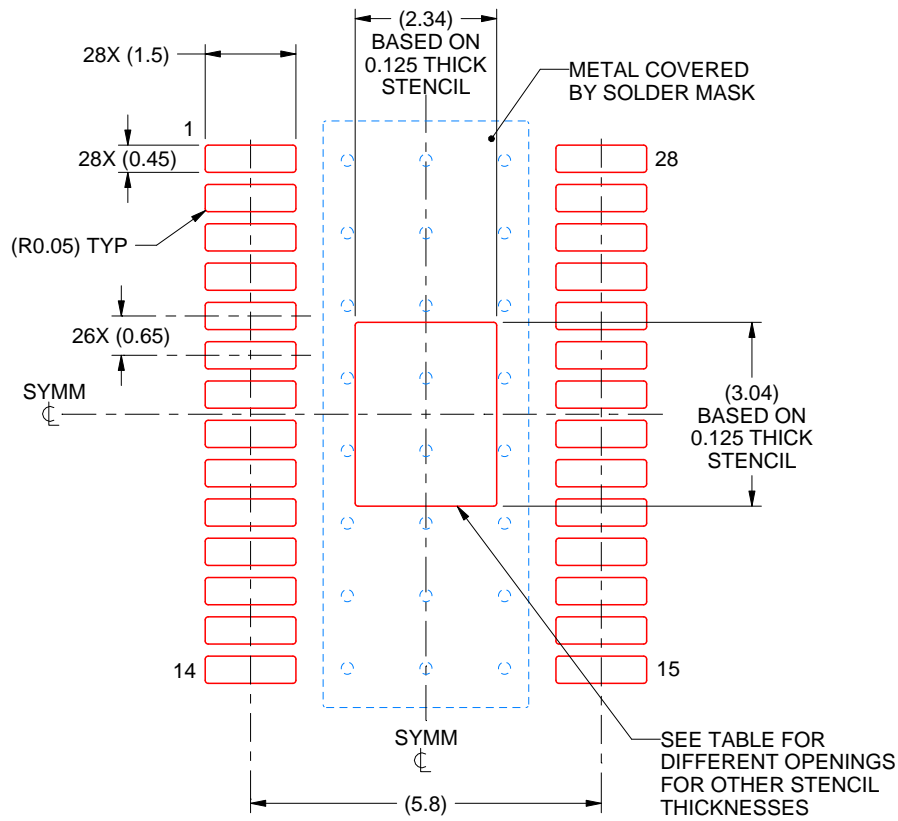
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028H

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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