

## DRV8329 4.5V 至 60V 三相 BLDC 栅极驱动器

### 1 特性

- 65V 三相半桥栅极驱动器
  - 可驱动 3 个高侧和 3 个低侧 N 沟道 MOSFET (NMOS)
  - 4.5V 至 60V 工作电压范围
  - 具有涓流电荷泵, 支持 100% 占空比
- 基于自举的栅极驱动器架构
  - 1000 mA 最大峰值拉电流
  - 2000mA 最大峰值灌电流
- 具有低输入失调电压的集成电流检测放大器 (针对 1 个分流器进行了优化)
  - 可调增益 (5、10、20、40 V/V)
- 硬件接口提供简单配置
- 温度为 25°C 时, 超低功耗休眠模式下的电流 <1uA
- 4 ns (典型值) 相位间传播延迟匹配
- 独立驱动器关断路径 (DRVOFF)
- 65V 耐压唤醒引脚 (nSLEEP)
- SHx 引脚瞬态负压可达 -10V
- 6x 和 3x PWM 模式
- 支持 3.3V 和 5V 逻辑输入
- 精密 LDO (AVDD), 3.3V ±3%, 80mA
- 紧凑型 QFN 封装和尺寸
- 可通过 VDSLVL 引脚调节 VDS 过流阈值
- 可通过 DT 引脚调节死区时间
- 具有电源块的高效系统设计
- 集成保护特性
  - PVDD 欠压闭锁 (PVDDUV)
  - GVDD 欠压 (GVDDUV)
  - 自举欠压 (BST\_UV)
  - 过流保护 (VDS\_OCP、SEN\_OCP)
  - 热关断 (OTSD)
  - 故障状态指示器 (nFAULT)

### 2 应用

- 无刷直流 (BLDC) 电机模块和 PMSM
- 无线园艺和电动工具、割草机
- 电器风扇和泵
- 伺服驱动器
- 电动自行车、电动踏板车和电动汽车
- 无线真空吸尘器
- 无人机
- 工业和物流机器人以及遥控玩具

### 3 说明

DRV8329 系列器件是适用于三相应用的集成栅极驱动器。这类器件具有三个半桥栅极驱动器, 每个驱动器都能够驱动高侧和低侧 N 沟道功率 MOSFET。该器件使用内部电荷泵生成合适的栅极驱动电压, 使用自举电路增强高侧 MOSFET。具有涓流电荷泵, 支持 100% 占空比。此栅极驱动架构支持高达 1A 的峰值栅极驱动拉电流和 2A 的峰值栅极驱动灌电流。DRV8329 由单一电源供电, 支持 4.5V 至 60V 的宽输入电源电压范围。

6x 和 3x PWM 模式可简化与控制器电路的连接。该器件具有集成的精密 3.3V LDO, 该 LDO 可用于为外部控制器供电, 并可用作 CSA 的基准电压。器件的配置设置可通过硬件 (H/W) 引脚来配置。

DRV8329 器件集成了低侧电流检测放大器, 可在驱动级的全部三个相位上进行电流检测, 以获得电流总和。

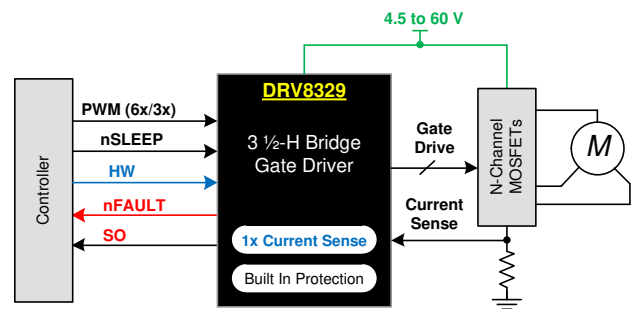
提供低功耗休眠模式, 可通过关断大部分内部电路实现低静态电流。针对欠压锁定、GVDD 故障、MOSFET 过流、MOSFET 短路和过热等情况, 提供内部保护功能。在 nFAULT 引脚上指示故障条件。

器件信息<sup>(1)</sup>

| 器件型号                       | 封装        | 封装尺寸 (标称值)      |
|----------------------------|-----------|-----------------|
| DRV8329AREE                | VQFN (36) | 5.00mm × 4.00mm |
| DRV8329BREE <sup>(2)</sup> | VQFN (36) | 5.00mm × 4.00mm |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

(2) 器件仅处于预发布状态



DRV8329 简化原理图



## Table of Contents

|  |           |  |           |
|--|-----------|--|-----------|
| <b>1 特性</b> .....                              | <b>1</b>  | 9.1 Application Information.....                       | 29        |
| <b>2 应用</b> .....                              | <b>1</b>  | 9.2 Typical Application.....                           | 29        |
| <b>3 说明</b> .....                              | <b>1</b>  | <b>10 Power Supply Recommendations</b> .....           | <b>44</b> |
| <b>4 Revision History</b> .....                | <b>2</b>  | 10.1 Bulk Capacitance Sizing.....                      | 44        |
| <b>5 Device Comparison Table</b> .....         | <b>3</b>  | <b>11 Layout</b> .....                                 | <b>45</b> |
| <b>6 Pin Configuration and Functions</b> ..... | <b>4</b>  | 11.1 Layout Guidelines.....                            | 45        |
| <b>7 Specification</b> .....                   | <b>6</b>  | 11.2 Layout Example.....                               | 47        |
| 7.1 Absolute Maximum Ratings.....              | 6         | 11.3 Thermal Considerations.....                       | 48        |
| 7.2 ESD Ratings Comm.....                      | 6         | <b>12 Device and Documentation Support</b> .....       | <b>49</b> |
| 7.3 Recommended Operating Conditions.....      | 7         | 12.1 Device Support.....                               | 49        |
| 7.4 Thermal Information 1pkg.....              | 7         | 12.2 Documentation Support.....                        | 49        |
| 7.5 Electrical Characteristics.....            | 8         | 12.3 Related Links.....                                | 49        |
| 7.6 Typical Characteristics.....               | 15        | 12.4 Receiving Notification of Documentation Updates.. | 49        |
| <b>8 Detailed Description</b> .....            | <b>16</b> | 12.5 Community Resources.....                          | 49        |
| 8.1 Overview.....                              | 16        | 12.6 Trademarks.....                                   | 49        |
| 8.2 Functional Block Diagram.....              | 17        | <b>13 Mechanical, Packaging, and Orderable</b>         |           |
| 8.3 Feature Description.....                   | 18        | <b>Information</b> .....                               | <b>49</b> |
| 8.4 Device Functional Modes.....               | 28        | 13.1 Tape and Reel Information.....                    | 53        |
| <b>9 Application and Implementation</b> .....  | <b>29</b> |  |           |

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (June 2022) to Revision A (October 2022) | Page |
|--|------|
| • 将器件状态更新为“生产数据”。 .....  | 1    |

## 5 Device Comparison Table

表 5-1. Different Device Variants

| DEVICE  | DEVICE VARIANT | Package                           | LDO output | DT pin and VDSSLVL | PWM_MODE |
|---------|----------------|-----------------------------------|------------|--------------------|----------|
| DRV8329 | DRV8329A       | 36-pin QFN<br>(5.00 mm x 4.00 mm) | 3.3 V      | Available          | 6x       |
|         | DRV8329B       |                                   |            |                    | 3x       |

## 6 Pin Configuration and Functions

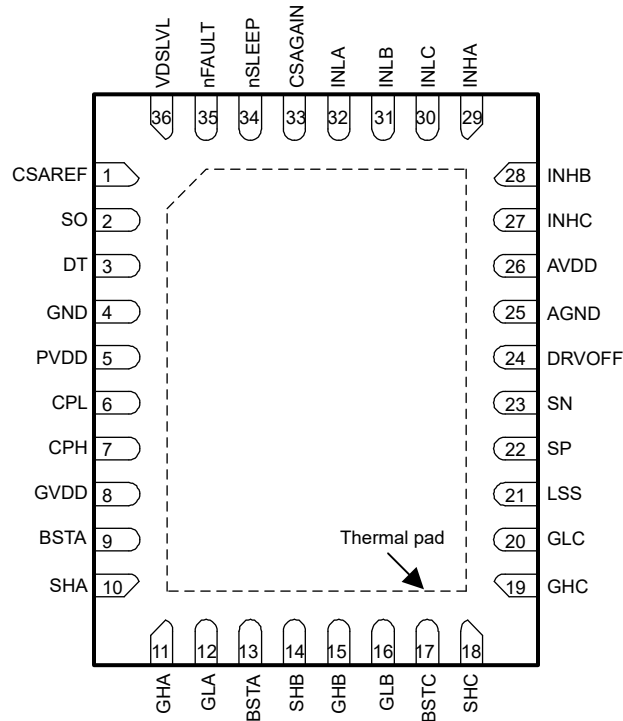


图 6-1. DRV8329 REE Package 36-pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions—36-Pin DRV8329 Devices

| NAME    | PIN NO. | TYPE  | DESCRIPTION  |
|---------|---------|-------|--|
|         | DRV8329 |       |  |
| AGND    | 25      | PWR   | Device analog ground. Refer <a href="#">Layout Guidelines</a> for the recommendation on connection.  |
| AVDD    | 26      | PWR-O | 3.3-V regulator output. Connect a X5R or X7R, 1-μF, >6.3-V ceramic capacitor between the AVDD and GND pins. This regulator can source up to 80 mA externally. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin. |
| BSTA    | 9       | O     | Bootstrap output pin. Connect a X5R or X7R, 1-μF, 25-V ceramic capacitor between BSTA and SHA  |
| BSTB    | 13      | O     | Bootstrap output pin. Connect a X5R or X7R, 1-μF, 25-V ceramic capacitor between BSTB and SHB  |
| BSTC    | 17      | O     | Bootstrap output pin. Connect a X5R or X7R, 1-μF, 25-V ceramic capacitor between BSTC and SHC  |
| CSAGAIN | 33      | I     | Gain settings for Current sense amplifier. The pin is a 4 level input pin set by an external resistor. See <a href="#">Low-Side Current Sense Amplifiers</a> for more information.   |
| CSAREF  | 1       | I     | Current sense amplifier reference. Connect a X5R or X7R, 0.1-μF, 6.3-V ceramic capacitor between the CSAREF and AGND pins.   |
| CPH     | 7       | PWR   | Charge pump switching node. Connect a X5R or X7R, PVDD-rated ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.  |
| CPL     | 6       | PWR   |  |
| DRVOFF  | 24      | I     | Independent driver shutdown path. Pulling DRVOFF high turns off all external MOSFETs by putting the gate drivers into the pull-down state. This signal bypasses and overrides the digital core of DRV8329.   |
| DT      | 3       | I     | Gate drive deadtime setting. Connect a resistor of value between 10 kΩ to 390 kΩ between DT and GND to adjust deadtime between 100 ns to 2000 ns. If pin is left floating or connected to GND fixed value of 55 ns deadtime is inserted.                       |
| GHA     | 11      | O     | High-side gate driver output. Connect to the gate of the high-side power MOSFET.   |
| GHB     | 15      | O     | High-side gate driver output. Connect to the gate of the high-side power MOSFET.   |
| GHC     | 19      | O     | High-side gate driver output. Connect to the gate of the high-side power MOSFET.   |
| GLA     | 12      | O     | Low-side gate driver output. Connect to the gate of the low-side power MOSFET.   |
| GLB     | 16      | O     | Low-side gate driver output. Connect to the gate of the low-side power MOSFET.   |

**表 6-1. Pin Functions—36-Pin DRV8329 Devices (continued)**

| NAME        | PIN NO. | TYPE  | DESCRIPTION   |
|-------------|---------|-------|---|
|             | DRV8329 |       |   |
| GLC         | 20      | O     | Low-side gate driver output. Connect to the gate of the low-side power MOSFET.  |
| GVDD        | 8       | PWR-O | Gate driver power supply output. Connect a X5R or X7R, 30-V rated ceramic $\geq 10\text{-}\mu\text{F}$ local capacitance between the GVDD and GND pins. TI recommends a capacitor value of $>10\times C_{BSTx}$ and voltage rating at least twice the normal operating voltage of the pin.                                  |
| GND         | 4       | PWR   | Device ground. Refer <a href="#">Layout Guidelines</a> for the recommendation on connection.  |
| INHA        | 29      | I     | High-side gate driver control input for Phase A. This pin controls the output of the high-side FET.   |
| INHB        | 28      | I     | High-side gate driver control input for Phase B. This pin controls the output of the high-side FET.   |
| INHC        | 27      | I     | High-side gate driver control input for Phase C. This pin controls the output of the high-side FET.   |
| INLA        | 32      | I     | Low-side gate driver control input for Phase A. This pin controls the output of the low-side FET.   |
| INLB        | 31      | I     | Low-side gate driver control input for Phase B. This pin controls the output of the low-side FET.   |
| INLC        | 30      | I     | Low-side gate driver control input for Phase C. This pin controls the output of the low-side FET.   |
| LSS         | 21      | PWR   | Low side source pin, connect all sources of the external low-side MOSFETs here. This pin is the sink path for the low-side gate driver, and serves as an input to monitor the low-side MOSFET VDS voltage and VSEN_OCP voltage.   |
| nFAULT      | 35      | OD    | Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor to 3.3V to 5.0V.  |
| nSLEEP      | 34      | I     | Sleep mode entry pin. When this pin is pulled logic low the device goes to a low-power sleep mode. An 1 to 1.2- $\mu\text{s}$ low pulse can be used to reset fault conditions without entering sleep mode.  |
| PVDD        | 5       | PWR   | Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1- $\mu\text{F}$ , $>2\times$ PVDD-rated ceramic and $>10\text{-}\mu\text{F}$ local capacitance between the PVDD and GND pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin. |
| SHA         | 10      | I/O   | High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.   |
| SHB         | 14      | I/O   | High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.   |
| SHC         | 18      | I/O   | High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.   |
| SO          | 2       | O     | Current sense amplifier output. Supports capacitive load or low pass filter (resistor in series and capacitor to GND)   |
| SP          | 22      | I     | Current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.   |
| SN          | 23      | I     | Current sense amplifier input. Connect to the low-side of the current shunt resistor.   |
| VDSLVL      | 36      | I     | VDS monitor trip point setting. Connect an analog level input from 0.1 V to 2.5 V to set a VDS monitor trip point setting for MOSFET overcurrent protection. See <a href="#">VDSLVL Selection</a> for more information.   |
| Thermal Pad |         | PWR   | Must be connected to GND  |

## 7 Specification

### 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

|   |  | MIN                | MAX                       | UNIT |
|---|--|--------------------|---------------------------|------|
| Power supply pin voltage  | PVDD                                   | -0.3               | 65                        | V    |
| Bootstrap pin voltage   | BSTx                                   | -0.3               | 80                        | V    |
| Bootstrap pin voltage   | BSTx with respect to SHx               | -0.3               | 20                        | V    |
| Bootstrap pin voltage   | BSTx with respect to GHx               | -0.3               | 20                        | V    |
| Charge pump pin voltage   | CPL, CPH                               | -0.3               | V <sub>GVDD</sub>         | V    |
| Gate driver regulator pin voltage                               | GVDD                                   | -0.3               | 20                        | V    |
| Analog regulator pin voltage                                    | AVDD                                   | -0.3               | 4                         | V    |
| Logic pin voltage (nSLEEP)                                      | nSLEEP                                 | -0.3               | 65                        | V    |
| Logic pin voltage   | DRVOFF, DT, INHx, INLx, nFAULT, VDSLVL | -0.3               | 6                         | V    |
| High-side gate drive pin voltage                                | GHx                                    | -8                 | 80                        | V    |
| Transient 500-ns high-side gate drive pin voltage               | GHx                                    | -10                | 80                        | V    |
| High-side gate drive pin voltage                                | GHx with respect to SHx                | -0.3               | 20                        | V    |
| High-side source pin voltage                                    | SHx                                    | -8                 | 70                        | V    |
| Transient 500-ns high-side source pin voltage                   | SHx                                    | -10                | 72                        | V    |
| Low-side gate drive pin voltage                                 | GLx with respect to LSS                | -0.3               | 20                        | V    |
| Transient 500-ns low-side gate drive pin voltage <sup>(2)</sup> | GLx with respect to LSS                | -1                 | 20                        | V    |
| Low-side gate drive pin voltage                                 | GLx with respect to GVDD               |                    | 0.3                       | V    |
| Transient 500-ns low-side gate drive pin voltage                | GLx with respect to GVDD               |                    | 1                         | V    |
| Low-side source sense pin voltage                               | LSS                                    | -1                 | 1                         | V    |
| Transient 500-ns low-side source sense pin voltage              | LSS                                    | -10                | 8                         | V    |
| Gate drive current  | GHx, GLx                               | Internally Limited | Internally Limited        | A    |
| Current sense amplifier reference input pin voltage             | CSAREF                                 | -0.3               | 5.5                       | V    |
| Shunt amplifier input pin voltage                               | SN, SP                                 | -1                 | 1                         | V    |
| Transient 500-ns shunt amplifier input pin voltage              | SN, SP                                 | -10                | 8                         | V    |
| Shunt amplifier output pin voltage                              | SO                                     | -0.3               | V <sub>CSAREF</sub> + 0.3 | V    |
| Junction temperature, T <sub>J</sub>                            |  | -40                | 150                       | °C   |
| Storage temperature, T <sub>stg</sub>                           |  | -65                | 150                       | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) Supports upto 5A for 500 nS when GLx-LSS is negative

### 7.2 ESD Ratings Comm

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±750  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

|                                  |  |                                     | MIN  | NOM | MAX                | UNIT |
|----------------------------------|--|-------------------------------------|------|-----|--------------------|------|
| V <sub>PVDD</sub>                | Power supply voltage   | PVDD                                | 4.5  |     | 60                 | V    |
| V <sub>PVDD_RAMP</sub>           | Power supply voltage ramp rate at power up                         | PVDD                                |      |     | 30                 | V/us |
| V <sub>PVDD_RAMP</sub>           | Power supply voltage ramp rate during operation                    | PVDD                                |      |     | 4                  | V/us |
| V <sub>BST</sub>                 | Bootstrap pin voltage with respect to SHx                          | nSLEEP = High, INHx is switching    | 4    |     | 20                 | V    |
| I <sub>AVDD</sub> <sup>(1)</sup> | Regulator external load current                                    | AVDD                                |      |     | 80                 | mA   |
| I <sub>TRICKLE</sub>             | Trickle charge pump external load current                          | BSTx                                |      |     | 2                  | μA   |
| V <sub>IN</sub>                  | Logic input voltage  | DRVOFF, INHx, INLx, nSLEEP          | 0    |     | 5.5                | V    |
| V <sub>IN</sub>                  | Logic input voltage  | DT, VDSLVL                          | 0    |     | 3.4                | V    |
| f <sub>PWM</sub>                 | PWM frequency  | INHx, INLx                          | 0    |     | 200                | kHz  |
| V <sub>OD</sub>                  | Open drain pullup voltage  | nFAULT                              |      |     | 5.5                | V    |
| I <sub>OD</sub>                  | Open drain output current  | nFAULT                              |      |     | -10                | mA   |
| I <sub>GS</sub> <sup>(1)</sup>   | Total average gate-drive current (Low Side and High Side Combined) | I <sub>GHx</sub> , I <sub>GLx</sub> |      |     | 30                 | mA   |
| V <sub>CSAREF</sub>              | Current sense amplifier reference voltage                          | CSAREF                              | 2.8  |     | 5.5                | V    |
| I <sub>SO</sub>                  | Shunt amplifier output current                                     | SO                                  |      |     | 5                  | mA   |
| V <sub>SHSL</sub>                | Slew Rate on SHx pins  |                                     |      |     | 4                  | V/ns |
| C <sub>BSTx</sub>                | Capacitor between BSTx and SHx                                     |                                     |      |     | 4.7 <sup>(2)</sup> | μF   |
| C <sub>GVDD</sub>                | Capacitor between GVDD and GND                                     |                                     |      |     | 130                | μF   |
| T <sub>A</sub>                   | Operating ambient temperature                                      |                                     | - 40 |     | 125                | °C   |
| T <sub>J</sub>                   | Operating junction temperature                                     |                                     | - 40 |     | 150                | °C   |

(1) Power dissipation and thermal limits must be observed

(2) Current flowing through boot diode (DBOOT) needs to be limited for C<sub>BSTx</sub> > 4.7μF.

### 7.4 Thermal Information 1pkg

| THERMAL METRIC <sup>(1)</sup> |  | DRV8329    | UNIT |
|-------------------------------|--|------------|------|
|                               |  | REE (WQFN) |      |
|                               |  | 36         |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 37.3       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 25.2       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 15.8       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 15.8       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 4.5        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

4.5 V ≤ V<sub>PVDD</sub> ≤ 60 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>PVDD</sub> = 24 V

| PARAMETER                                |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|--|---|--|-----|-----|-----|------|
| <b>POWER SUPPLIES (AVDD, PVDD, GVDD)</b> |   |  |     |     |     |      |
| I <sub>PVDDQ</sub>                       | PVDD sleep mode current                                 | V <sub>PVDD</sub> = 24V, nSLEEP = 0, T <sub>A</sub> = 25°C   |     |     | 1   | μA   |
|  |   | nSLEEP = LOW   |     |     | 2   | μA   |
| I <sub>PVDDS</sub>                       | PVDD standby mode current                               | V <sub>PVDD</sub> = 24 V; nSLEEP = HIGH, INHx = INLx = LOW, DRVOFF = HIGH  |     | 2   | 4   | mA   |
|  |   | nSLEEP = HIGH, INHx = INLx = LOW, DRVOFF = HIGH  |     | 3   | 5.5 | mA   |
| I <sub>PVDD</sub>                        | PVDD active mode current                                | V <sub>PVDD</sub> = 24 V, nSLEEP = HIGH, INHx = INLx = Switching@20kHz, No FETs connected  |     | 4   | 7   | mA   |
|  |   | nSLEEP = HIGH, INHx = INLx = Switching@20kHz, No FETs connected  |     | 5   | 10  | mA   |
|  |   | V <sub>PVDD</sub> = 8 V, nSLEEP = HIGH, INHx = INLx = LOW, No FETs connected   |     | 5   | 10  | mA   |
|  |   | V <sub>PVDD</sub> = 24 V, nSLEEP = HIGH, INHx = INLx = LOW, No FETs connected  |     | 5   | 7   | mA   |
| I <sub>BSx</sub>                         | Bootstrap pin leakage current                           | V <sub>BSTx</sub> = V <sub>SHx</sub> = 60V, V <sub>GVDD</sub> = 0V, nSLEEP = LOW   | 5   | 10  | 16  | μA   |
| I <sub>BS_TRAN</sub>                     | Bootstrap pin active mode transient leakage current     | INHx = INHx = Switching@20kHz, No FETs connected   | 60  | 115 | 300 | μA   |
| I <sub>BS_DC_SRC</sub>                   | Bootstrap pin active mode leakage static source current | INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V <sub>PVDD</sub> = V <sub>SHx</sub> = V <sub>GVDD</sub> = 12V, V <sub>BSTx</sub> - V <sub>SHx</sub> = 5V  | 135 | 200 | 280 | μA   |
|  |   | INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V <sub>PVDD</sub> = V <sub>SHx</sub> = V <sub>GVDD</sub> = 12V, V <sub>BSTx</sub> - V <sub>SHx</sub> = 7V  | 70  | 105 | 145 | μA   |
|  |   | INHx = LOW, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V <sub>PVDD</sub> = V <sub>SHx</sub> = V <sub>GVDD</sub> = 12V, V <sub>BSTx</sub> - V <sub>SHx</sub> = 5V   | 25  | 50  | 90  | μA   |
|  |   | INHx = LOW, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V <sub>PVDD</sub> = V <sub>SHx</sub> = V <sub>GVDD</sub> = 12V, V <sub>BSTx</sub> - V <sub>SHx</sub> = 7V   | 16  | 28  | 50  | μA   |
| I <sub>BS_DC_SINK</sub>                  | Bootstrap pin active mode leakage static sink current   | INHx = LOW, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V <sub>PVDD</sub> = V <sub>SHx</sub> = V <sub>GVDD</sub> = 12V, V <sub>BSTx</sub> - V <sub>SHx</sub> = 12V  | 10  | 40  | 90  | μA   |
|  |   | INHx = High, INLx = LOW, INLy = INLz = HIGH, nSLEEP = HIGH, V <sub>PVDD</sub> = V <sub>SHx</sub> = V <sub>GVDD</sub> = 12V, V <sub>BSTx</sub> - V <sub>SHx</sub> = 12V | 14  | 45  | 91  | μA   |
| I <sub>SHx</sub>                         | Source pin leakage current                              | INHx = INLx = LOW, V <sub>BSTx</sub> - V <sub>SHx</sub> = 15, V <sub>SHx</sub> = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW   | 80  | 145 | 210 | μA   |
|  |   | INHx = INLx = LOW, V <sub>BSTx</sub> - V <sub>SHx</sub> = 11, V <sub>SHx</sub> = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW   | 15  | 20  | 30  | μA   |
|  |   | INHx = High, INLx = LOW, V <sub>BSTx</sub> - V <sub>SHx</sub> = 15, V <sub>SHx</sub> = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW   | 80  | 145 | 210 | μA   |
|  |   | INHx = HIGH, INLx = LOW, V <sub>BSTx</sub> - V <sub>SHx</sub> = 11, V <sub>SHx</sub> = 0 to 60V, nSLEEP = HIGH, DRVOFF = LOW   | 13  | 25  | 35  | μA   |



4.5 V ≤ V<sub>PVDD</sub> ≤ 60 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>PVDD</sub> = 24 V

| PARAMETER   |   | TEST CONDITIONS  | MIN                       | TYP  | MAX  | UNIT |
|---|---|--|---------------------------|------|------|------|
| t <sub>WAKE</sub>                                   | Turnon time (nSLEEP)                                  | nSLEEP = HIGH to Active mode (Outputs Ready), DRVOFF = LOW, C <sub>GVDD</sub> = 10 uF, C <sub>BSTx</sub> = 1 uF                |                           | 1    | 2    | ms   |
|   |   | nSLEEP = High to Active mode (Outputs Ready). C <sub>GVDD</sub> = 100 uF, C <sub>AVDD</sub> = 10 uF, C <sub>BSTx</sub> = 10 uF |                           | 10   | 15   | ms   |
|   |   | V <sub>PVDD</sub> = 12V, nSLEEP = HIGH to Active mode (Outputs Ready), DRVOFF = LOW, C <sub>GVDD</sub> = 10 uF                 |                           | 1    | 2    | ms   |
|   | Turnon time (DRVOFF)                                  | DRVOFF = LOW to Active mode (Outputs Ready), nSLEEP = High   |                           | 0.05 | 0.1  | ms   |
| t <sub>SLEEP</sub>                                  | Turnoff time  | nSLEEP = LOW to Sleep mode   |                           |      | 20   | us   |
| t <sub>RST</sub>                                    | Minimum Reset Pulse Time                              | nSLEEP = LOW period to reset faults  | 1                         |      | 1.2  | us   |
| V <sub>GVDD_RT</sub>                                | GVDD Gate driver regulator voltage (Room Temperature) | V <sub>PVDD</sub> ≥ 40 V, I <sub>GS</sub> = 10 mA, T <sub>J</sub> = 25°C   | 11.8                      | 13   | 15   | V    |
|   |   | 22 V ≤V <sub>PVDD</sub> ≤ 40 V, I <sub>GS</sub> = 30 mA, T <sub>J</sub> = 25°C   | 11.8                      | 13   | 15   | V    |
|   |   | 8 V ≤V <sub>PVDD</sub> ≤ 22 V, I <sub>GS</sub> = 30 mA, T <sub>J</sub> = 25°C  | 11.8                      | 13   | 15   | V    |
|   |   | 6.75 V ≤V <sub>PVDD</sub> ≤ 8 V, I <sub>GS</sub> = 10 mA, T <sub>J</sub> = 25°C  | 11.8                      | 13   | 14.5 | V    |
|   |   | 4.5 V ≤V <sub>PVDD</sub> ≤ 6.75 V, I <sub>GS</sub> = 10 mA, T <sub>J</sub> = 25°C  | 2*V <sub>PVDD</sub> - 1   | 13.5 | V    |      |
| V <sub>GVDD</sub>                                   | GVDD Gate driver regulator voltage                    | V <sub>PVDD</sub> ≥ 40 V, I <sub>GS</sub> = 10 mA  | 11.5                      |      | 15.5 | V    |
|   |   | 22 V ≤V <sub>PVDD</sub> ≤ 40 V, I <sub>GS</sub> = 30 mA  | 11.5                      |      | 15.5 | V    |
|   |   | 8 V ≤V <sub>PVDD</sub> ≤ 22 V; I <sub>GS</sub> = 30 mA   | 11.5                      |      | 15.5 | V    |
|   |   | 6.75 V ≤V <sub>PVDD</sub> ≤ 8 V, I <sub>GS</sub> = 10 mA   | 11.5                      |      | 14.5 | V    |
|   |   | 4.5 V ≤V <sub>PVDD</sub> ≤ 6.75 V, I <sub>GS</sub> = 10 mA   | 2*V <sub>PVDD</sub> - 1.4 | 13.5 | V    |      |
| V <sub>AVDD_RT</sub>                                | AVDD Analog regulator voltage (Room Temperature)      | V <sub>PVDD</sub> ≥ 6 V, 0 mA ≤ I <sub>AVDD</sub> ≤ 30 mA, T <sub>J</sub> = 25°C   | 3.26                      | 3.3  | 3.33 | V    |
|   |   | V <sub>PVDD</sub> ≥ 6 V, 30 mA ≤ I <sub>AVDD</sub> ≤ 80 mA, T <sub>J</sub> = 25°C  | 3.2                       | 3.3  | 3.4  | V    |
|   |   | V <sub>PVDD</sub> ≤ 6 V, 0 mA ≤ I <sub>AVDD</sub> ≤ 50 mA, T <sub>J</sub> = 25°C   | 3.13                      | 3.3  | 3.46 | V    |
| V <sub>AVDD</sub>                                   | AVDD Analog regulator voltage                         | V <sub>PVDD</sub> ≥ 6 V, 0 mA ≤ I <sub>AVDD</sub> ≤ 80 mA  | 3.2                       | 3.3  | 3.4  | V    |
|   |   | V <sub>PVDD</sub> ≤ 6 V, 0 mA ≤ I <sub>AVDD</sub> ≤ 50 mA  | 3.125                     | 3.3  | 3.5  | V    |
| LOGIC-LEVEL INPUTS (DRVOFF, INHx, INLx, nSLEEP etc) |   |  |                           |      |      |      |
| V <sub>IL</sub>                                     | Input logic low voltage                               | DRVOFF   |                           |      | 0.8  | V    |
|   |   | INLx, INHx pins  |                           |      | 0.8  | V    |
| V <sub>IH</sub>                                     | Input logic high voltage                              | DRVOFF   | 2.2                       |      |      | V    |
|   |   | INLx, INHx pins  | 2.2                       |      |      | V    |
| V <sub>HYS</sub>                                    | Input hysteresis                                      | DRVOFF   | 200                       | 400  | 650  | mV   |
|   |   | INLx, INHx pins  | 45                        | 240  | 350  | mV   |
| I <sub>IL</sub>                                     | Input logic low current                               | V <sub>PIN</sub> (Pin Voltage) = 0 V;  | -1                        | 0    | 1    | μA   |
| I <sub>IH</sub>                                     | Input logic high current                              | nSLEEP, V <sub>PIN</sub> (Pin Voltage) = 65 V;   | 3                         | 6.5  | 10   | μA   |
|   |   | nSLEEP, V <sub>PIN</sub> (Pin Voltage) = 5 V;  | 3                         | 6    | 10   | μA   |
|   |   | Other pins, V <sub>PIN</sub> (Pin Voltage) = 5 V;  | 7                         | 20   | 35   | μA   |
| R <sub>PD_DRVOFF</sub>                              | Input pulldown resistance                             | DRVOFF To GND  | 100                       | 200  | 300  | k Ω  |
| R <sub>PD_nSLEEP</sub>                              | Input pulldown resistance                             | nSLEEP To GND  | 500                       | 800  | 1500 | k Ω  |

4.5 V ≤ V<sub>PVDD</sub> ≤ 60 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>PVDD</sub> = 24 V

| PARAMETER                                |   | TEST CONDITIONS   | MIN                   | TYP                    | MAX                   | UNIT |
|--|---|---|-----------------------|------------------------|-----------------------|------|
| R <sub>PD</sub>                          | Input pulldown resistance   | All other pins To GND   | 150                   | 250                    | 350                   | kΩ   |
| <b>FOUR-LEVEL INPUTS (GAIN)</b>          |   |   |                       |                        |                       |      |
| V <sub>L1</sub>                          | Input level 1 voltage   | Tied to GND   | 0                     | 0.18*AV <sub>DD</sub>  |                       | V    |
| V <sub>L2</sub>                          | Input level 2 voltage   | 50 kΩ +/- 5% tied to GND  | 0.48*AV <sub>DD</sub> | 0.5*AV <sub>DD</sub>   | 0.52*AV <sub>DD</sub> | V    |
| V <sub>L3</sub>                          | Input level 3 voltage   | 200 kΩ +/- 5% tied to GND   | 0.82*AV <sub>DD</sub> | 0.833*AV <sub>DD</sub> | 0.85*AV <sub>DD</sub> | V    |
| V <sub>L4</sub>                          | Input level 4 voltage   | HiZ or Connect to AVDD  |                       | AVDD                   |                       | V    |
| R <sub>PU</sub>                          | Input pullup resistance   | GAIN To AVDD  | 80                    | 100                    | 120                   | kΩ   |
| <b>OPEN-DRAIN OUTPUTS (nFAULT etc)</b>   |   |   |                       |                        |                       |      |
| V <sub>OL</sub>                          | Output logic low voltage  | I <sub>OD</sub> = 5 mA  |                       |                        | 0.4                   | V    |
| I <sub>OZ</sub>                          | Output logic high current   | V <sub>OD</sub> = 5 V   | -1                    |                        | 1                     | μA   |
| C <sub>OD</sub>                          | Output capacitance  | V <sub>OD</sub> = 5 V   |                       |                        | 30                    | pF   |
| <b>GATE DRIVERS (GHx, GLx, SHx, SLx)</b> |   |   |                       |                        |                       |      |
| V <sub>GSHx_LO</sub>                     | High-side gate drive low level voltage  | I <sub>GLx</sub> = -100 mA; V <sub>GVDD</sub> = 12V; No FETs connected                          | 0.05                  | 0.11                   | 0.24                  | V    |
| V <sub>GSHx_HI</sub>                     | High-side gate drive high level voltage (V <sub>BSTx</sub> - V <sub>GHx</sub> ) | I <sub>GHx</sub> = 100 mA; V <sub>GVDD</sub> = 12V; No FETs connected                           | 0.28                  | 0.44                   | 0.82                  | V    |
| V <sub>GSLx_LO</sub>                     | Low-side gate drive low level voltage   | I <sub>GLx</sub> = -100 mA; V <sub>GVDD</sub> = 12V; No FETs connected                          | 0.05                  | 0.11                   | 0.27                  | V    |
| V <sub>GSLx_HI</sub>                     | Low-side gate drive high level voltage (V <sub>GVDD</sub> - V <sub>GHx</sub> )  | I <sub>GHx</sub> = 100 mA; V <sub>GVDD</sub> = 12V; No FETs connected                           | 0.28                  | 0.44                   | 0.82                  | V    |
| V <sub>GSH_100_PH</sub>                  | High-side gate drive voltage in steady state with 100 % duty cycle (GHx- SHx)   | INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, V <sub>PVDD</sub> > 15V, V <sub>GVDD</sub> ≥ 11.5V | 8.4                   | 9.6                    | 11.1                  | V    |
|  |   | INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, V <sub>GVDD</sub> ≥ 11.5V                          | 7.5                   | 8.3                    | 9                     | V    |
|  |   | INHx = HIGH, INLx = LOW, INLy = INLz = HIGH, 7V ≥ V <sub>GVDD</sub> ≥ 8V                        | 5.7                   | 6.5                    | 7.6                   | V    |
| R <sub>DS(ON)_PU_HS</sub>                | High-side pullup switch resistance  | I <sub>GHx</sub> = 100 mA; V <sub>GVDD</sub> = 12V  | 2.7                   | 4.5                    | 8.4                   | Ω    |
| R <sub>DS(ON)_PD_HS</sub>                | High-side pulldown switch resistance  | I <sub>GHx</sub> = 100 mA; V <sub>GVDD</sub> = 12V  | 0.5                   | 1.1                    | 2.4                   | Ω    |
| R <sub>DS(ON)_PU_LS</sub>                | Low-side pullup switch resistance   | I <sub>GLx</sub> = 100 mA; V <sub>GVDD</sub> = 12V  | 2.7                   | 4.5                    | 8.3                   | Ω    |
| R <sub>DS(ON)_PD_LS</sub>                | Low-side pulldown switch resistance   | I <sub>GLx</sub> = 100 mA; V <sub>GVDD</sub> = 12V  | 0.5                   | 1.1                    | 2.8                   | Ω    |
| I <sub>DRIVEP_HS</sub>                   | High-side peak source gate current  | V <sub>GSHx</sub> = 12V   | 550                   | 1000                   | 1575                  | mA   |
| I <sub>DRIVEN_HS</sub>                   | High-side peak sink gate current  | V <sub>GSHx</sub> = 0V  | 1150                  | 2000                   | 2675                  | mA   |
| I <sub>DRIVEP_LS</sub>                   | Low-side peak source gate current   | V <sub>GSLx</sub> = 12V   | 550                   | 1000                   | 1575                  | mA   |
| I <sub>DRIVEN_LS</sub>                   | Low-side peak sink gate current   | V <sub>GSLx</sub> = 0V  | 1150                  | 2000                   | 2675                  | mA   |
| R <sub>PD_LS</sub>                       | Low-side passive pull down  | GLx to LSS  | 80                    | 100                    | 120                   | kΩ   |
| R <sub>PDSA_HS</sub>                     | High-side semiactive pull down  | GHx to SHx, V <sub>GSHx</sub> = 2V  | 8                     | 10                     | 12.5                  | kΩ   |
| <b>GATE DRIVERS TIMINGS</b>              |   |   |                       |                        |                       |      |
| t <sub>PDR_LS</sub>                      | Low-side rising propagation delay   | INLx to GLx rising, V <sub>GVDD</sub> > 8V  | 70                    | 100                    | 145                   | ns   |
| t <sub>PDF_LS</sub>                      | Low-side falling propagation delay  | INLx to GLx falling, V <sub>GVDD</sub> > 8V   | 70                    | 100                    | 135                   | ns   |
| t <sub>PDR_HS</sub>                      | High-side rising propagation delay  | INHx to GHx rising, V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V               | 65                    | 100                    | 145                   | ns   |
| t <sub>PDF_HS</sub>                      | High-side falling propagation delay   | INHx to GHx falling, V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V              | 70                    | 100                    | 140                   | ns   |

4.5 V  $\leq V_{PVDD} \leq 60$  V,  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{PVDD} = 24$  V

| PARAMETER  |   | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT   |
|--|---|---|-------|------|------|--------|
| t <sub>PD_MATCH_P<br/>H</sub>                    | Matching propagation delay per phase  | GLx turning ON to GLx turning OFF,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx  | -25   | ±4   | 25   | ns     |
|  |   | GLx turning OFF to GHx turning ON,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx  | -28   | ±4   | 28   | ns     |
|  |   | GHx turning ON to GHx turning OFF,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx  | -25   | ±4   | 25   | ns     |
|  |   | GHx turning OFF to GLx turning ON,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx  | -25   | ±4   | 25   | ns     |
| t <sub>PD_MATCH_P<br/>H_PH</sub>                 | Matching propagation delay phase to phase                                   | GHx turning ON to GHy turning ON,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx   | -10   | ±4   | 10   | ns     |
|  |   | GLx turning ON to GLy turning ON,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx   | -10   | ±4   | 10   | ns     |
|  |   | GHx turning OFF to GHy turning OFF,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx | -15   | ±4   | 15   | ns     |
|  |   | GLx turning OFF to GLy turning OFF,<br>V <sub>GVDD</sub> = V <sub>BSTx</sub> - V <sub>SHx</sub> > 8V; SHx = 0V to 60V, No load on GHx and GLx | -10   | ±4   | 10   | ns     |
| t <sub>PW_MIN</sub>                              | Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx |   | 18    | 32   | 45   | ns     |
| t <sub>DEAD</sub>                                | Gate drive dead time configurable range                                     |   | 50    |      | 2000 | ns     |
| t <sub>DEAD</sub>                                | Gate drive dead time  | DT pin floating   | 35    | 55   | 90   | ns     |
|  |   | DT pin connected to GND   | 25    | 55   | 80   | ns     |
|  |   | 10 kΩ between DT pin and GND  | 75    | 100  | 140  | ns     |
|  |   | 390 kΩ between DT pin and GND   | 1350  | 2000 | 2650 | ns     |
| BOOTSTRAP DIODES                                 |   |   |       |      |      |        |
| V <sub>BOOTD</sub>                               | Bootstrap diode forward voltage   | I <sub>BOOT</sub> = 100 μA  |       |      | 0.8  | V      |
|  |   | I <sub>BOOT</sub> = 100 mA  |       |      | 1.6  | V      |
| R <sub>BOOTD</sub>                               | Bootstrap dynamic resistance ( Δ V <sub>BOOTD</sub> / Δ I <sub>BOOT</sub> ) | I <sub>BOOT</sub> = 100 mA and 50 mA  | 4.5   | 5.5  | 9    | Ω      |
| CURRENT SHUNT AMPLIFIERS (SNx, SOx, SPx, CSAREF) |   |   |       |      |      |        |
| A <sub>CSA</sub>                                 | Sense amplifier gain  | CSAGAIN = Tied to GND   | 4.92  | 5    | 5.05 | V/V    |
|  |   | CSAGAIN = 50kΩ ±5% tied to GND  | 9.9   | 10   | 10.1 | V/V    |
|  |   | CSAGAIN = 200kΩ ±5% tied to GND   | 19.75 | 20   | 20.2 | V/V    |
|  |   | CSAGAIN =Hi-Z;  | 39.6  | 40   | 40.6 | V/V    |
| A <sub>CSA_ERR</sub>                             | Sense amplifier gain error  | T <sub>J</sub> = 25°C   | -1.5  |      | 1.5  | %      |
| A <sub>CSA_ERR_D<br/>RIFT</sub>                  | Sense amplifier gain error temperature drift                                |   | -20   |      | 20   | ppm/°C |
| NL   | Non linearity Error   |   |       | 0.01 | 0.05 | %      |

4.5 V ≤ V<sub>PVDD</sub> ≤ 60 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>PVDD</sub> = 24 V

| PARAMETER              |                                    | TEST CONDITIONS   | MIN   | TYP   | MAX                        | UNIT  |
|------------------------|------------------------------------|---|-------|-------|----------------------------|-------|
| t <sub>SET</sub>       | Settling time to ±1%               | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 5 V/V, C <sub>LOAD</sub> = 500pF                          |       | 0.6   | 1                          | μs    |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 10 V/V, C <sub>LOAD</sub> = 500pF                         |       | 0.6   | 1.1                        | μs    |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 20 V/V, C <sub>LOAD</sub> = 500pF                         |       | 0.7   | 1.2                        | μs    |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 40 V/V, C <sub>LOAD</sub> = 500pF                         |       | 0.8   | 1.7                        | μs    |
| t <sub>SET</sub>       | Settling time to ±1%               | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 5 V/V, C <sub>LOAD</sub> = 60pF                           |       | 0.3   | 0.5                        | μs    |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 10 V/V, C <sub>LOAD</sub> = 60pF                          |       | 0.3   | 0.5                        | μs    |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 20 V/V, C <sub>LOAD</sub> = 60pF                          |       | 0.3   | 0.65                       | μs    |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 40 V/V, C <sub>LOAD</sub> = 60pF                          |       | 0.3   | 0.8                        | μs    |
| BW                     | Bandwidth                          | A <sub>CSA</sub> = 5 V/V, C <sub>LOAD</sub> = 60-pF, small signal -3 dB                                 | 3     | 5     | 7                          | MHz   |
|                        |                                    | A <sub>CSA</sub> = 10 V/V, C <sub>LOAD</sub> = 60-pF, small signal -3 dB                                | 2.5   | 4.8   | 6.6                        | MHz   |
|                        |                                    | A <sub>CSA</sub> = 20 V/V, C <sub>LOAD</sub> = 60-pF, small signal -3 dB                                | 2     | 4     | 5.4                        | MHz   |
|                        |                                    | A <sub>CSA</sub> = 40 V/V, C <sub>LOAD</sub> = 60-pF, small signal -3 dB                                | 1.75  | 3     | 4.2                        | MHz   |
| t <sub>SR</sub>        | Output slew rate                   | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 5 V/V, C <sub>LOAD</sub> = 60-pF, low to high transition  |       | 12    |                            | V/μs  |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 10 V/V, C <sub>LOAD</sub> = 60-pF, low to high transition |       | 13    |                            | V/μs  |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 20 V/V, C <sub>LOAD</sub> = 60-pF, low to high transition |       | 11    |                            | V/μs  |
|                        |                                    | V <sub>STEP</sub> = 1.6 V, A <sub>CSA</sub> = 40 V/V, C <sub>LOAD</sub> = 60-pF, low to high transition |       | 11    |                            | V/μs  |
| V <sub>SWING</sub>     | Output voltage range               | V <sub>CSAREF</sub> = 3   | 0.25  |       | 2.75                       | V     |
| V <sub>SWING</sub>     | Output voltage range               | V <sub>CSAREF</sub> = 5.5   | 0.25  |       | 5.25                       | V     |
| V <sub>SWING</sub>     | Output voltage range               | V <sub>CSAREF</sub> = 3 to 5.5 V  | 0.25  |       | V <sub>CSAREF</sub> - 0.25 | V     |
| V <sub>COM</sub>       | Common-mode input range            |   | -0.15 |       | 0.15                       | V     |
| V <sub>DIFF</sub>      | Differential-mode input range      |   | -0.3  |       | 0.3                        | V     |
| V <sub>OFF</sub>       | Input offset voltage               | V <sub>SP</sub> = V <sub>SN</sub> = GND; T <sub>J</sub> = -40°C, CSA_VREF = 0                           | -1.5  |       | 1.5                        | mV    |
| V <sub>OFF</sub>       | Input offset voltage               | V <sub>SP</sub> = V <sub>SN</sub> = GND; T <sub>J</sub> = 25°C, CSA_VREF = 0                            | -1.2  |       | 1.2                        | mV    |
| V <sub>OFF</sub>       | Input offset voltage               | V <sub>SP</sub> = V <sub>SN</sub> = GND; T <sub>J</sub> = 175°C, CSA_VREF = 0                           | -1.5  |       | 1.5                        | mV    |
| V <sub>OFF</sub>       | Input offset voltage               | V <sub>SP</sub> = V <sub>SN</sub> = GND   | -1.5  |       | 1.5                        | mV    |
| V <sub>OFF_DRIFT</sub> | Input drift offset voltage         | V <sub>SP</sub> = V <sub>SN</sub> = GND   |       | 8     | 10                         | μV/°C |
| V <sub>BIAS</sub>      | Output voltage bias ratio          | V <sub>SP</sub> = V <sub>SN</sub> = GND   | 0.122 | 0.125 | 0.128                      | V     |
| V <sub>BIAS_ACC</sub>  | Output voltage bias ratio accuracy | V <sub>SP</sub> = V <sub>SN</sub> = GND   | -1.2  |       | 1.2                        | %     |
| I <sub>BIAS</sub>      | Input bias current                 | V <sub>SP</sub> = V <sub>SN</sub> = GND, V <sub>CSAREF</sub> = 3V to 5.5V                               |       |       | 100                        | μA    |
| I <sub>BIAS_OFF</sub>  | Input bias current offset          | I <sub>SP</sub> - I <sub>SN</sub>   | -1    |       | 1                          | μA    |
| I <sub>CSASRC</sub>    | SO output sink current capability  |   | 5     | 7     | 11                         | mA    |

4.5 V ≤ V<sub>PVDD</sub> ≤ 60 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>PVDD</sub> = 24 V

| PARAMETER                 |   | TEST CONDITIONS  | MIN   | TYP  | MAX   | UNIT |
|---------------------------|---|--|-------|------|-------|------|
| I <sub>CSASRC</sub>       | SO ouput source current capability  |  | 2     | 3.7  | 6.6   | mA   |
| CMRR                      | Common-mode rejection ratio   | DC   |       | 80   |       | dB   |
|                           |   | 20 kHz   |       | 65   |       | dB   |
| PSRR                      | Power-supply rejection ratio (CSAREF)                                       | CSAREF to SOx, DC, Differential                                  |       | 80   |       | dB   |
|                           |   | CSAREF to SOx, 20 kHz, Differential                              |       | 70   |       | dB   |
| PSRR                      | Power-supply rejection ratio (CSAREF)                                       | CSAREF to SOx, 20 kHz, Single Ended                              |       | 40   |       | dB   |
| I <sub>CSA_SUP</sub>      | Supply current for CSA  | V <sub>CSAREF</sub> = 3.V to 5.5V                                |       | 1.5  | 2.1   | mA   |
| T <sub>CMREC</sub>        | Common mode recovery time   |  |       | 0.6  | 0.7   | us   |
| C <sub>LOAD</sub>         | Maximum load capacitance  |  |       | 10   |       | nF   |
| V <sub>OFF_OUT</sub>      | Output offset error   | A <sub>CSA</sub> = 5 V/V   | -3    |      | 3     | mV   |
|                           |   | A <sub>CSA</sub> = 10 V/V  | -4    |      | 4     | mV   |
|                           |   | A <sub>CSA</sub> = 20 V/V  | -5    |      | 5     | mV   |
|                           |   | A <sub>CSA</sub> = 40 V/V  | -6    |      | 6     | mV   |
| PROTECTION CIRCUITS       |   |  |       |      |       |      |
| V <sub>PVDD_UV</sub>      | PVDD undervoltage lockout threshold   | V <sub>PVDD</sub> rising   | 4.3   | 4.4  | 4.5   | V    |
|                           |   | V <sub>PVDD</sub> falling  | 4     | 4.1  | 4.25  |      |
| V <sub>PVDD_UV_HYS</sub>  | PVDD undervoltage lockout hysteresis  | Rising to falling threshold                                      | 225   | 265  | 325   | mV   |
| t <sub>PVDD_UV_DG</sub>   | PVDD undervoltage deglitch time   |  | 10    | 20   | 30    | μs   |
| V <sub>AVDD_POR</sub>     | AVDD supply POR threshold   | AVDD rising  | 2.7   | 2.85 | 3.0   | V    |
|                           |   | AVDD falling   | 2.5   | 2.65 | 2.8   |      |
| V <sub>AVDD_POR_HYS</sub> | AVDD POR hysteresis   | Rising to falling threshold                                      | 170   | 200  | 250   | mV   |
| t <sub>AVDD_POR_DG</sub>  | AVDD POR deglitch time  |  | 7     | 12   | 22    | μs   |
| V <sub>GVDD_UV</sub>      | GVDD undervoltage threshold   | V <sub>GVDD</sub> rising   | 7.3   | 7.5  | 7.8   | V    |
|                           |   | V <sub>GVDD</sub> falling  | 6.4   | 6.7  | 6.9   | V    |
| V <sub>GVDD_UV_HYS</sub>  | GVDD undervoltage hysteresis  | Rising to falling threshold                                      | 800   | 900  | 1000  | mV   |
| t <sub>GVDD_UV_DG</sub>   | GVDD undervoltage deglitch time   |  | 5     | 10   | 15    | μs   |
| V <sub>BST_UV</sub>       | Bootstrap undervoltage threshold  | V <sub>BSTx</sub> - V <sub>SHx</sub> ; V <sub>BSTx</sub> rising  | 3.9   | 4.45 | 5     | V    |
|                           |   | V <sub>BSTx</sub> - V <sub>SHx</sub> ; V <sub>BSTx</sub> falling | 3.7   | 4.2  | 4.8   | V    |
| V <sub>BST_UV_HYS</sub>   | Bootstrap undervoltage hysteresis   | Rising to falling threshold                                      | 150   | 220  | 285   | mV   |
| t <sub>BST_UV_DG</sub>    | Bootstrap undervoltage deglitch time  |  | 2     | 4    | 6     | μs   |
| V <sub>DS_LVL_RNG</sub>   | V <sub>DS</sub> overcurrent protection threshold linear range               |  | 0.1   |      | 2.5   | V    |
| V <sub>DS_DIS</sub>       | V <sub>DS</sub> overcurrent protection disable resistor                     | VDSLVL pin to GVDD   | 70    | 100  | 500   | kΩ   |
| V <sub>DS_LVL</sub>       | V <sub>DS</sub> overcurrent protection threshold Reference                  | VDSLVL = 100 kΩ to GVDD  | 3     | 4.2  | 5.5   | V    |
|                           |   | VDSLVL = 0.1V  | 0.065 | 0.1  | 0.145 | V    |
|                           |   | VDSLVL pin = 2.5V  | 2.2   | 2.5  | 2.8   |      |
| V <sub>SENSE_LVL</sub>    | V <sub>SENSE</sub> overcurrent protection threshold                         | LSS to GND pin = 0.5V  | 0.48  | 0.5  | 0.52  | V    |
| t <sub>DS_BLK</sub>       | V <sub>DS</sub> overcurrent protection blanking time                        |  | 0.5   | 1    | 2.7   | μs   |
| t <sub>DS_DG</sub>        | V <sub>DS</sub> and V <sub>SENSE</sub> overcurrent protection deglitch time |  | 1.5   | 3    | 5     | μs   |
| t <sub>SD_SINK_DIG</sub>  | DRVOFF peak sink current duration   |  | 3     | 5    | 7     | μs   |
| t <sub>SD_DIG</sub>       | DRVOFF digital shutdown delay   |  | 0.5   | 1.5  | 2.2   | μs   |
| t <sub>SD</sub>           | DRVOFF analog shutdown delay  |  | 7     | 14   | 21    | μs   |

$4.5\text{ V} \leq V_{\text{PVDD}} \leq 60\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_{\text{J}} \leq 150^{\circ}\text{C}$  (unless otherwise noted). Typical limits apply for  $T_{\text{A}} = 25^{\circ}\text{C}$ ,  $V_{\text{PVDD}} = 24\text{ V}$

| PARAMETER         |                              | TEST CONDITIONS        | MIN | TYP | MAX | UNIT               |
|-------------------|------------------------------|------------------------|-----|-----|-----|--------------------|
| $T_{\text{OTSD}}$ | Thermal shutdown temperature | $T_{\text{J}}$ rising; | 160 | 170 | 187 | $^{\circ}\text{C}$ |
| $T_{\text{HYS}}$  | Thermal shutdown hysteresis  |                        | 16  | 20  | 23  | $^{\circ}\text{C}$ |

## 7.6 Typical Characteristics

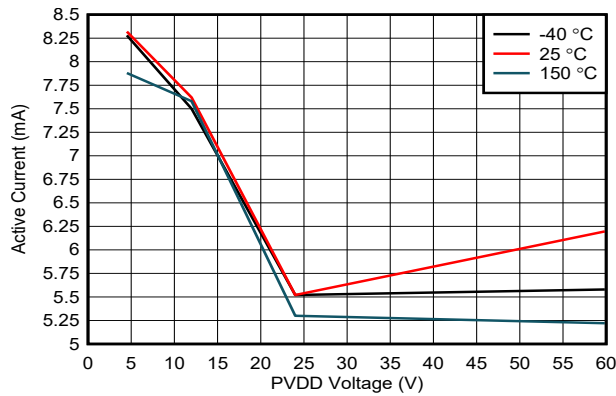


图 7-1. Supply Current over PVDD Voltage

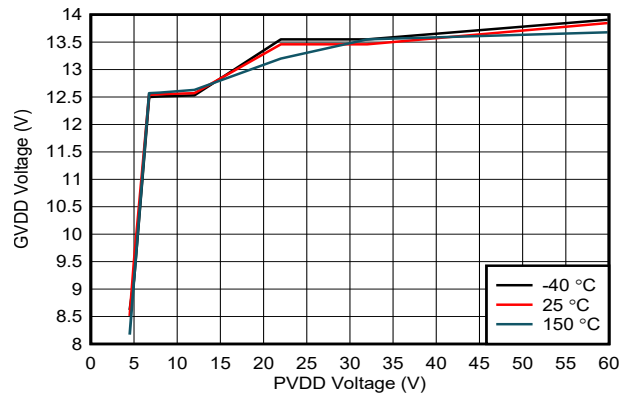


图 7-2. GVDD Voltage over PVDD Voltage

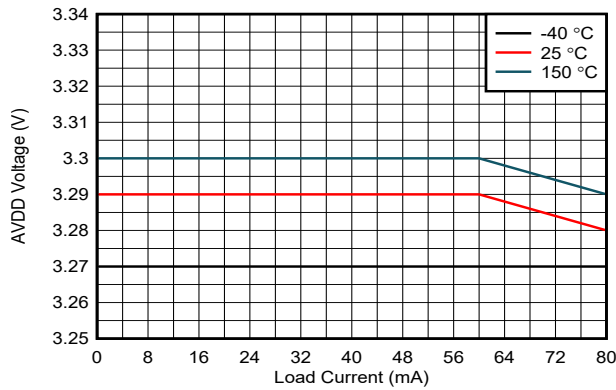


图 7-3. AVDD Voltage over Load Current

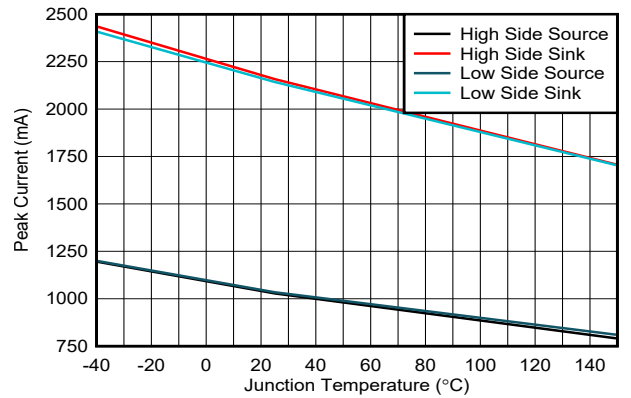


图 7-4. Driver Peak Current over Junction Temperature

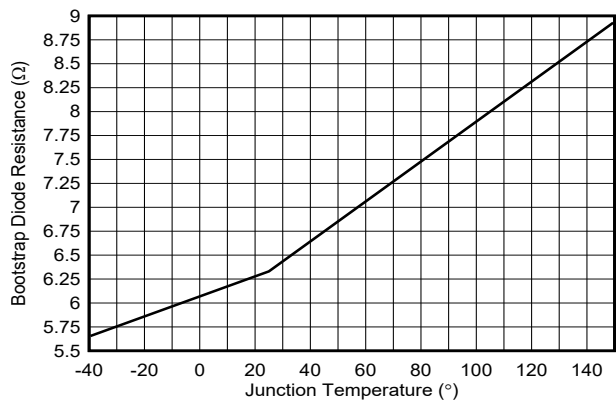


图 7-5. Bootstrap Diode Resistance over Junction Temperature

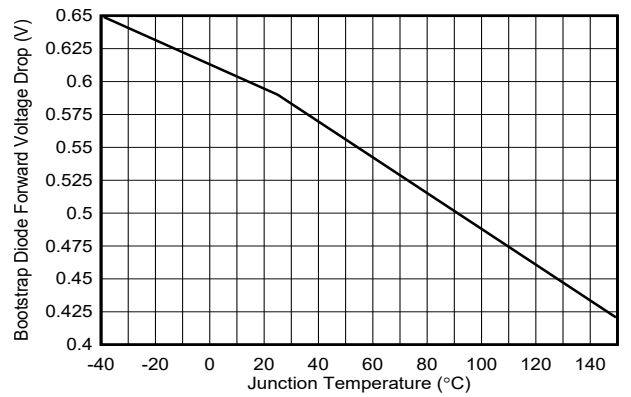


图 7-6. Bootstrap Diode Forward Voltage Drop over Junction Temperature

## 8 Detailed Description

### 8.1 Overview

The DRV8329 family of devices is an integrated three-phase gate driver supporting an input voltage range of 4.5-V to 60-V. These devices decrease system component count, cost, and complexity by integrating three independent half-bridge gate drivers, trickle charge pump, and a charge pump with linear regulator for the supply voltages of the high-side and low-side gate drivers. DRV8329 also integrates an accurate low voltage regulator (AVDD) capable of supporting 3.3 V at 80 mA output. A hardware interface allows for simple configuration of the motor driver and control of the motor.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1-A source, 2-A sink peak gate drive currents with a 30-mA average output current. A bootstrap circuit with capacitor generates the supply voltage of the high-side gate drive and a trickle charge pump is employed to support 100% duty cycle. The supply voltage of the low-side gate driver is generated using a charge pump with linear regulator GVDD from the PVDD power supply that regulates to 12 V.

In addition to the high level of device integration, the DRV8329 family of devices provides a wide range of integrated protection features. These features include power supply undervoltage lockout (PVDDUV), regulator undervoltage lockout (GVDDUV), Bootstrap Voltage undervoltage lockout (BSTUV),  $V_{DS}$  overcurrent monitoring (OCP), Sense resistor overcurrent monitoring (SEN\_OCP) and overtemperature shutdown (TSD). Fault events are indicated by the nFAULT pin.

The DRV8329 is available in 0.4-mm pitch, 5 × 4 mm 36-pin QFN surface-mount packages.



## 8.2 Functional Block Diagram

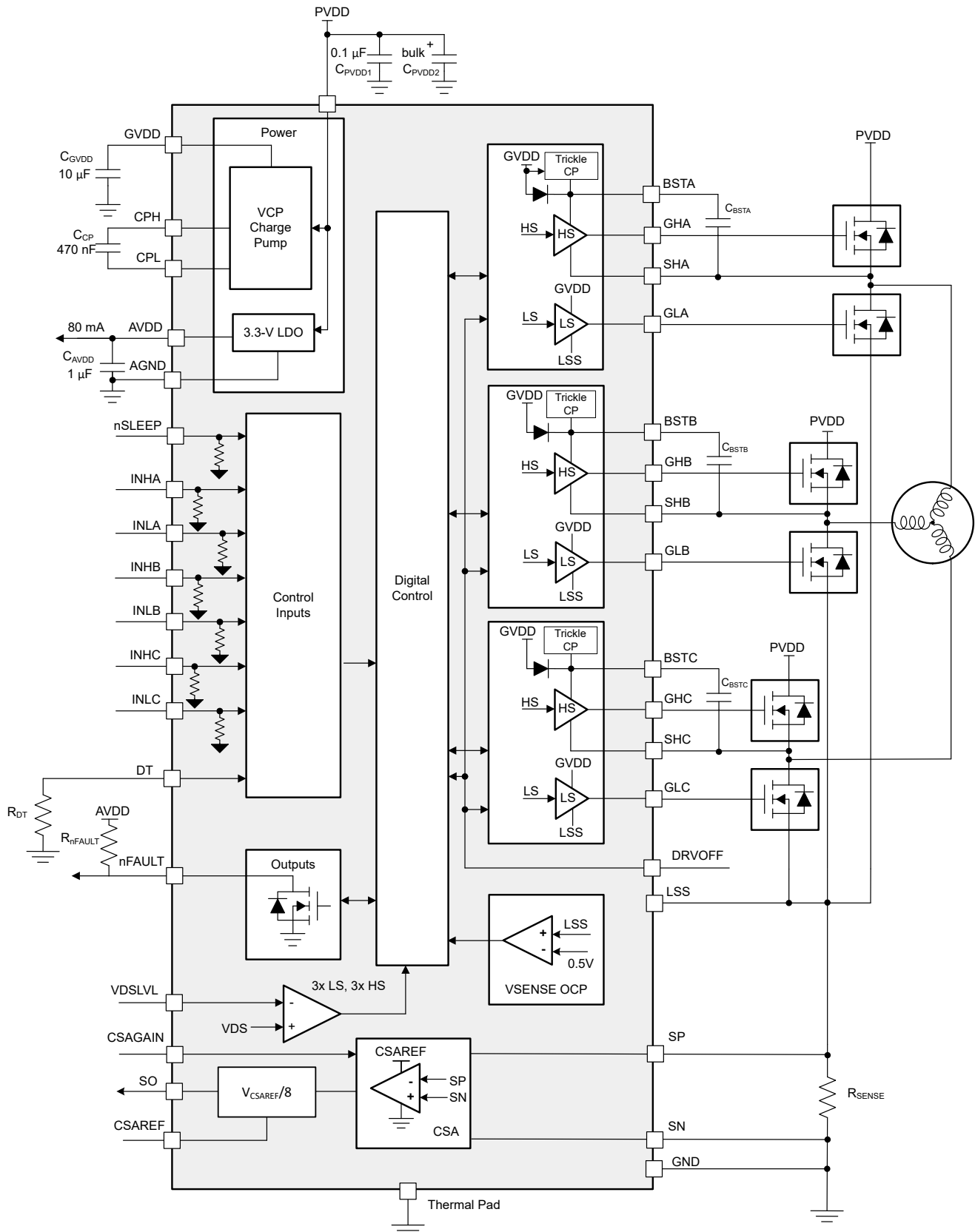


图 8-1. Block Diagram of DRV8329

## 8.3 Feature Description

表 8-1 lists the recommended values of the external components for the gate driver and the buck regulator.

表 8-1. DRV8329 External Components

| COMPONENTS          | PIN 1              | PIN 2  | RECOMMENDED   |
|---------------------|--------------------|--------|---|
| C <sub>PVDD1</sub>  | PVDD               | PGND   | X5R or X7R, 0.1-μF, >2x PVDD-rated capacitor  |
| C <sub>PVDD2</sub>  | PVDD               | PGND   | ≥ 10 μF, >2x PVDD-rated capacitor   |
| C <sub>CP</sub>     | CPH                | CPL    | X5R or X7R, 470-nF, PVDD-rated capacitor  |
| C <sub>GVDD</sub>   | GVDD               | GND    | X5R or X7R, ≥10-μF, 25V-rated capacitor   |
| C <sub>AVDD</sub>   | AVDD               | AGND   | X5R or X7R, ≥1-μF, 6.3-V capacitor  |
| C <sub>BSTx</sub>   | BSTx               | SHx    | X5R or X7R, 1-μF (typical), 25V-rated capacitor   |
| R <sub>nFAULT</sub> | VCC <sup>(1)</sup> | nFAULT | Pullup resistor (10 kΩ)   |
| R <sub>DT</sub>     | DT                 | AGND   | Hardware interface resistor. Refer to <a href="#">Deadtime and Cross-Conduction Prevention</a> for the details. |

(1) The VCC pin is not a pin on the DRV8329, but a VCC supply voltage pullup is required for the open-drain output, nFAULT. This pin can also be pulled up to AVDD.

### 8.3.1 Three BLDC Gate Drivers

The DRV8329 family of devices integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A charge pump is used to generate the GVDD to supply the correct gate bias voltage across a wide operating voltage range. The low side gate outputs are driven directly from GVDD, while the high side gate outputs are driven using a bootstrap circuit with an integrated diode. An internal trickle charge pump provides support for 100% duty cycle operation. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

#### 8.3.1.1 PWM Control Modes

##### 8.3.1.1.1 6x PWM Mode

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in 表 8-2.

表 8-2. 6x PWM Mode Truth Table

| INLx | INHx | GLx | GHx | SHx  |
|------|------|-----|-----|------|
| 0    | 0    | L   | L   | Hi-Z |
| 0    | 1    | L   | H   | H    |
| 1    | 0    | H   | L   | L    |
| 1    | 1    | L   | L   | Hi-Z |

### 8.3.1.1.2 3x PWM Mode

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in 表 8-3.

表 8-3. 3x PWM Mode Truth Table

| INLx | INHx | GLx | GHx | SHx  |
|------|------|-----|-----|------|
| 0    | X    | L   | L   | Hi-Z |
| 1    | 0    | H   | L   | L    |
| 1    | 1    | L   | H   | H    |

### 8.3.1.2 Device Hardware Interface

The DRV8329 utilize a hardware interface to configure different device settings. These hardware configurable inputs are DT and VDSLVL. General fault information is reported on the nFAULT pin.

- The DT pin configures the gate drive dead time. The dead time can adjusted by changing the resistor value from the DT pin to GND.
- The VDSLVL pin configures the voltage threshold of the  $V_{DS}$  overcurrent monitors. The voltage applied to the VDSLVL pin is directly used as reference for the VDS comparator

For more information on the hardware interface, see 节 8.3.3.

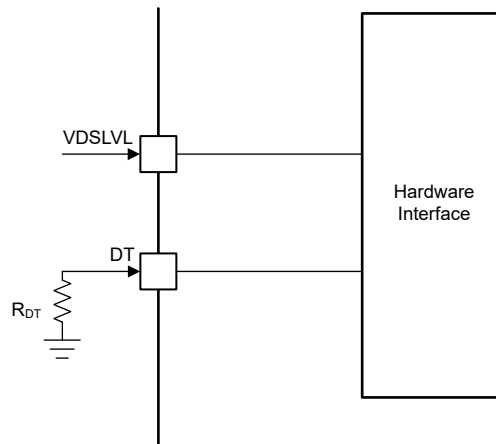


图 8-2. Hardware Interface

### 8.3.1.3 Gate Drive Architecture

The gate driver device use a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD regulator supply. The operating mode of GVDD depends on the voltage of PVDD, when the PVDD > 18V, the GVDD voltage is generated by an LDO, whereas PVDD < 18V, the GVDD voltage is generated by a charge pump. For the high-side gate drivers a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used between BSTx and SHx pins. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent voltage drop due to the leakage currents of the driver and external MOSFET.

The high-side gate driver has a semi-active pulldown and low side gate has passive pulldown to help prevent the external MOSFET from turning ON during sleep state or when the power supply is disconnected.

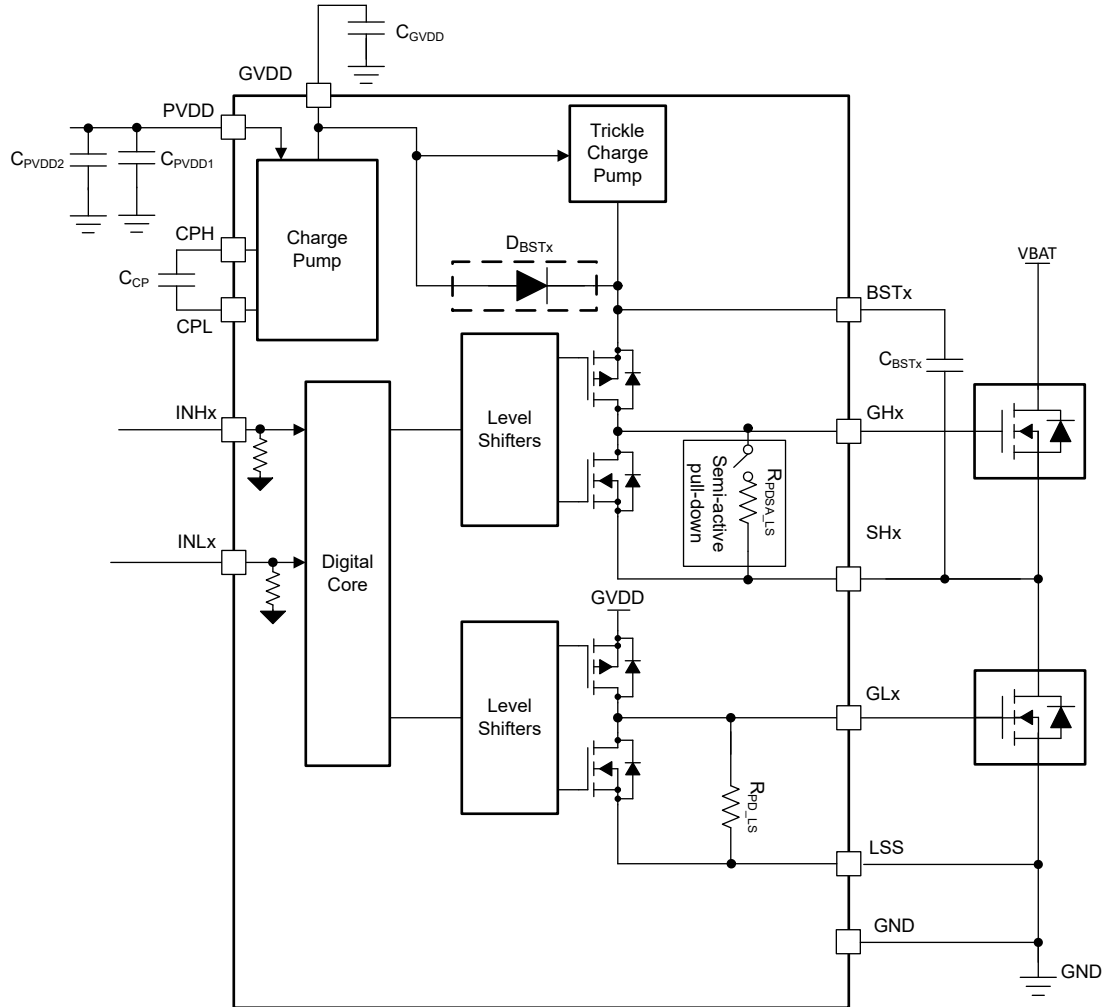


图 8-3. Gate Driver Block Diagram

#### 8.3.1.3.1 Propagation Delay

The propagation delay time ( $t_{pd}$ ) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the digital propagation delay, and the delay through the analog gate drivers.

To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

#### 8.3.1.3.2 Deadtime and Cross-Conduction Prevention

In the DRV8329, high- and low-side inputs operate independently, with an exception to prevent cross conduction when the high and low side of the same half-bridge are turned ON at same time. The device turns OFF high- and low- side output to prevent shoot through when high- and low-side inputs are logic high at same time.

The DRV8329 also provides dead time insertion to prevent both external MOSFETs of each half-bridge from switching on at the same time. In devices with a DT pin, deadtime can be linearly adjusted between 100 ns and 2000 ns by connecting a resistor between DT and ground. When the DT pin is left floating or connected to GND, a fixed deadtime of 55 ns (typical value) is inserted. The value of the resistor can be calculated using following equation.

$$R_{DT}(k\Omega) = \frac{Deadtime(ns)}{5} - 10 k\Omega \quad (1)$$

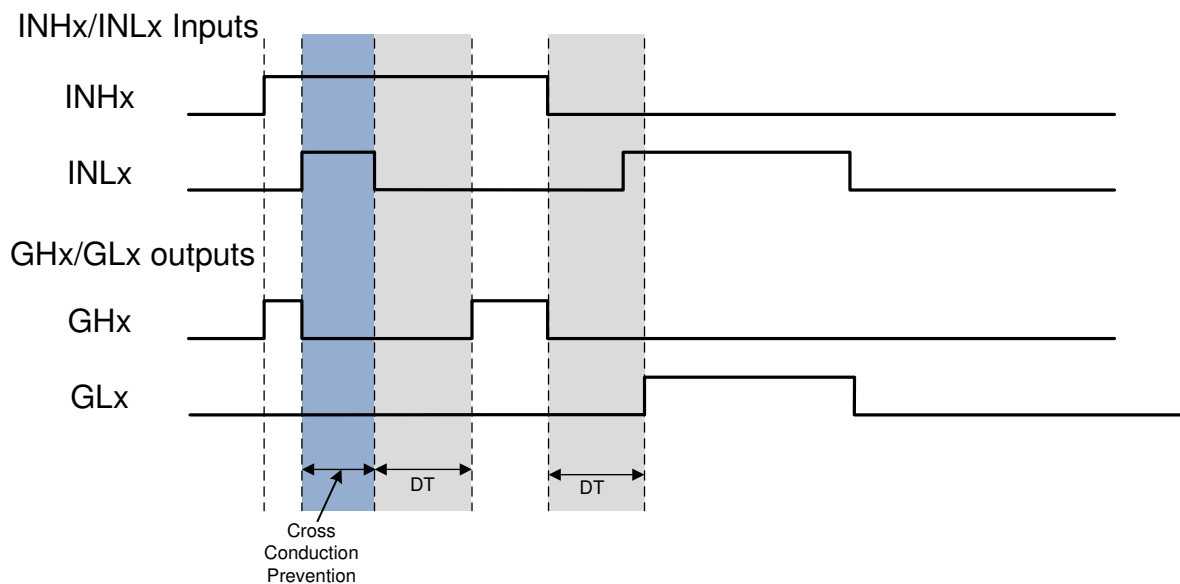


图 8-4. Cross Conduction Prevention and Deadtime Insertion

### 8.3.2 AVDD Linear Voltage Regulator

A 3.3-V, 80-mA linear regulator is available for use by external circuitry. The output of the LDO is fixed to 3.3-V. This regulator can provide the supply voltage for a low-power MCU or other circuitry with low supply current needs. The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1-μF, 6.3-V ceramic capacitor routed back to the AGND pin.

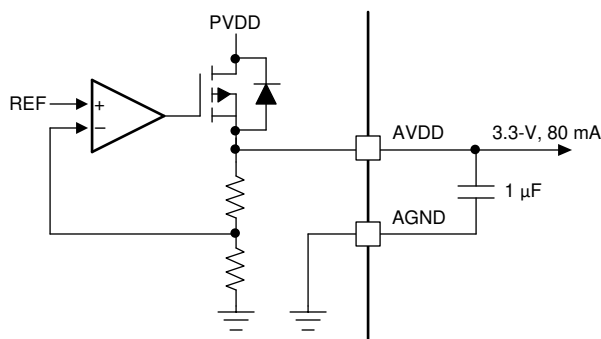


图 8-5. AVDD Linear Regulator Block Diagram

The power dissipated in the device by the AVDD linear regulator can be calculated as follows:  $P = (V_{PVDD} - V_{AVDD}) \times I_{AVDD}$

For example, at a  $V_{PVDD}$  of 24 V, drawing 20 mA out of AVDD results in a power dissipation as shown in 方程式 2.

$$P = (24 \text{ V} - 3.3 \text{ V}) \times 20 \text{ mA} = 414 \text{ mW} \quad (2)$$

### 8.3.3 Pin Diagrams

图 8-6 shows the input structure for the logic level pins, INHx and INLx. The input can be driven with a voltage or external resistor.

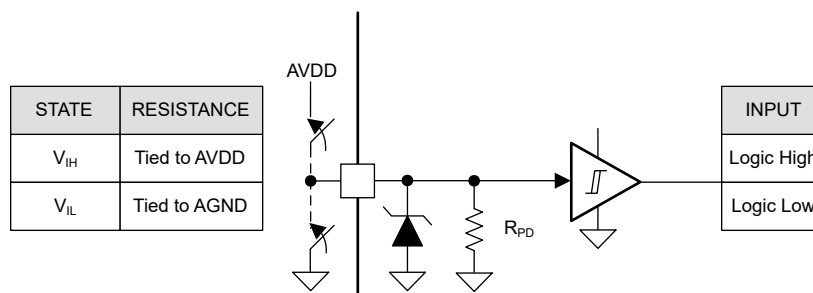


图 8-6. Logic-Level Input Pin Structure

图 8-7 shows the structure of the four level input pins, MODE and CSAGAIN, on hardware interface devices. The input can be set with an external resistor.

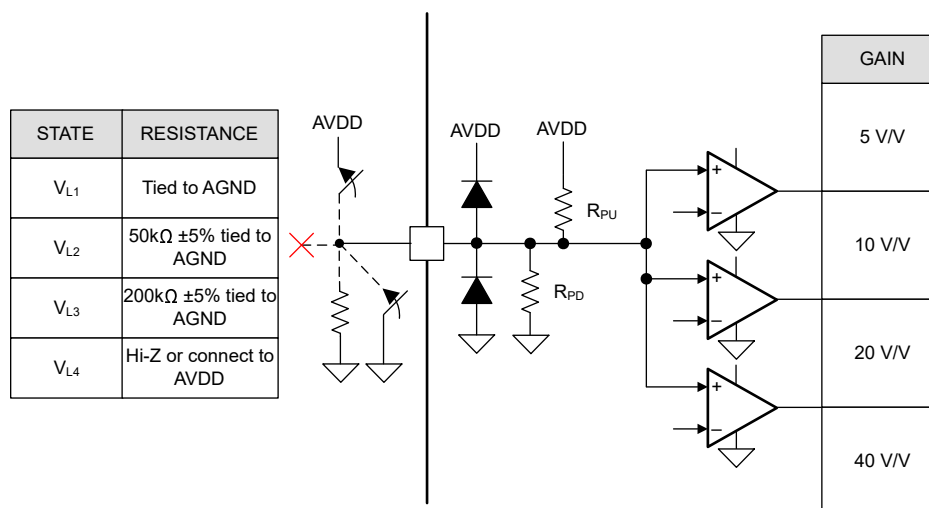


图 8-7. Four Level Input Pin Structure

图 8-8 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function correctly.

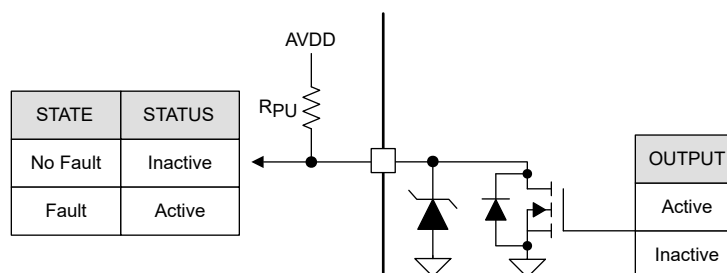


图 8-8. Open-Drain Output Pin Structure

### 8.3.4 Low-Side Current Sense Amplifiers

The DRV8329 integrates a high-performance low-side current sense amplifier for current measurements using a low-side shunt resistor. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. The current sense amplifier can be used to sense the sum of the half-bridge currents. The current sense amplifiers includes features such as configurable gain (CSAGAIN), and a voltage reference pin (CSAREF). The DRV8329 generates internally a common voltage of  $V_{CSAREF}/8$ .

The gain setting is adjustable between four different levels (5 V/V, 10 V/V, 20 V/V, and 40 V/V). Gain settings can be configured through CSAGAIN pin.

表 8-4. CSA Gain setting

| CSAGAIN pin                  | CSA Gain Setting |
|------------------------------|------------------|
| Connect to GND               | 5 V/V            |
| 50 k $\Omega$ +/- 5% to GND  | 10 V/V           |
| 200 k $\Omega$ +/- 5% to GND | 20 V/V           |
| HiZ or Connect to AVDD       | 40 V/V           |

#### 8.3.4.1 Current Sense Operation

DRV8329 internally generates a common mode voltage of  $V_{CSAREF}/8$  to obtain maximum resolution for current measurement. SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (CSAGAIN).

Use 方程式 3 to calculate the current through the shunt resistor ( $R_{SENSE}$ ).

$$I = \frac{V_{SO} - \frac{V_{CSAREF}}{8}}{CSAGAIN \times R_{SENSE}} \quad (3)$$

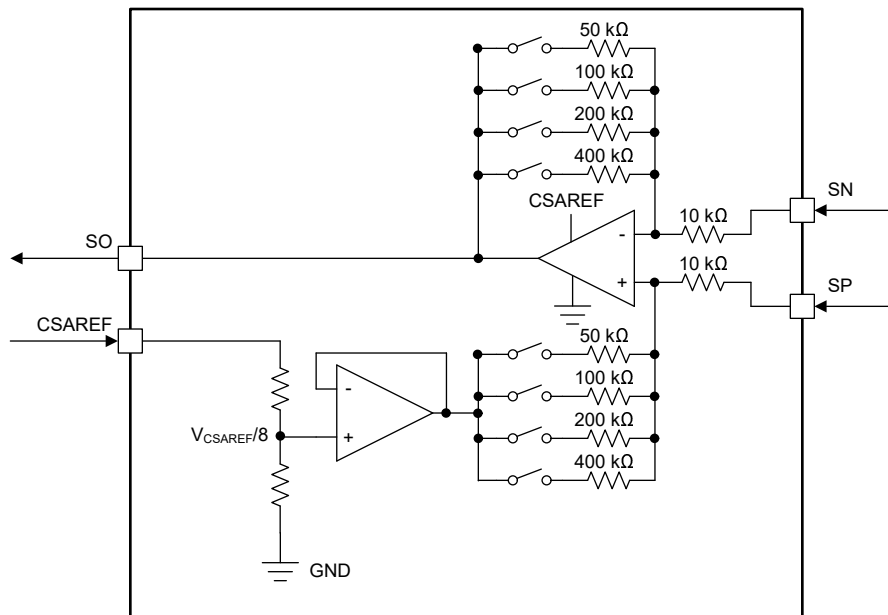


图 8-9. Current-Sense Configuration

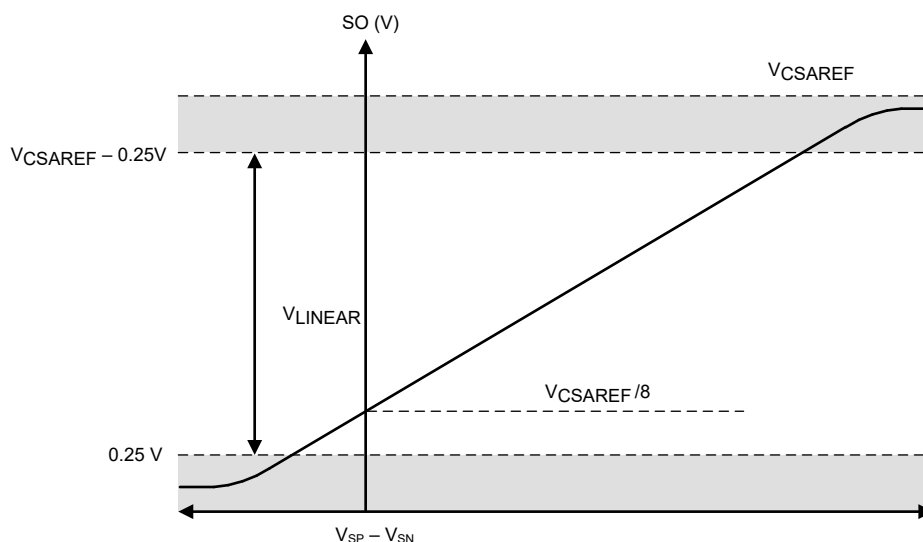


图 8-10. Current-Sense Output

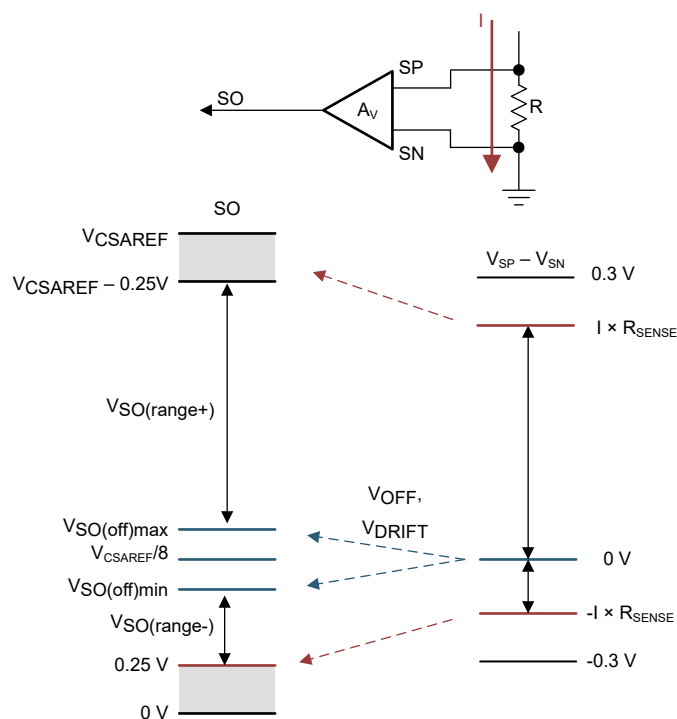


图 8-11. Current-Sense Regions

### 8.3.5 Gate Driver Shutdown Sequence (DRVOFF)

When DRVOFF is driven high, the gate driver goes into shutdown, overriding signals on inputs pins INHx and INLx. DRVOFF bypasses the digital control logic inside the device, and is connected directly to the gate driver output (see 图 8-12). This pin provides a mechanism for externally monitored faults to disable the gate driver by directly bypassing an external controller or the internal control logic. When the DRV8329 detects that the DRVOFF pin is driven high, it disables the gate driver and puts it into pull-down mode (see 图 8-13). The gate driver shutdown sequence proceeds as shown in 图 8-13. When the gate driver initiates the shutdown sequence, the active driver pull-down is applied at  $I_{\text{SINK}}$  current for the  $t_{\text{SD\_SINK\_DIG}}$  time, after which the gate driver moves to passive pull-down mode.



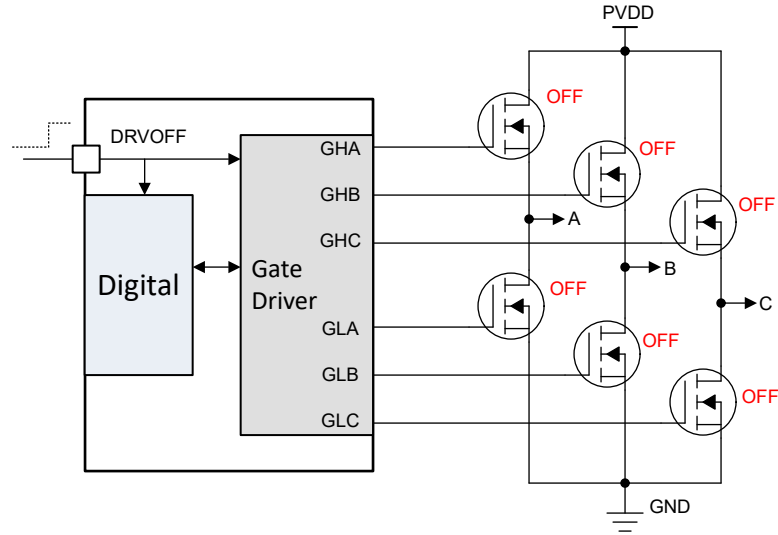


图 8-12. DRV8329 DRVOFF Gate Driver Output State

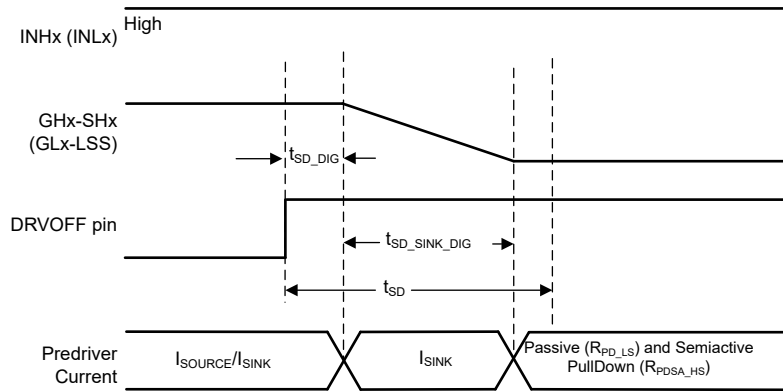


图 8-13. Gate Driver Shutdown Sequence

### 8.3.6 Gate Driver Protective Circuits

The DRV8329 are protected against PVDD undervoltage and overvoltage, AVDD power-on reset, bootstrap undervoltage, GVDD undervoltage, MOSFET  $V_{DS}$  and  $V_{SENSE}$  overcurrent events.

表 8-5. Fault Action and Response

| FAULT                             | CONDITION   | CONFIGURATION                            | REPORT | GATE DRIVER             | LOGIC    | RECOVERY                                 |
|-----------------------------------|---|--|--------|-------------------------|----------|--|
| PVDD undervoltage (PVDD_UV)       | $V_{PVDD} < V_{PVDD\_UV}$                             | -  | nFAULT | Disabled <sup>1</sup>   | Disabled | Automatic:<br>$V_{PVDD} > V_{PVDD\_UV}$  |
| AVDD POR (AVDD_POR)               | $V_{AVDD} < V_{AVDD\_POR}$                            | -  | nFAULT | Disabled <sup>1</sup>   | Disabled | Automatic:<br>$V_{AVDD} > V_{AVDD\_POR}$ |
| GVDD undervoltage (GVDD_UV)       | $V_{GVDD} < V_{GVDD\_UV}$                             | -  | nFAULT | Pulled Low <sup>2</sup> | Active   | Latched:<br>nSLEEP Reset Pulse           |
| BSTx undervoltage (BST_UV)        | $V_{BSTx} - V_{SHx} < V_{BST\_UV}$ and<br>INHx = High | -  | nFAULT | Pulled Low <sup>2</sup> | Active   | Latched:<br>nSLEEP Reset Pulse           |
| $V_{DS}$ overcurrent (VDS_OCP)    | $V_{DS} > V_{DS\_LVL}$                                | $0.1V < V_{VDSLVL} < 2.5V$               | nFAULT | Pulled Low <sup>2</sup> | Active   | Latched:<br>nSLEEP Reset Pulse           |
|                                   |   | VDSLVL pin 100k $\Omega$<br>tied to GVDD | None   | Active                  | Active   | No action                                |
| $V_{SENSE}$ overcurrent (SEN_OCP) | $V_{SP} > V_{SENSE\_LVL}$                             | -  | nFAULT | Pulled Low <sup>2</sup> | Active   | Latched:<br>nSLEEP Reset Pulse           |
|                                   |   | VDSLVL pin 100k $\Omega$<br>tied to GVDD | None   | Active                  | Active   | No action                                |
| Thermal shutdown (OTSD)           | $T_J > T_{OTSD}$                                      | -  | nFAULT | Pulled Low <sup>2</sup> | Active   | Latched:<br>nSLEEP Reset Pulse           |

1. Disabled: Passive pull down for GLx and semiactive pull down for GHx

2. Pulled Low: GHx and GLx are actively pulled low by the gate driver

#### 8.3.6.1 PVDD Supply Undervoltage Lockout (PVDD\_UV)

If at any time the power supply voltage on the PVDD pin falls below the  $V_{PVDD\_UV}$  threshold for longer than the  $t_{PVDD\_UV\_DG}$  time, the device detects a PVDD undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, the charge pump is disabled, the internal digital logic is disabled, and the nFAULT pin is driven low. Normal operation starts again (the gate driver becomes operable and the nFAULT pin is released) when the PVDD pin rises above  $V_{PVDD\_UV}$ .

#### 8.3.6.2 AVDD Power on Reset (AVDD\_POR)

If at any time the supply voltage on the AVDD pin falls below the  $V_{AVDD\_POR}$  threshold for longer than the  $t_{AVDD\_POR\_DG}$  time, the device enters an inactive state, disabling the gate driver, the charge pump, and the internal digital logic, and nFAULT is driven low. Normal operation (digital logic operational) requires nSLEEP to be asserted high and AVDD to exceed  $V_{AVDD\_POR}$  level.

#### 8.3.6.3 GVDD Undervoltage Lockout (GVDD\_UV)

If at any time the voltage on the GVDD pin falls lower than the  $V_{GVDD\_UV}$  threshold voltage for longer than the  $t_{GVDD\_UV\_DG}$  time, the device detects a GVDD undervoltage event. After detecting the GVDD\_UV undervoltage event, all of the gate driver outputs are driven low to disable the external MOSFETs, the charge pump is disabled and nFAULT pin is driven low. After the GVDD\_UV condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse ( $t_{RST}$ )

#### 备注

After the GVDD\_UV fault is cleared through an nSLEEP pin reset pulse, the nFAULT pin is held low until the GVDD capacitor is refreshed by the charge pump. After the GVDD capacitor is charged, the nFAULT pin is automatically released. The duration that the nFAULT pin is low after the fault is cleared will not exceed  $t_{WAKE}$  time.

### 8.3.6.4 BST Undervoltage Lockout (BST\_UV)

If at any time the voltage across BSTx and SHx pins falls lower than the  $V_{BST\_UV}$  threshold voltage for longer than the  $t_{BST\_UV\_DG}$  time, the device detects a BST undervoltage event. After detecting the BST\_UV event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. After the BST\_UV condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse ( $t_{RST}$ ).

### 8.3.6.5 MOSFET $V_{DS}$ Overcurrent Protection (VDS\_OCP)

The device has adjustable  $V_{DS}$  voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the  $V_{DS}$  voltage drop across the external MOSFET  $R_{DS(on)}$ . The high-side VDS monitors measure between the PVDD and SHx pins and the low-side VDS monitors measure between the SHx and LSS pins. If the voltage across external MOSFET exceeds the  $V_{DS\_LVL}$  threshold for longer than the  $t_{DS\_DG}$  deglitch time, a VDS\_OCP event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The VDS threshold can be set between 0.1 V to 2.5 V by applying a voltage on the VDSLVL pin. VDS OCP can be disabled by connecting VDSLVL to GVDD through a 100 k $\Omega$  resistor. After the VDS\_OCP condition is cleared, the fault state remains latched and can be cleared through the nSLEEP pin reset pulse ( $t_{RST}$ ).

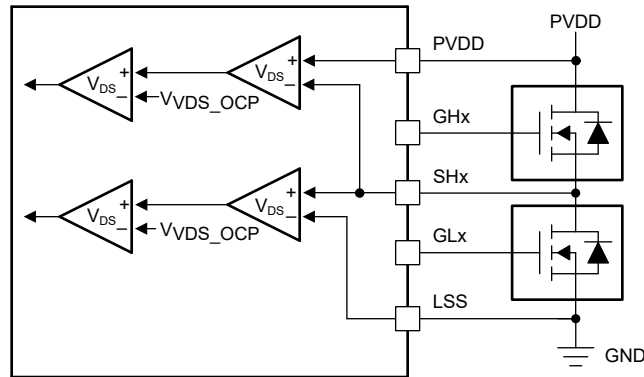


图 8-14. DRV8329  $V_{DS}$  Monitors

### 8.3.6.6 $V_{SENSE}$ Overcurrent Protection (SEN\_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between the LSS and GND pins. If at any time the voltage on the LSS input exceeds the  $V_{SEN\_OCP}$  threshold for longer than the  $t_{DS\_DEG}$  deglitch time, a SEN\_OCP event is recognized. After detecting the SEN\_OCP overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and the nFAULT pin is driven low. The  $V_{SENSE}$  threshold is fixed at 0.5 V and deglitch time is fixed to 3  $\mu$ s. After the SEN\_OCP condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse ( $t_{RST}$ ). SEN\_OCP can be disabled by connecting VDSLVL to GVDD through a 100 k $\Omega$  resistor.

### 8.3.6.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit ( $T_{OTSD}$ ), an OTSD event is recognized. After detecting the OTSD overtemperature event, all of the gate driver outputs are driven low to disable the external MOSFETs, charge pump is disabled and nFAULT pin is driven low. After OTSD condition is cleared, the fault state remains latched and can be cleared through an nSLEEP pin reset pulse ( $t_{RST}$ ).

## 8.4 Device Functional Modes

### 8.4.1 Gate Driver Functional Modes

#### 8.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8329. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the GVDD regulator is disabled and the AVDD regulator is disabled. The  $t_{\text{SLEEP}}$  time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The  $t_{\text{WAKE}}$  time must elapse before the device is ready for inputs.

---

#### 备注

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are not active. After the regulators have been active, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the  $t_{\text{SLEEP}}$  or  $t_{\text{WAKE}}$  time.

---

#### 8.4.1.2 Operating Mode

When the nSLEEP pin is high and the  $V_{\text{PVDD}}$  voltage is greater than the  $V_{\text{PVDD\_UV}}$  voltage, the device goes to operating mode. The  $t_{\text{WAKE}}$  time must elapse before the device is ready for inputs. In this mode the GVDD regulator and AVDD regulator are active.

#### 8.4.1.3 Fault Reset (nSLEEP Reset Pulse)

In the case of device latched faults, the DRV8329 goes into a partial shutdown state to help protect the external power MOSFETs and system.

---

#### 备注

If the user wants to put the device into sleep state after latched fault event, the inputs INHx and INLx needs to be pulled low prior to driving the nSLEEP pin. If the inputs INHx and INLx are not driven low, then the fault is reset after nSLEEP is driven low for the  $t_{\text{RST}}$  time and there can be pulses on gate driver outputs GHx and GLx prior to device entering sleep. The duration of pulses on GHx and GLx can be of duration  $t_{\text{SLEEP}}$  if INHx and INLx are not pulled low.

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## 9 Application and Implementation

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### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 9.1 Application Information

The DRV8329 family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the [节 9.2](#) section highlight how to use and configure the DRV8329 family of devices.

### 9.2 Typical Application

#### 9.2.1 Three Phase Brushless-DC Motor Control

In this application, the DRV8329 is used to drive a three-phase Brushless-DC motor.

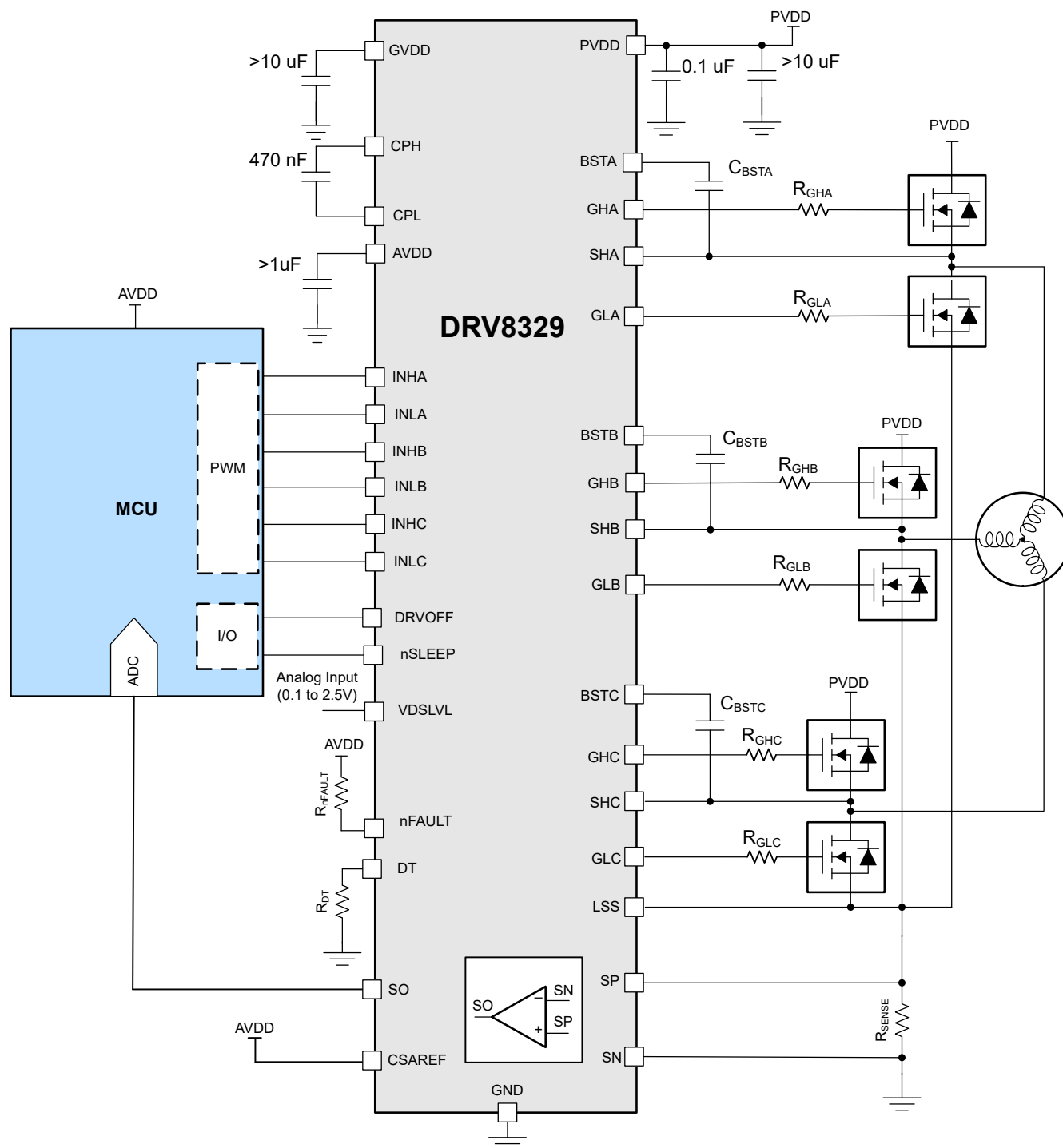


图 9-1. DRV8329 Application Diagram

### 9.2.1.1 Detailed Design Procedure

节 9.2.1.1 lists the example input parameters for the system design.

表 9-1. Design parameters

| DESIGN PARAMETERS | REFERENCE  | EXAMPLE VALUE |
|-------------------|------------|---------------|
| Supply voltage    | $V_{PVDD}$ | 24 V          |

**表 9-1. Design parameters (continued)**

| DESIGN PARAMETERS             | REFERENCE         | EXAMPLE VALUE |
|-------------------------------|-------------------|---------------|
| Motor peak current            | I <sub>PEAK</sub> | 20 A          |
| PWM Frequency                 | f <sub>PWM</sub>  | 20 kHz        |
| MOSFET VDS Slew Rate          | SR                | 120 V/us      |
| MOSFET input gate capacitance | Q <sub>G</sub>    | 54 nC         |
| MOSFET input gate capacitance | Q <sub>GD</sub>   | 14 nC         |
| Dead time                     | t <sub>dead</sub> | 200 ns        |
| Overcurrent protection        | I <sub>OCP</sub>  | 30 A          |

#### 9.2.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 18-V, 24-V or 36-V). The DRV8329 allows for a range of possible operating voltages from 4.5-V to 60-V.

#### 9.2.1.1.2 Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. 方程式 4 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \quad (4)$$

$$= 12 \text{ V} - 0.85 \text{ V} - 4.45 \text{ V} = 6.7 \text{ V}$$

where

- V<sub>GVDD</sub> is the supply voltage of the gate drive
- V<sub>BOOTD</sub> is the forward voltage drop of the bootstrap diode
- V<sub>BSTUV</sub> is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.7 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with 方程式 5:

$$Q_{TOT} = Q_G + \frac{I_{LBS\_TRAN}}{f_{SW}} \quad (5)$$

$$= 54 \text{ nC} + 115 \text{ } \mu\text{A} / 20 \text{ kHz} = 54 \text{ nC} + 5.8 \text{ nC} = 59.8 \text{ nC}$$

where

- Q<sub>G</sub> is the total MOSFET gate charge
- I<sub>LBS\_TRAN</sub> is the bootstrap pin leakage current
- f<sub>SW</sub> is the PWM frequency

The minimum bootstrap capacitor can then be estimated as below assuming 1V of ΔV<sub>BSTx</sub>:

$$C_{BST\_MIN} = Q_{TOT} / \Delta V_{BSTX} \quad (6)$$

$$= 59.8 \text{ nC} / 1 \text{ V} = 59.8 \text{ nF}$$

The calculated value of minimum bootstrap capacitor is 59.8 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions.

It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommended to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \quad (7)$$

$$= 10 \times 100 \text{ nF} = 1 \text{ } \mu\text{F}$$

For this example application, choose a 1- $\mu\text{F}$   $C_{GVDD}$  capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long-term reliability of the system.

#### 备注

For higher power system requiring 100% duty cycle support for longer duration it is recommended to use  $C_{BSTx}$  of  $\geq 1 \text{ } \mu\text{F}$  and  $C_{GVDD}$  of  $\geq 10 \text{ } \mu\text{F}$ .

#### 9.2.1.1.3 Gate Drive Current

Selecting an appropriate gate drive current is essential when turning on or off power MOSFETs gates to switch motor current. The amount of gate drive current and input capacitance of the MOSFETs determines the drain-to-source voltage slew rate ( $V_{DS}$ ). Gate drive current can be sourced from GVDD into the MOSFET gate ( $I_{SOURCE}$ ) or sunk from the MOSFET gate into SHx or LSS ( $I_{SINK}$ ).

Using too high of a gate drive current can turn on MOSFETs too quickly which may cause excessive ringing,  $dV/dt$  coupling, or cross-conduction from switching large amounts of current. If parasitic inductances and capacitances exist in the system, voltage spiking or ringing may occur which can damage the MOSFETs or DRV8329 device.

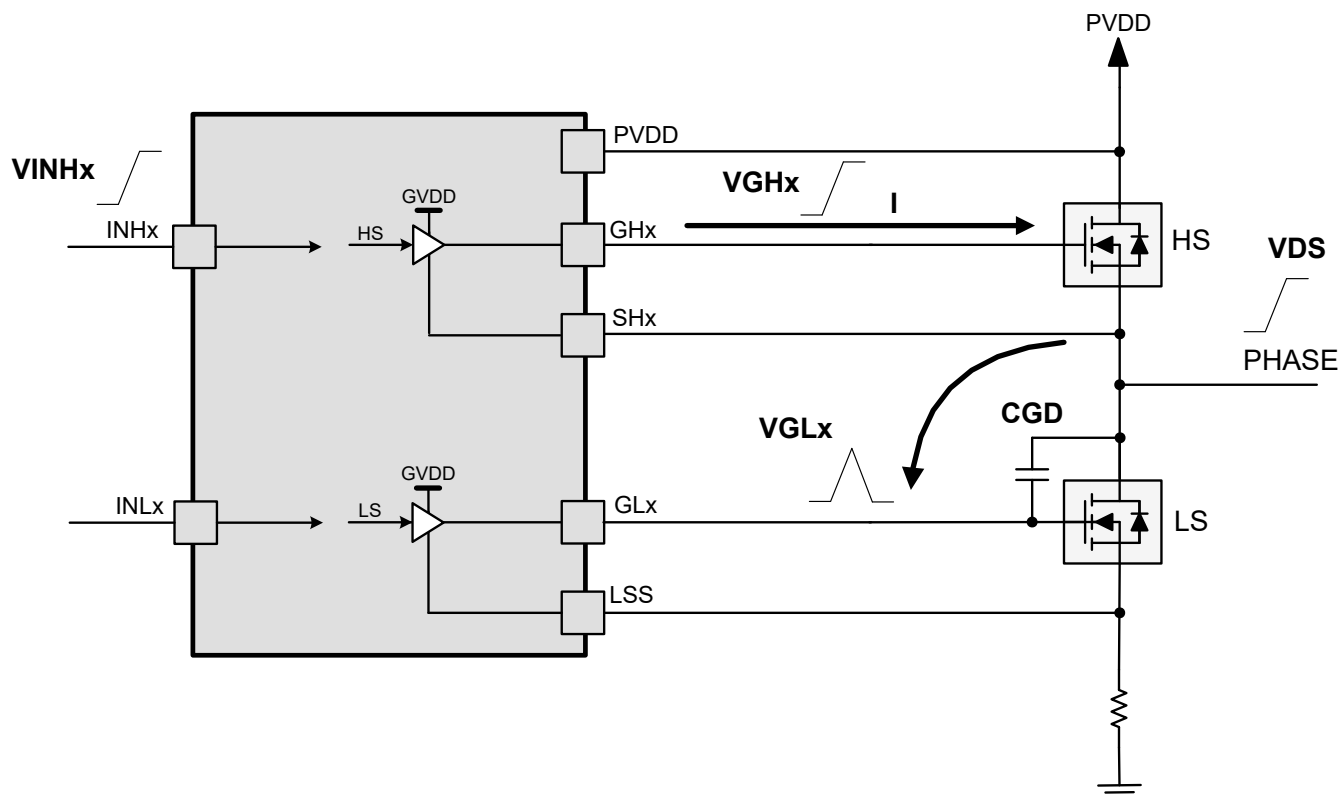


图 9-2. Effects of high gate drive current

On the other hand, using too low of a gate drive current causes long  $V_{DS}$  slew rates. Turning on the MOSFETs too slowly may heat up the MOSFETs due to  $R_{DS(on)}$  switching losses.



The relationship between gate drive current  $I_{GATE}$ , MOSFET gate-to-drain charge  $Q_{GD}$ , and  $V_{DS}$  slew rate switching time  $t_{rise,fall}$  are described by the following equations:

$$SR_{DS} = \frac{V_{DS}}{t_{rise,fall}} \quad (8)$$

$$I_{GATE} = \frac{Q_{gd}}{t_{rise,fall}} \quad (9)$$

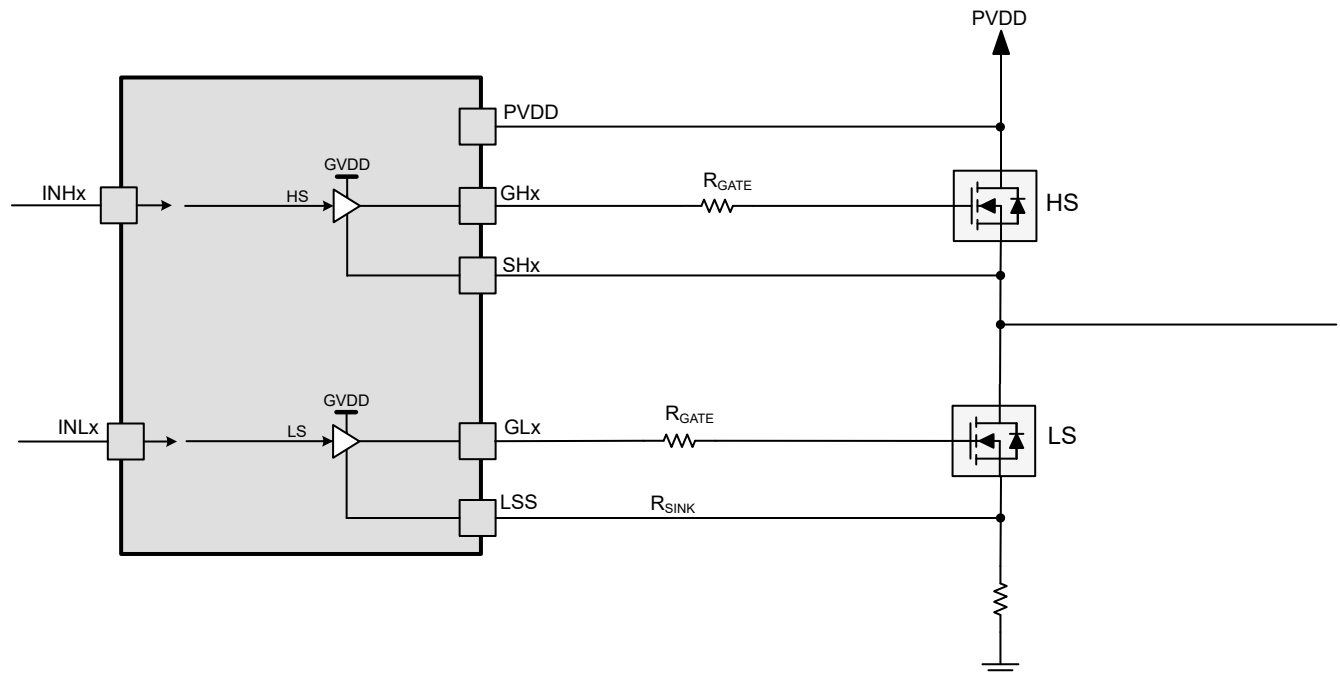
It is recommend to evaluate at lower gate drive currents and increase gate drive current settings to avoid damage from unintended operation during initial evaluation.

#### 9.2.1.1.4 Gate Resistor Selection

The slew rate of the SHx connection will be dependent on the rate at which the gate of the external MOSFETs is controlled. The pull-up/pull-down strength of the DRV8329 is fixed internally, hence the slew rate of gate voltage can be controlled with an external series gate resistor. In some applications, the gate charge of the MOSFET, which is the load on gate driver device, is significantly larger than the gate driver peak output current capability. In such applications, external gate resistors can limit the peak output current of the gate driver. External gate resistors are also used to dampen ringing and noise.

The specific parameters of the MOSFET, system voltage, and board parasitics will all affect the final SHx slew rate, so generally selecting an optimal value or configuration of external gate resistor is an iterative process.

To lower the gate drive current, a series resistor  $R_{GATE}$  can be placed on the gate drive outputs to control the current for the source and sink current paths. A single gate resistor will have the same gate path for source and sink gate current, so larger  $R_{GATE}$  values will yield similar SHx slew rates. Note that gate drive current varies by PVDD voltage, junction temperature, and process variation of the device. Gate resistor values can be estimated with +/-30% accuracy using the [Gate Resistor Calculator](#).



**图 9-3. Gate driver outputs with series resistors**

Typically, it is recommended to have the sink current be twice the source current to implement a strong pulldown from gate to the source to ensure the MOSFET stays off while the opposite FET is switching. This can be implemented discretely by providing a separate path through a resistor for the source and sink currents by placing a diode and sink resistor ( $R_{SINK}$ ) in parallel to the source resistor ( $R_{SOURCE}$ ). Using the same value of

source and sink resistors results in half the equivalent resistance for the sink path. This yields twice the gate drive sink current compared to the source current, and SHx will slew twice as fast when turning off the MOSFET.

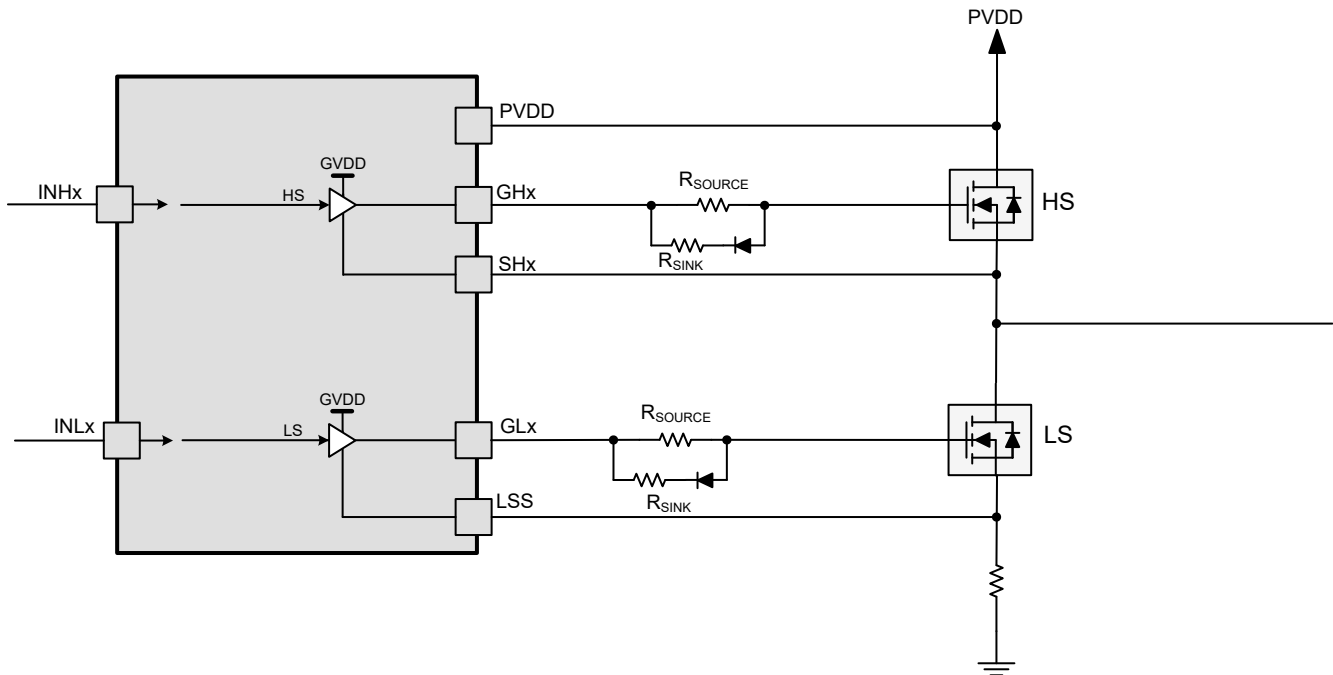


图 9-4. Gate driver outputs with separate source and sink current paths

#### 9.2.1.1.5 System Considerations in High Power Designs

Higher power system designs can require design and application considerations that are not regarded in lower power system designs. It is important to combat the volatile nature of higher power systems by implementing troubleshooting guidelines, external components and circuits, driver product features, or layout techniques. For more information, please visit the [System Design Considerations for High-Power Motor Driver Applications](#) application note.

##### 9.2.1.1.5.1 Capacitor Voltage Ratings

Use capacitors with voltage ratings that are 2x the supply voltage (PVDD, GVDD, AVDD, etc). Capacitors can experience up to half the rated capacitance due to poor DC voltage rating performance.

For example, since the bootstrap voltage is around 12 to 13-V with respect to SHx (BSTx-SHx) then the BSTx-SHx capacitor should be rated for 25-V or greater.

##### 9.2.1.1.5.2 External Power Stage Components

External components in the power stage are not required by design but are helpful in suppressing transients, managing inductor coil energy, mitigating supply pumping, dampening phase ringing, or providing strong gate-to-source pulldown paths. These components are used for system tuning and debuggability so the BLDC motor system is robust while avoiding damage to the DRV8329 device or external MOSFETs.

图 9-5 shows examples of power stage components that can be optimally placed in the design.

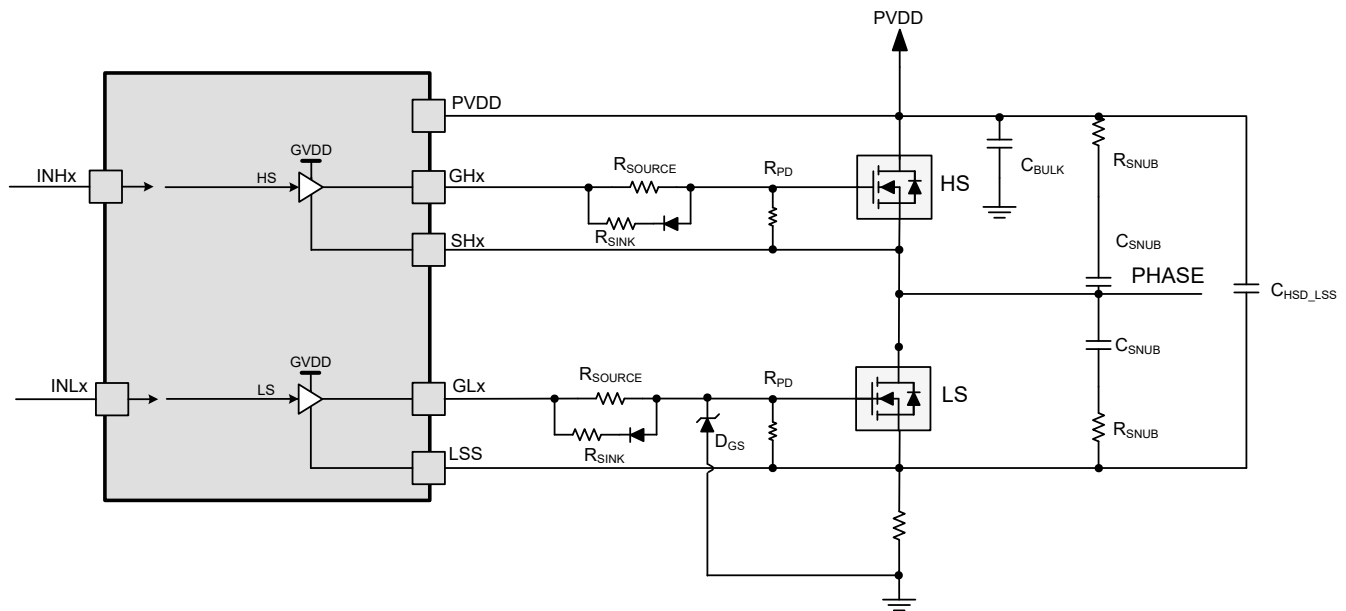


图 9-5. Optional external power stage components

Some examples of issues and external components that can resolve those issues are found in 表 9-2:

表 9-2. Common issues and resolutions for power stage debugging

| Issue  | Resolution   | Component(s)  |
|--|--|---|
| Gate drive current required is too large, resulting in very fast MOSFET $V_{DS}$ slew rate | Series resistors required for gate drive current adjustability             | 0-100 $\Omega$ series resistors (RGATE/ RSOURCE) at gate driver outputs (GHx/ GLx), optional sink resistor (RSINK) and diode in parallel with gate resistor for adjustable sink current |
| Ringing at phase' s switch node (SHx) resulting in high EMI emissions                      | RC snubbers placed in parallel to each HS/LS MOSFET to dampen oscillations | Resistor (RSNUB) and Capacitor (CSNUB) placed parallel to the MOSFET, calculate RC values based on ringing frequency using <a href="#">Proper RC Snubber Design for Motor Drivers</a>   |
| Negative transients at low-side source (LSS) below minimum specification                   | HS drain to LS source capacitor to suppress negative bouncing              | 0.01uF-1uF, VM-rated capacitor from PVDD- LSS (CHSD_LSS) placed near LS MOSFET' s source  |
| Negative transient at low-side gate (GLx) below minimum specification                      | Gate-to-ground Zener diode to clamp negative voltage                       | GVDD voltage rated Zener diode (DGS) with anode connected to GND and cathode connected to GLx   |
| Extra protection required to ensure MOSFET is turned off if gate drive signals are Hi-Z    | External gate-to-source pulldown resistors (after series gate resistors)   | 10 k $\Omega$ to 100 k $\Omega$ resistor (RPD) connected from gate to source for each MOSFET  |

#### 9.2.1.1.5.3 Parallel MOSFET Configuration

If higher MOSFET continuous drain current ratings are required for the motor, parallel MOSFETs can be used for higher current capability. However, this requires special schematic and layout design requirements to switch both MOSFETs simultaneously because one MOSFET may turn on faster than the other due to process variation.

It is recommended to place the MOSFETs close together with a common gate signal that splits as close as possible to the MOSFETs gates. If gate resistance is required, calculate the equivalent resistance required for the equivalently rated MOSFET, and place the gate resistors as close as possible to the MOSFET' s gate input to dampen any coupling into the gate driver.

For more information, please visit the [Driving Parallel MOSFETs](#) application brief.

#### 9.2.1.1.6 Dead Time Resistor Selection

Dead time insertion is available in the DRV8329 via a resistor ( $R_{DT}$ ) from the DT pin to ground as shown in 图 9-6. The ranges of dead time in the DRV8329 is 100 ns to 2000 ns when  $R_{DT}$  is tied to GND from the DT pin. A linear interpolation of the resistance value is used to set the appropriate dead time.

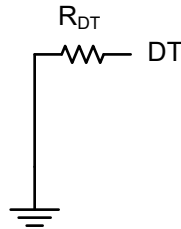


图 9-6. Dead time resistor

Dead time (in nanoseconds) can be calculated from the dead time resistor calculation in 方程式 1.

Dead time can also be implemented from the PWM inputs generated by an MCU. If dead time is inserted at the PWM inputs and the DRV8329, then the driver output PWM dead time is the larger of the two dead times. For instance, if 200 ns dead time is inserted at the MCU inputs and 50 ns dead time is inserted in the DRV8329 via the DT pin, then the output driver PWM dead time will be 200 ns.

#### 9.2.1.1.7 VDSLVL Selection

VDSLVL is an analog voltage used to directly set the VDS overcurrent threshold for overcurrent protection. It can be sourced directly from an analog voltage source (such as a digital-to-analog converter) or divided down from a voltage rail (such as a resistor divider from AVDD) as shown in 图 9-7.

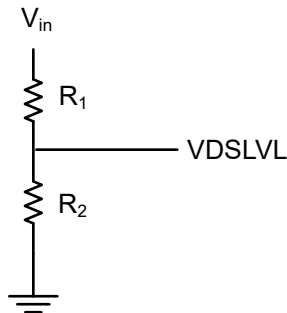


图 9-7. Resistor divider to set VDSLVL from a voltage rail

方程式 10 and 方程式 11 can be used to set the required VDSLVL voltage using a resistor divider from a voltage source to establish an overcurrent limit given the  $R_{DS(on)}$  of the MOSFETs used:

$$V_{VDSLVL} = I_{OC} \times R_{ds(on)} \quad (10)$$

$$\frac{R_1}{R_2} = \frac{V_{in}}{V_{VDSLVL}} - 1 \quad (11)$$

where:

- $V_{VDSLVL}$  = VDSLVL voltage
- $I_{OCP}$  = VDS overcurrent limit
- $R_{DS(on)}$  = MOSFET on-resistance
- $V_{IN}$  = voltage source for VDSLVL voltage divider
- $R_1/R_2$  = resistor ratio for setting VDSLVL

For example, if a resistor divider from AVDD is used to set an overcurrent trip threshold of 30-A and the MOSFET  $R_{DS(ON)} = 10\text{m}\Omega$ , then  $V_{DSLVL} = 0.3\text{V}$ .

In some applications, there will be a difference between battery voltage (VBAT) to directly drive motor power and PVDD voltage to power the DRV8329. Because high-side VDS monitoring is referenced from PVDD-SHx, VDSLVL needs to be selected appropriately to accommodate for the difference in VBAT and PVDD.

方程式 12 helps select an appropriate VDSLVL if there is a difference between PVDD and VDSLVL:

$$V_{DSLVL} = (V_{BAT} - PVDD) + I_{OC} * R_{DS(ON)} \quad (12)$$

For instance, if  $V_{BAT} = 24.0\text{ V}$ ,  $PVDD = 23.3\text{ V}$ ,  $R_{dson} = 10\text{-m}\Omega$ , and  $I_{OC} = 30\text{-A}$ , then VDSLVL should equal 1.0V to detect a 30-A overcurrent event across the high-side FET and a 100-A overcurrent event across the low-side FET.

#### 9.2.1.1.8 AVDD Power Losses

An integrated LDO can supply 3.3-V (up to 80-mA) as power rails for external ICs or supply the pullup voltages for resistors and switches. The power loss from AVDD with respect to PVDD, AVDD voltage, and AVDD current is  $P_{AVDD} = (V_{PVDD} - V_{AVDD}) \times I_{AVDD}$ .

Higher power losses occur due larger dropout from PVDD to 3.3 V or increased AVDD load current.

#### 9.2.1.1.9 Current Sensing and Output Filtering

The SO pin is typically sampled by an analog-to-digital converter in the MCU to calculate the total motor phase current. A phase current calculation is used for closed-loop feedback such as overcurrent protection or sensorless trapezoidal or Field-oriented control commutation

An example calculation for phase current is shown below for a system using  $V_{SO} = 1.4\text{ V}$ ,  $V_{CSAREF} = 3.3\text{V}$ ,  $CSAGAIN = 20\text{ V/V}$ , and  $R_{SENSE} = 1\text{ m}\Omega$ .

$$I = \frac{V_{SO} - \frac{V_{CSAREF}}{8}}{CSAGAIN \times R_{SENSE}} \quad (13)$$

$$I = \frac{1.4\text{ V} - \frac{3.3\text{ V}}{8}}{20\text{ V/V} \times 0.001} \quad (14)$$

$$I = 49.375\text{ A} \quad (15)$$

Sometimes high frequency noise can appear at the SO signals based on voltage ripple at VREF, added inductance at the SO traces, or routing of SO traces near high frequency components. It is recommended to add a low-pass RC filter close to the MCU with cutoff frequency at least 10 times the PWM switching frequency for trapezoidal commutation and 100 times the PWM switching frequency for sinusoidal commutation to filter high frequency noise. A recommended RC filter is 330-ohms, 470-pF to add minimal parallel capacitance to the ADC and current mirroring circuitry. The cutoff frequency for the low-pass RC filter is in 方程式 16.

$$f_c = \frac{1}{2\pi RC} \quad (16)$$

#### 9.2.1.1.10 Power Dissipation and Junction Temperature Losses

To calculate the junction temperature of the DRV8329 from power losses, use 方程式 17. Note that the thermal resistance  $\theta_{JA}$  depends on PCB configurations such as the ambient temperature, numbers of PCB layers, copper thickness on top and bottom layers, and the PCB area.

$$T_J[^\circ\text{C}] = P_{loss}[W] \times \theta_{JA}\left[\frac{^\circ\text{C}}{W}\right] + T_A[^\circ\text{C}] \quad (17)$$

The table below shows summary of equations for calculating each loss in the DRV8329.

表 9-3. DRV8329 Power Losses

| Loss type                  | Equation  |
|----------------------------|---|
| Standby power              | $P_{\text{standby}} = V_{\text{PVDD}} \times I_{\text{PVDD}}$   |
| GVDD CP mode (PVDD < 18V)  | $P_{\text{LDO}} = 2 \times V_{\text{PVDD}} \times I_{\text{GVDD}} - V_{\text{GVDD}} \times I_{\text{GVDD}}$ |
| GVDD LDO mode (PVDD > 18V) | $P_{\text{LDO}} = (V_{\text{PVDD}} - V_{\text{GVDD}}) \times I_{\text{GVDD}}$                               |
| AVDD LDO                   | $P_{\text{LDO}} = (V_{\text{PVDD}} - V_{\text{AVDD}}) \times I_{\text{AVDD}}$                               |

### 9.2.2 Application Curves

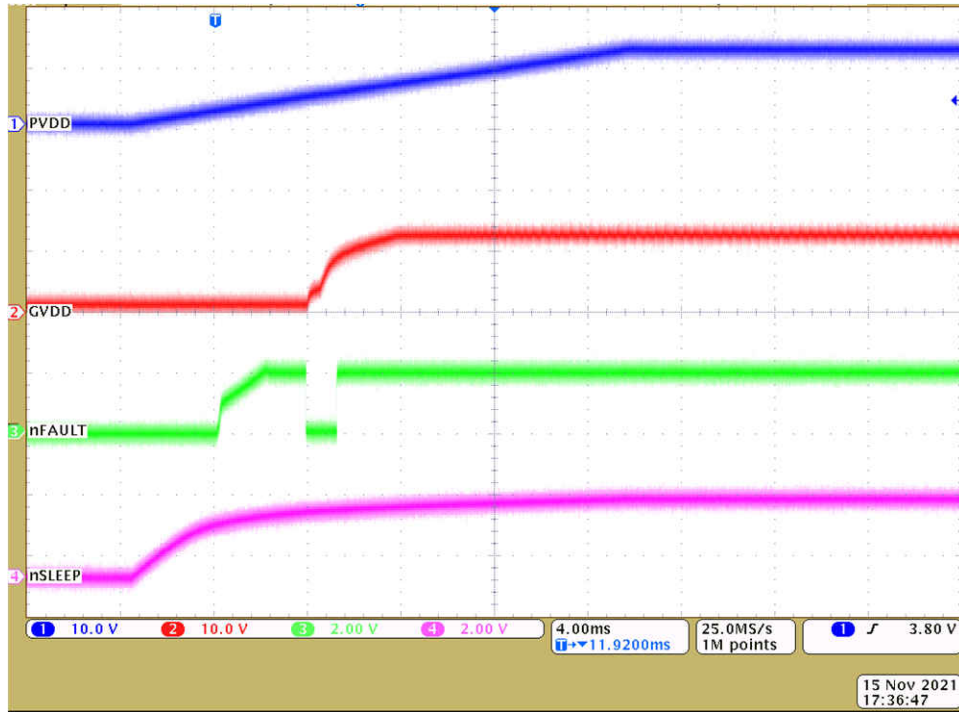


图 9-8. Device Powerup with PVDD

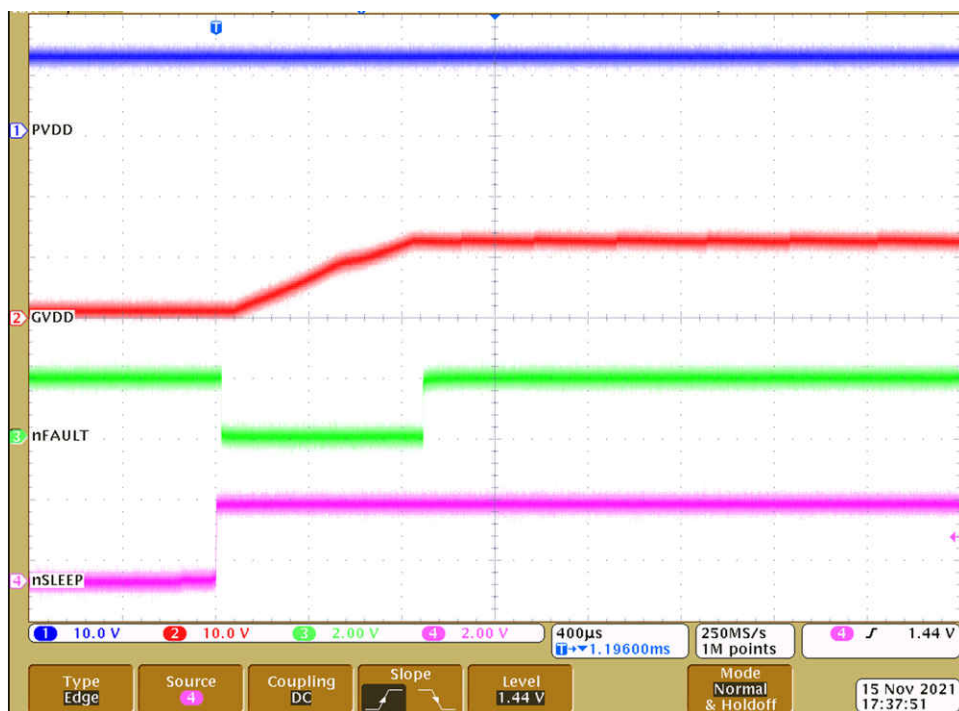


图 9-9. Device Powerup with nSLEEP

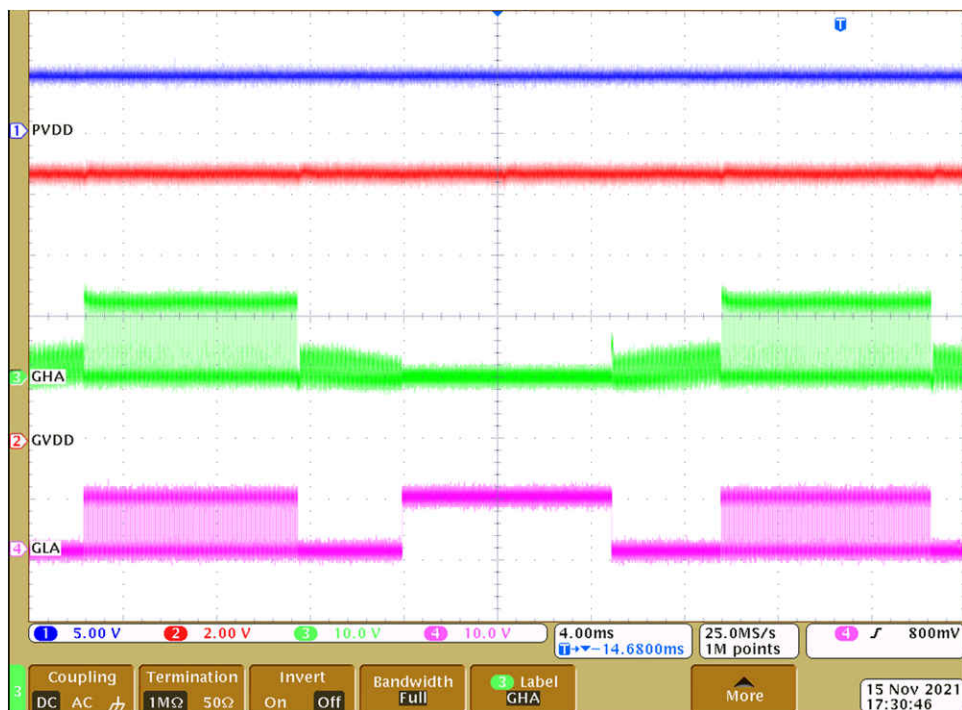


图 9-10. GVDD voltage threshold (PVDD = 4.5 V)



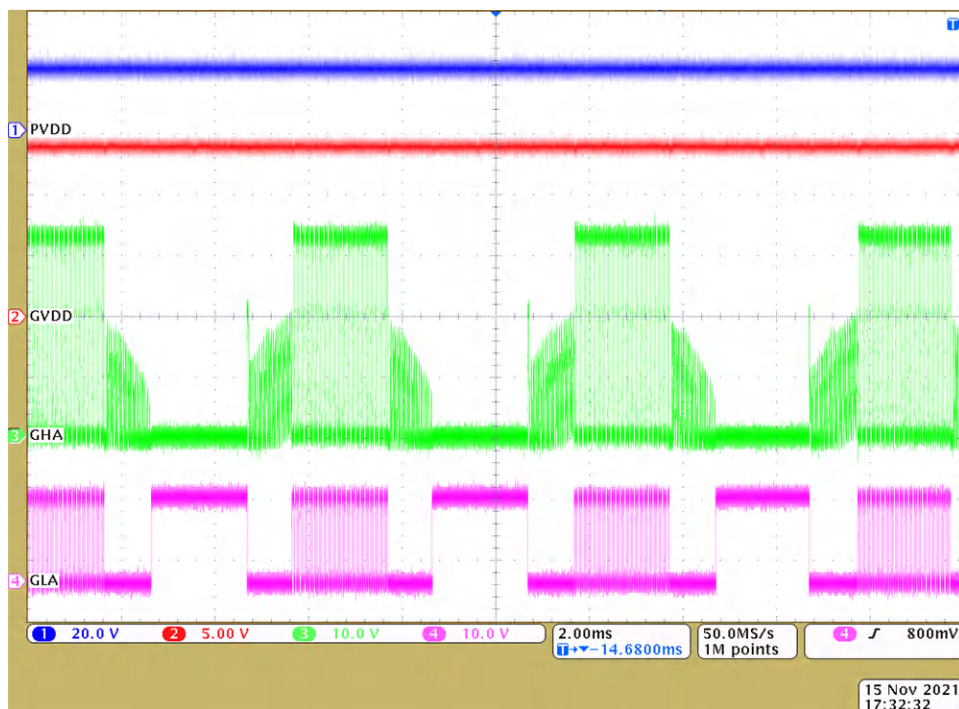


图 9-11. GVDD voltage threshold (PVDD = 20V)

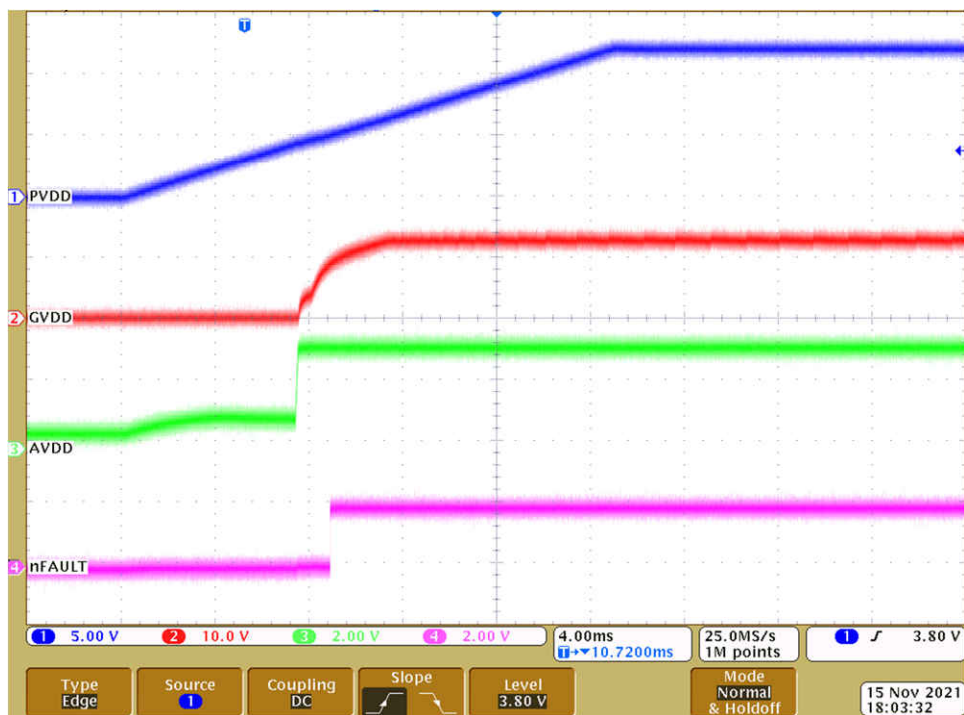


图 9-12. AVDD powerup



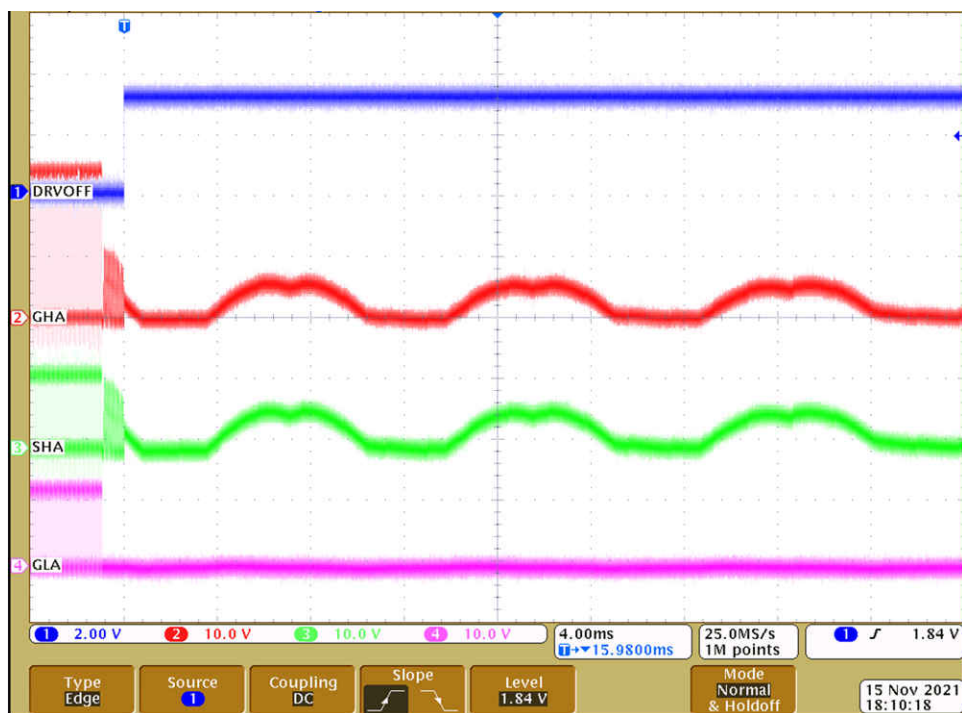


图 9-13. DRVOFF operation

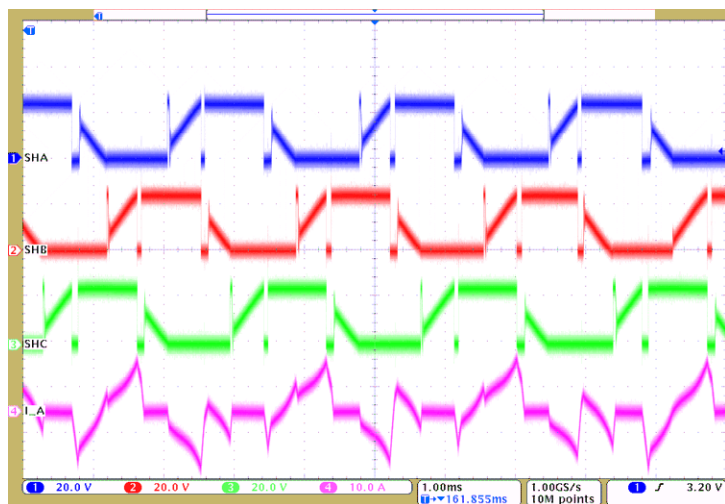


图 9-14. Driver operation at 100% duty cycle

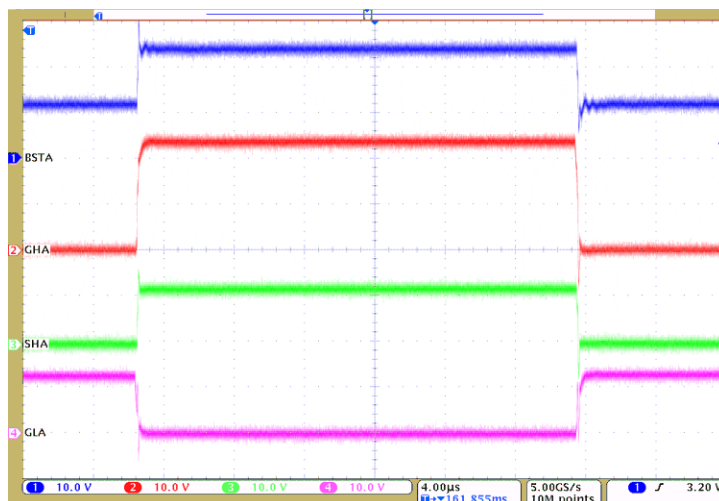


图 9-15. Driver PWM operation, 20 kHz, 50% duty cycle, zoomed

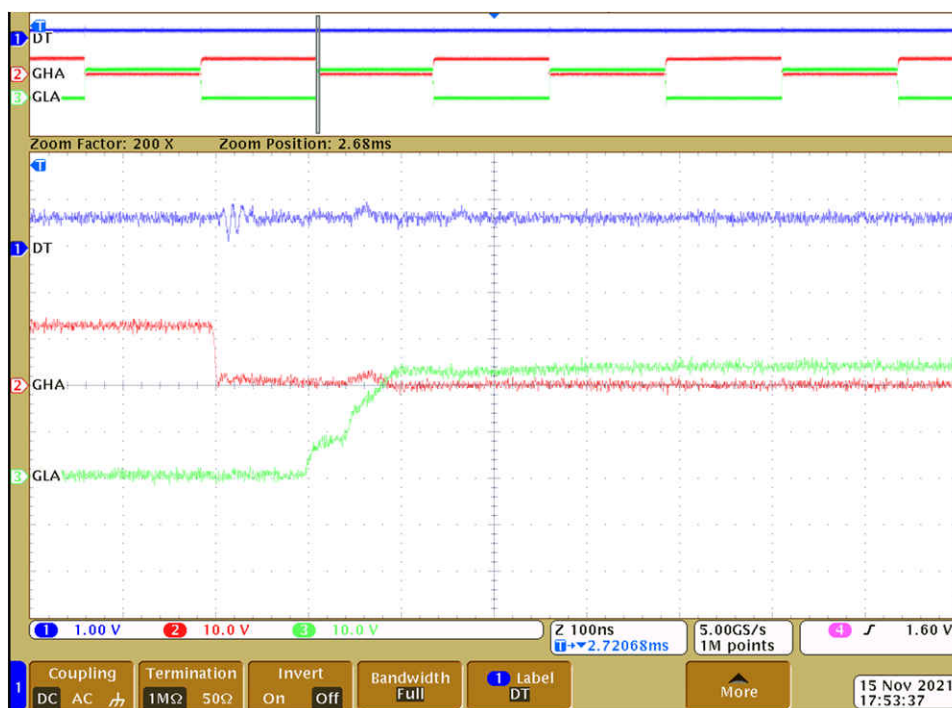


图 9-16. Driver dead time of 100 ns (DT = 10 k $\Omega$  to GND)

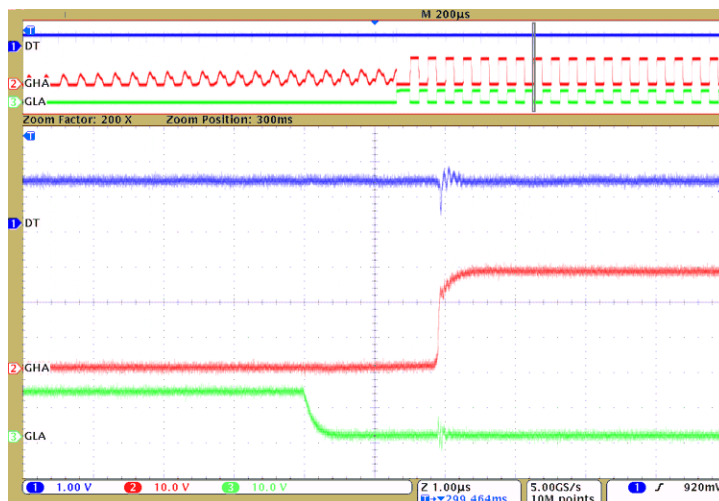


图 9-17. Driver dead time of 2000 ns (DT = 390 k $\Omega$  to GND)

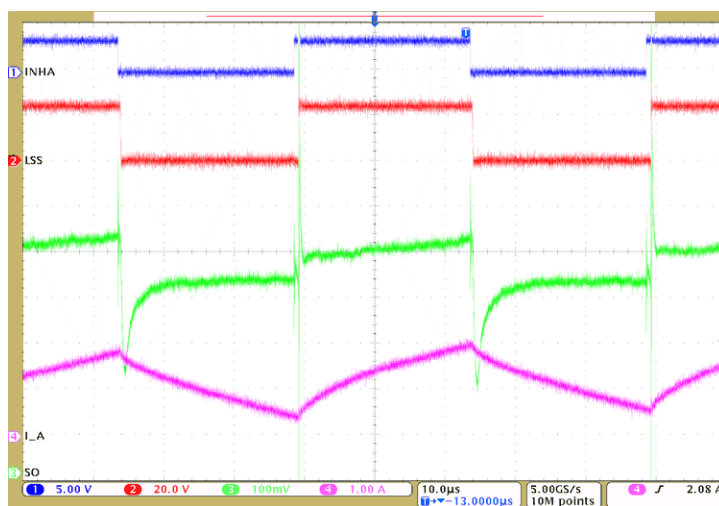


图 9-18. Current sense amplifier operation (GAIN = 40 V/V)

## 10 Power Supply Recommendations

The DRV8329 family of devices is designed to operate from an input voltage supply (PVDD) range from 4.5 V to 60 V. A 10- $\mu$ F and 0.1- $\mu$ F ceramic capacitor rated for PVDD must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the PVDD pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

### 10.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

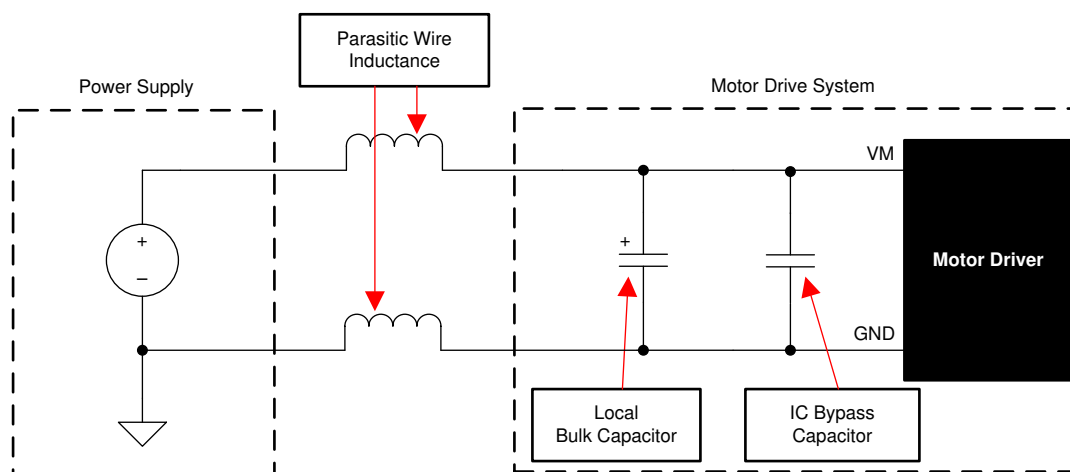


图 10-1. Motor Drive Supply Parasitics Example

## 11 Layout

### 11.1 Layout Guidelines

Bypass the PVDD pin to the PGND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1  $\mu$ F. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for PVDD. This component can be electrolytic. This capacitance must be at least 10  $\mu$ F.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 470 nF, rated for PVDD, and be of type X5R or X7R.

The bootstrap capacitors (BSTx-SHx) should be placed closely to device pins to minimize loop inductance for the gate drive paths.

The dead time resistor ( $R_{DT}$ ) should be placed as close as possible to the DT pin.

Bypass the AVDD pin to the AGND pin with a 1- $\mu$ F low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

When designing higher power systems, physics in the PCB layout can cause parasitic inductances, capacitances, and impedances that deter the performance of the system as shown in [Figure 11-1](#). Understanding the parasitics that are present in a higher power motor drive system can help designers mitigate their effects through good PCB layout. For more information, please visit the [System Design Considerations for High-Power Motor Driver Applications](#) and [Best Practices for Board Layout of Motor Drivers](#) application notes.

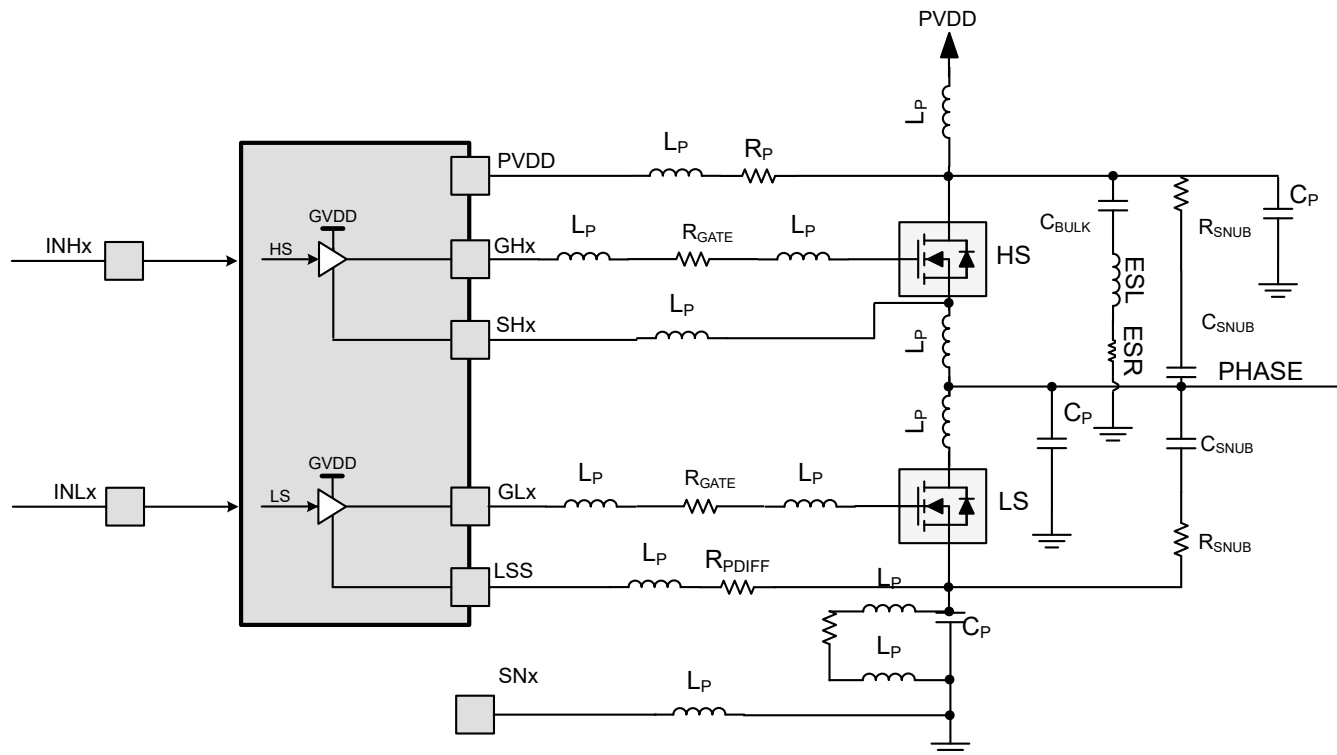


图 11-1. Parasitics in the PCB of a BLDC motor driver powerstage

Gate drive traces (BSTx, GHx, SHx, GLx, LSS) should be at least 15-20mil wide and as short as possible to the MOSFET gates to minimize parasitic inductances and impedances. This helps supply large gate drive currents, turn MOSFETs on efficiently, and improves VGS and VDS monitoring. If a shunt resistor is used to monitor the low-side current from LSS to GND, ensure the shunt resistor selected is wide to minimize inductance introduced at the low-side source LSS.

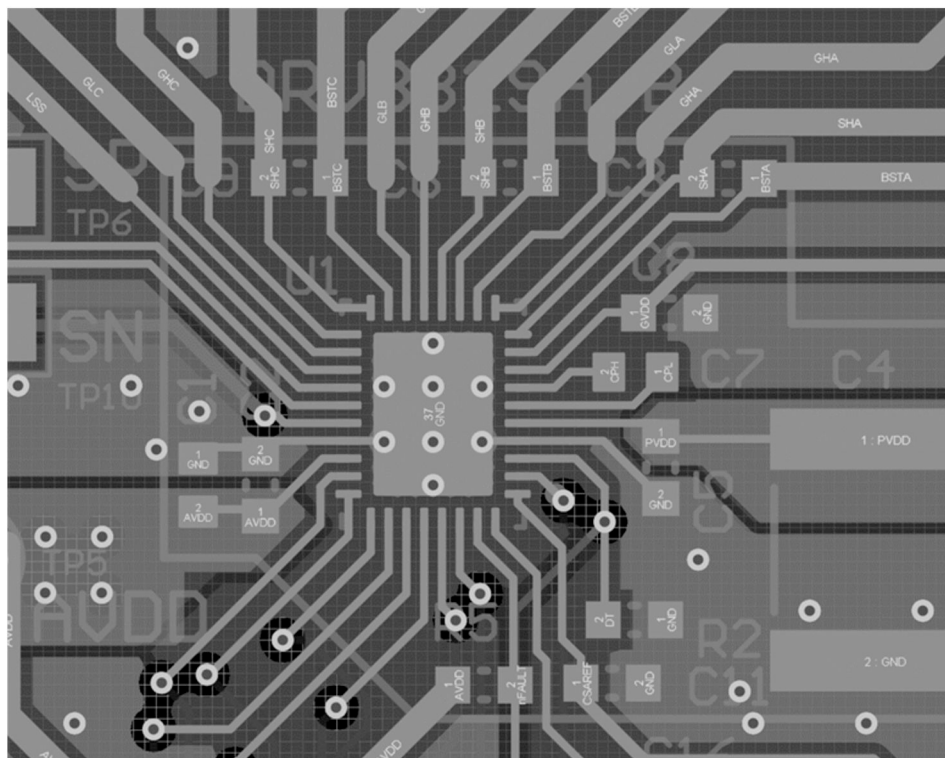
TI recommends connecting all non-power stage circuitry (including the thermal pad) to GND to reduce parasitic effects and improve power dissipation from the device. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

## 11.2 Layout Example

### DRV8329 Layout



11-2. Layout of DRV8329 device



## Power Stage Layout

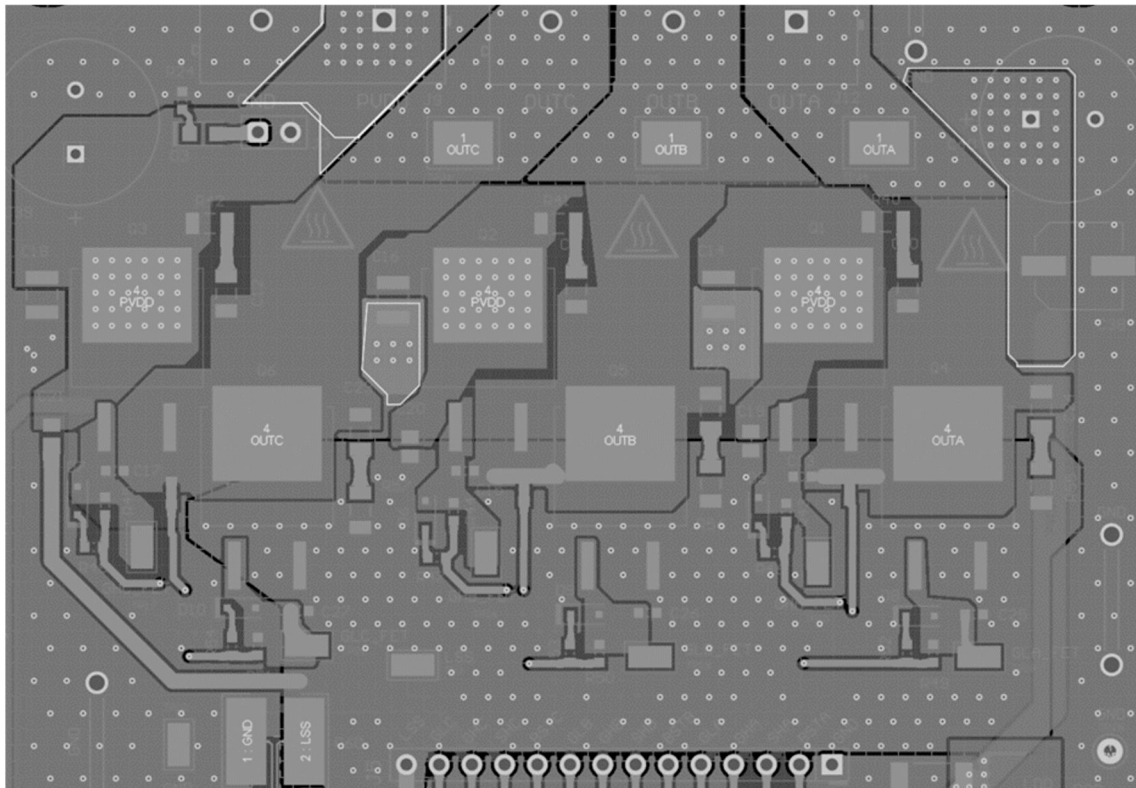


图 11-3. Layout of inverter power stage

## 11.3 Thermal Considerations

The DRV8329 has thermal shutdown (TSD) to protect against overtemperature. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### 11.3.1 Power Dissipation

The DRV8329 integrates a variety of circuits that contribute to total power losses. These power losses include standby power losses, GVDD power losses, and AVDD power losses.

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

- Refer to the application note [Power Delivery in Cordless Power Tools Using DRV8329](#)
- Texas Instruments, [DRV8329AEVM evaluation module](#)
- Refer to the application note [System Design Considerations for High-Power Motor Driver Applications](#)
- Refer to the E2E FAQ [How to Conduct a BLDC Schematic Review and Debug](#)
- Refer to the application note [Best Practices for Board Layout of Motor Drivers](#)
- Refer to the application note [QFN and SON PCB Attachment](#)
- Refer to the application note [Cut-Off Switch in High-Current Motor-Drive Applications](#)
- Refer to the application note [Hardware design considerations for an efficient vacuum cleaner using a BLDC motor](#)
- Refer to the application note [Hardware Design Considerations for an Electric Bicycle Using a BLDC Motor](#)
- Refer to the application note [Sensored 3-Phase BLDC Motor Control Using MSP430](#)

#### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

#### 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

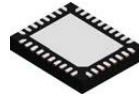
#### 12.5 Community Resources

#### 12.6 Trademarks

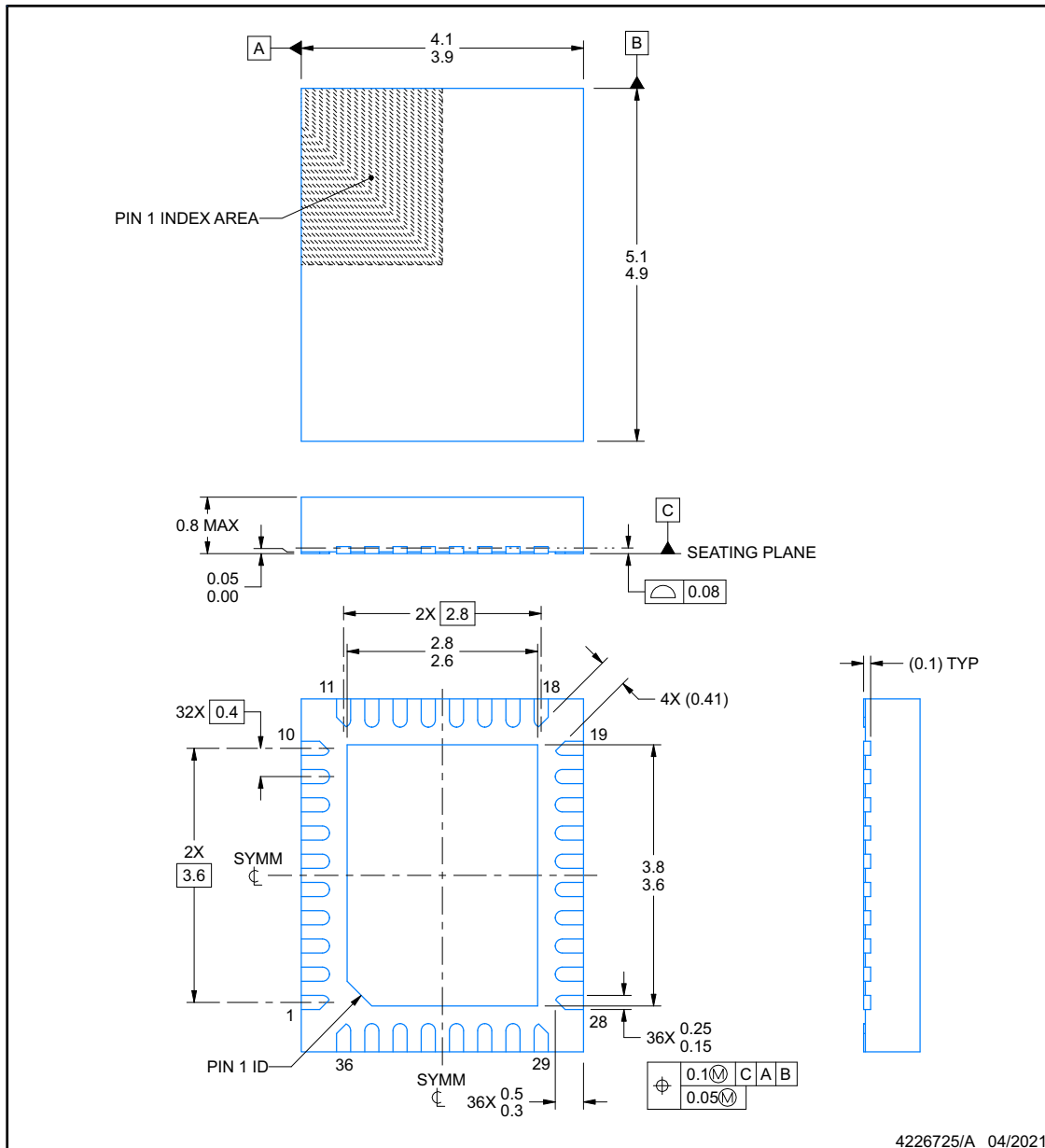
所有商标均为其各自所有者的财产。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**REE0036A****PACKAGE OUTLINE****WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

**NOTES:**

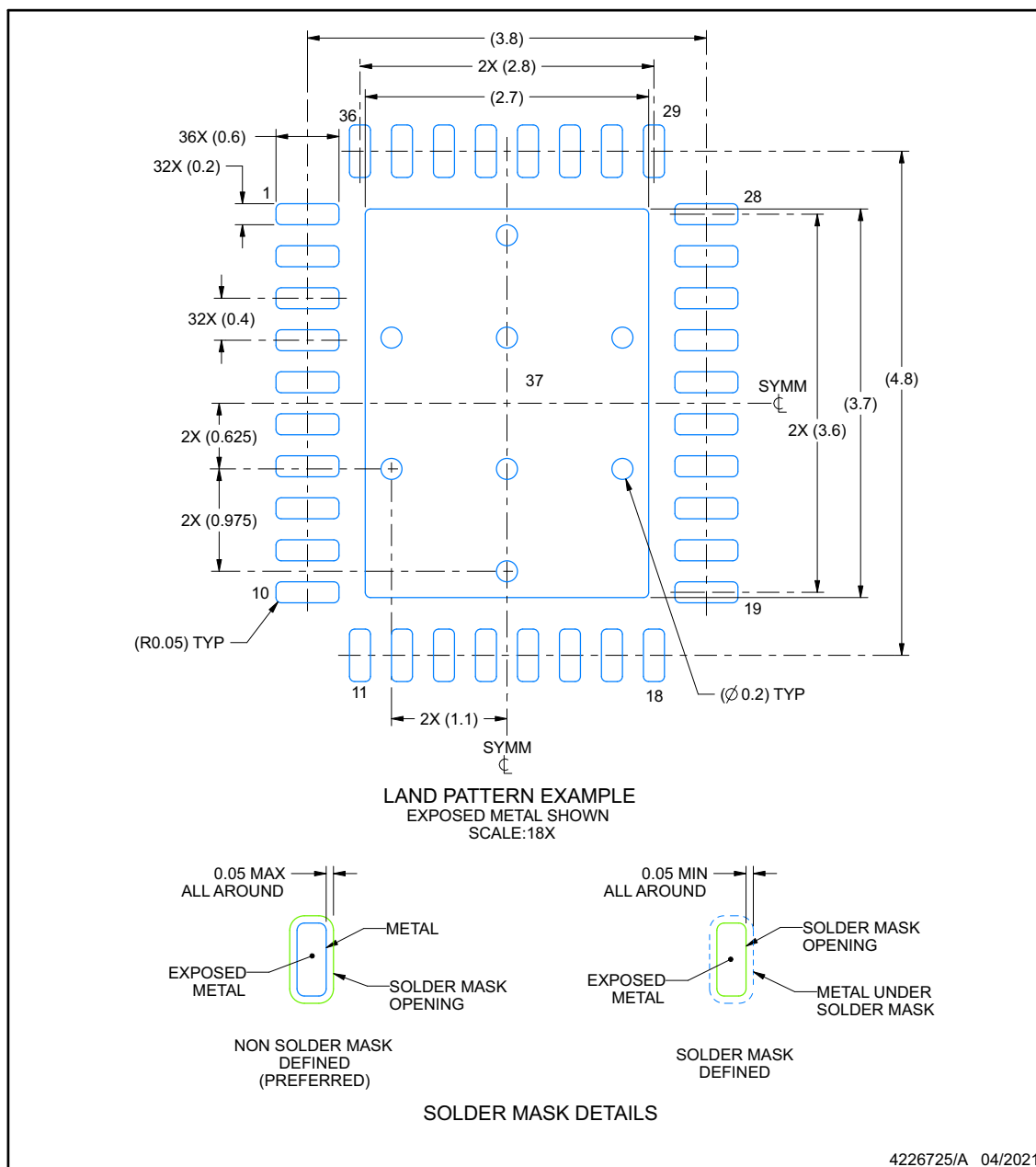
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**REE0036A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

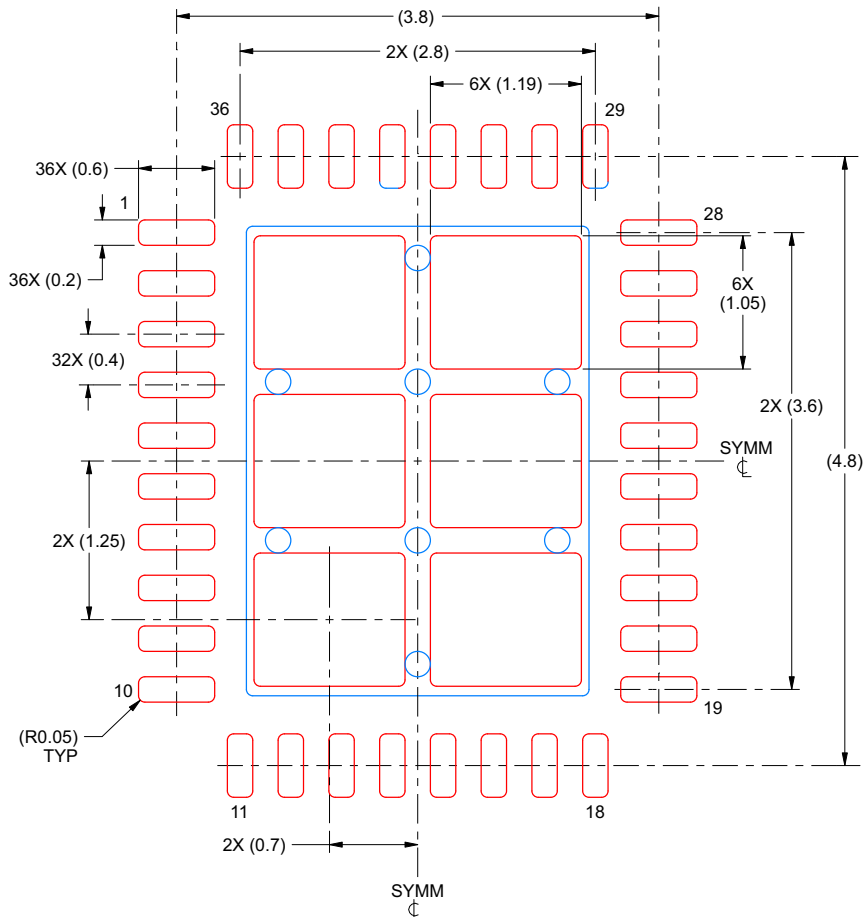


NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

**EXAMPLE STENCIL DESIGN****REE0036A****WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

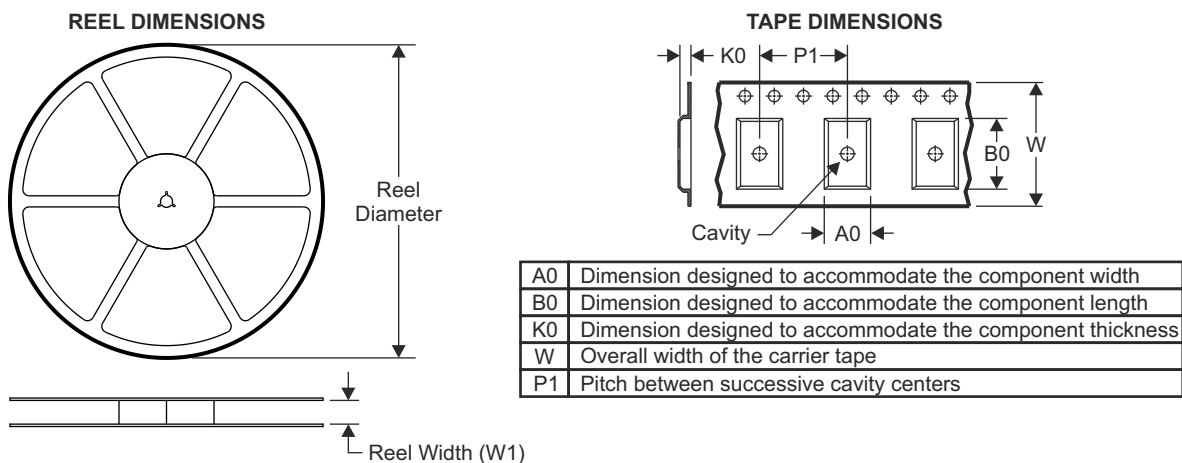
EXPOSED PAD  
75% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4226725/A 04/2021

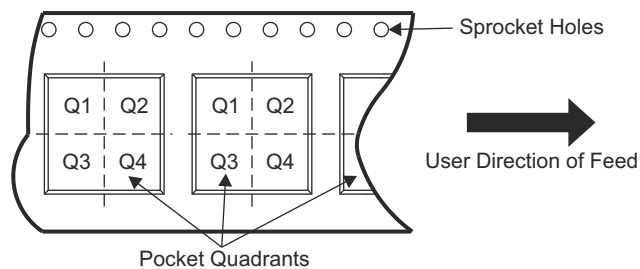
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 13.1 Tape and Reel Information

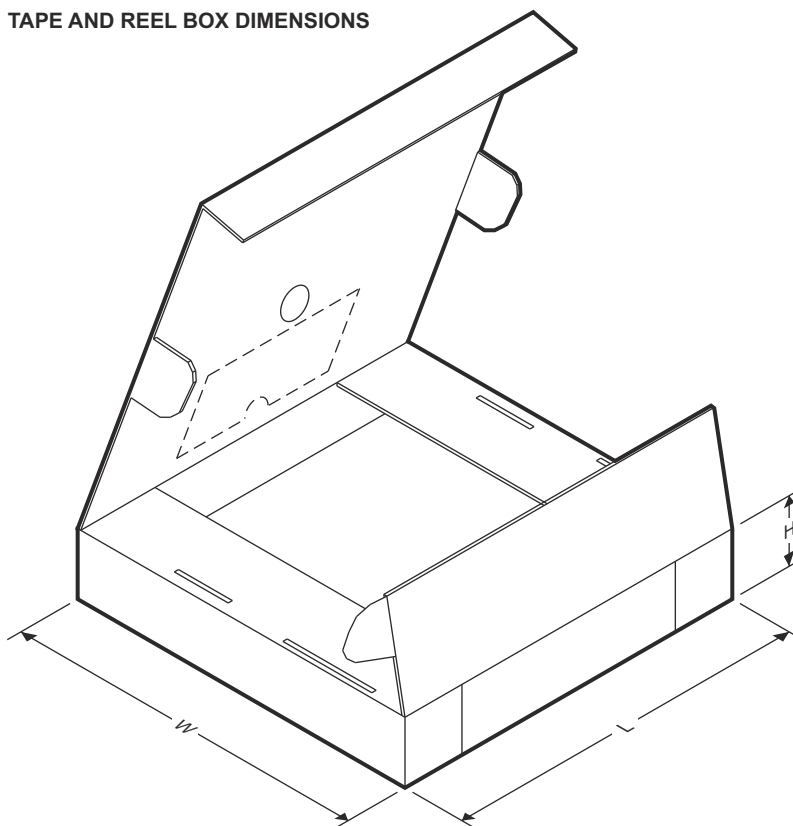


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PDRV8329AREER | WQFN         | REE             | 36   | 5000 | 330.0              | 12.4               | 4.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PDRV8329AREER | WQFN         | REE             | 36   | 5000 | 367.0       | 367.0      | 35.0        |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DRV8329AREER     | ACTIVE        | WQFN         | REE                | 36   | 5000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | DRV<br>8329A            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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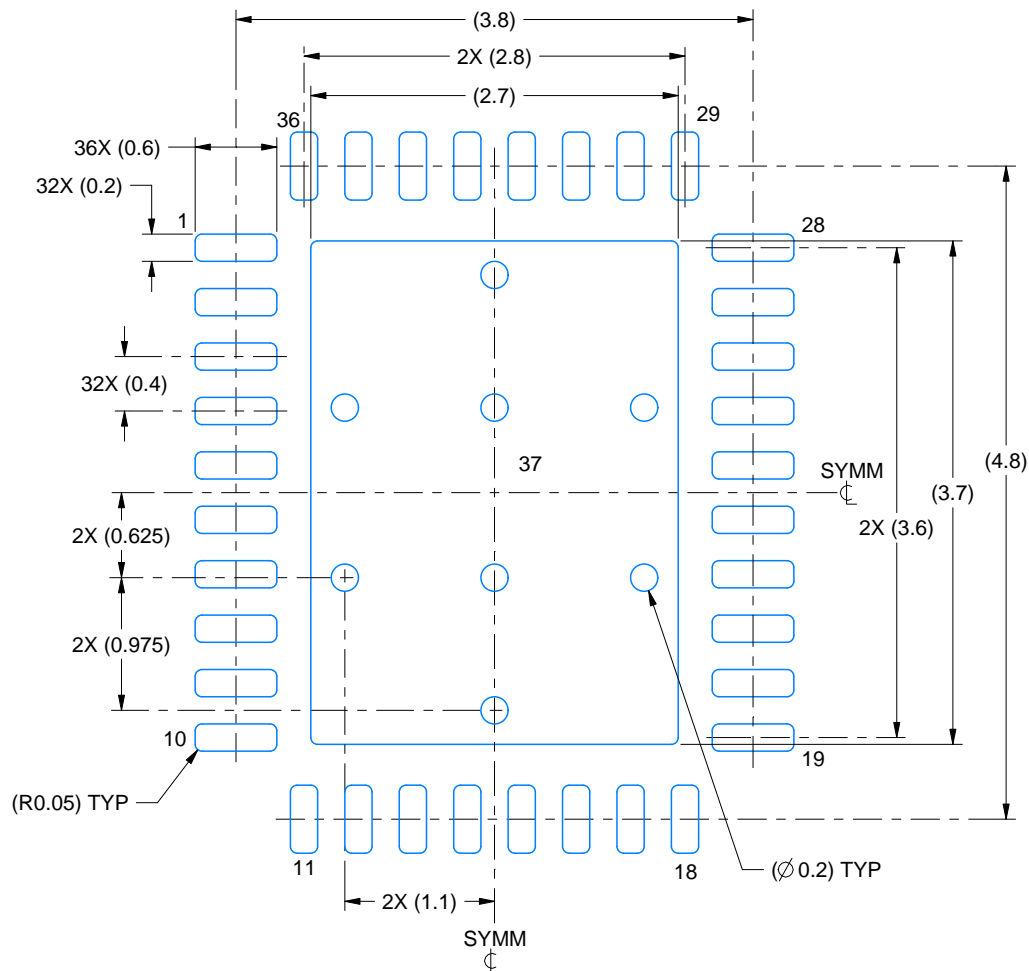


# EXAMPLE BOARD LAYOUT

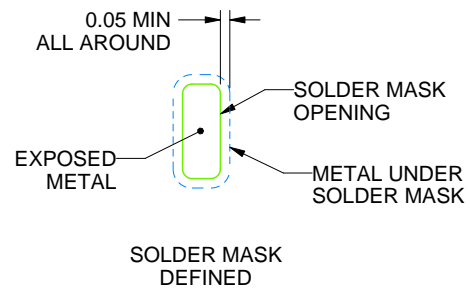
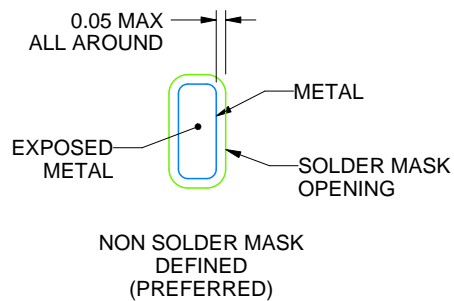
REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

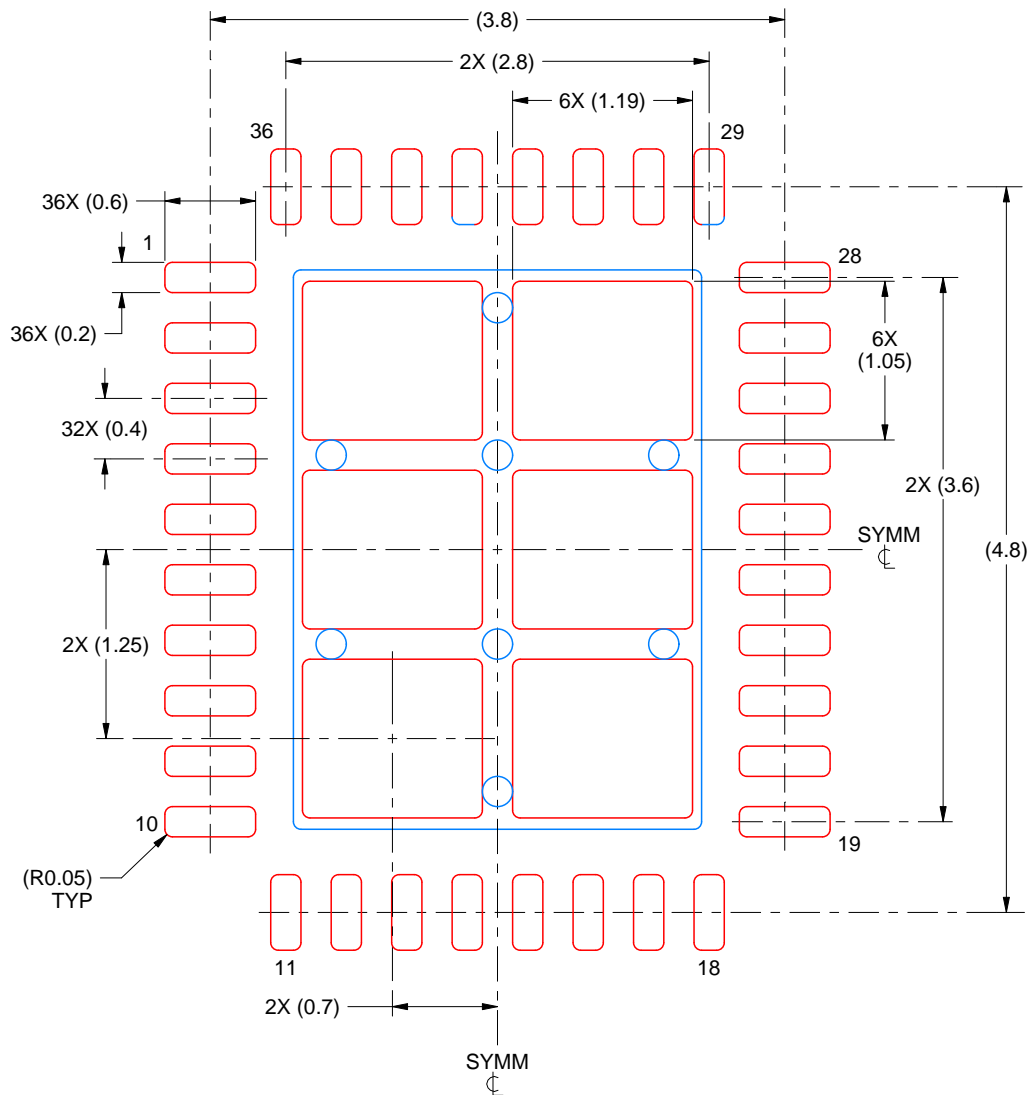
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 EXPOSED PAD  
 75% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:20X

4226725/A 04/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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