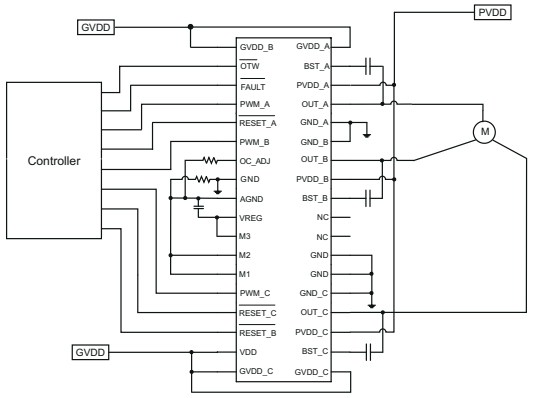
DRV83x2 三相 PWM 电机驱动器

1 特性

- 带低 $R_{DS(on)}$ MOSFET（T_J = 25°C 条件下为 80mΩ）的高效功率级（高达 97%）
- 运行电源电压高达 50V（绝对最大值 70V）
- DRV8312（电源焊盘朝下）：高达 3.5A 的连续相电流（6.5A 峰值）
- DRV8332（电源焊盘朝上）：高达 8A 的连续相电流（13A 峰值）
- 三相半桥独立控制
- PWM 运行频率高达 500kHz
- 片内集成欠压、过温、过载和短路保护功能
- 可编程逐周期电流限制保护
- 针对每个半桥的独立电源和接地引脚
- 智能栅极驱动和交叉导电预防
- 无需外部缓冲器或肖特基二极管

2 应用

- 无刷直流 (BLDC) 电机
- 三相永久磁性同步电机
- 逆变器
- 半桥驱动器
- 机器人控制系统



简化版应用图

3 说明

DRV83x2 是具有高级保护系统的高性能、集成式三相电机驱动器。

由于功率 MOSFET 的低 $R_{DS(on)}$ 和智能栅极驱动设计，这些电机驱动器的效率可高达 97%。凭借高效率、更小的电源和散热器等特性，此类器件非常适合节能应用。

DRV83x2 需要两个电源，一个为 GVDD 和 VDD 提供 12V 电源，另一个为 PVDD 提供高达 50V 的电源。DRV83x2 可以在高达 500kHz 的开关频率下运行，同时仍保持精确控制和高效率。这些器件还具有创新的保护系统，可保护器件免受可能损坏系统的各种故障条件的影响。这些保护是短路保护、过流保护、欠压保护和两级过热保护。DRV83x2 具有限流电路，可防止器件在电机启动等负载瞬态期间关闭。一个可编程过流检测器可实现可调电流限值和保护级别以满足不同的电机需要。

DRV83x2 的每个半桥都有独特的独立电源和接地引脚。借助这些引脚可以通过外部分流电阻提供电流测量，并支持具有不同电源电压要求的半桥驱动器。

器件信息

(1)器件型号	封装	封装尺寸（标称值）
DRV8312	HTSSOP (44)	14.00mm x 6.10mm
DRV8332	HSSOP (36)	15.90 mm × 11.00 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (July 2014) to Revision F (May 2022) — **Page**

- Updated the Programming-Resistor Values and OC Threshold table 11

Changes from Revision D (January 2014) to Revision E (July 2014) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分 1

Changes from Revision C (October 2013) to Revision D (January 2014) — **Page**

- Changed GND_A, GND_B, and GND_C pins description to remove text "requires close decoupling capacitor to ground" 4
- Changed M2 pin description From: Mode selection pin 4
- Added the THERMAL INFORMATION table 7
- Added text to the Overcurrent (OC) Protection section - "It is important to note..." 11
- Added text to the Overcurrent (OC) Protection section - "The values in 表 7-2 show typical..." 11

Changes from Revision B (September 2013) to Revision C (October 2013) — **Page**

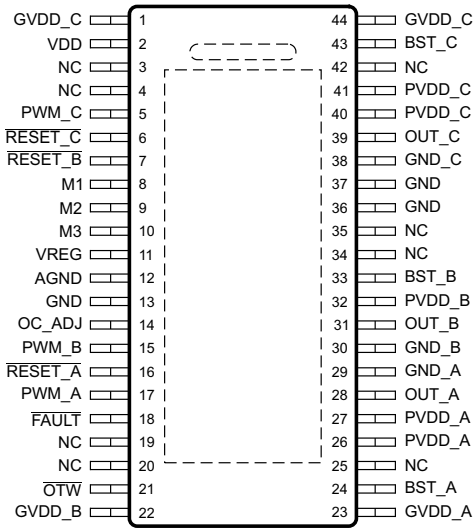
- Changed text in the Overcurrent (OC) Protection section From: "cause the device to shutdown immediately." To: "cause the device to shutdown." 11
- Changed Changed text in the Overcurrent (OC) Protection section From: " $\overline{\text{RESET\_B}}$, and / or must be asserted." To: ", and must be asserted" 11
- Changed paragraph in the DEVICE RESET "A rising-edge transition..." 13

Changes from Revision A (July 2013) to Revision B (September 2013) — **Page**

- Changed the description of pin M3 From: AGND connection is recommended To: VREG connection is recommended 4

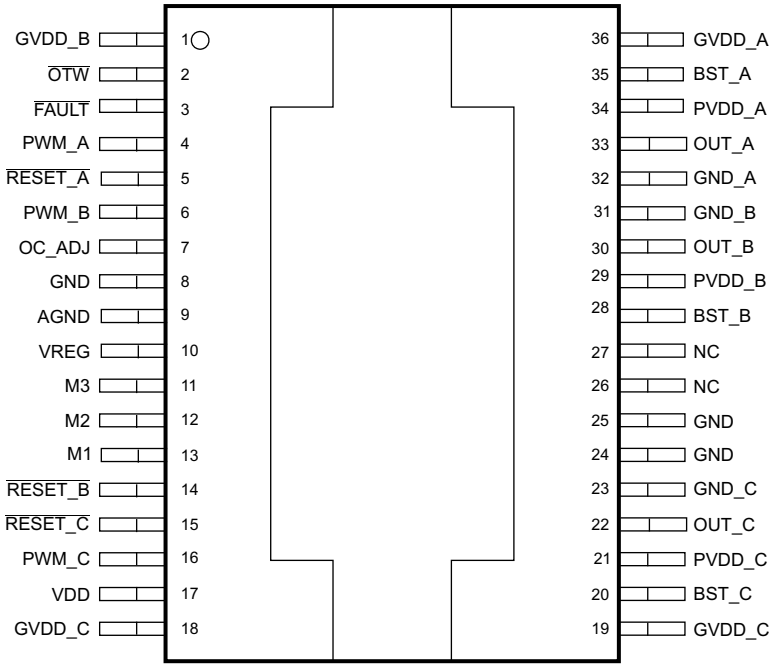
Changes from Revision * (May 2010) to Revision A (July 2013)	Page
• Changed text in the OC_ADJ Pin section From: "For accurate control of the oevercurrent protection..." To: "For accurate control of the overcurrent protection..."	24

5 Pin Configuration and Functions



DRV8312: 44-pin TSSOP power pad down DDW package. This package contains a thermal pad that is located on the bottom side of the device for dissipating heat through PCB.

图 5-1. DV8312 HTSSOP (DDW) (Top View)



DRV8332: 36-pin PSOP3 DKD package. This package contains a thick heat slug that is located on the top side of the device for dissipating heat through heatsink.

图 5-2. DRV8332 HSSOP (DKD) (Top View)

表 5-1. Pin Functions

PIN			I/O TYPE (1)	DESCRIPTION
NAME	DRV8312	DRV8332		
AGND	12	9	P	Analog ground
BST_A	24	35	P	High side bootstrap supply (BST), external capacitor to OUT_A required
BST_B	33	28	P	High side bootstrap supply (BST), external capacitor to OUT_B required

表 5-1. Pin Functions (continued)

PIN			I/O TYPE (1)	DESCRIPTION
NAME	DRV8312	DRV8332		
BST_C	43	20	P	High side bootstrap supply (BST), external capacitor to OUT_C required
GND	13, 36, 37	8	P	Ground
GND_A	29	32	P	Power ground for half-bridge A
GND_B	30	31	P	Power ground for half-bridge B
GND_C	38	23	P	Power ground for half-bridge C
GVDD_A	23	36	P	Gate-drive voltage supply
GVDD_B	22	1	P	Gate-drive voltage supply
GVDD_C	1, 44	18, 19	P	Gate-drive voltage supply
M1	8	13	I	Mode selection pin
M2	9	12	I	Reserved mode selection pin. AGND connection is recommended
M3	10	11	I	Reserved mode selection pin, VREG connection is recommended
NC	3, 4, 19, 20, 25, 34, 35, 42	26, 27	-	No connection pin. Ground connection is recommended
OC_ADJ	14	7	O	Analog overcurrent programming pin, requires resistor to AGND
$\overline{\text{OTW}}$	21	2	O	Overtemperature warning signal, open-drain, active-low. An internal pullup resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pullup resistor to 5 V
OUT_A	28	33	O	Output, half-bridge A
OUT_B	31	30	O	Output, half-bridge B
OUT_C	39	22	O	Output, half-bridge C
PVDD_A	26, 27	34	P	Power supply input for half-bridge A requires close decoupling capacitor to ground.
PVDD_B	32	29	P	Power supply input for half-bridge B requires close decoupling capacitor to gound.
PVDD_C	40, 41	21	P	Power supply input for half-bridge C requires close decoupling capacitor to ground.
PWM_A	17	4	I	Input signal for half-bridge A
PWM_B	15	6	I	Input signal for half-bridge B
PWM_C	5	16	I	Input signal for half-bridge C
$\overline{\text{RESET\_A}}$	16	5	I	Reset signal for half-bridge A, active-low
$\overline{\text{RESET\_B}}$	7	14	I	Reset signal for half-bridge B, active-low
$\overline{\text{RESET\_C}}$	6	15	I	Reset signal for half-bridge C, active-low
$\overline{\text{FAULT}}$	18	3	O	Fault signal, open-drain, active-low. An internal pullup resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pullup resistor to 5 V
VDD	2	17	P	Power supply for digital voltage regulator requires capacitor to ground for decoupling.
VREG	11	10	P	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND.
THERMAL PAD	--	N/A	T	Solder the exposed thermal pad at the bottom of the DRV8312DDW package to the landing pad on the PCB. Connect the landing pad through vias to large ground plate for better thermal dissipation.
HEAT SLUG	N/A	--	T	Mount heatsink with thermal interface to the heat slug on the top of the DRV8332DKD package to improve thermal dissipation.

(1) I = input, O = output, P = power, T = thermal

Mode Selection Pins

MODE PINS			DESCRIPTION
M3	M2	M1	
1	0	0	Three-phase or three half bridges with cycle-by-cycle current limit
1	0	1	Three-phase or three half bridges with OC latching shutdown (no cycle-by-cycle current limit)
0	x	x	Reserved

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted(1)

	MIN	MAX	UNIT
VDD to GND	–0.3	13.2	V
GVDD_X to GND	–0.3	13.2	V
PVDD_X to GND_X (2)	–0.3	70	V
OUT_X to GND_X (2)	–0.3	70	V
BST_X to GND_X (2)	–0.3	80	V
Transient peak output current (per pin), pulse width limited by internal overcurrent protection circuit		16	A
Transient peak output current for latch shut down (per pin)		20	A
VREG to AGND	–0.3	4.2	V
GND_X to GND	–0.3	0.3	V
GND to AGND	–0.3	0.3	V
PWM_X, $\overline{\text{RESET\_X}}$ to GND	–0.3	VREG + 0.5	V
OC_ADJ, M1, M2, M3 to AGND	–0.3	4.2	V
$\overline{\text{FAULT}}$, $\overline{\text{OTW}}$ to GND	–0.3	7	V
Continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$)		9	mA
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These are the maximum allowed voltages for transient spikes. Absolute maximum DC voltages are lower.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Charged Device Model (HBM) ESD Stress Voltage (1)	±1500	V

(1) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
PVDD_X	Half bridge X (A, B, or C) DC supply voltage	0	50	52.5	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	10.8	12	13.2	V
VDD	Digital regulator supply voltage	10.8	12	13.2	V
I_{O_PULSE}	Pulsed peak current per output pin (could be limited by thermal)			15	A
I_O	Continuous current per output pin (DRV8332)			8	A
F_{SW}	PWM switching frequency			500	kHz
R_{OCP_CBC}	OC programming resistor range in cycle-by-cycle current limit modes	22		200	kΩ
R_{OCP_OCL}	OC programming resistor range in OC latching shutdown modes	19		200	kΩ
C_{BST}	Bootstrap capacitor range	33		220	nF
t_{ON_MIN}	Minimum PWM pulse duration, low side, for charging the Bootstrap capacitor		50		ns
T_A	Operating ambient temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC		DRV8312 DDW PACKAGE 44 PINS	DRV8332 DKD PACKAGE 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.5	13.3 (with heat sink)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.8	0.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	13.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter	5.4	13.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	N/A	

6.5 Dissipation Ratings

PARAMETER	DRV8312	DRV8332
$R_{\theta JC}$, junction-to-case (power pad / heat slug) thermal resistance	1.1 °C/W	0.9 °C/W
$R_{\theta JA}$, junction-to-ambient thermal resistance	25 °C/W	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.
Exposed power pad / heat slug area	34 mm^2	80 mm^2

6.6 Power Deratings (DRV8312)

(1) PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
44-PIN TSSOP (DDW)	5.0 W	40.0 mW/°C	3.2 W	2.6 W	1.0 W

(1) Based on EVM board layout

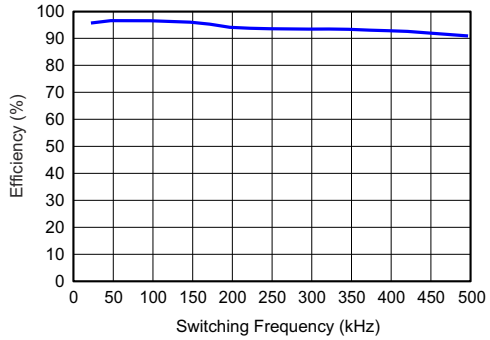
6.7 Electrical Characteristics

T_A = 25°C, PVDD = 50 V, GVDD = VDD = 12 V, f_{Sw} = 400 kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
V_{REG}	Voltage regulator, only used as a reference node	VDD = 12 V	2.95	3.3	3.65	V
I_{VDD}	VDD supply current	Idle, reset mode		9	12	mA
		Operating, 50% duty cycle		10.5		
I_{GVDD_X}	Gate supply current per half-bridge	Reset mode		1.7	2.5	mA
		Operating, 50% duty cycle		8		
I_{PVDD_X}	Half-bridge X (A, B, or C) idle current	Reset mode		0.7	1	mA
OUTPUT STAGE						
$R_{DS(on)}$	MOSFET drain-to-source resistance, low side (LS)	T_J = 25°C, GVDD = 12 V		80		mΩ
	MOSFET drain-to-source resistance, high side (HS)	T_J = 25°C, GVDD = 12 V		80		mΩ
V_F	Diode forward voltage drop	T_J = 25°C - 125°C, I_O = 5 A		1		V
t_R	Output rise time	Resistive load, I_O = 5 A		14		ns
t_F	Output fall time	Resistive load, I_O = 5 A		14		ns
t_{PD_ON}	Propagation delay when FET is on	Resistive load, I_O = 5 A		38		ns
t_{PD_OFF}	Propagation delay when FET is off	Resistive load, I_O = 5 A		38		ns
t_{DT}	Dead time between HS and LS FETs	Resistive load, I_O = 5 A		5.5		ns
I/O PROTECTION						
$V_{uvp,G}$	Gate supply voltage GVDD_X undervoltage protection threshold			8.5		V
$V_{uvp,hyst}$ (1)	Hysteresis for gate supply undervoltage event			0.8		V
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{hyst} (1)	Hysteresis temperature to reset $\overline{OTW}$ event			25		°C
OTSD(1)	Overtemperature shut down			150		°C
$OTE\text{-}OTW_{differential}$ (1)	OTE-OTW overtemperature detect temperature difference			25		°C
$OTSD_{HYST}$ (1)	Hysteresis temperature for $\overline{FAULT}$ to be released following an OTSD event			25		°C
I_{OC}	Overcurrent limit protection	Resistor—programmable, nominal, R_{OCP} = 27 kΩ		9.7		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected FET(s)		250		ns
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, M1, M2, M3	2		3.6	V
V_{IH}	High-level input voltage	$\overline{RESET\_A}$, $\overline{RESET\_B}$, $\overline{RESET\_C}$	2		3.6	V
V_{IL}	Low-level input voltage	PWM_A, PWM_B, PWM_C, M1, M2, M3, $\overline{RESET\_A}$, $\overline{RESET\_B}$, $\overline{RESET\_C}$			0.8	V
I_{lkg}	Input leakage current		-100		100	μA
OTW / FAULT						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{FAULT}$ to VREG		20	26	35	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor only	2.95	3.3	3.65	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V

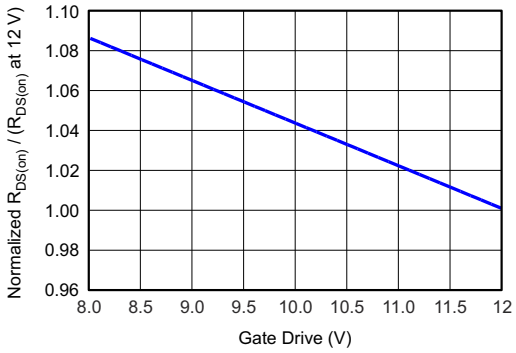
(1) Specified by design

6.8 Typical Characteristics



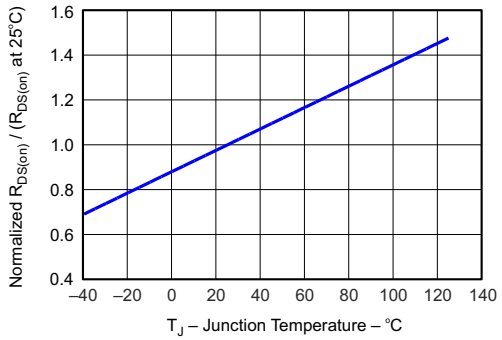
Full Bridge Load: 5 A; PVDD = 50 V; T_c = 75°C

图 6-1. Efficiency vs Switching Frequency (DRV8332)



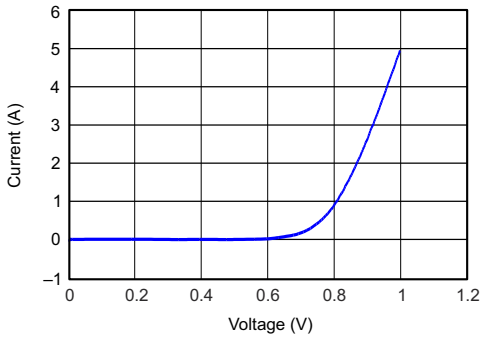
T_J = 25°C

图 6-2. Normalized $R_{DS(on)}$ vs Gate Drive



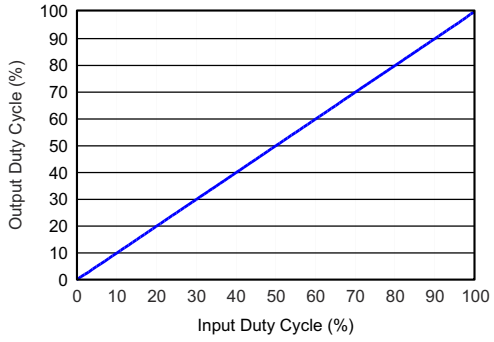
GVDD = 12 V

图 6-3. Normalized $R_{DS(on)}$ vs Junction Temperature



T_J = 25°C

图 6-4. Drain To Source Diode Forward On Characteristics



F_S = 500 kHz; T_C = 25°C

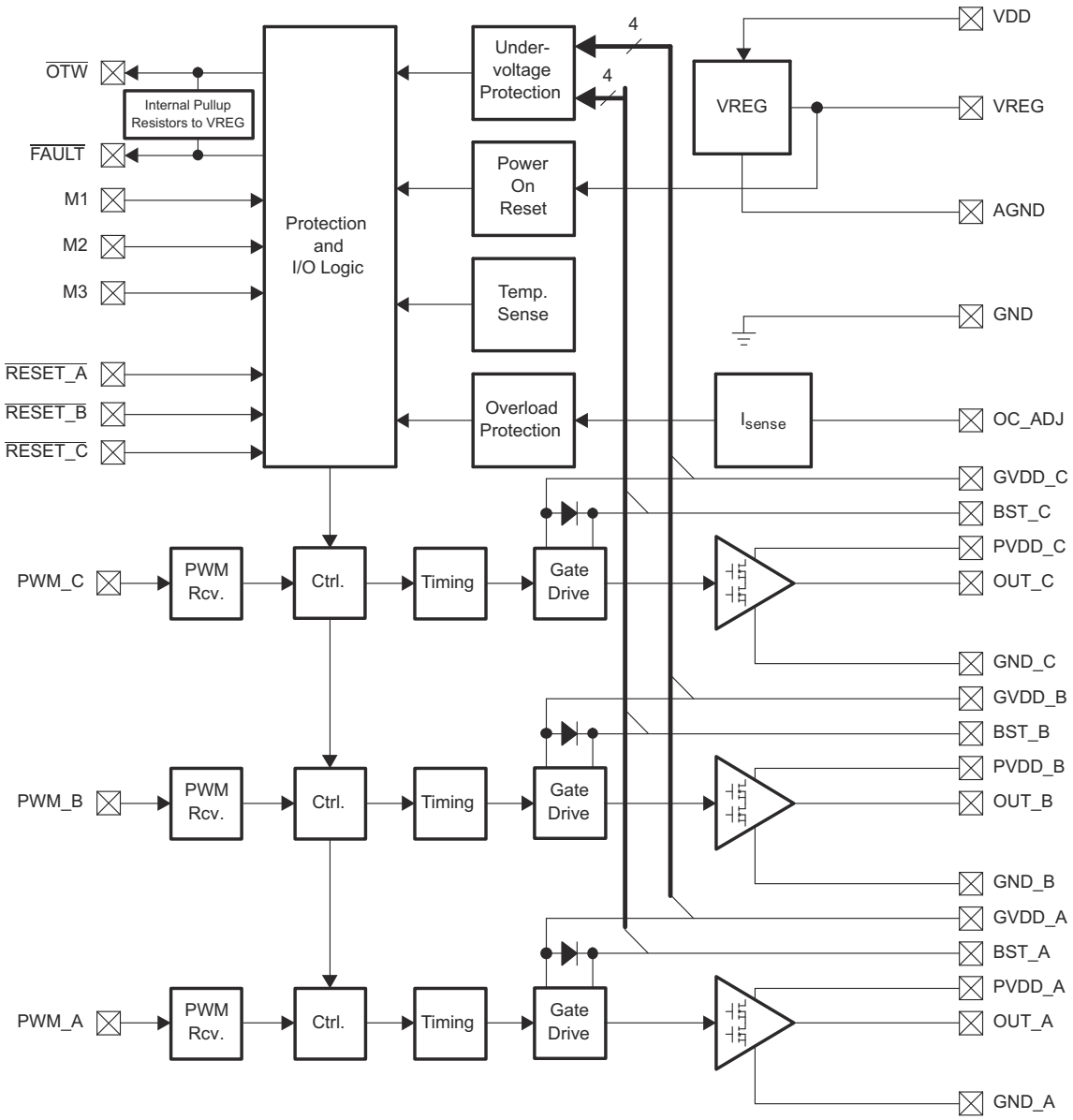
图 6-5. Output Duty Cycle vs Input Duty Cycle

7 Detailed Description

7.1 Overview

The DRV83x2 devices have three high-current half-H bridge outputs that are controlled by the six inputs PWM_x and $\overline{\text{RESET\_x}}$. When $\overline{\text{RESET\_A}}$ is low, OUT_A becomes high-impedance, allowing current to flow through the internal body diodes of the high-side and low-side FETs. When $\overline{\text{RESET\_A}}$ is high and PWM_A is low, OUT_A is driven low with its low-side FET enabled. When $\overline{\text{RESET\_A}}$ is high and PWM_A is high, OUT_A is driven high with its high-side FET enabled. Likewise is true for B and C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Error Reporting

The $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown, such as overtemperatue shut down, overcurrent shut-down, or undervoltage protection, is signaled by the $\overline{\text{FAULT}}$ pin going low. Likewise, $\overline{\text{OTW}}$ goes low when the device junction temperature exceeds 125°C (see 表 7-1).

表 7-1. Protection Mode Signal Descriptions

$\overline{\text{FAULT}}$	$\overline{\text{OTW}}$	DESCRIPTION
0	0	Overtemperature warning and (overtemperature shut down or overcurrent shut down or undervoltage protection) occurred
0	1	Overcurrent shut-down or GVDD undervoltage protection occurred
1	0	Overtemperature warning
1	1	Device under normal operation

TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an $\overline{\text{OTW}}$ signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to internal VREG (3.3 V) is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

7.3.2 Device Protection System

The DRV83x2 contain advanced protection circuits carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overcurrent, overtemperature, and undervoltage. The DRV83x2 respond to a fault by immediately setting the half bridge outputs in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overcurrent or overtemperature, the device automatically recovers when the fault condition has been removed or the gate supply voltage has increased. For highest possible reliability, reset the device externally no sooner than 1 second after the shutdown when recovering from an overcurrent shut down (OCSD) or OTSD fault.

7.3.2.1 Bootstrap Capacitor Undervoltage Protection

When the device runs at a low switching frequency (for example, less than 10 kHz with a 100-nF bootstrap capacitor), the bootstrap capacitor voltage might not be able to maintain a proper voltage level for the high-side gate driver. A bootstrap capacitor undervoltage protection circuit (BST_UVP) will prevent potential failure of the high-side MOSFET. When the voltage on the bootstrap capacitors is less than the required value for safe operation, the DRV83x2 will initiate bootstrap capacitor recharge sequences (turn off high side FET for a short period) until the bootstrap capacitors are properly charged for safe operation. This function may also be activated when PWM duty cycle is too high (for example, less than 20 ns off time at 10 kHz). Note that bootstrap capacitor might not be able to be charged if no load or extremely light load is presented at output during BST_UVP operation, so it is recommended to turn on the low side FET for at least 50 ns for each PWM cycle to avoid BST_UVP operation if possible.

For applications with lower than 10 kHz switching frequency and not to trigger BST_UVP protection, a larger bootstrap capacitor can be used (for example, 1-uF capacitor for 800-Hz operation). When using a bootstrap capacitor larger than 220 nF, it is recommended to add 5 ohm resistors between 12V GVDD power supply and GVDD_X pins to limit the inrush current on the internal bootstrap diodes.

7.3.2.1.1 Overcurrent (OC) Protection

The DRV83x2 have independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. There are two settings for OC protection through mode selection pins: cycle-by-cycle (CBC) current limiting mode and OC latching (OCL) shut down mode.

In CBC current limiting mode, the detector outputs are monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, that is, it performs a CBC current-limiting function rather than prematurely shutting down the device. This feature can effectively limit the inrush current during motor start-up or transient without damaging the device. During short to power and

short to ground conditions, since the current limit circuitry might not be able to control the current to a proper level, a second protection system triggers a latching shutdown, resulting in the related half bridge being set in the high-impedance (Hi-Z) state. Current limiting and overcurrent protection are independent for half-bridges A, B, and C, respectively.

图 7-1 illustrates cycle-by-cycle operation with high side OC event and 图 7-2 shows cycle-by-cycle operation with low side OC. Dashed lines are the operation waveforms when no CBC event is triggered and solid lines show the waveforms when CBC event is triggered. In CBC current limiting mode, when low side FET OC is detected, the device will turn off the affected low side FET and keep the high side FET at the same half bridge off until next PWM cycle; when high side FET OC is detected, the device will turn off the affected high side FET and turn on the low side FET at the half bridge until next PWM cycle.

It is important to note that if the input to a half bridge is held to a constant value when an over current event occurs in CBC, then the associated half bridge will be in a HI-Z state upon the over current event ending. Cycling IN_X will allow OUT_X to resume normal operation.

In OC latching shut down mode, the CBC current limit and error recovery circuits are disabled and an overcurrent condition will cause the device to shutdown. After shutdown, $\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$, and $\overline{\text{RESET\_C}}$ must be asserted to restore normal operation after the overcurrent condition is removed.

For added flexibility, the OC threshold is programmable using a single external resistor connected between the OC_ADJ pin and AGND pin. See 表 7-2 for information on the correlation between programming-resistor value and the OC threshold.

The values in 表 7-2 show typical OC thresholds for a given resistor. Assuming a fixed resistance on the OC_ADJ pin across multiple devices, a 20% device-to-device variation in OC threshold measurements is possible. Therefore, this feature is designed for system protection and not for precise current control.

表 7-2. Programming-Resistor Values and OC Threshold

OC-ADJUST RESISTOR VALUES (kΩ)	MAXIMUM CURRENT BEFORE OC OCCURS (A)
19(1)	13.2
22	11.6
24	10.7
27	9.7
30	8.8
36	7.4

(1) Recommended to use in OC Latching Mode Only

It should be noted that a properly functioning overcurrent detector assumes the presence of a proper inductor or power ferrite bead at the power-stage output. Short-circuit protection is not ensured with a direct short at the output pins of the power stage.

7.3.2.2 Overtemperature Protection

The DRV83x2 have a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTSD is latched in this case and $\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$, and $\overline{\text{RESET\_C}}$ must be asserted low to clear the latch.

7.3.2.3 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV83x2 fully protect the device in any power-up / down and brownout situation. While powering up, the POR circuit resets the overcurrent circuit and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors have increased above the UVP threshold.

7.3.2.4 Device Reset

Three reset pins are provided for independent control of half-bridges A, B, and C. When $\overline{\text{RESET\_X}}$ is asserted low, two power-stage FETs in half-bridges X are forced into a high-impedance (Hi-Z) state.

A rising-edge transition on reset input allows the device to resume operation after a shut-down fault. That is, when half-bridge X has OC shutdown in CBC mode, a low to high transition of $\overline{\text{RESET\_X}}$ pin will clear the fault and $\overline{\text{FAULT}}$ pin. When an OTSD or OC shutdown in Latching mode occurs, all three $\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$, and $\overline{\text{RESET\_C}}$ need to have a low to high transition to clear the fault and reset $\overline{\text{FAULT}}$ signal.

7.4 Device Functional Modes

7.4.1 Different Operational Modes

The DRV83x2 support two different modes of operation:

- Three-phase (3PH) or three half bridges (HB) with CBC current limit
- Three-phase or three half bridges with OC latching shutdown (no CBC current limit)

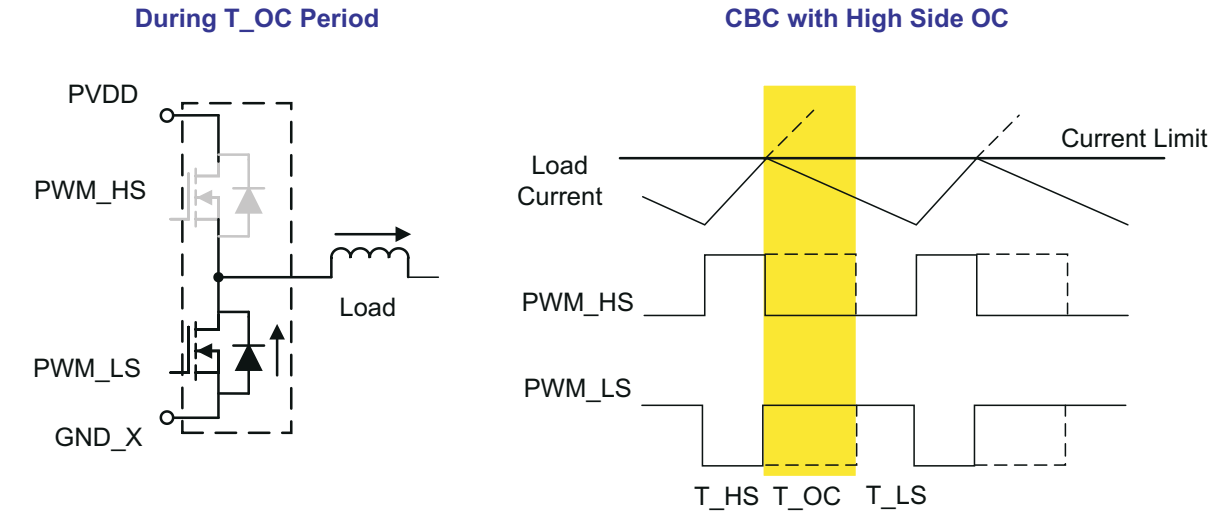
Because each half bridge has independent supply and ground pins, a shunt sensing resistor can be inserted between PVDD to PVDD_X or GND_X to GND (ground plane). A high side shunt resistor between PVDD and PVDD_X is recommended for differential current sensing because a high bias voltage on the low side sensing could affect device operation. If low side sensing has to be used, a shunt resistor value of 10 mΩ or less or sense voltage 100 mV or less is recommended.

图 8-1 and 图 8-4 show the three-phase application examples, and 图 8-5 shows how to connect to DRV83x2 with some simple logic to accommodate conventional 6 PWM inputs control.

We recommend using a complementary control scheme for switching phases to prevent circulated energy flowing inside the phases and to make current limiting feature active all the time. Complementary control scheme also forces the current flowing through sense resistors all the time to have a better current sensing and control of the system.

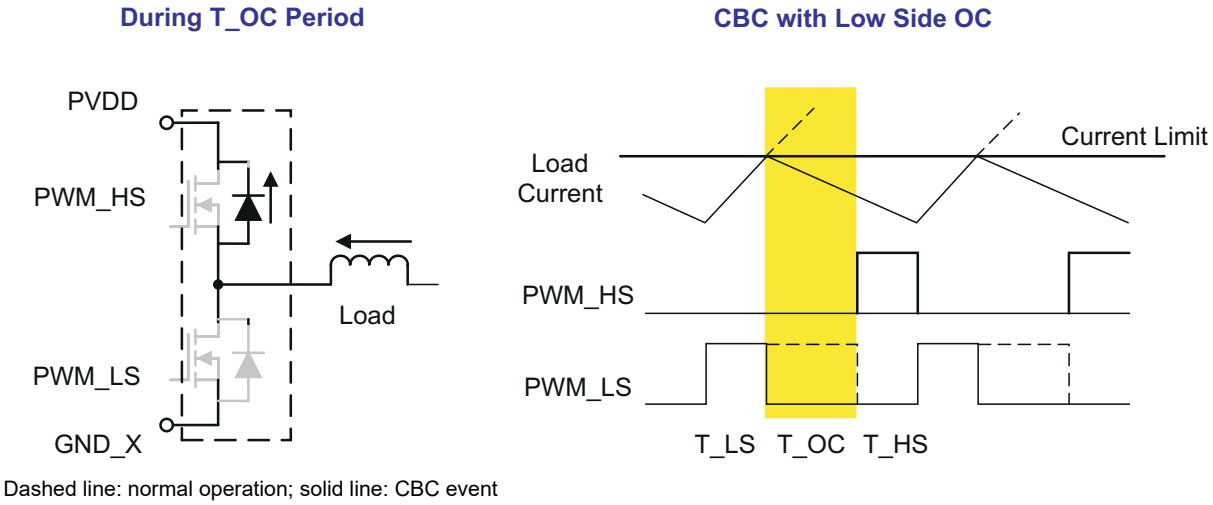
图 8-6 shows six steps trapezoidal scheme with hall sensor control and 图 8-7 shows six steps trapezoidal scheme with sensorless control. The hall sensor sequence in real application might be different than the one we showed in 图 8-6 depending on the motor used. Please check motor manufacture datasheet for the right sequence in applications. In six step trapezoidal complementary control scheme, a half bridge with larger than 50% duty cycle will have a positive current and a half bridge with less than 50% duty cycle will have a negative current. For normal operation, changing PWM duty cycle from 50% to 100% will adjust the current from 0 to maximum value with six steps control. It is recommended to apply a minimum 50 ns to 100 ns PWM pulse at each switching cycle at lower side to properly charge the bootstrap cap. The impact of minimum pulse at low side FET is pretty small, for example, the maximum duty cycle is 99.9% with 100 ns minimum pulse on low side. $\overline{\text{RESET\_X}}$ pin can be used to get channel X into high impedance mode. If you prefer PWM switching one channel but hold low side FET of the other channel on (and third channel in Hi-Z) for 2-quadrant mode, OT latching shutdown mode is recommended to prevent the channel with low side FET on stuck in Hi-Z during OC event in CBC mode.

The DRV83x2 can also be used for sinusoidal waveform control and field oriented control. Please check TI website MCU motor control library for control algorithms.



Dashed line: normal operation; solid line: CBC event

图 7-1. Cycle-by-Cycle Operation With High-Side OC



Dashed line: normal operation; solid line: CBC event

图 7-2. Cycle-by-Cycle Operation With Low-Side OC

8 Application and Implementation

备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The DRV83x2 devices are typically used to drive 3-phase brushless DC motors.

8.2 Typical Applications

8.2.1 Three-Phase Operation

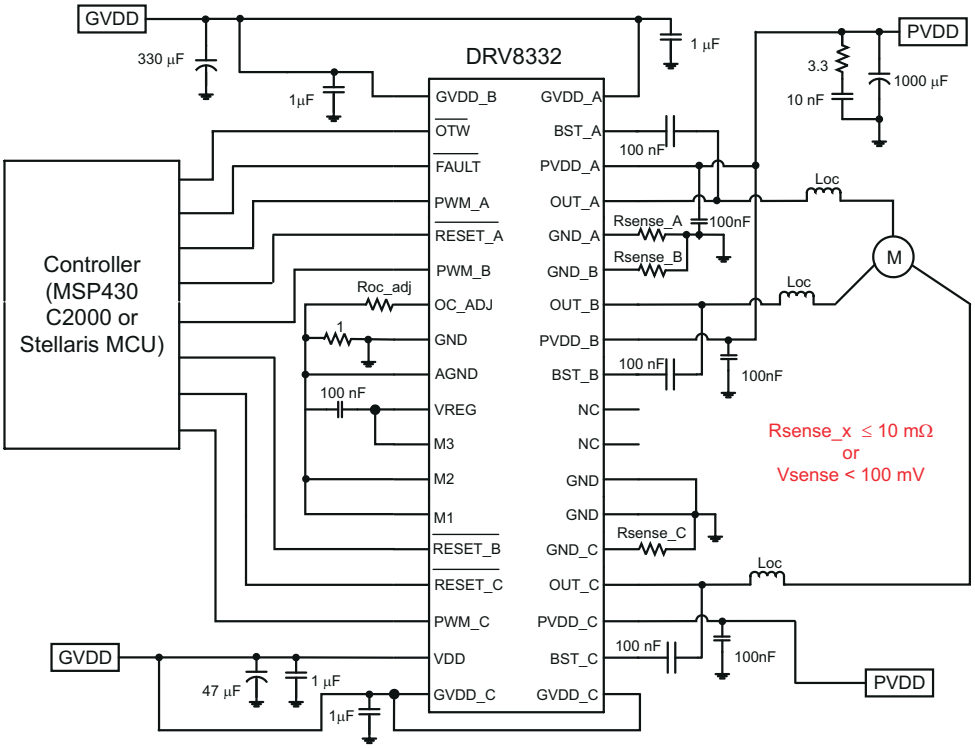


图 8-1. DRV8332 Application Diagram for Three-Phase Operation Schematic

8.2.1.1 设计要求

本节介绍了设计注意事项。

表 8-1. 设计参数

设计参数	基准	示例值
电机电压	PVDD_x	24V
电机电流（峰值和 RMS）	I_{PVDD}	6A 峰值，3A RMS
过流阈值	OC_{TH}	OC_ADJ = 27kΩ，9.7A
过流行为	OC	M1 = 0，逐周期

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Motor Voltage

BLDC motors are typically rated for a certain voltage. Higher voltages generally have the advantage of causing current to change faster through the inductive windings, which allows for higher RPMs. Lower voltages allow for more accurate control of phase currents.

8.2.1.2.2 Current Requirement of 12 V Power Supply

The DRV83x2 require a 12-V power supply for GVDD and VDD pins. The total supply current is pretty low at room temp (less than 50 mA), but the current could increase significantly when the device temperature goes too high (for example, above 125°C), especially at heavy load conditions due to substrate current collection by 12-V guard rings. So it is recommended to design the 12-V power supply with current capability at least 5-10% of your load current and no less than 100 mA to assure the device performance across all temperature range.

8.2.1.2.3 Voltage of Decoupling Capacitor

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. The high frequency decoupling capacitor should use ceramic capacitor with X5R or better rating. For a 50-V application, a minimum voltage rating of 63 V is recommended.

8.2.1.2.4 Overcurrent Threshold

When choosing the resistor value for OC_ADJ, consider the peak current allowed under normal system behavior, the resistor tolerance, and the fact that the 表 7-2 currents have a ±10% tolerance. For example, if 6A is the highest system current allowed across all normal behavior, a 27kΩ OC_ADJ resistor with 10% tolerance is a reasonable choice, as it would set the OC_{TH} to approximately 8A – 12A.

8.2.1.2.5 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals I_{RMS}^{2} x R. For example, if peak motor current is 3A, RMS motor current is 2 A, and a 0.05Ω sense resistor is used, the resistor will dissipate $2A^2$ x 0.05Ω = 0.2W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.1.2.6 Output Inductor Selection

For normal operation, inductance in motor (assume larger than 10 µH) is sufficient to provide low di/dt output (for example, for EMI) and proper protection during overload condition (CBC current limiting feature). So no additional output inductors are needed during normal operation.

However during a short condition, the motor (or other load) could be shorted, so the load inductance might not present in the system anymore; the current in short condition can reach such a high level that may exceed the abs max current rating due to extremely low impendence in the short circuit path and high di/dt before oc detection circuit kicks in. So a ferrite bead or inductor is recommended to use the short-circuit protection feature in DRV83x2. With an external inductor or ferrite bead, the current will rise at a much slower rate and reach a

lower current level before oc protection starts. The device will then either operate CBC current limit or OC shut down automatically (when current is well above the current limit threshold) to protect the system.

For a system that has limited space, a power ferrite bead can be used instead of an inductor. The current rating of ferrite bead has to be higher than the RMS current of the system at normal operation. A ferrite bead designed for very high frequency is NOT recommended. A minimum impedance of 10 Ω or higher is recommended at 10 MHz or lower frequency to effectively limit the current rising rate during short circuit condition.

The TDK MPZ2012S300A and MPZ2012S101A (with size of 0805 inch type) have been tested in our system to meet short circuit conditions in the DRV8312. But other ferrite beads that have similar frequency characteristics can be used as well.

For higher power applications, such as in the DRV8332, there might be limited options to select suitable ferrite bead with high current rating. If an adequate ferrite bead cannot be found, an inductor can be used.

The inductance can be calculated as:

$$Loc\_\min = \frac{PVDD \cdot Toc\_delay}{Ipeak - Iave} \tag{1}$$

where

- Toc_delay = 250 ns
- Ipeak = 15 A (below abs max rating).

Because an inductor usually saturates quickly after reaching its current rating, it is recommended to use an inductor with a doubled value or an inductor with a current rating well above the operating condition.

8.2.1.3 Application Curves

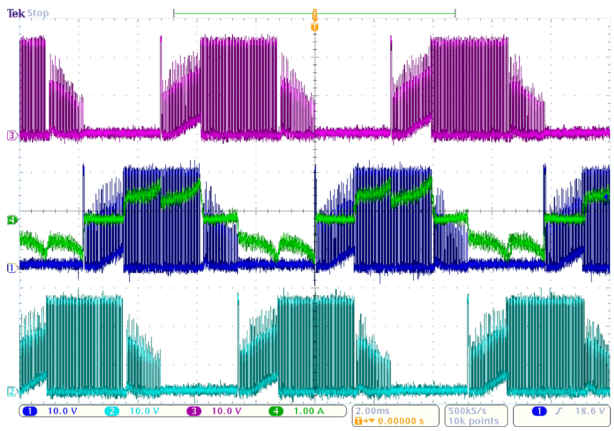


图 8-2. Three-Phase BLDC Commutation With Current Shown for 1 Phase

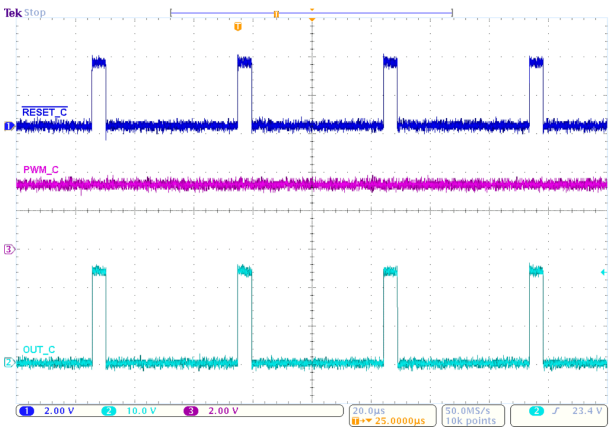


图 8-3. Input and Output Functionality

8.2.2 DRV8312 Application Diagram for Three-Phase Operation

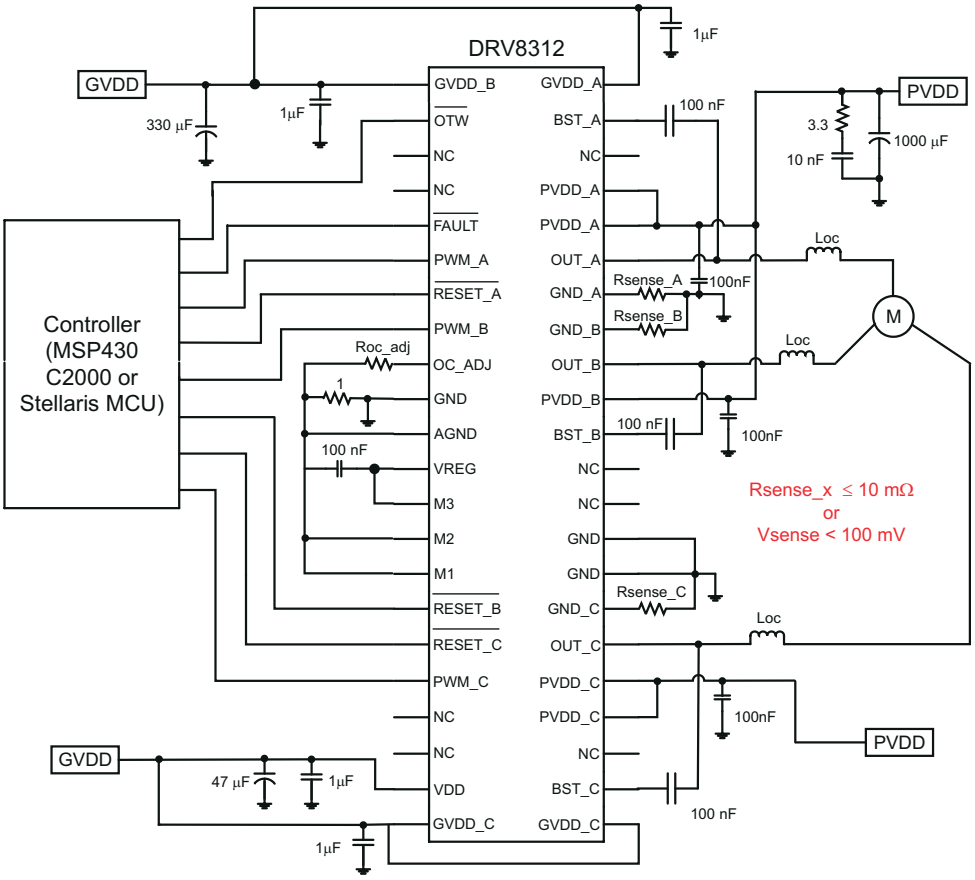


图 8-4. DRV8312 Application Diagram for Three-Phase Operation Schematic

8.2.3 Control Signal Logic With Conventional 6 PWM Input Scheme

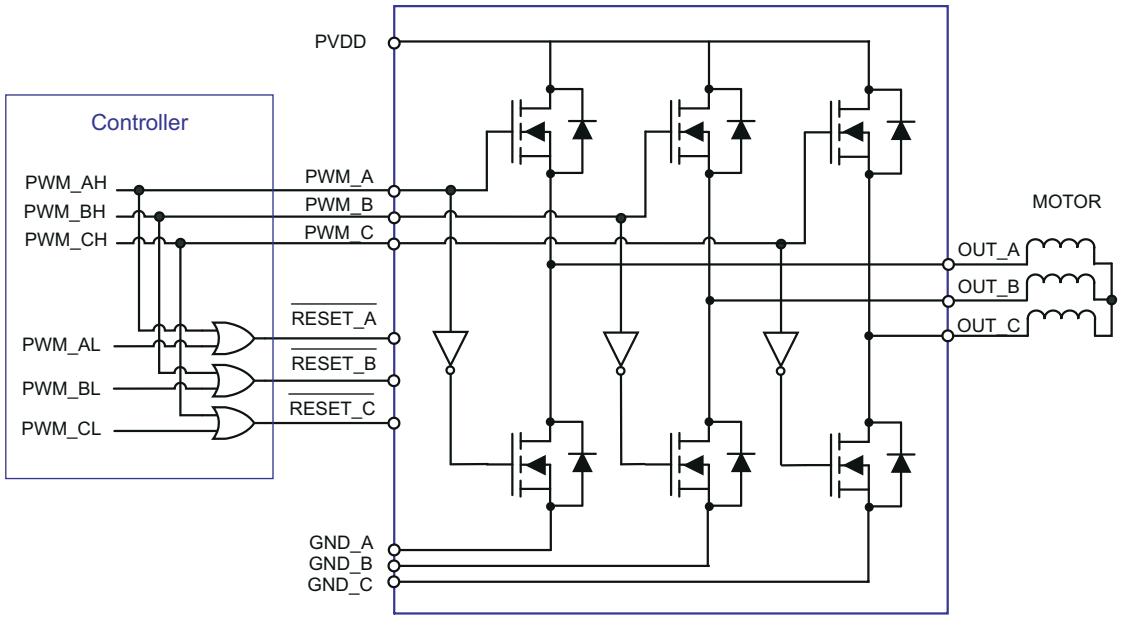


图 8-5. Control Signal Logic With Conventional 6 PWM Input Schematic

8.2.4 Hall Sensor Control With 6 Steps Trapezoidal Scheme

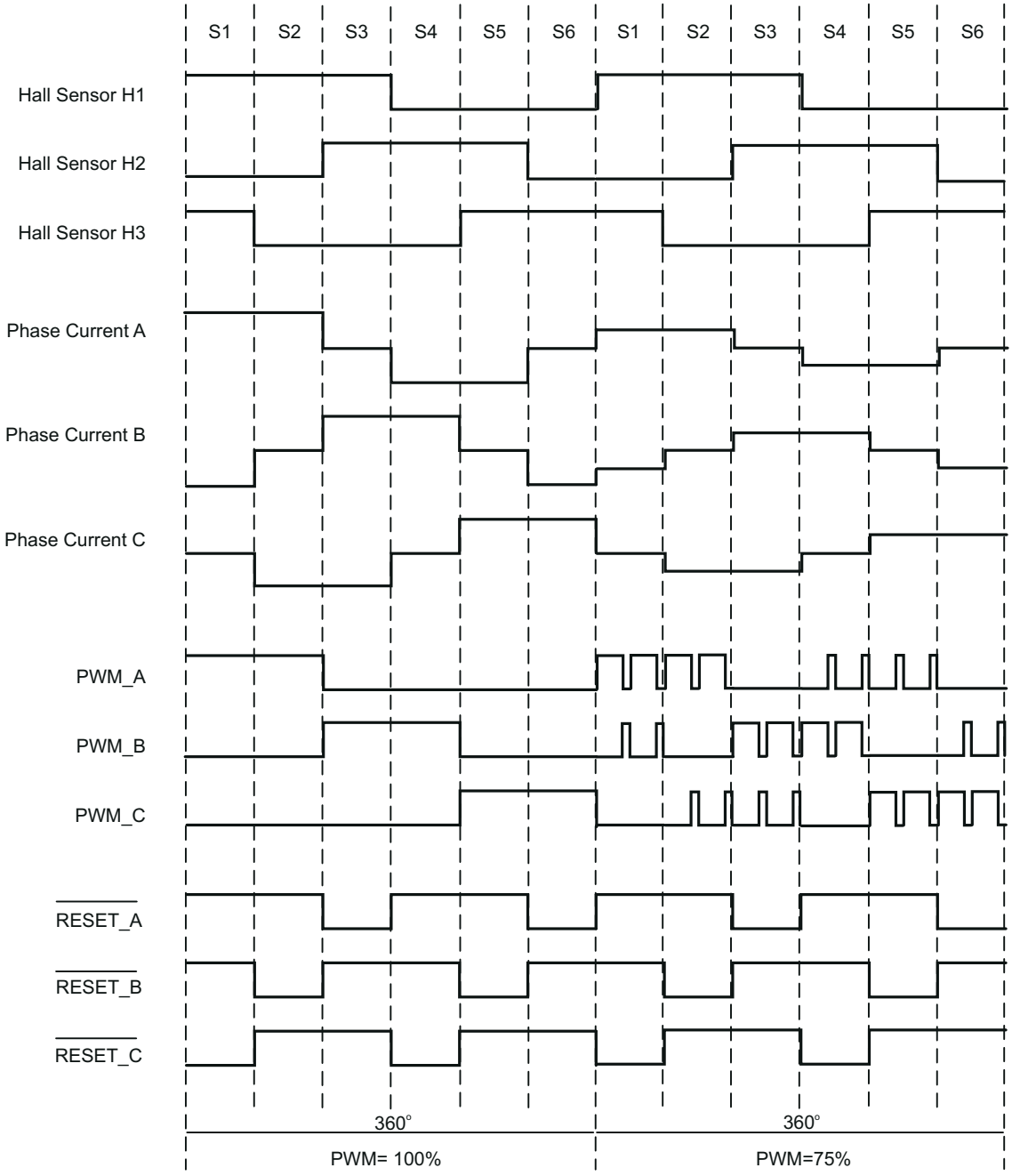


图 8-6. Hall Sensor Control With 6 Steps Trapezoidal Scheme Schematic

8.2.5 Sensorless Control With 6 Steps Trapezoidal Scheme

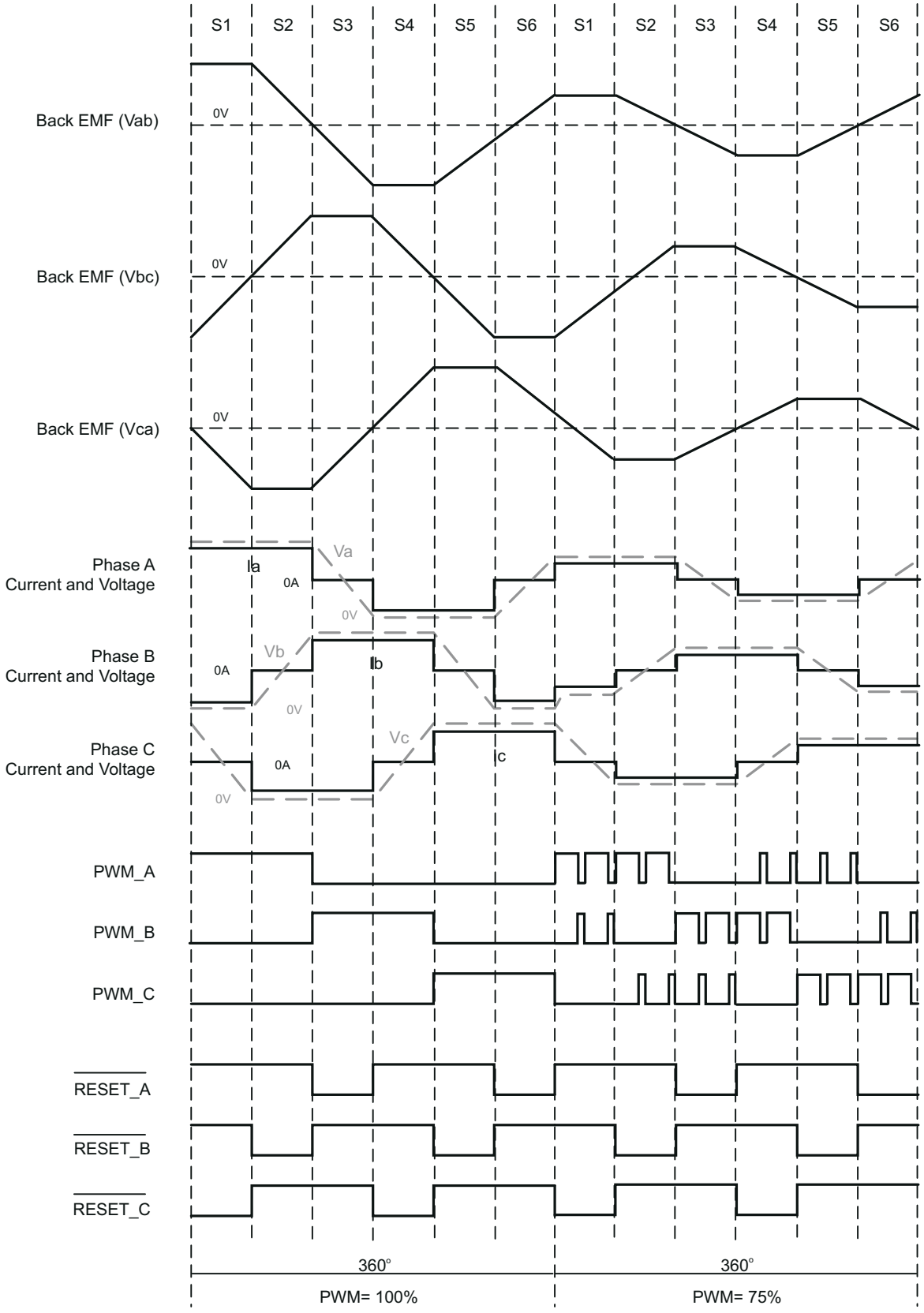


图 8-7. Sensorless Control With 6 Steps Trapezoidal Scheme Schematic

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply’s capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

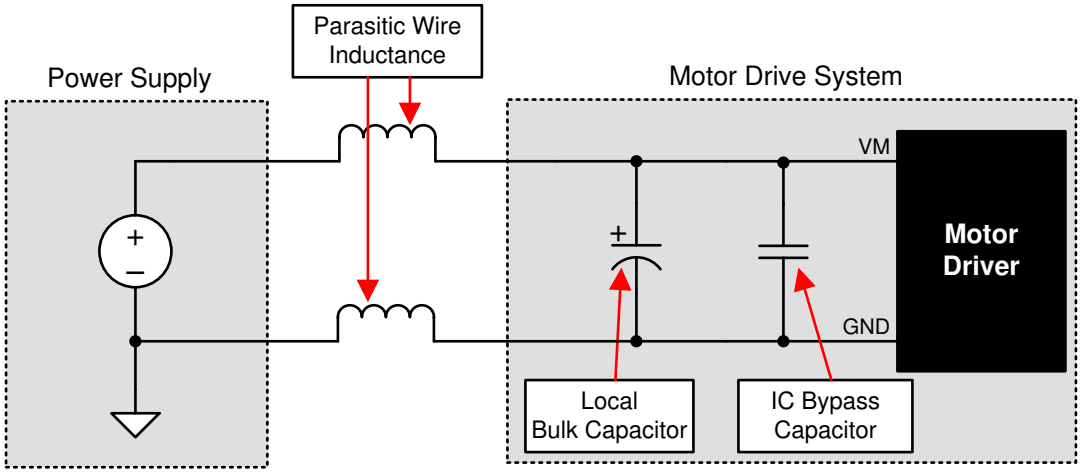


图 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

9.2 System Power-Up and Power-Down Sequence

9.2.1 Powering Up

The DRV83x2 do not require a power-up sequence. The outputs of the H-bridges remain in a high impedance state until the gate-drive supply voltage GVDD_X and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, holding $\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$, and $\overline{\text{RESET\_C}}$ in a low state while powering up the device is recommended. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

9.2.2 Powering Down

The DRV83x2 do not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the UVP voltage threshold (see the *Electrical*

Characteristics section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$ and $\overline{\text{RESET\_C}}$ low during power down to prevent any unknown state during this transition.

9.3 System Design Recommendations

9.3.1 VREG Pin

The VREG pin is used for internal logic and should not be used as a voltage source for external circuitries. The capacitor on VREG pin should be connected to AGND.

9.3.2 VDD Pin

The transient current in VDD pin could be significantly higher than average current through VDD pin. A low resistive path to GVDD should be used. A 22-µF to 47-µF capacitor should be placed on VDD pin beside the 100-nF to 1-µF decoupling capacitor to provide a constant voltage during transient.

9.3.3 OTW Pin

$\overline{\text{OTW}}$ reporting indicates the device approaching high junction temperature. This signal can be used with MCU to decrease system power when $\overline{\text{OTW}}$ is low in order to prevent OT shut down at a higher temperature.

No external pull up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{OTW}}$ pin has an internal pullup resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull up resistor to 5V is needed.

9.3.4 FAULT Pin

The $\overline{\text{FAULT}}$ pin reports any fault condition resulting in device shut down. No external pull up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{FAULT}}$ pin has an internal pullup resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull upresistor to 5V is needed.

9.3.5 OC_ADJ Pin

For accurate control of the overcurrent protection, the OC_ADJ pin has to be connected to AGND through an OC adjust resistor.

9.3.6 PWM_X and RESET_X Pins

It is recommanded to connect these pins to either AGND or GND when they are not used, and these pins only support 3.3V logic.

9.3.7 Mode Select Pins

Mode select pins (M1, M2, and M3) should be connected to either VREG (for logic high) or AGND for logic low. It is not recommended to connect mode pins to board ground if 1-Ω resistor is used between AGND and GND.

10 Layout

10.1 Layout Guidelines

10.1.1 PCB Material Recommendation

- FR-4 Glass Epoxy material with 2 oz. copper on both top and bottom layer is recommended for improved thermal performance (better heat sinking) and less noise susceptibility (lower PCB trace inductance).

10.1.2 Ground Plane

- Because of the power level of these devices, it is recommended to use a big unbroken single ground plane for the whole system / board.
- The ground plane can be easily made at bottom PCB layer.
- In order to minimize the impedance and inductance of ground traces, the traces from ground pins should keep as short and wide as possible before connected to bottom ground plane through vias.
- Multiple vias are suggested to reduce the impedance of vias. Try to clear the space around the device as much as possible especially at bottom PCB side to improve the heat spreading.

10.1.3 Decoupling Capacitor

- High frequency decoupling capacitors (100 nF) should be placed close to PVDD_X pins and with a short ground return path to minimize the inductance on the PCB trace.

10.1.4 AGND

- AGND is a localized internal ground for logic signals. A 1-Ω resistor is recommended to be connected between GND and AGND to isolate the noise from board ground to AGND.
- There are other two components are connected to this local ground: 0.1-µF capacitor between VREG to AGND and Roc_adj resistor between OC_ADJ and AGND.
- Capacitor for VREG should be placed close to VREG and AGND pins and connected without vias.

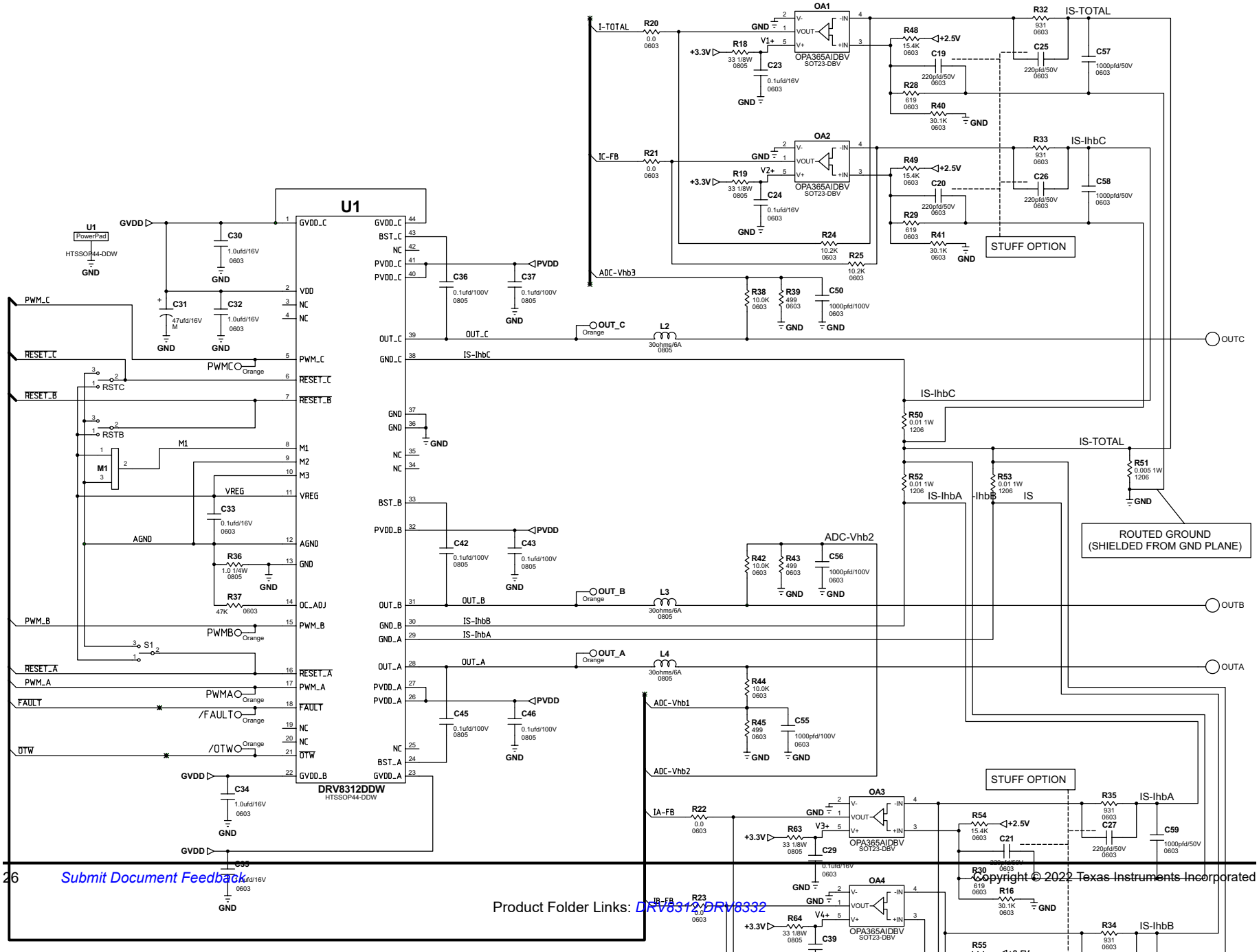
10.2 Layout Example

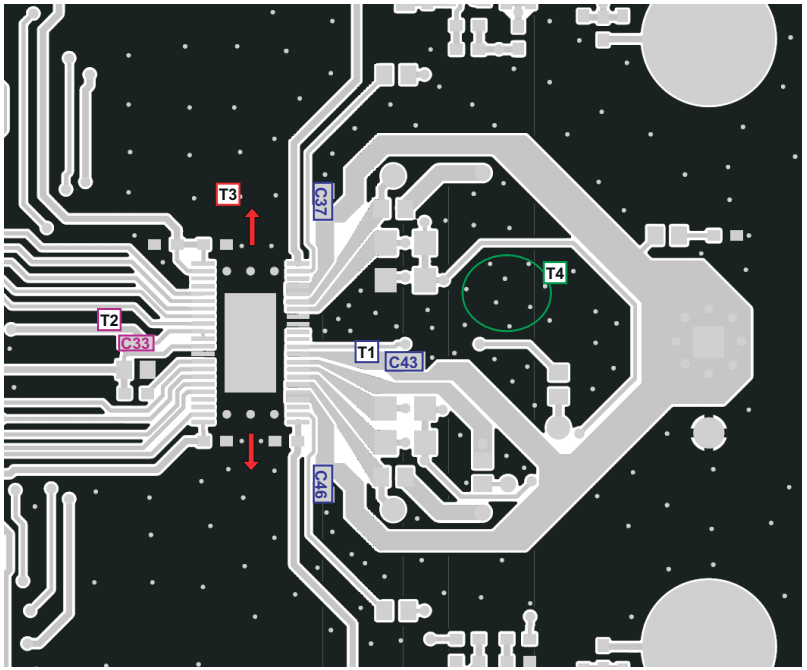
10.2.1 Current Shunt Resistor

- If current shunt resistor is connected between GND_X to GND or PVDD_X to PVDD, make sure there is only one single path to connect each GND_X or PVDD_X pin to shunt resistor, and the path is short and symmetrical on each sense path to minimize the measurement error due to additional resistance on the trace.

An example of the schematic and PCB layout of DRV8312 are shown in 图 10-1, 图 10-2, and 图 10-3.

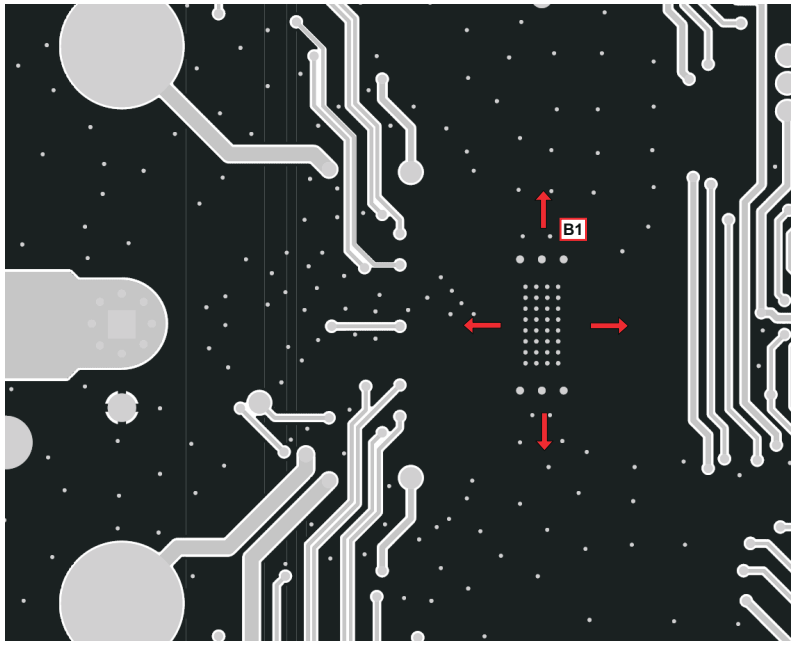
10.2.1.1





T1: PVDD decoupling capacitors C37, C43, and C46 should be placed very close to PVDD_X pins and ground return path.
T2: VREG decoupling capacitor C33 should be placed very close to VREG abd AGND pins.
T3: Clear the space above and below the device as much as possible to improve the thermal spreading.
T4: Add many vias to reduce the impedance of ground path through top to bottom side. Make traces as wide as possible for ground path such as GND_X path.

图 10-2. Printed Circuit Board – Top Layer



B1: Do not block the heat transfer path at bottom side. Clear as much space as possible for better heat spreading.

图 10-3. Printed Circuit Board – Bottom Layer

10.3 Thermal Considerations

The thermally enhanced package provided with the DRV8332 is designed to interface directly to heat sink using a thermal interface compound in between, (that is, Ceramique from Arctic Silver, TIMTronics 413, and so on). The heat sink then absorbs heat from the ICs and couples it to the local air. It is also a good practice to connect the heatsink to system ground on the PCB board to reduce the ground noise.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this example the power pad or heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed power pad or heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W or °C-mm^2/W). The approximate exposed heat slug size is as follows:

- DRV8332, 36-pin PSOP3 ····· 0.124 in^2 (80 mm^2)

The thermal resistance of a thermal pad is considered higher than a thin thermal grease layer and is not recommended. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

See the TI application report, *IC Package Thermal Metrics* (SPRA953), for more thermal information.

10.3.1 Thermal Via Design Recommendation

Thermal pad of the DRV8312 is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB in order to deliver the power specified in the datasheet. The figure below shows the recommended thermal via and land pattern design for the DRV8312. For additional information, see TI application report, PowerPad Made Easy (SLMA004) and PowerPad Layout Guidelines (SLOA120).

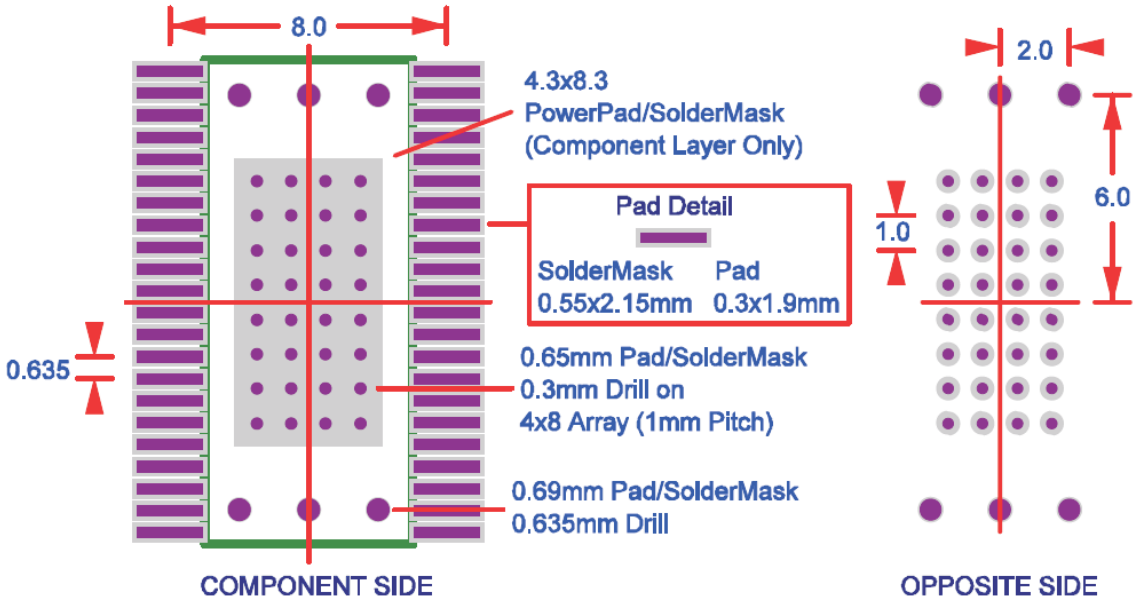


图 10-4. DRV8312 Thermal Via Footprint

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8312	Click here	Click here	Click here	Click here	Click here
DRV8332	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

所有商标均为其各自所有者的财产。

11.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8312DDW	Active	Production	HTSSOP (DDW) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDW.A	Active	Production	HTSSOP (DDW) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDW.B	Active	Production	HTSSOP (DDW) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDWR	Active	Production	HTSSOP (DDW) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDWR.A	Active	Production	HTSSOP (DDW) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDWR.B	Active	Production	HTSSOP (DDW) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDWRG4	Active	Production	HTSSOP (DDW) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDWRG4.A	Active	Production	HTSSOP (DDW) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312
DRV8312DDWRG4.B	Active	Production	HTSSOP (DDW) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8312

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

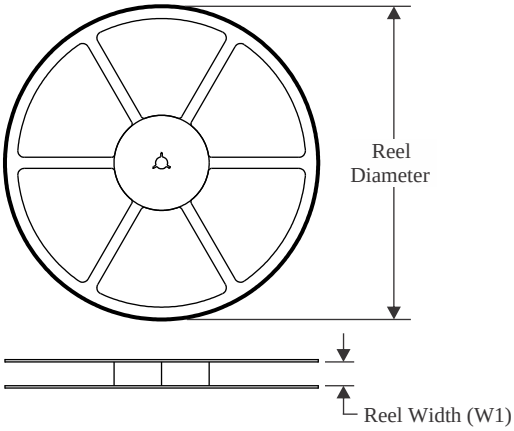
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8332 :

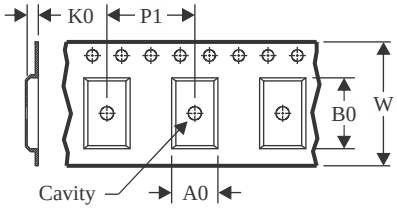
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

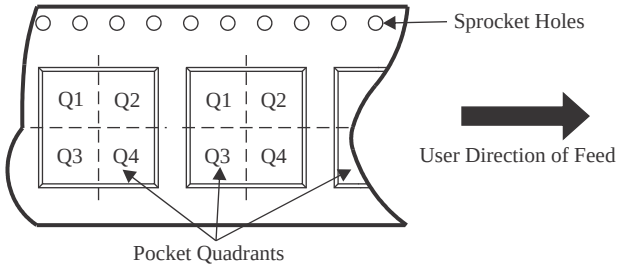


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

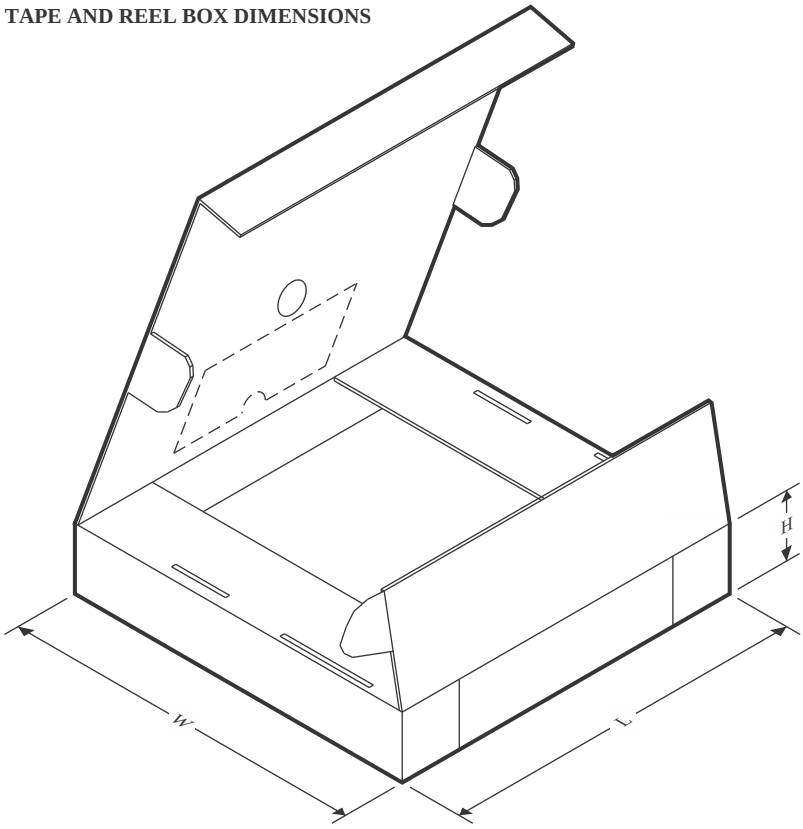
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8312DDWR	HTSSOP	DDW	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
DRV8312DDWRG4	HTSSOP	DDW	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

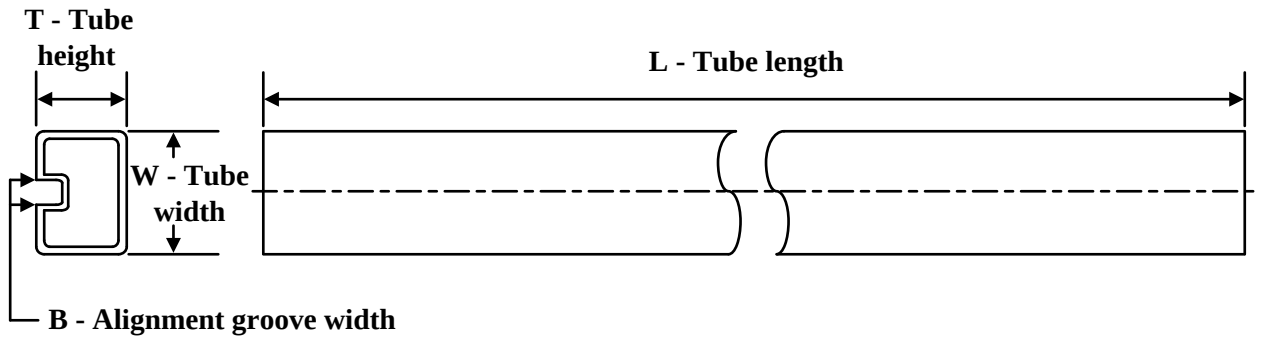
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8312DDWR	HTSSOP	DDW	44	2000	350.0	350.0	43.0
DRV8312DDWRG4	HTSSOP	DDW	44	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8312DDW	DDW	HTSSOP	44	35	530	11.89	3600	4.9
DRV8312DDW.A	DDW	HTSSOP	44	35	530	11.89	3600	4.9
DRV8312DDW.B	DDW	HTSSOP	44	35	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

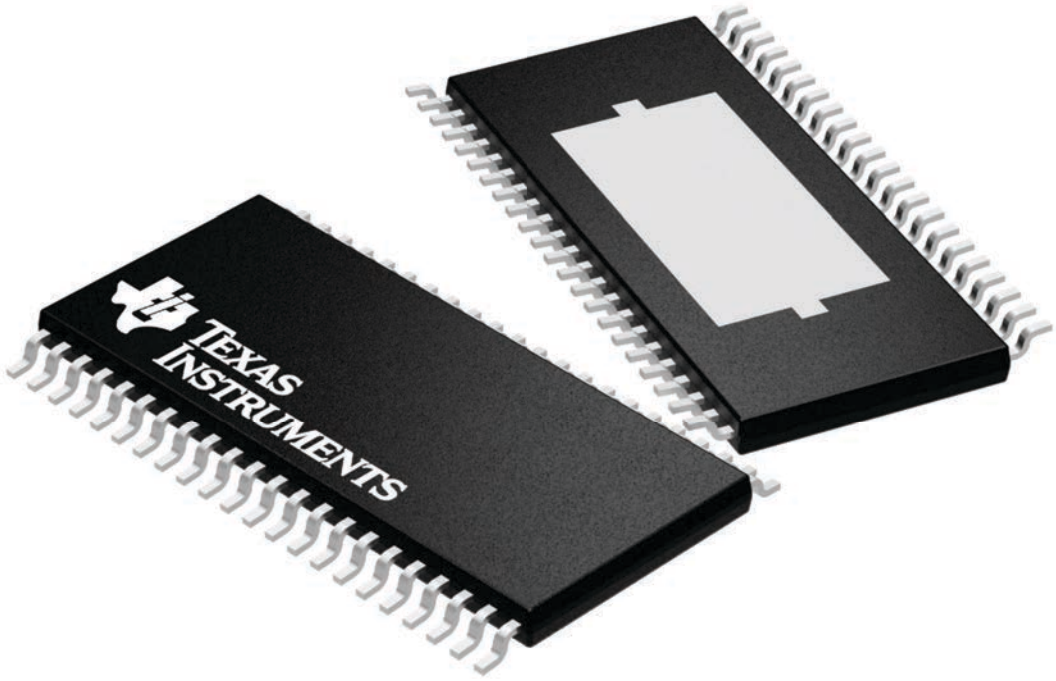
DDW 44

PowerPAD TSSOP - 1.2 mm max height

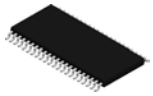
6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224876/A

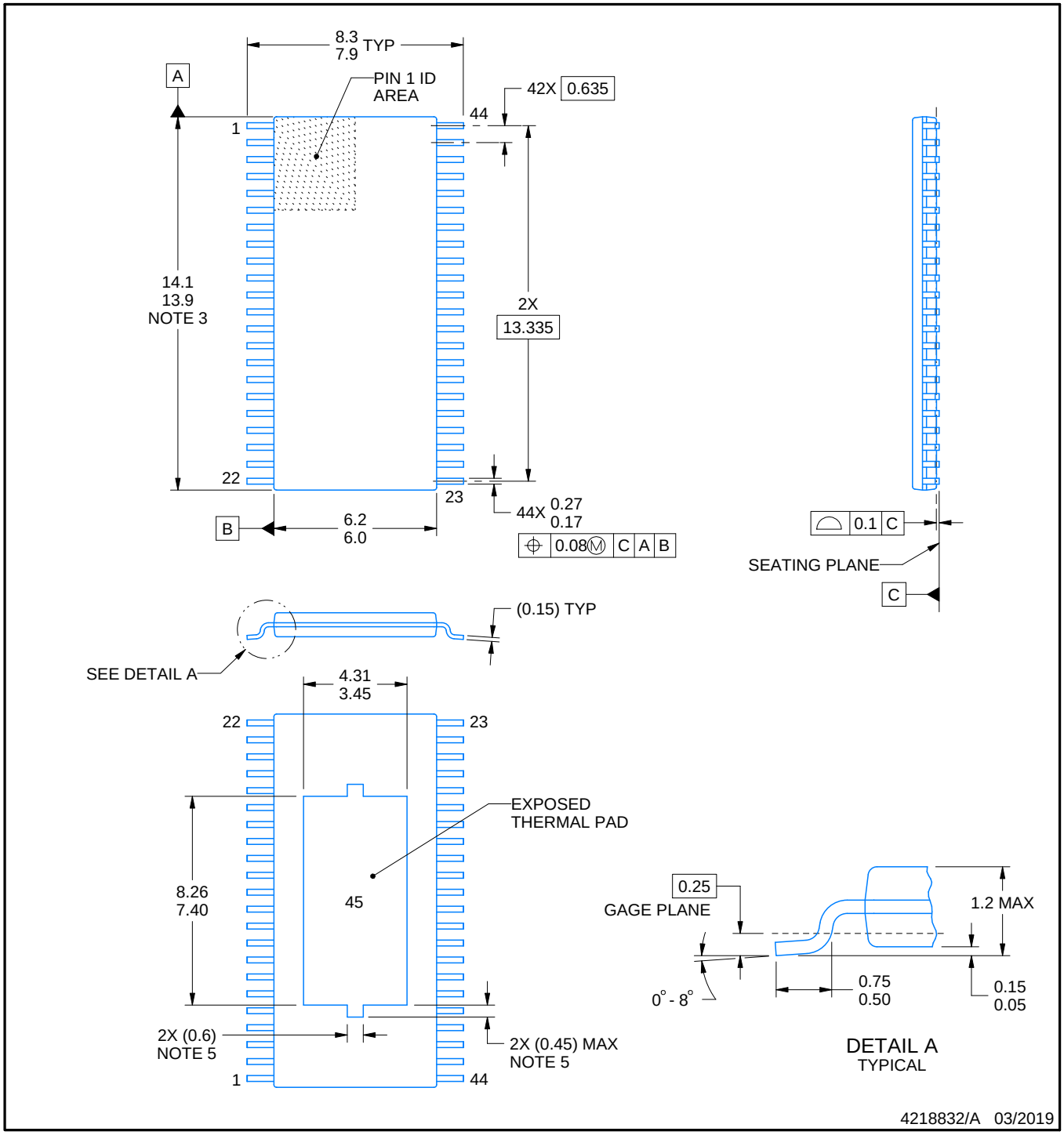


PACKAGE OUTLINE

DDW0044B

PowerPAD™ TSSOP - 1.2 mm max height

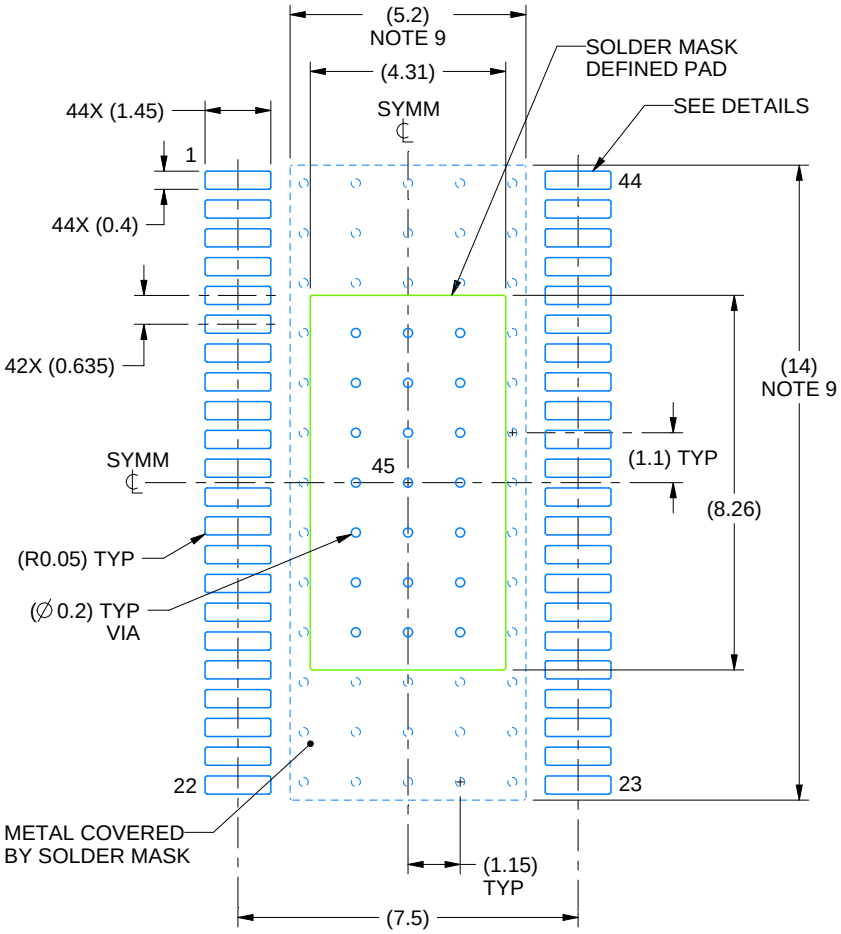
PLASTIC SMALL OUTLINE



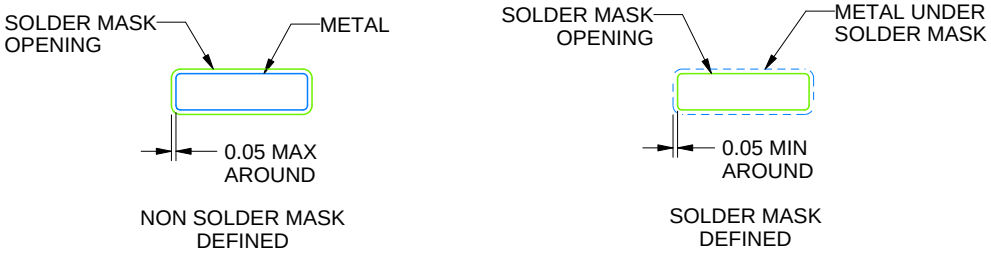
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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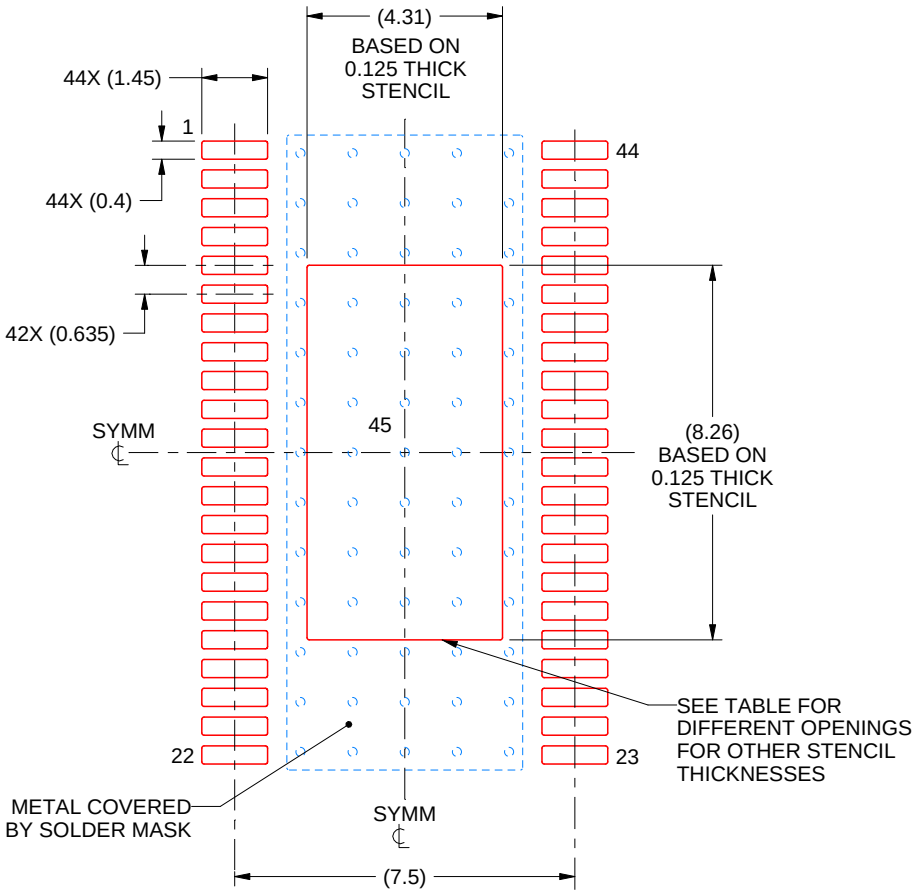
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.82 X 9.23
0.125	4.31 X 8.26 (SHOWN)
0.15	3.93 X 7.54
0.175	3.64 X 6.98

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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