DRV8300U：100V 三相 BLDC 栅极驱动器

1 特性

- 100V 三相半桥栅极驱动器
  - 驱动 N 沟道 MOSFET (NMOS)
  - 栅极驱动器电源 (GVDD)：5-20V
  - MOSFET 电源 (SHx) 支持高达 100V 的电压
- 集成自举二极管 (DRV8300UD 器件)
- 支持反相和同相 INLx 输入
- 自举栅极驱动架构
  - 750mA 拉电流
  - 1.5A 灌电流
- 支持由高达 15 节串联电池供电的应用
- 支持标准 MOSFET 的更高 BSTUV（8V 典型值）和 GVDDUV（7.6V 典型值）阈值
- SHx 引脚具有低漏电流（小于 55μA）
- 绝对最大 BSTx 电压高达 125V
- SHx 引脚瞬态负压可达 -22V
- 内置跨导保护
- 针对 QFN 封装型号，可通过 DT 引脚调节死区时间
- 针对 TSSOP 封装型号，固定插入 200ns 死区时间
- 支持 3.3V 和 5V 逻辑输入（绝对最大值为 20V）
- 4ns 典型传播延迟匹配
- 紧凑型 QFN 和 TSSOP 封装
- 具有电源块的高效系统设计
- 集成保护特性
  - BST 欠压锁定 (BSTUV)
  - GVDD 欠压 (GVDDUV)

2 应用

- 电动自行车、电动踏板车和电动汽车
- 风扇、泵和伺服驱动器
- 无刷直流 (BLDC) 电机模块和 PMSM
- 无线园艺和电动工具、割草机
- 无线真空吸尘器
- 无人机、机器人和遥控玩具
- 工业和物流机器人

3 说明

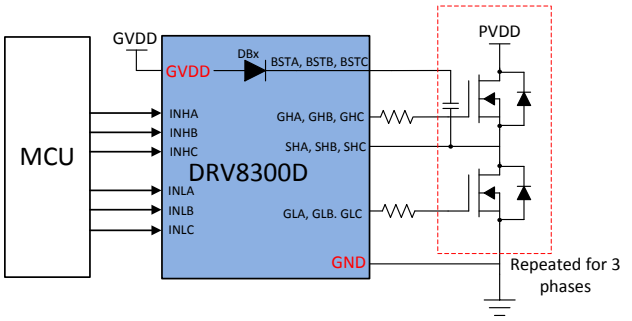
DRV8300U 是一款 100V 三相半桥栅极驱动器，能够驱动高侧和低侧 N 沟道功率 MOSFET。DRV8300UD 使用集成自举二极管和外部电容为高侧 MOSFET 生成合适的栅极驱动电压。GVDD 用于为低侧 MOSFET 生成栅极驱动电压。栅极驱动架构支持高达 750mA 的峰值拉电流和 1.5A 的灌电流。

相位引脚 SHx 能够承受显著的负电压瞬变；而高侧栅极驱动器电源 BSTx 和 GHx 能够支持更高的正电压瞬变 (125V) 绝对最大值，从而提高系统的鲁棒性。较小的传播延迟和延迟匹配参数可尽可能降低死区时间要求，从而进一步提高效率。通过 GVDD 和 BST 欠压锁定为低侧和高侧提供欠压保护。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV8300UDPW	TSSOP (20)	6.40mm × 4.40mm
DRV8300UDIPW	TSSOP (20)	6.40mm × 4.40mm
DRV8300UDRGE	VQFN (24)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



DRV8300UD 的简化原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2022) to Revision A (October 2022)	Page
• 将器件状态更新为“量产数据”	1

5 Device Comparison Table

Device Variants	Package	Integrated Bootstrap Diode	GLx polarity with respect to INLx Input	Deadtime
DRV8300UD	20-Pin TSSOP	Yes	Inverted	Fixed
DRV8300UDI		Yes	Non-Inverted	Fixed
DRV8300UD	24-Pin VQFN	Yes	Non-Inverted or Inverted	Variable

表 5-1. DRV8300 vs DRV8300U comparison

Parameters	DRV8300	DRV8300U
GVDDUV rising	4.6-V (typ)	8.3-V (typ)
GVDDUV falling	4.35-V (typ)	8-V (typ)
BSTUV rising	4.2-V (typ)	8-V (typ)
BSTUV falling	4-V (typ)	7.6-V(typ)

6 Pin Configuration and Functions

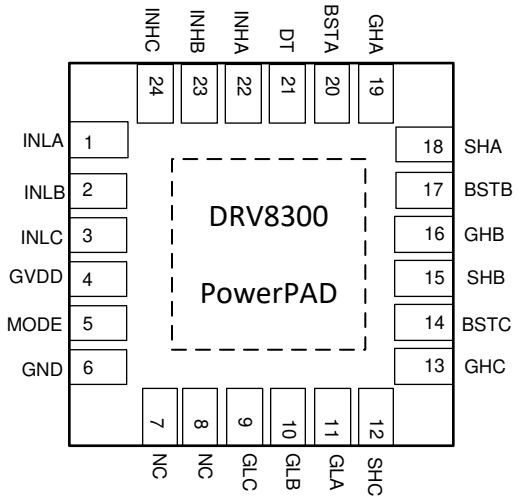


图 6-1. DRV8300UD RGE Package 24-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions—24-Pin DRV8300U Devices

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
BSTC	14	O	Bootstrap output pin. Connect capacitor between BSTC and SHC
DT	21	I	Deadtime input pin. Connect resistor to ground for variable deadtime, fixed deadtime when left it floating
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
INHA	22	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	23	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	24	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	1	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	2	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	3	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	5	I	Mode Input controls polarity of GLx compared to INLx inputs. Mode pin floating: GLx output polarity same(Non-Inverted) as INLx input Mode pin to GVDD: GLx output polarity inverted compared to INLx input
NC	7, 8	NC	No internal connection. This pin can be left floating or connected to system ground.
GND	6	PWR	Device ground.
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	4	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

(1) PWR = power, I = input, O = output, NC = no connection

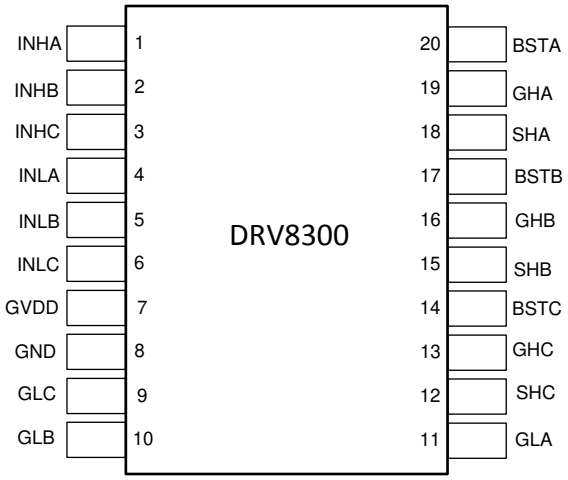


图 6-2. DRV8300UD, DRV8300UDI PW Package 20-Pin TSSOP Top View

表 6-2. Pin Functions—20-Pin DRV8300U Devices

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
BSTC	14	O	Bootstrap output pin. Connect capacitor between BSTC and SHC
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
INHA	1	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	2	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	3	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	4	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	5	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	6	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
GND	8	PWR	Device ground.
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	7	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

1. PWR = power, I = input, O = output, NC = no connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD	-0.3	21.5	V
Bootstrap pin voltage	BSTx	-0.3	125	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	21.5	V
Logic pin voltage	INHx, INLx, MODE, DT	-0.3	V_{GVDD}+0.3	V
High-side gate drive pin voltage	GHx	-22	125	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	22	V
Transient 500-ns high-side gate drive pin voltage	GHx with respect to SHx	-5	22	V
Low-side gate drive pin voltage	GLx	-0.3	V_{GVDD}+0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx	-5	V_{GVDD}+0.3	V
High-side source pin voltage	SHx	-22	110	V
Ambient temperature, T_A		– 40	125	°C
Junction temperature, T_J		– 40	150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

7.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD	8.7		20	V
V_{SHx}	High-side source pin voltage	SHx	-2		85	V
V_{SHx}	Transient 2µs high-side source pin voltage	SHx	-22		85	V
V_{BST}	Bootstrap pin voltage	BSTx	5		105	V
V_{BST}	Bootstrap pin voltage	BSTx with respect to SHx	5		20	V
V_{IN}	Logic input voltage	INHx, INLx, MODE, DT	0		GVDD	V
f_{PWM}	PWM frequency	INHx, INLx	0		200	kHz
V_{SHSL}	Slew rate on SHx pin (DRV8300UD and DRV8300UDI)				2	V/ns
C_{BOOT} (1)	Capacitor between BSTx and SHx (DRV8300UD and DRV8300UDI)				1	µF
T_A	Operating ambient temperature		– 40		125	°C
T_J	Operating junction temperature		– 40		150	°C

(1) Current flowing through boot diode (D_{BOOT}) needs to be limited for C_{BOOT} > 1µF

7.4 Thermal Information

THERMAL METRIC(1)		DRV8300U		UNIT
		PW (TSSOP)	RGE (VQFN)	
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.4	49.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	26.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.4	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

8.7 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (GVDD, BSTx)						
I_{GVDD}	GVDD standby mode current	INHx = INLX = 0; V_{BSTx} = V_{GVDD}	400	800	1400	µA
	GVDD active mode current	INHx = INLX = Switching @20kHz; V_{BSTx} = V_{GVDD}; NO FETs connected	400	825	1400	µA
IL_{BSx}	Bootstrap pin leakage current	V_{BSTx} = V_{SHx} = 85V; V_{GVDD} = 0V	2	4	7	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	INHx = Switching@20kHz	30	105	220	µA
IL_{BS_DC}	Bootstrap pin active mode leakage static current	INHx = High	30	85	150	µA
IL_{SHx}	High-side source pin leakage current	INHx = INLX = 0; V_{BSTx} - V_{SHx} = 12V; V_{SHx} = 0 to 85V	30	55	80	µA
LOGIC-LEVEL INPUTS (INHx, INLx, MODE)						
V_{IL_MODE}	Input logic low voltage	Mode pin			0.6	V
V_{IL}	Input logic low voltage	INLx, INHx pins			0.8	V
V_{IH_MODE}	Input logic high voltage	Mode pin	3.7			V
V_{IH}	Input logic high voltage	INLx, INHx pins	2.0			V
V_{HYS_MODE}	Input hysteresis	Mode pin	1600	2000	2400	mV
V_{HYS}	Input hysteresis	INLx, INHx pins	40	100	260	mV
I_{IL_INLx}	INLx Input logic low current	V_{PIN} (Pin Voltage) = 0 V; INLx in non-inverting mode	-1	0	1	µA
		V_{PIN} (Pin Voltage) = 0 V; INLx in inverting mode	5	20	30	µA
I_{IH_INLx}	INLx Input logic high current	V_{PIN} (Pin Voltage) = 5 V; INLx in non-inverting mode	5	20	30	µA
		V_{PIN} (Pin Voltage) = 5 V; INLx in inverting mode	0	0.5	1.5	µA
I_{IL}	INHx, MODE Input logic low current	V_{PIN} (Pin Voltage) = 0 V;	-1	0	1	µA
I_{IH}	INHx, MODE Input logic high current	V_{PIN} (Pin Voltage) = 5 V;	5	20	30	µA
R_{PD_INHx}	INHx Input pulldown resistance	To GND	120	200	280	kΩ
R_{PD_INLx}	INLx Input pulldown resistance	To GND, INLx in non-inverting mode	120	200	280	kΩ
R_{PU_INLx}	INLx Input pullup resistance	To INT_5V, INLx in inverting mode	120	200	280	kΩ
R_{PD_MODE}	MODE Input pulldown resistance	To GND	120	200	280	kΩ

8.7 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVERS (GHx, GLx, SHx, SLx)						
V_{GHx_LO}	High-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
V_{GLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
I_{DRIVEP_HS}	High-side peak source gate current	GHx-SHx = 12V	400	750	1200	mA
I_{DRIVEN_HS}	High-side peak sink gate current	GHx-SHx = 0V	850	1500	2100	mA
I_{DRIVEP_LS}	Low-side peak source gate current	GLx = 12V	400	750	1200	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	GLx = 0V	850	1500	2100	mA
t_{PD}	Input to output propagation delay	INHx, INLx to GHx, GLx; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	70	125	180	ns
t_{PD_match}	Matching propagation delay per phase	GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t_{PD_match}	Matching propagation delay phase to phase	GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t_{R_GLx}	GLx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{R_GHx}	GHx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{F_GLx}	GLx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{F_GHx}	GHx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{DEAD}	Gate drive dead time	DT pin floating	150	215	280	ns
		DT pin connected to GND	150	215	280	ns
		40 kΩ between DT pin and GND	150	200	260	ns
		400 kΩ between DT pin and GND	1500	2000	2600	ns
t_{PW_MIN}	Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx		40	70	150	ns
BOOTSTRAP DIODES(DRV8300UD, DRV8300UDI)						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA	0.45	0.7	0.85	V
		I_{BOOT} = 100 mA	2	2.3	3.1	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 80 mA	11	15	25	Ω
PROTECTION CIRCUITS						
V_{GVDDUV}	Gate Driver Supply undervoltage lockout (GVDDUV)	Supply rising	8	8.3	8.6	V
		Supply falling	7.8	8	8.25	V
V_{GVDDUV_HYS}	Gate Driver Supply UV hysteresis	Rising to falling threshold	295	330	360	mV
t_{GVDDUV}	Gate Driver Supply undervoltage deglitch time		5	10	13	µs

8.7 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BSTUV}	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply rising	7.5	8	8.7	V
	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply falling	6.9	7.6	8.4	V
V_{BSTUV_HYS}	Bootstrap UV hysteresis	Rising to falling threshold	250	400	850	mV
t_{BSTUV}	Bootstrap undervoltage deglitch time		5.5	10	22	µs

7.6 Timing Diagrams

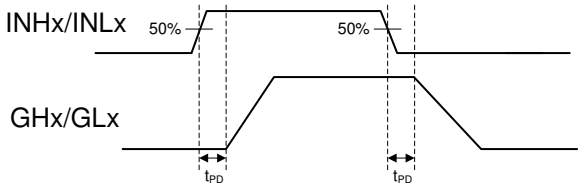


图 7-1. Propagation Delay(t_{PD})

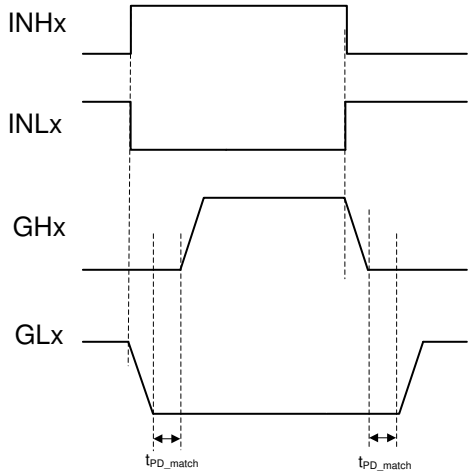


图 7-2. Propagation Delay Match (t_{PD_match})

7.7 Typical Characteristics

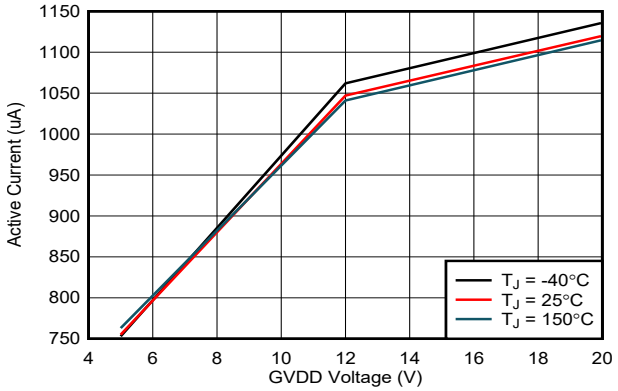


图 7-3. Supply Current Over GVDD Voltage

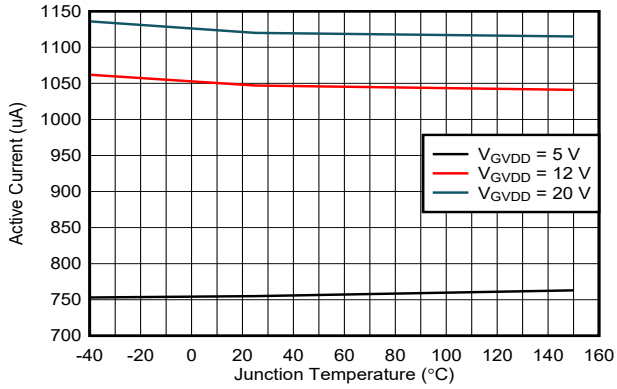


图 7-4. Supply Current Over Temperature

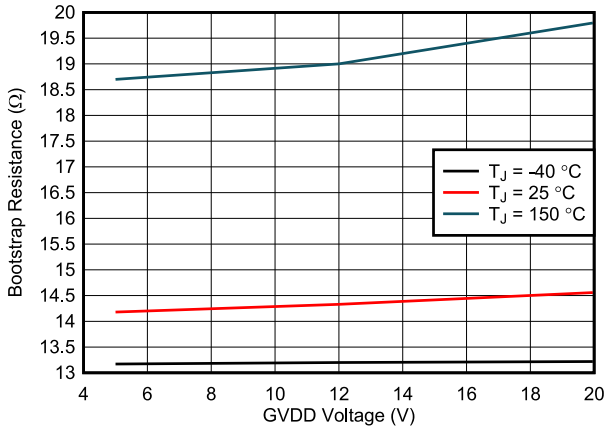


图 7-5. Bootstrap Resistance Over GVDD Voltage

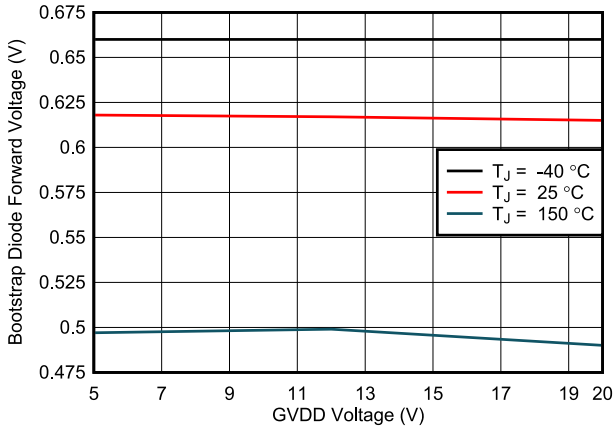


图 7-6. Bootstrap Diode Forward Voltage over GVDD Voltage

8 Detailed Description

8.1 Overview

The DRV8300U family of devices is a gate driver for three-phase motor drive applications. These devices decrease system component count, saves PCB space and cost by integrating three independent half-bridge gate drivers and optional bootstrap diodes.

DRV8300U supports external N-channel high-side and low-side power MOSFETs and can drive 750-mA source, 1.5-A sink peak currents with total combined 30-mA average output current. The DRV8300U family of devices are available in 0.5-mm pitch QFN and 0.65-mm pitch TSSOP surface-mount packages. The QFN size is 4 × 4 mm (0.5-mm pin pitch) for the 24-pin package, and TSSOP body size is 6.5 × 4.4 mm (0.65-mm pin pitch) for the 20-pin package.

8.2 Functional Block Diagram

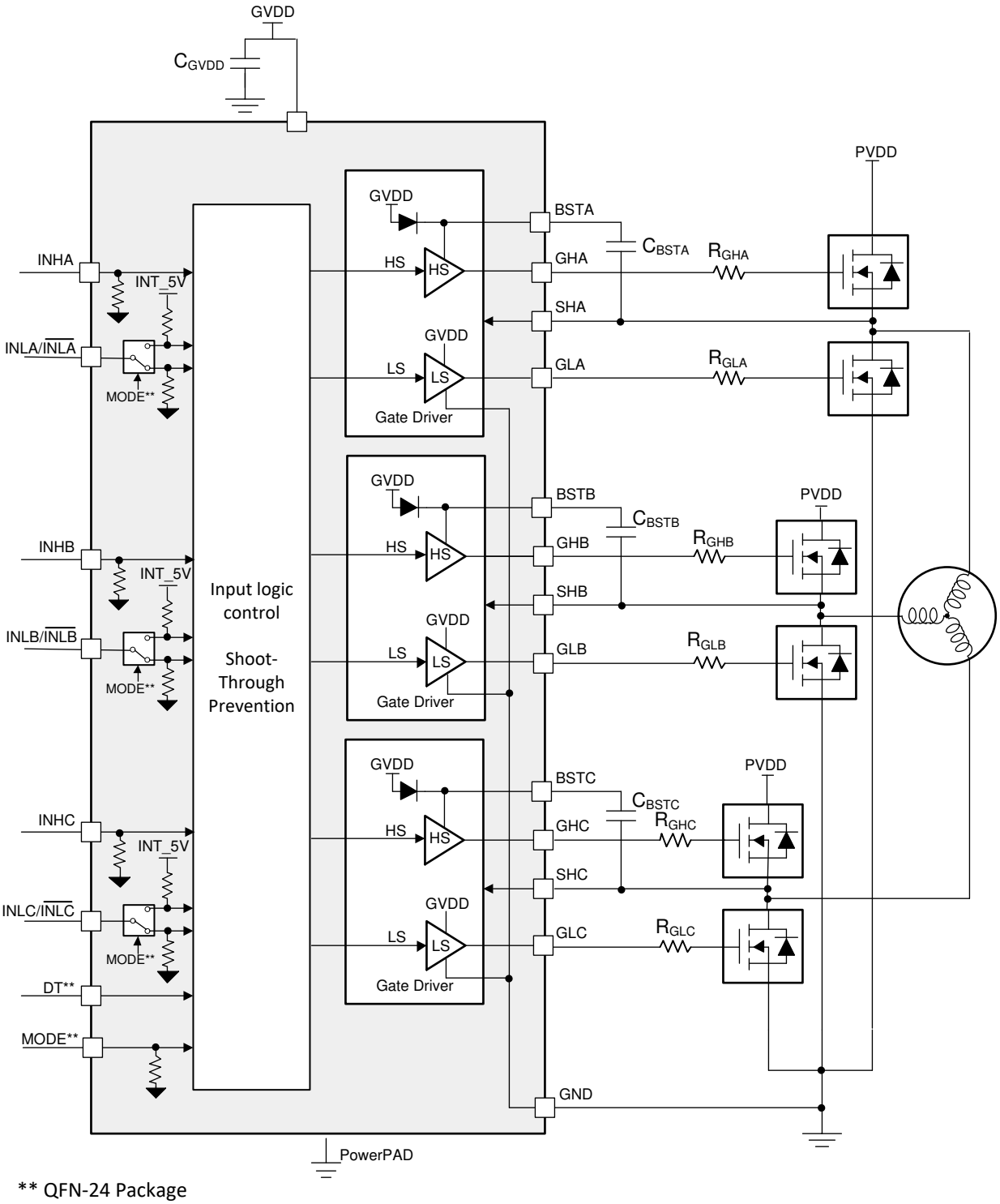


图 8-1. Block Diagram for DRV8300UD

8.3 Feature Description

8.3.1 Three BLDC Gate Drivers

The DRV8300U integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Input on GVDD provides the gate bias voltage for the low-side MOSFETs. The high voltage is generated using bootstrap capacitor and GVDD supply. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

8.3.1.1 Gate Drive Timings

8.3.1.1.1 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the input deglitcher delay and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. The analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

8.3.1.1.2 Deadtime and Cross-Conduction Prevention

In the DRV8300U, high-side and low-side inputs operate independently, with an exception to prevent cross conduction when high and low side are turned ON at same time. The DRV8300U turns OFF high-side and low-side output to prevent shoot through when the both high-side and low-side inputs are at logic HIGH at same time.

The DRV8300U also provides option to insert additional deadtime to prevent the external high-side and low-side MOSFET from switching on at the same time. In the devices with DT pin (QFN package), deadtime can be linearly adjusted between 200 ns to 2000 ns by configuring resistor value between DT and GND. When the DT pin is left floating, fixed deadtime of 200 nS (typical value) is inserted. The value of resistor can be calculated using 方程式 1.

$$R_{DT}\,(k\Omega) = \frac{Deadtime\ (nS)}{5} \tag{1}$$

In the devices without DT pin (TSSOP package), fixed deadtime of 200 ns (typical value) is inserted to prevent high and low side gate output turning ON at same time.

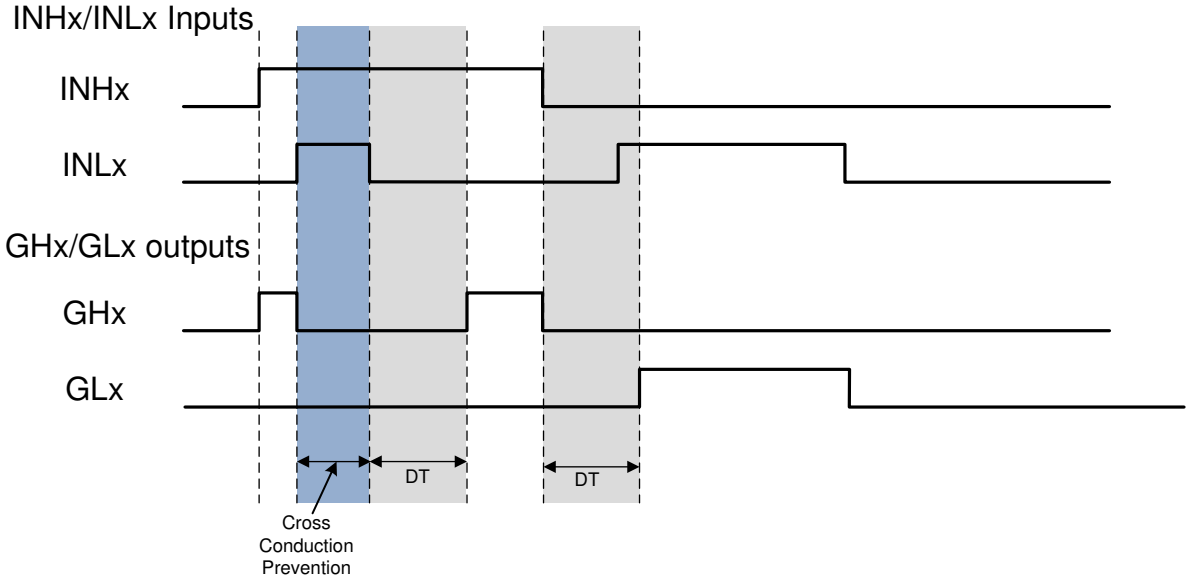


图 8-2. Cross Conduction Prevention and Deadtime Insertion

8.3.1.2 Mode (Inverting and non inverting INLx)

The DRV8300U has flexibility of accepting different kind of inputs on INLx. In the devices with MODE pin (QFN package), the DRV8300U provides option of configuring the GLx outputs to be inverted or non-inverted compared to polarity of signal on INLx pins. When the MODE pin is left floating, the INLx is configured to be in non-inverting mode and GLx output is in phase with respect to INLx (see 图 8-3), whereas when the MODE pin is connected to GVDD, GLx output is out of phase with respect to INLx (see 图 8-4). In devices without MODE pin (TSSOP package device), there are different device option available for inverting and non inverting inputs (see 节 5).

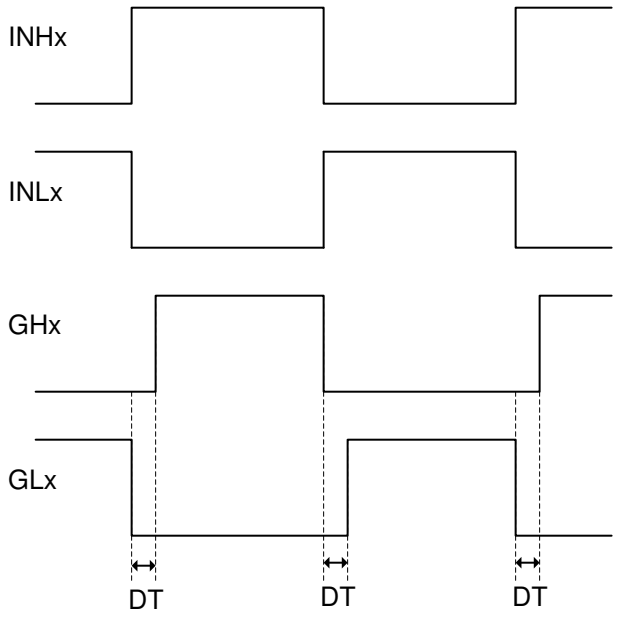


图 8-3. Non-Inverted INLx inputs

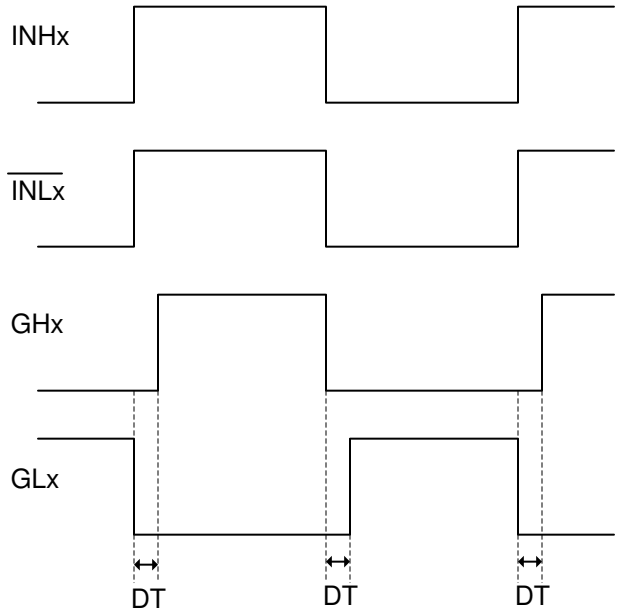


图 8-4. Inverted INLx inputs

8.3.2 Pin Diagrams

图 8-5 shows the input structure for the logic level pins INHx, INLx. INHx and non-inverted INLx has passive pull down, so when inputs are floating the output the gate driver will be pulled low. 图 8-6 shows the input structure for the inverted INLx pins. The inverted INLx has passive pull up, so when inputs are floating the output of the low-side gate driver will be pulled low.

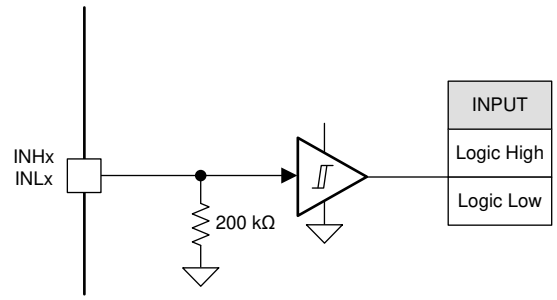


图 8-5. INHx and non-inverted INLx Logic-Level Input Pin Structure

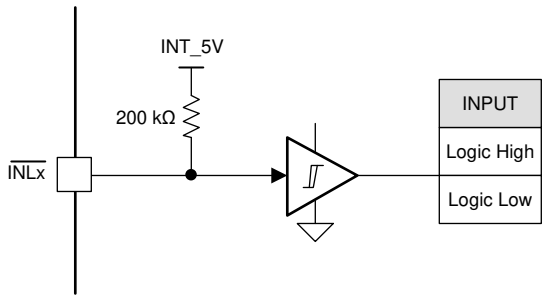


图 8-6. Inverted INLx Logic-Level Input Pin Structure

8.3.3 Gate Driver Protective Circuits

The DRV8300U is protected against BSTx undervoltage and GVDD undervoltage events.

表 8-1. Fault Action and Response

FAULT	CONDITION	GATE DRIVER	RECOVERY
V_{BSTx} undervoltage (BSTUV)	$V_{BSTx} < V_{BSTUV}$	GHx - Hi-Z	Automatic: $V_{BSTx} > V_{BSTUV}$ and low to high PWM edge detected on INHx pin
GVDD undervoltage (GVDDUV)	$V_{GVDD} < V_{GVDDUV}$	Hi-Z	Automatic: $V_{GVDD} > V_{GVDDUV}$

8.3.3.1 V_{BSTx} Undervoltage Lockout (BSTUV)

The DRV8300U has separate voltage comparator to detect undervoltage condition for each phases. If at any time the voltage on the BSTx pin falls lower than the V_{BSTUV} threshold, high side external MOSFETs of that particular phase is disabled by disabling (Hi-Z) GHx pin. Normal operation starts again when the BSTUV condition clears and low to high PWM edge is detected on INHx input of the same phase that BSTUV condition was detected. BSTUV protection ensures that high-side MOSFETs are not driven when the BSTx pins has lower value.

8.3.3.2 GVDD Undervoltage Lockout (GVDDUV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDDUV} threshold voltage, all of the external MOSFETs are disabled. Normal operation starts again when the GVDDUV condition clears. GVDDUV protection ensures that external MOSFETs are not driven when the GVDD input is at lower value.

8.4 Device Functional Modes

The DRV8300U is in operating (active) mode, whenever the GVDD and BST pins are higher than the UV threshold (GVDD > $V_{GVDDUV}$and V_{BSTX} > V_{BSTUV}). In active mode, the gate driver output GHx and GLX will follow respective inputs INHx and INLx.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8300U family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the 节 9.2 section highlight how to use and configure the DRV8300U.

9.2 Typical Application

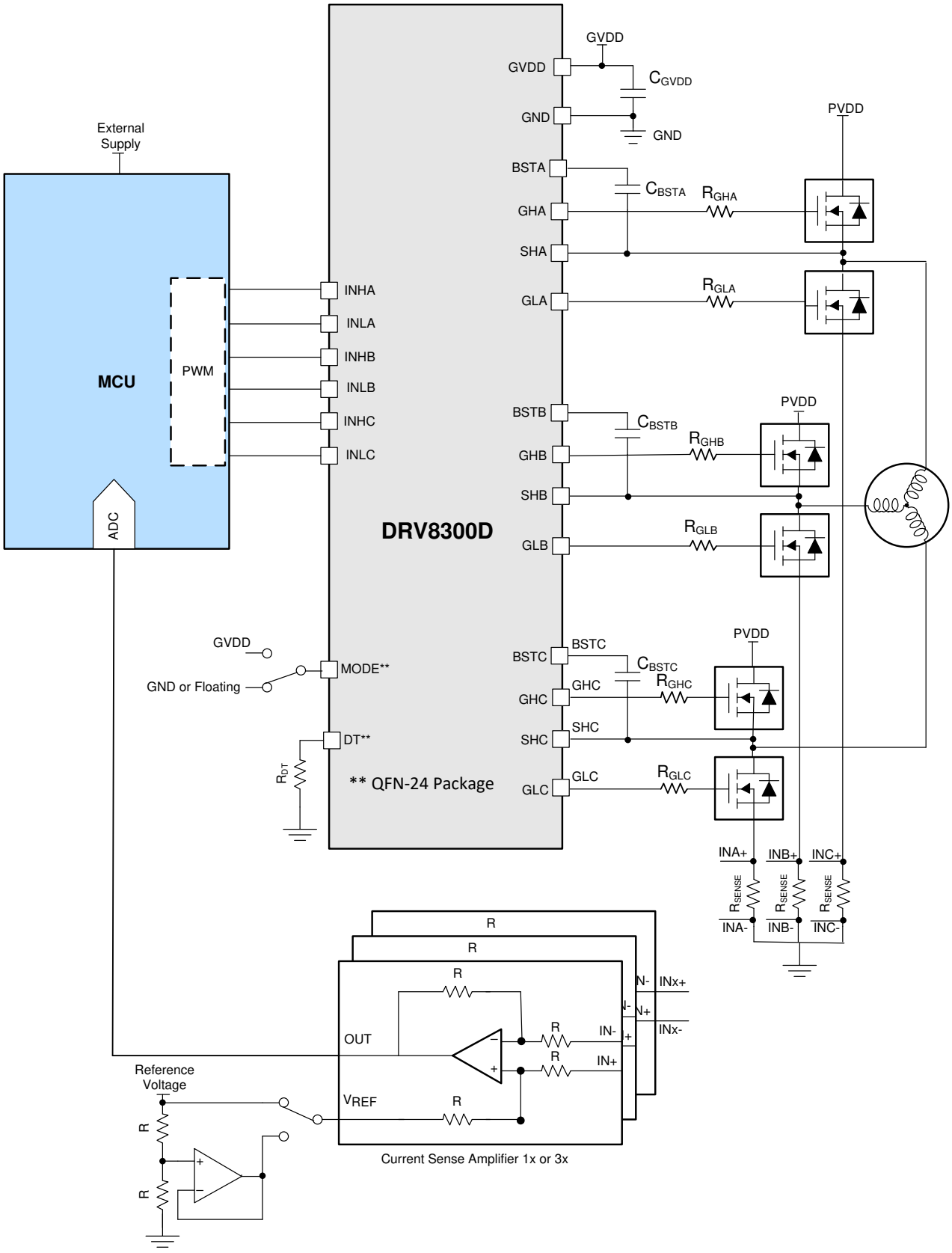


图 9-1. Application Schematic

9.2.1 Design Requirements

表 9-1 lists the example design input parameters for system design.

表 9-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
MOSFET	-	CSD19532Q5B
Gate Supply Voltage	V_{GVDD}	12 V
Gate Charge	Q_G	48 nC

9.2.2 Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. 方程式 2 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \quad (2)$$

=12 V – 0.85 V – 4.5 V = 6.65 V

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.65 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with 方程式 3:

$$Q_{TOT} = Q_G + \frac{IL_{BS\_TRANS}}{f_{SW}} \quad (3)$$

=48 nC + 220 μA/20 kHz = 50 nC + 11 nC = 59 nC

where

- Q_G is the total MOSFET gate charge
- I_{LBS_TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor an then be estimated as below assuming 1V ΔV_{BSTx}:

$$C_{BST\_MIN} = {Q_{TOT}}/{\Delta V_{BSTX}} \quad (4)$$

= 59 nC / 1 V = 59 nF

The calculated value of minimum bootstrap capacitor is 59 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \quad (5)$$

= 10*100 nF= 1 μF

For this example application choose 1 µF C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

9.2.3 Application Curves

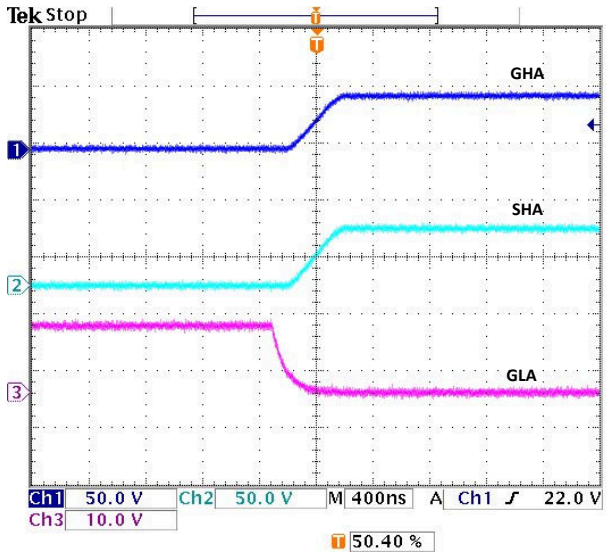


图 9-2. Gate voltages, SHx rising with 15 ohm gate resistor and CSD19532Q5B MOSFET

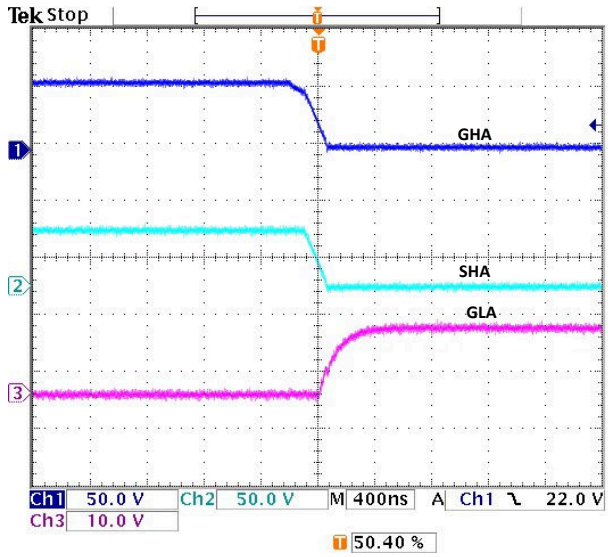


图 9-3. Gate voltages, SHx falling with 15 ohm gate resistor and CSD19532Q5B MOSFET

10 Power Supply Recommendations

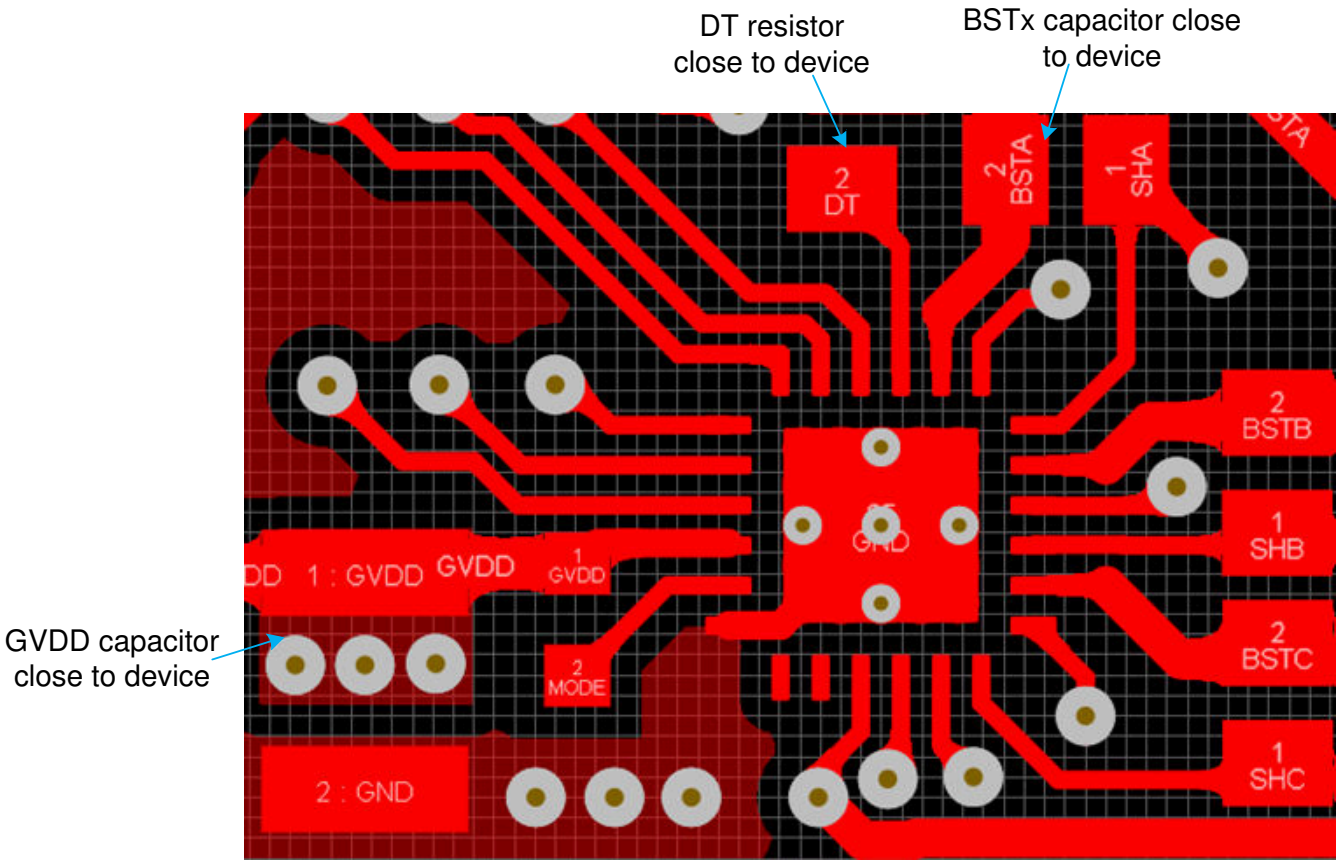
The DRV8300U is designed to operate from an input voltage supply (GVDD) range from 4.8 V to 20 V. A local bypass capacitor should be placed between the GVDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and GND pin, and another high capacitance value surfacemount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the GHx pins are sourced from the BSTx pins. Therefore, capacitor across the BSTx to SHx is recommended, it should be high enough capacitance value capacitor to deliver GHx pulses

11 Layout

11.1 Layout Guidelines

- Low ESR/ESL capacitors must be connected close to the device between GVDD and GND and between BSTx and SHx pins to support high peak currents drawn from GVDD and BSTx pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground.
- In order to avoid large negative transients on the switch node (SHx) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET must be minimized.
- In order to avoid unexpected transients, the parasitic inductance of the GHx, SHx, and GLx connections must be minimized. Minimize the trace length and number of vias wherever possible. Minimum 10 mil and typical 15 mil trace width is recommended.
- Resistance between DT and GND must be place as close as possible to device
- Place the gate driver as close to the MOSFETs as possible. Confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area by reducing trace length. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs.
- In QFN package device variants, NC pins can be connected to GND to increase ground conenction between thermal pad and external ground plane.
- Refer to sections *General Routing Techniques and MOSFET Placement and Power Stage Routing* in Application Report

11.2 Layout Example



12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8300UDIPWR	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8300UDI
DRV8300UDIPWR.A	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8300UDI
DRV8300UDPWR	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8300UD
DRV8300UDPWR.A	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8300UD
DRV8300UDRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8300UD
DRV8300UDRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	8300UD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

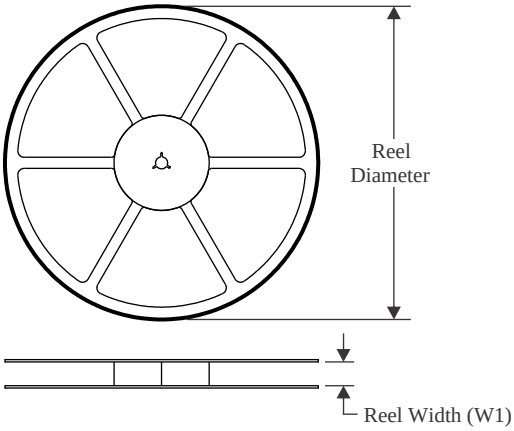
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

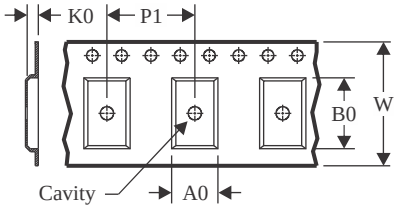
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

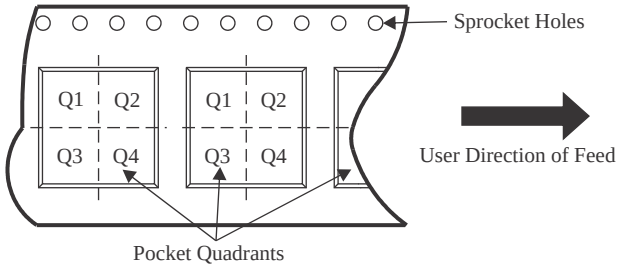


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

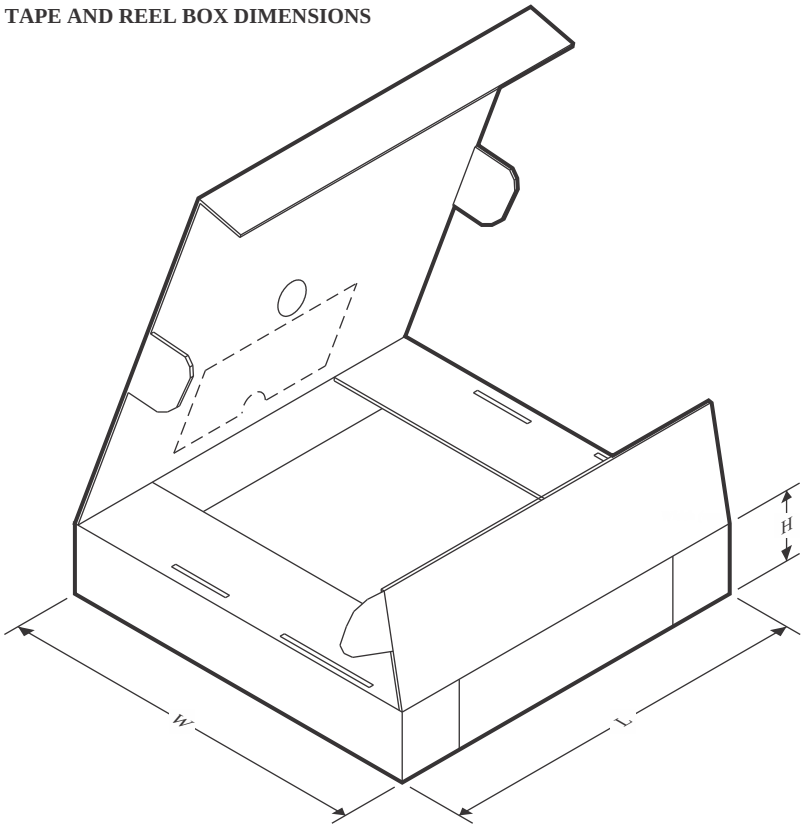
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8300UDIPWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
DRV8300UDPWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
DRV8300UDRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

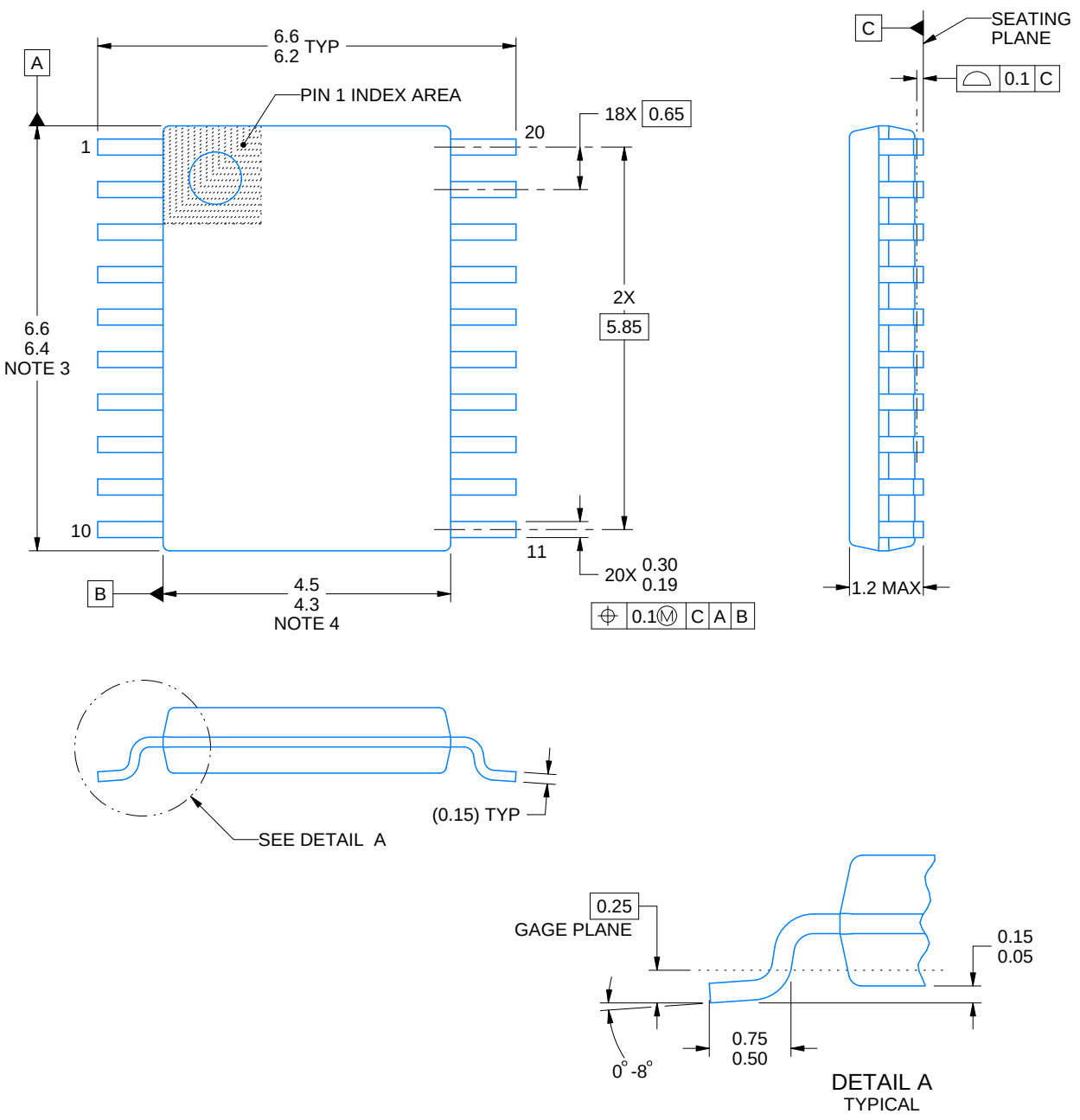
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8300UDIPWR	TSSOP	PW	20	3000	353.0	353.0	32.0
DRV8300UDPWR	TSSOP	PW	20	3000	353.0	353.0	32.0
DRV8300UDRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0020A

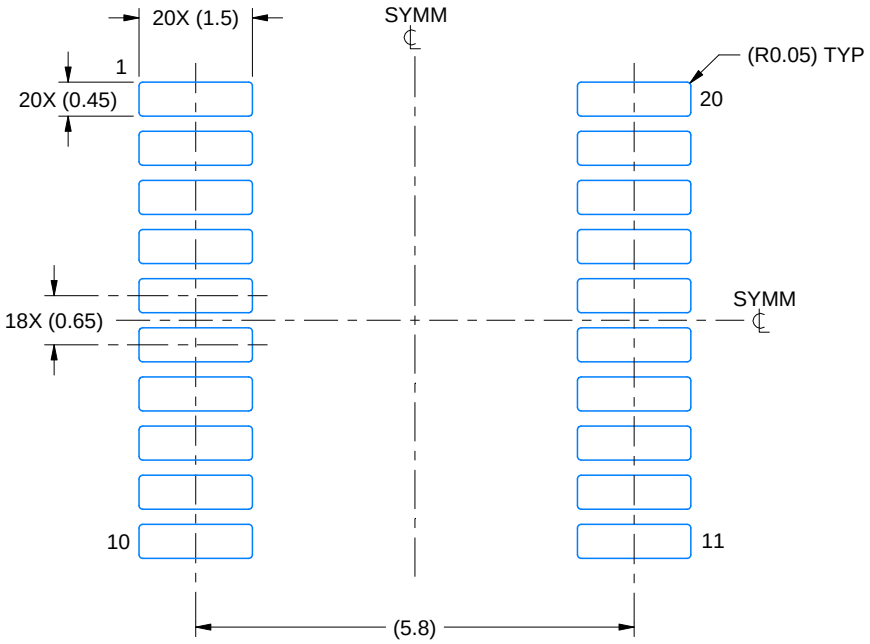
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



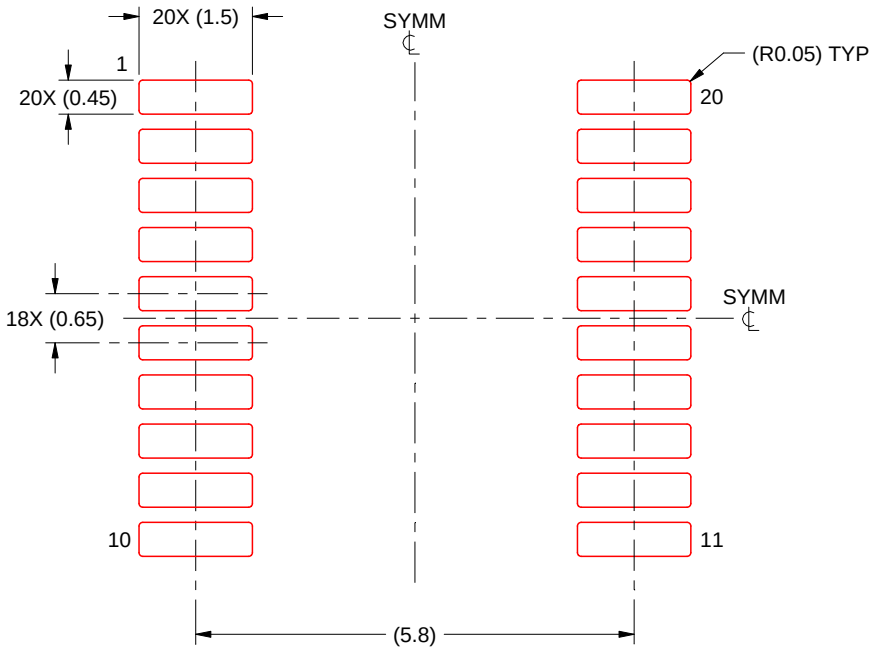
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

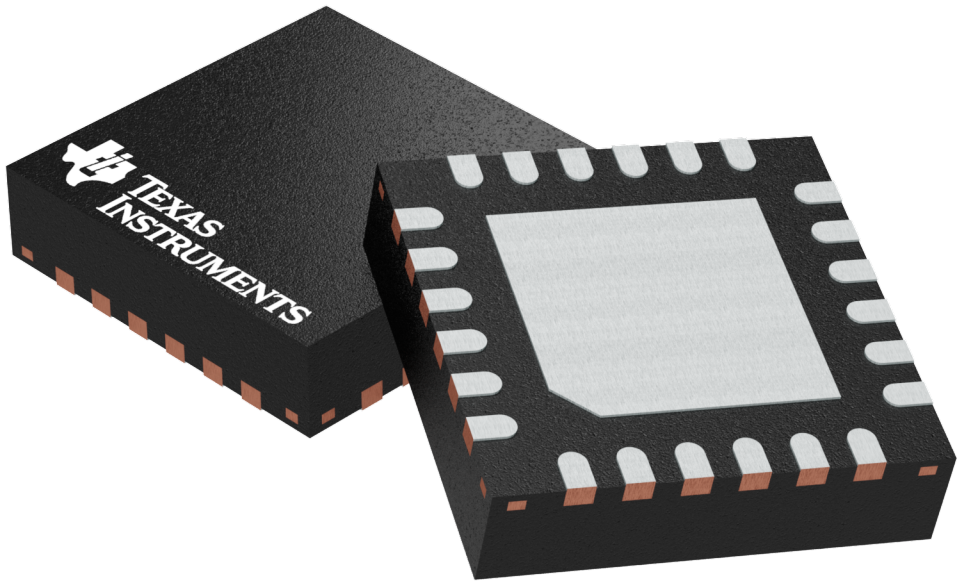
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

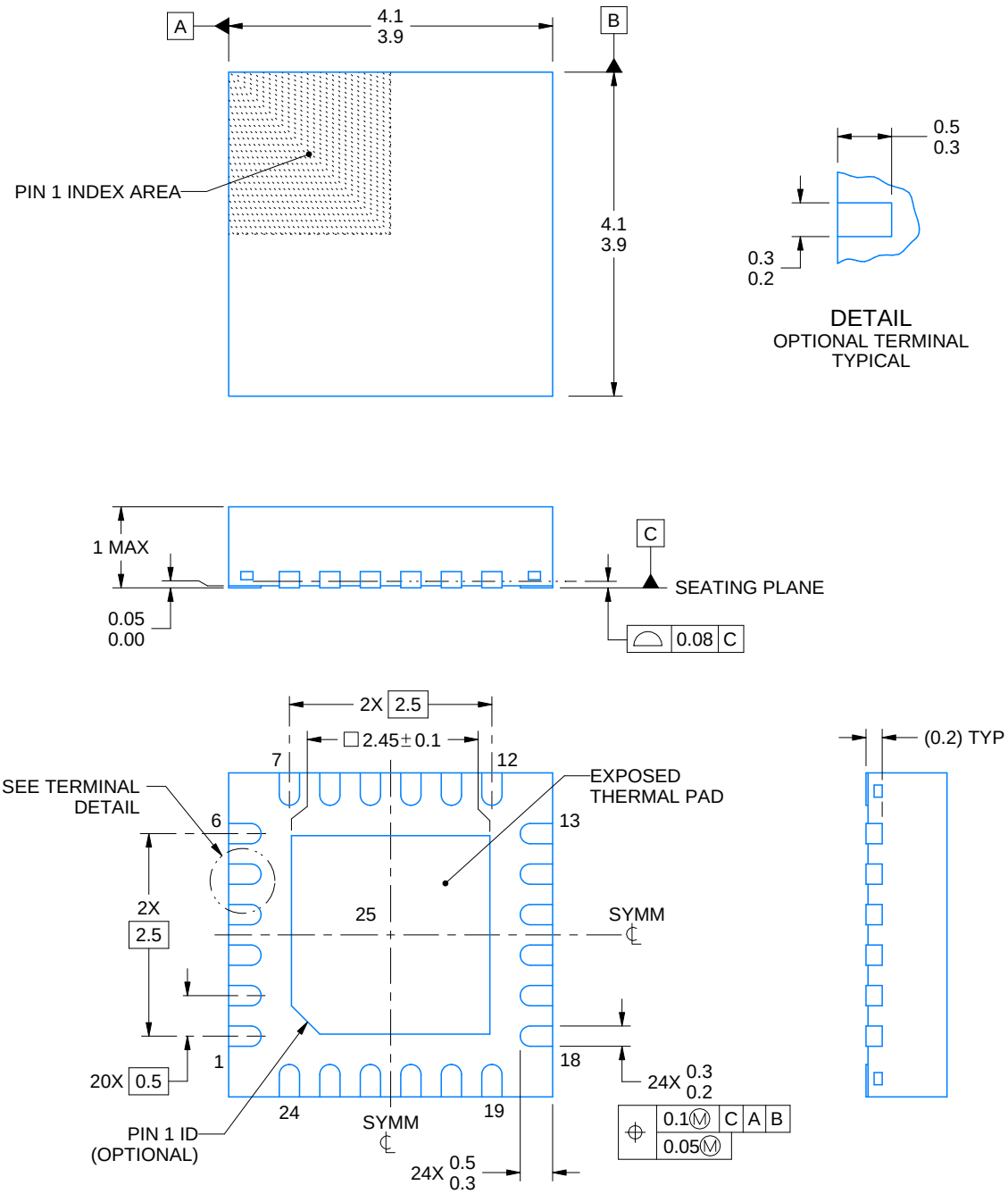
4204104/H

PACKAGE OUTLINE

RGE0024B

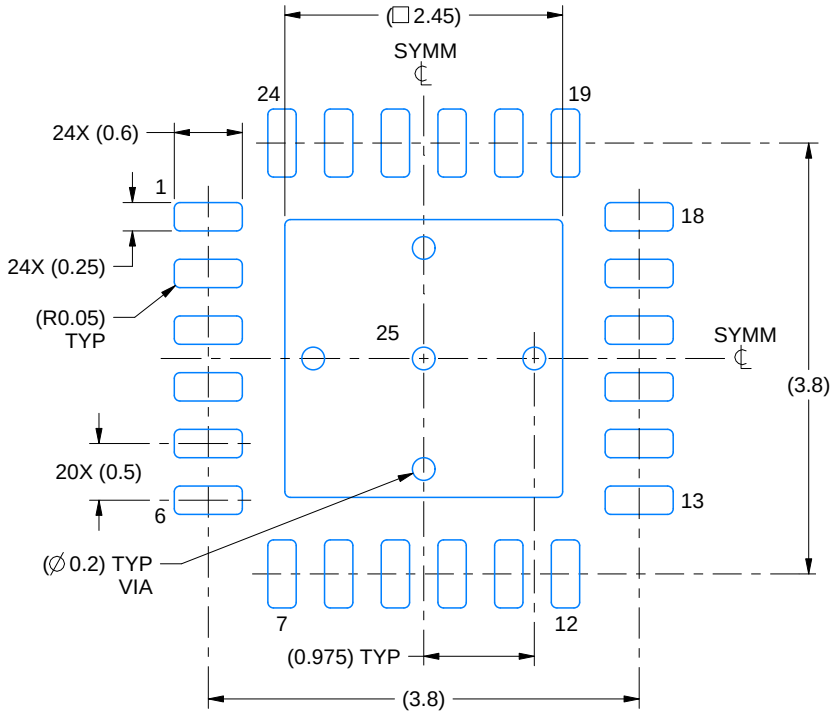
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

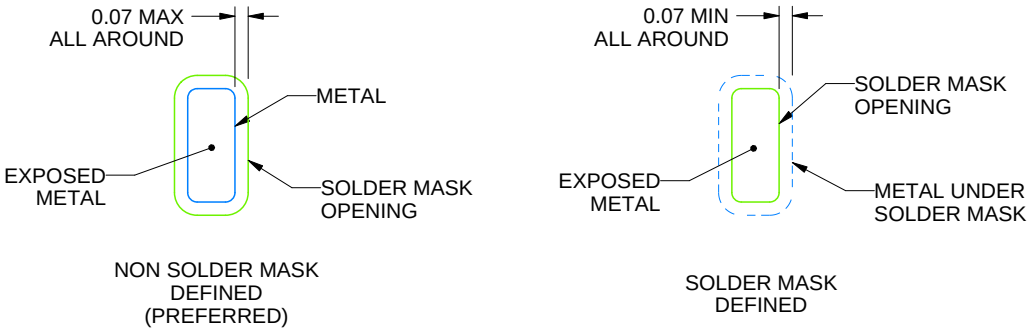


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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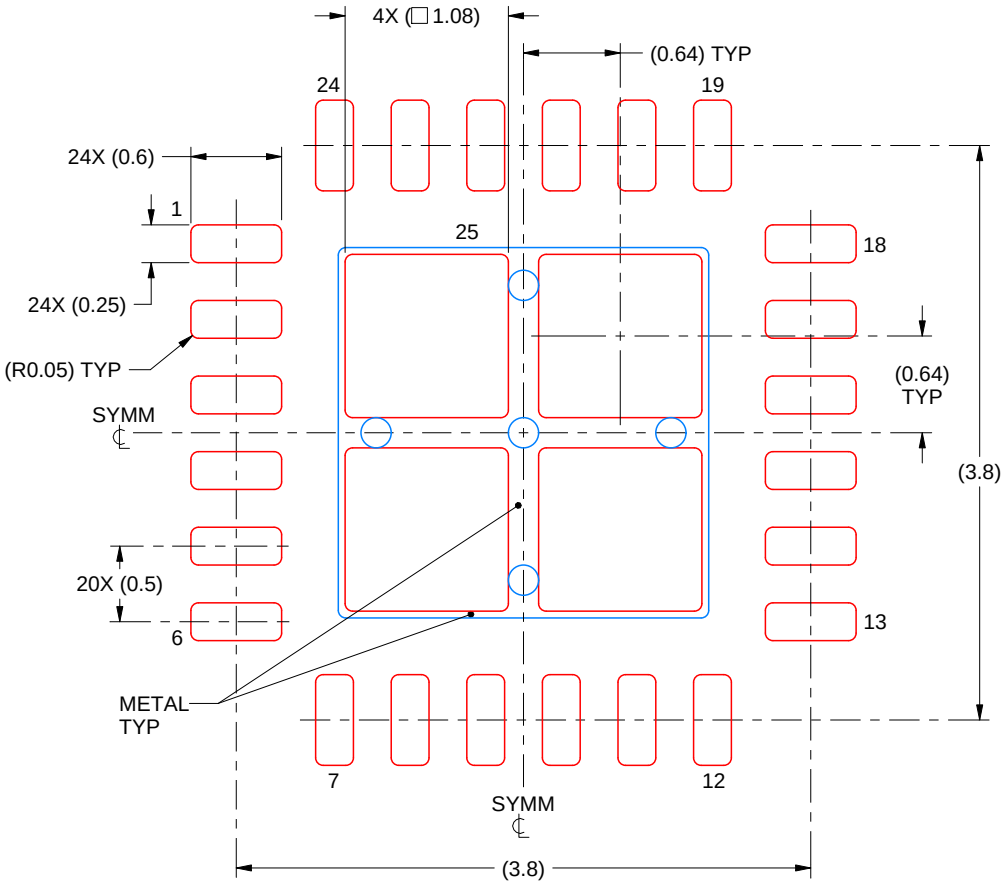
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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