适用于闭环磁电流传感器的 DRV401-Q1 传感器信号调节器件

1 特性

- 汽车电子 应用认证
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 1C
  - 器件带电器件模型 (CDM) ESD 分类等级 C6
- 单电源：5V
- 电源输出：H 桥
- 专为驱动电感负载而设计
- 出色的直流精度
- 宽系统带宽
- 高分辨率、低温漂移
- 内置去磁系统
- 丰富的故障检测功能
- 外部高功率驱动器选项
- 紧凑型封装

2 应用

- 汽车
- 汽车中的电机控制 应用
- 磁通门电流感应
- 发电机和交流发电机监测和控制
- 频率和电压逆变器
- 电机驱动控制器
- 系统功耗
- 光伏系统

3 说明

DRV401-Q1 器件完全符合汽车 应用要求 并适用于电机控制驱动和电池监测系统。

与磁传感器搭配使用时，DRV401-Q1 能够以高精确度监测交流和直流电流。

可提供的功能包括：探头激励、探头信号的信号调节、信号环路放大器、补偿线圈的 H 桥驱动器和提供与初级电流成正比的输出电压的模拟信号输出级。它具有过载和故障检测功能，以及瞬态噪声抑制功能。

DRV401-Q1 器件可直接驱动补偿线圈或与外部电源驱动器连接。因此，DRV401-Q1 与传感器相结合，可用于测量各种大小的电流。

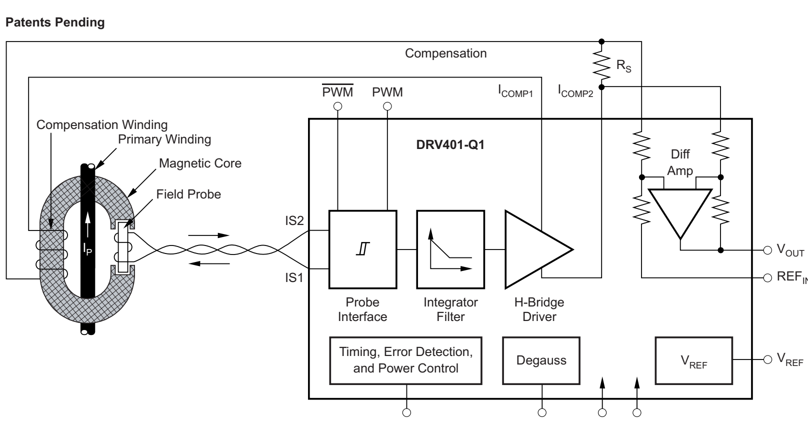
为维持最高精度，DRV401-Q1 可在加电时根据需要对传感器进行去磁。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV401-Q1	VQFN-20	5.00mm × 5.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

闭环磁感应



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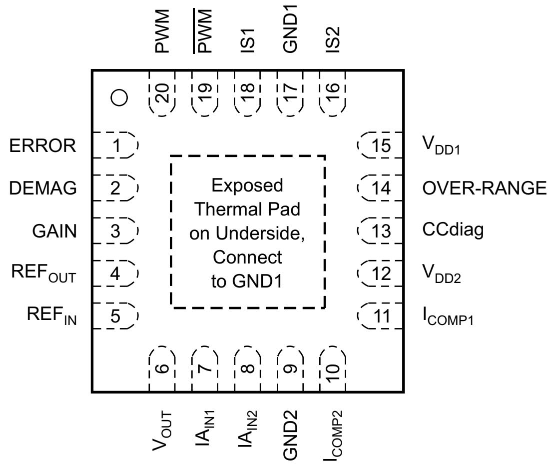
4 修订历史记录

日期	修订版本	注释
2016 年 12 月	*	首次发布。

5 Pin Configuration and Functions

RGW Package
20-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CCdiag	13	I	Control input for wire-break detection: high = enable
DEMAG	2	I	Control input; See the *Demagnetization* section.
ERROR	1	O	Error flag: open-drain output. See the *Error Conditions* section.
GAIN	3	I	Control input for open-loop gain: low = normal, high = −8 dB
GND1	17	—	Ground connection
GND2	9	—	Ground connection. Connect to GND1.
IA_{IN1}	8	I	Inverting input of differential amplifier
IA_{IN2}	7	I	Noninverting input of differential amplifier
I_{COMP1}	11	O	Output 1 of compensation coil driver
I_{COMP2}	10	O	Output 2 of compensation coil driver
IS1	18	I/O	Probe connection 1
IS2	16	I/O	Probe connection 2
OVER-RANGE	14	O	Open-drain output for overrange indication: low = overrange
$\overline{PWM}$	19	O	PWM output from probe circuit (inverted)
PWM	20	O	PWM output from probe circuit
REF_{OUT}	4	O	Output for internal 2.5-V reference voltage
REF_{IN}	5	I	Input for zero reference to differential amplifier
Thermal pad	—	—	Exposed thermal pad. Connect to GND1.
V_{DD1}	15	—	Supply voltage
V_{DD2}	12	—	Supply voltage. Connect to V_{DD1}.
V_{OUT}	6	O	Output for differential amplifier

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		7	V
	Signal input pin	−0.5	V_{DD} + 0.5	
Differential amplifier	Signal input pin	–10	10	
Current	Signal input pin, IS1 and IS2	–75	75	mA
	Pins other than IS1 and IS2	–25	25	
	I_{COMP} short circuit	0	250	
Temperature	Operating, T_A	–50	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	Pins IA_{IN1} and IA_{IN2}	±1000	V
			All other pins	±5000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Power supply voltage, V_{DD1}, V_{DD2}	4.5	5	5.5	V
Specified temperature range	–40	25	+125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		DRV401-Q1	UNIT
		RGW (VQFN)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIFFERENTIAL AMPLIFIER						
V_{OS}	Offset voltage, RTO[1][2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V Gain = 4 V/V		±0.01	±0.1	mV
dV_{OS}/dT	Offset voltage drift, RTO[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V T_A = –40°C to 125°C I_{COMP} = 0 mA		±0.1	±1	µV/°C
CMRR	Offset voltage vs common-mode, RTO	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V −1 V to 6 V, V_{REF} = 2.5 V		±50	±250	µV/V
PSRR	Offset voltage vs power supply, RTO	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V V_{REF} not included		±4	±50	µV/V
SIGNAL INPUT						
	Common-mode voltage range	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	–1		(V_{DD}) + 1	V
SIGNAL OUTPUT						
	Signal overrange indication (OVER-RANGE), delay[2]	R_L = 10 kΩ to 2.5 V, V_{REFIN} = 2.5 V, T_A = –40°C to 125°C, I_{COMP} = 0 mA, V_{IN} = 1-V step. See [2]		2.5 to 3.5		µs
	Voltage output swing from negative rail[2], OVER-RANGE trip level	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V I = 2.5 mA, CMP trip level		48	85	mV
	Voltage output swing from positive rail[2], OVER-RANGE trip level	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V I = −2.5 mA, CMP trip level	V_{DD} – 85	V_{DD} – 48		mV
I_{SC}	Short-circuit current[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V V_{OUT} connected to GND		–18		mA
		R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V V_{OUT} connected to V_{DD}		20		mA
	Gain, V_{OUT}/V_{IN_DIFF}	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V T_A = –40°C to 125°C		4		V/V
	Gain error	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V		±0.02%	±0.3%	
	Gain error drift	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V T_A = –40°C to 125°C I_{COMP} = 0 mA		±0.1		ppm/°C
	Linearity error	V_{REFIN} = 2.5 V R_L = 1 kΩ		10		ppm
FREQUENCY RESPONSE						
$BW_{–3\ dB}$	Bandwidth[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V		2		MHz
SR	Slew rate[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V CMVR = −1 V to 4 V		6.5		V/µs

(1) Parameter value referred-to-output (RTO).
(2) θ_{JP} = 结至焊盘热阻

Electrical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_S	Settling time, large-signal[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V dV ±2 V to 1%, no external filter		0.9		µs
	Settling time[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V dV ±0.4 V to 0.01%		14		µs
INPUT RESISTANCE						
	Differential	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	16.5	20	23.5	kΩ
	Common-mode	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	41	50	59	kΩ
	External reference input	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V	41	50	59	kΩ
NOISE						
e_n	Output voltage noise density, RTO[2]	R_L = 10 kΩ to 2.5 V V_{REFIN} = 2.5 V f = 1 kHz, compensation loop disabled		170		$nV/\sqrt{Hz}$
COMPENSATION LOOP						
DC STABILITY						
	Offset error [3]	Probe f = 250 kHz, R_{LOAD} = 20 Ω, deviation from 50% PWM, pin gain = L		0.03%		
	Offset error drift [2]	Probe f = 250 kHz, R_{LOAD} = 20 Ω, deviation from 50% PWM, pin gain = L, T_A = –40°C to 125°C		7.5		ppm/°C
	Gain [2]	Probe f = 250 kHz, R_{LOAD} = 20 Ω, pin gain = L, $\lvert V_{ICOMP1}\rvert - \lvert V_{ICOMP2}\rvert$	–200	25	200	ppm/V
PSRR	Power-supply rejection ratio	Probe f = 250 kHz, R_{LOAD} = 20 Ω		500		ppm/V
FREQUENCY RESPONSE						
	Open-loop gain	Probe f = 250 kHz, R_{LOAD} = 20 Ω, two modes, 7.8 kHz		24/32		dB
PROBE COIL LOOP						
	Input voltage clamp range	Field probe current < 50 mA	–0.7 to V_{DD} + 0.7	V		
R_{HIGH}	Internal resistor, IS1 or IS2 to V_{DD1} [2]		47	59	71	Ω
R_{LOW}	Internal resistor, IS1 or IS2 to GND1 [2]		60	75	90	Ω
	Resistance mismatch between IS1 and IS2 [2]	ppm of R_{HIGH} + R_{LOW}		300	1500	ppm
	Total input resistance	T_A = –40°C to 125°C I_{COMP} = 0 mA		134	200	Ω
	Comparator threshold current		22	28	34	mA
	Minimum probe loop half-cycle [2]		250	280	310	ns
	Probe loop minimum frequency		250			kHz
	No oscillation detect (error) suppression			35		µs
COMPENSATION COIL DRIVER, H-BRIDGE						
	Peak current [2]	V_{ICOMP1} – V_{ICOMP2} = 4 V_{PP} T_A = –40°C to 125°C I_{COMP} = 0 mA		250		mA
	Voltage swing	20-Ω load	4.2			V_{PP}

(3) For VAC sensors, 0.2% of PWM offset approximately corresponds to 10-mA primary current per offset per winding.

Electrical Characteristics (continued)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCM}	Output common-mode voltage			V_{DD2} / 2		V
	Wire break detect, threshold current (4)			33	57	mA
VOLTAGE REFERENCE						
	Voltage (2)	No load	2.495	2.5	2.505	V
	Voltage drift (2)	No load, T_A = – 40°C to 125°C I_{COMP} = 0 mA		±5	±50	ppm/°C
PSRR	Power-supply rejection ratio (2)			±15	±200	µV/V
	Load regulation (2)	Load to GND and V_{DD} dI = 0 mA to 5 mA		0.15		mV/mA
I_{SC}	Short-circuit current	REF_{OUT} connected to V_{DD}		20		mA
		REF_{OUT} connected to GND		–18		mA
DEMAGNETIZATION						
	Duration	At T_A = –40°C to 125°C I_{COMP} = 0 mA; see the *Demagnetization* section		106	130	ms
DIGITAL I/O						
LOGIC INPUTS (DEMAG, GAIN, and CCdiag PINS)						
	Pull-up high current (CCdiag)	CMOS-type levels, 3.5 < V_{IN} < V_{DD}		160		µA
	Pull-up low current (CCdiag)	CMOS-type levels, 0 < V_{IN} < 1.5		5		µA
	Logic input leakage current	CMOS-type levels, 0 < V_{IN} < V_{DD}		0.01		µA
	Logic level, input: L/H	CMOS-type levels		2.1/2.8		
	Hysteresis	CMOS-type levels		0.7		
OUTPUTS (ERROR AND OVER-RANGE PINS)						
	Logic level, output: L	4-mA sink		0.3		V
	Logic level, input: H			No internal pull-up		
OUTPUTS (PWM AND $\overline{PWM}$ PINS)						
	Logic level L	Push-pull type, 4-mA sink		0.2		V
	Logic level H	Push-pull type, 4-mA source		V_{DD} – 0.4		V
POWER SUPPLY						
V_{DD}	Specified voltage range	T_A = –40°C to 125°C I_{COMP} = 0 mA	4.5	5	5.5	V
V_{RST}	Power-on reset threshold			1.8		V
I_Q	Quiescent current [I(V_{DD1}) + I(V_{DD2})]	I_{COMP} = 0 mA, sensor not connected			6.8	mA
	Brownout voltage level			4		V
	Brownout indication delay			135		µs
TEMPERATURE RANGE						
T_J	Specified range		–40		125	°C
T_J	Operating range		–50		150	°C

(4) See the *Compensation Driver* subsection in the *Detailed Description* section.

6.6 Typical Characteristics

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

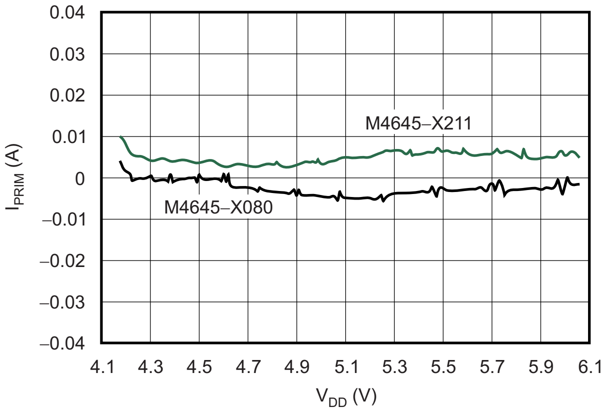
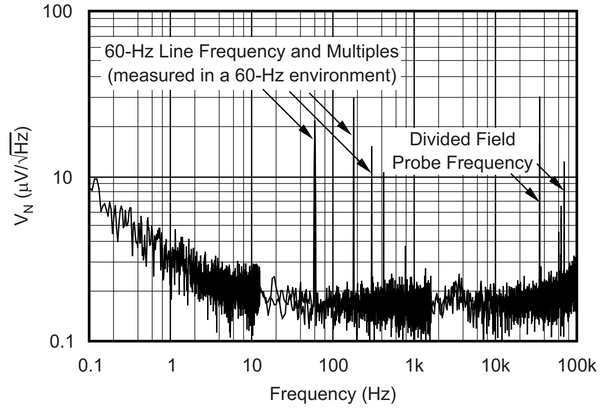


图 1. DRV401-Q1 Device and Sensor: Offset vs Supply Voltage



Sensor M4645−X080, R_{SHUNT} = 10 Ω, Mode = Low

图 2. DRV401-Q1 Device and Sensor: Output Voltage Noise Density

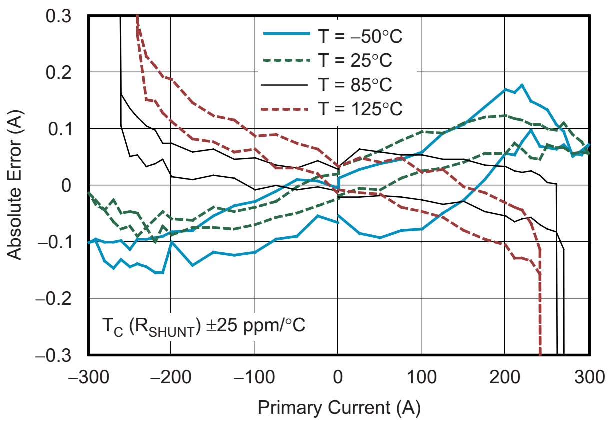
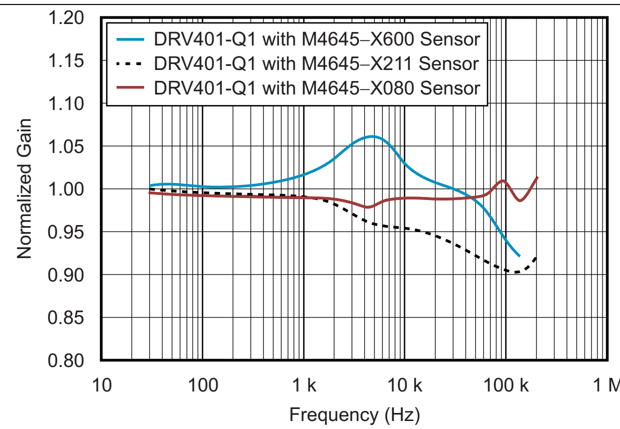
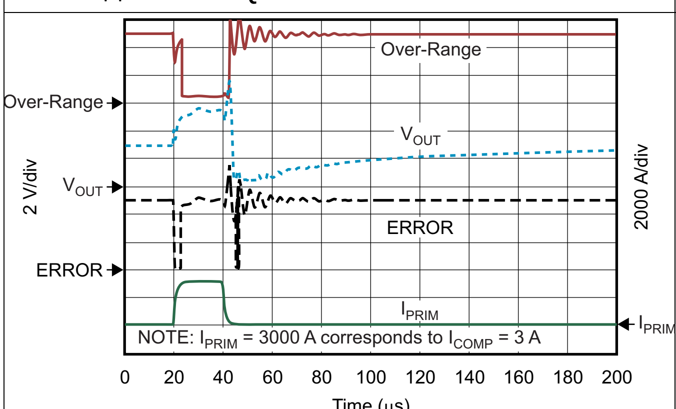


图 3. DRV401-Q1 Device and Sensor: Absolute Error



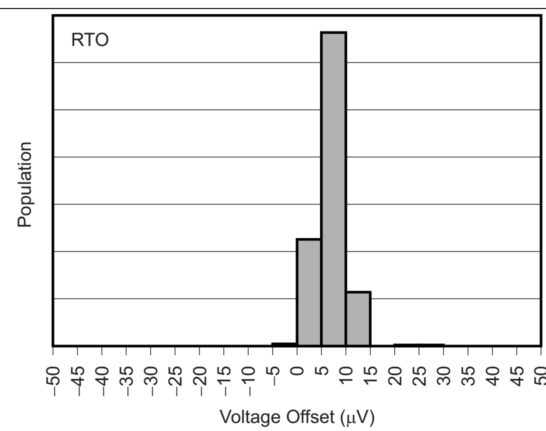
Soldered DWP−20 with 1-in² copper pad. Measurements by Vacuumschmelze GmbH.

图 4. Gain Flatness vs Frequency



Measurements by Vacuumschmelze GmbH.

图 5. 3-A I_{COMP} Overload Recovery



Measurements by Vacuumschmelze GmbH.

图 6. Differential Amplifier: Voltage Offset Production Distribution

Typical Characteristics (接下页)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

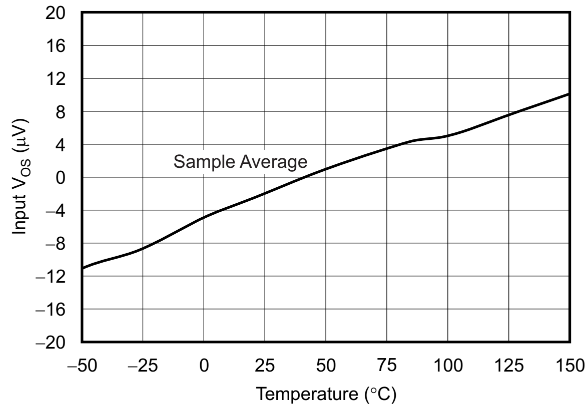


图 7. Differential Amplifier: Offset Voltage vs Temperature, RTO

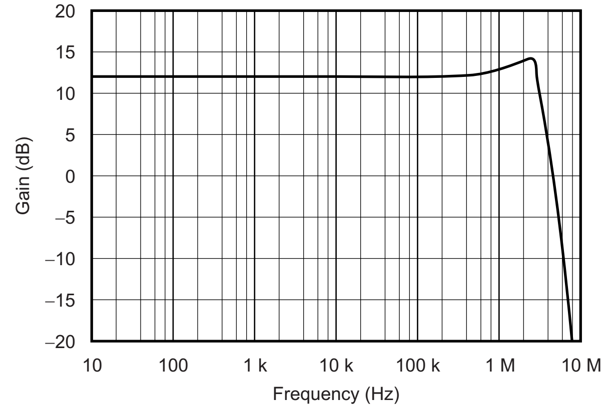


图 8. Differential Amplifier: Gain vs Frequency

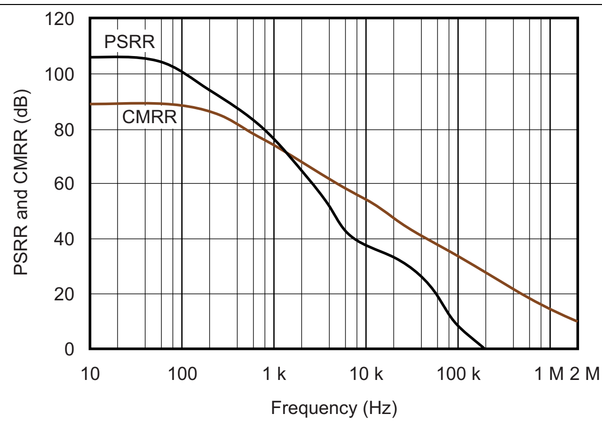


图 9. Differential Amplifier: PSRR and CMRR vs Frequency

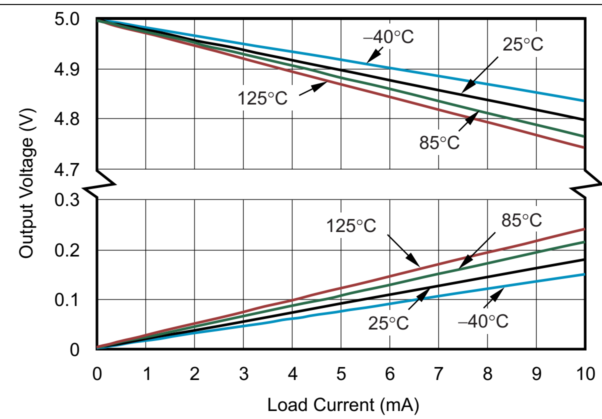


图 10. Differential Amplifier: Output Voltage vs Output Current

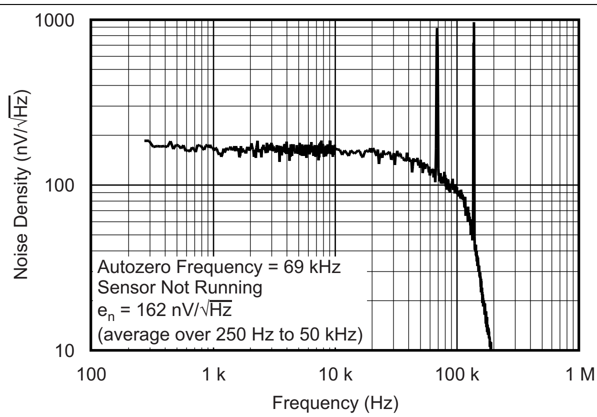


图 11. Differential Amplifier: Output Noise Density

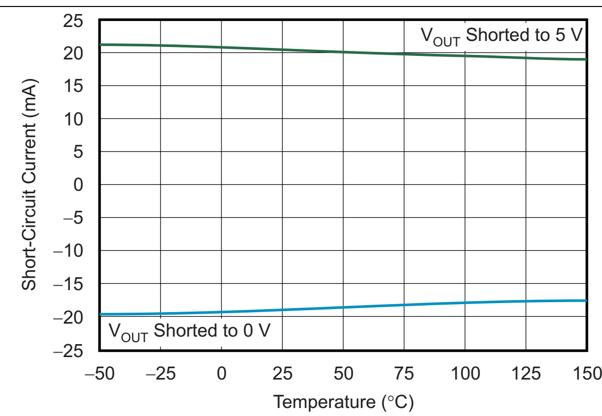


图 12. Differential Amplifier: Short-Circuit Current vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

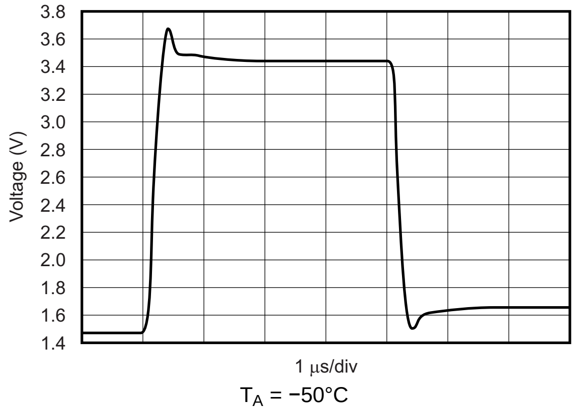


图 13. Differential Amplifier: Large-Signal Step Response

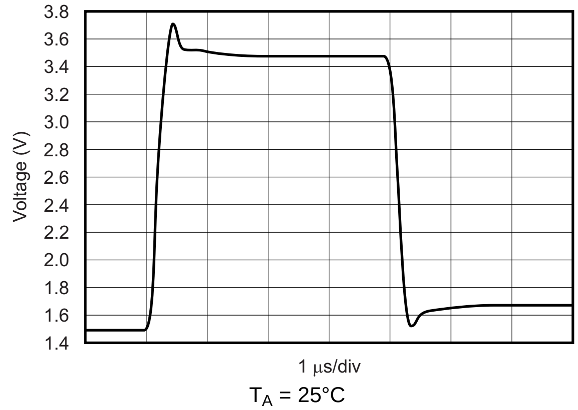


图 14. Differential Amplifier: Large-Signal Step Response

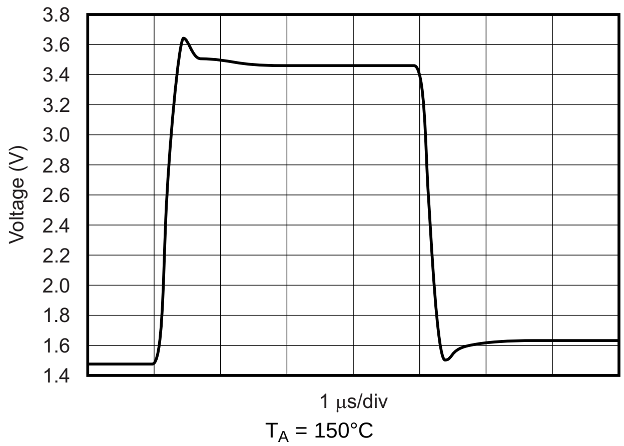


图 15. Differential Amplifier: Large-Signal Step Response

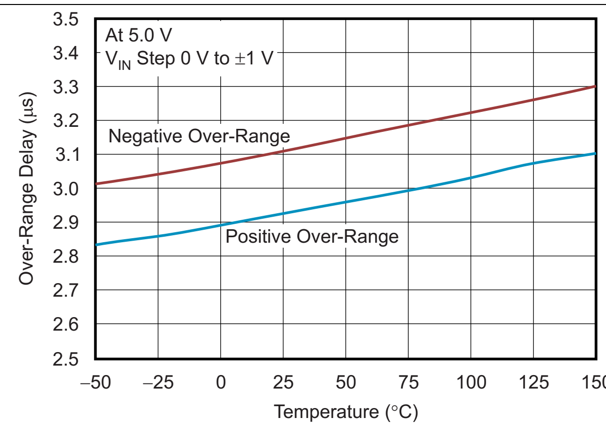


图 16. Differential Amplifier: Overrange Delay vs Temperature

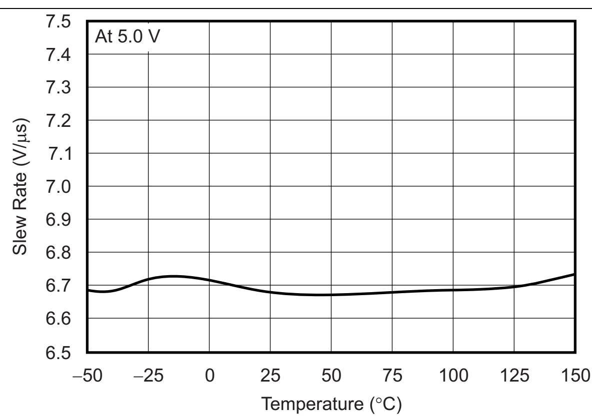


图 17. Differential Amplifier: Positive Slew Rate vs Temperature

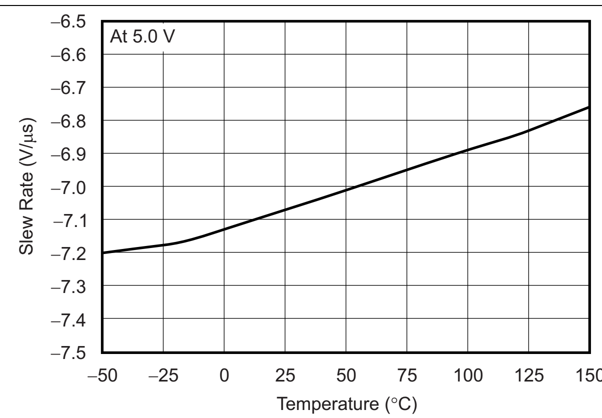


图 18. Differential Amplifier: Negative Slew Rate vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

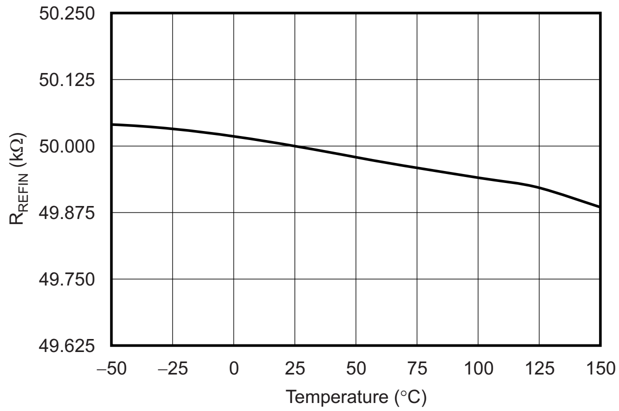


图 19. Differential Amplifier: REF_{IN} Resistance vs Temperature

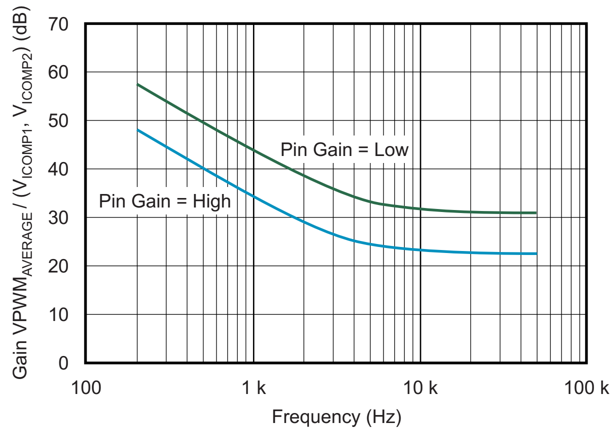


图 20. Compensation Loop: Small-Signal Gain

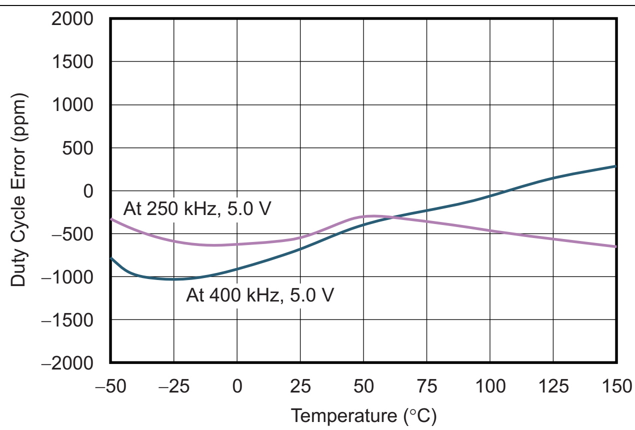


图 21. Compensation Loop: Duty Cycle Error vs Temperature

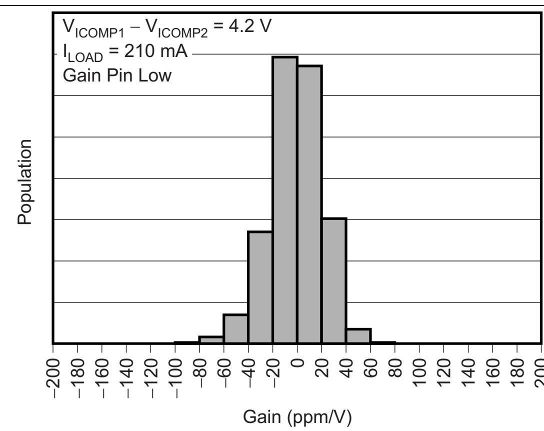


图 22. Compensation Loop: DC Gain: Duty Cycle Error Change

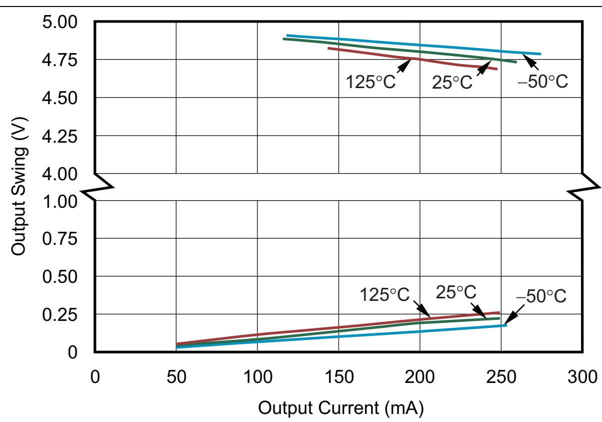


图 23. I_{COMP} Output Swing to Rail vs Output Current

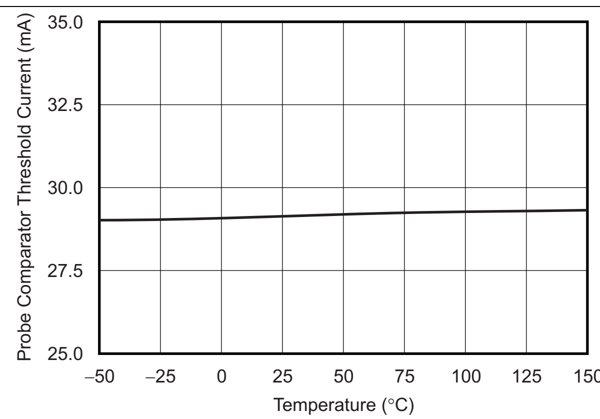


图 24. Probe Comparator Threshold Current vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

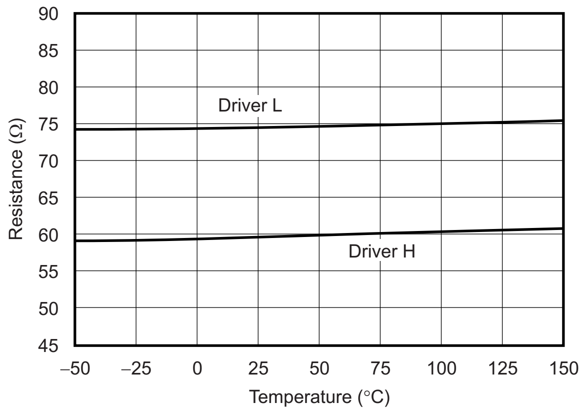


图 25. Probe Driver: Internal Resistor vs Temperature

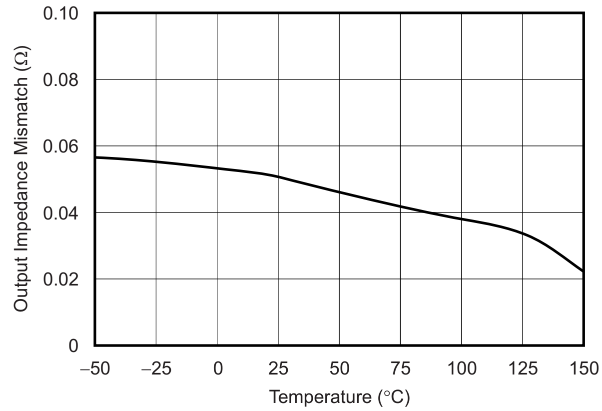


图 26. Output Impedance Mismatch of IS1 and IS2 vs Temperature

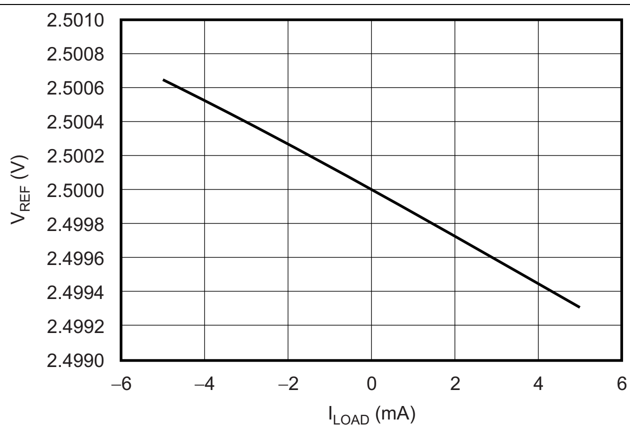


图 27. Voltage Reference vs Load Current

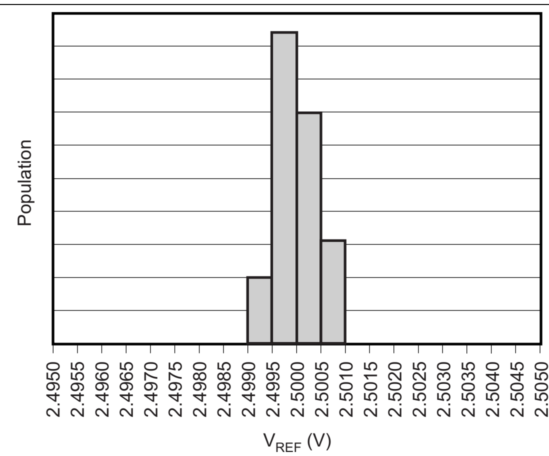


图 28. Voltage Reference Production Distribution

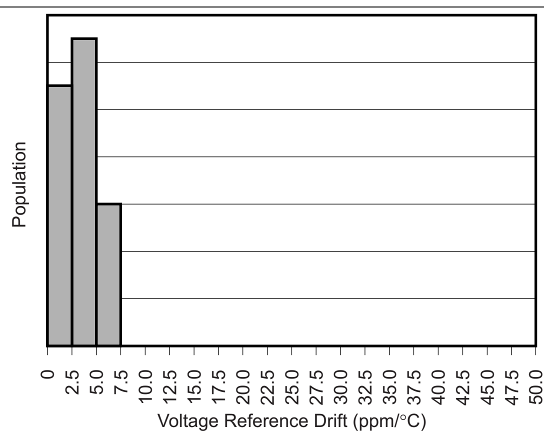


图 29. Voltage Reference Drift Production Distribution

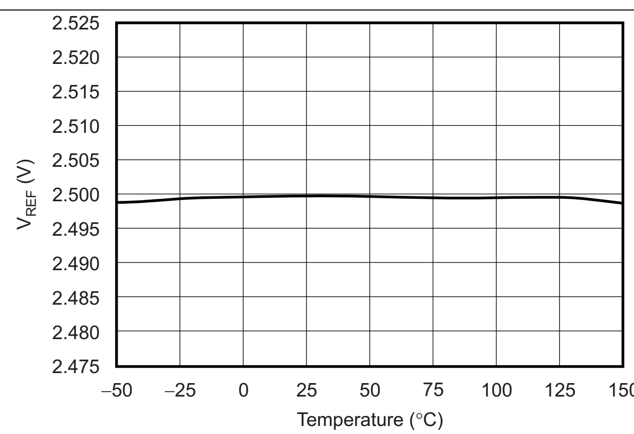


图 30. Voltage Reference vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V with external 100-kHz filter bandwidth, (unless otherwise noted)

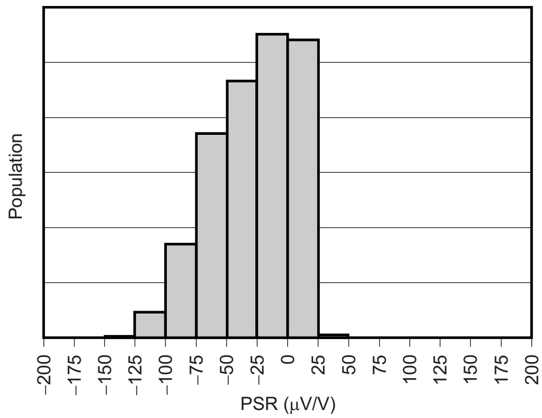


图 31. Voltage Reference Power-Supply Rejection Production Distribution

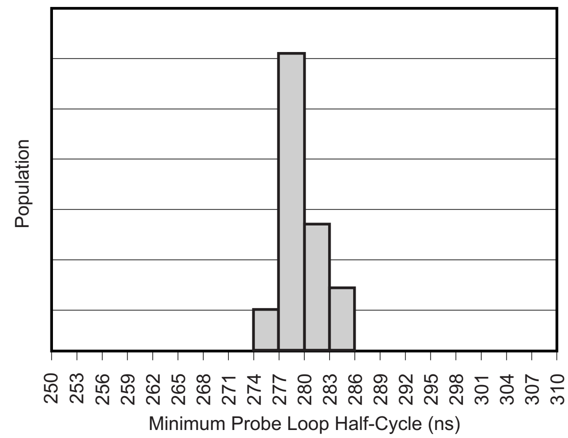


图 32. Oscillator Production Distribution

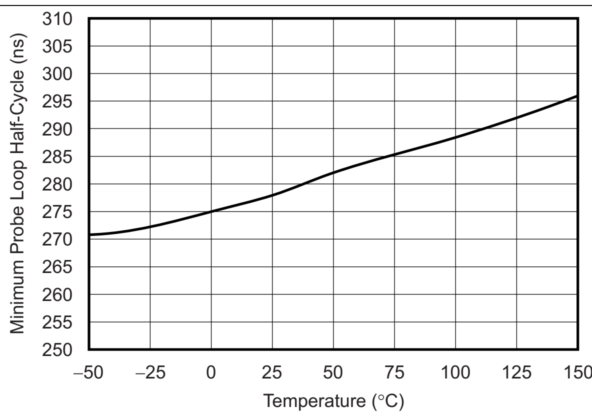


图 33. Oscillator vs Temperature

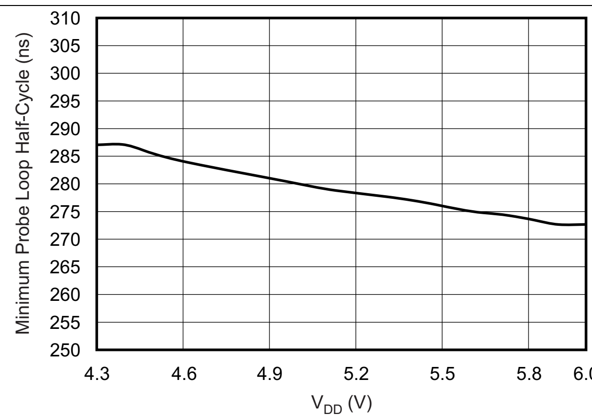


图 34. Oscillator vs Supply Voltage

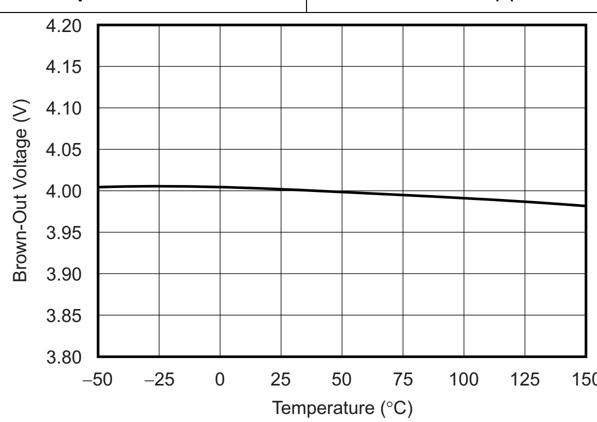


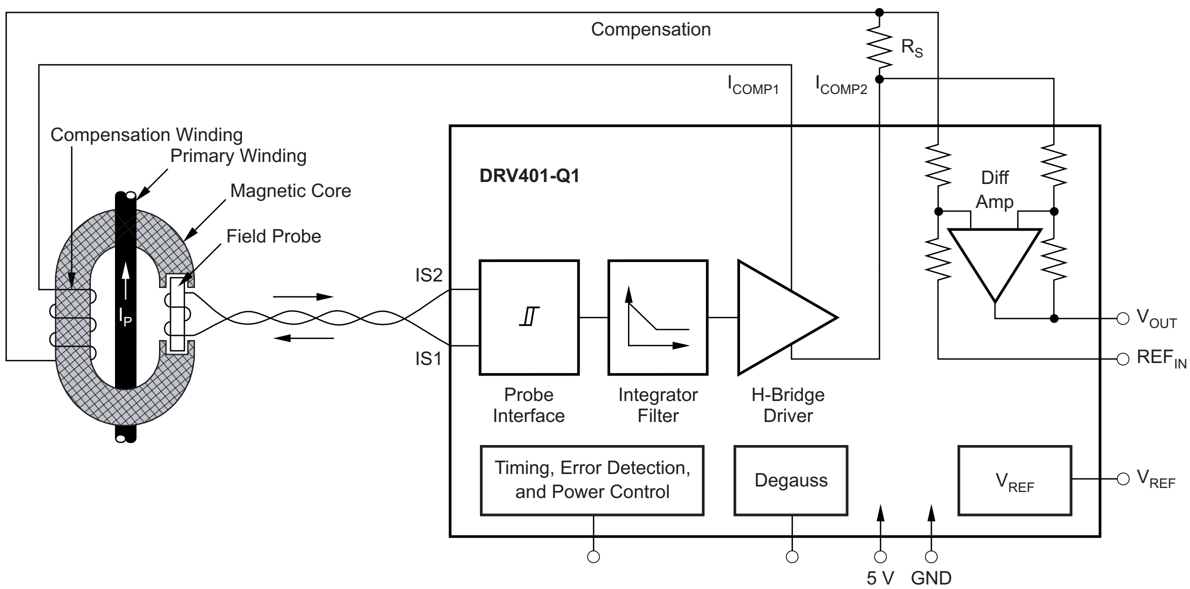
图 35. Brownout Voltage vs Temperature

7 Detailed Description

7.1 Overview

Closed-loop current sensors measure current over wide frequency ranges, including dc. These types of devices offer a contact-free method, as well as excellent galvanic isolation performance combined with high resolution, accuracy, and reliability. The DRV401-Q1 is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation.

7.2 Functional Block Diagram



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7.3 Feature Description

The DRV401-Q1 operates from a single 5-V supply. The DRV401-Q1 is a complete sensor signal conditioning circuit that directly connects to the current sensor, providing all necessary functions for the sensor operation. The DRV401-Q1 device provides magnetic field probe excitation, signal conditioning, and compensation coil driver amplification. In addition, the device detects error conditions and handles overload situations. A precise differential amplifier allows translation of the compensation current into an output voltage using a small shunt resistor. A buffered voltage reference is used for comparator, analog-to-digital converter (ADC), or bipolar zero reference voltages.

Dynamic error correction ensures high dc precision over temperature and long-term accuracy. The DRV401-Q1 uses analog signal conditioning, and the internal loop filter and integrator are switched capacitor-based circuits. Therefore, the DRV401-Q1 device allows combination with high-precision sensors for exceptional accuracy and resolution.

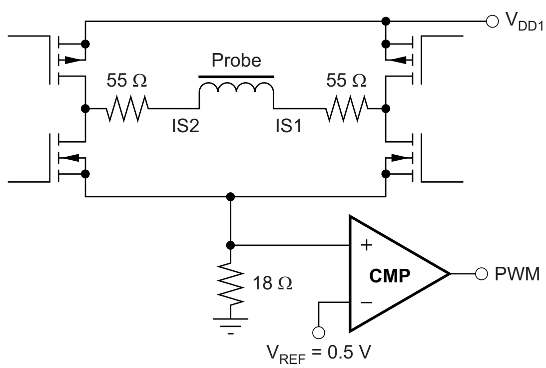
A demagnetization cycle initiates on demand or on power-up. The cycle reduces offset and restores high performance after a strong overload condition. An internal clock and counter logic generate the degauss function. The same clock controls power-up, overload detection and recovery, error, and time-out conditions.

The DRV401-Q1 device is built on a highly reliable CMOS process. Unique protection cells at critical connections enable the design to handle inductive energy.

7.3.1 Magnetic Probe (Sensor) Interface

The magnetic field probe consists of an inductor wound on a soft magnetic core. The probe is connected between pins IS1 and IS2 of the probe driver that applies approximately 5 V (the supply voltage) through resistors across the probe coil, as shown in 图 36.

Typically, the probe core reaches saturation at a current of 28 mA, as shown in 图 36. The comparator is connected to V_{REF} by approximately 0.5 V. A current comparator detects the saturation and inverts the excitation voltage polarity, causing the probe circuit to oscillate in a frequency range of 250 kHz to 550 kHz. The oscillating frequency is a function of the magnetic properties of the probe core and the coil.



NOTE: MOS components function as switches only.

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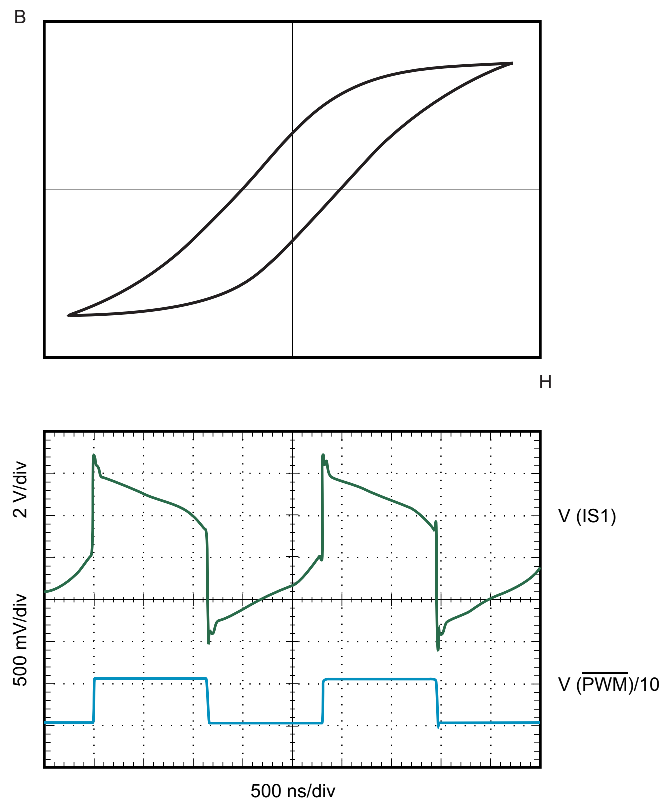
The probe is connected between S1 and S2.

图 36. Magnetic Probe, Hysteresis, and Duty Cycle: Simplified Probe Circuit

The current rise rate is a function of the coil inductance: dI = L × V × dT. However, the inductance of the field probe is low while the core material is in saturation (the horizontal part of the hysteresis curve) and is high at the vertical part of the hysteresis curve. The resulting inductance and the series resistance determine the output voltage and current versus time performance characteristic.

Feature Description (接下页)

Without external magnetic influence, the duty cycle is exactly 50% because of the inherent symmetry of the magnetic hysteresis; the probe inductor is driven from −B saturation through the high inductance range to +B saturation and back again in a time-symmetric manner, as shown in 图 37.

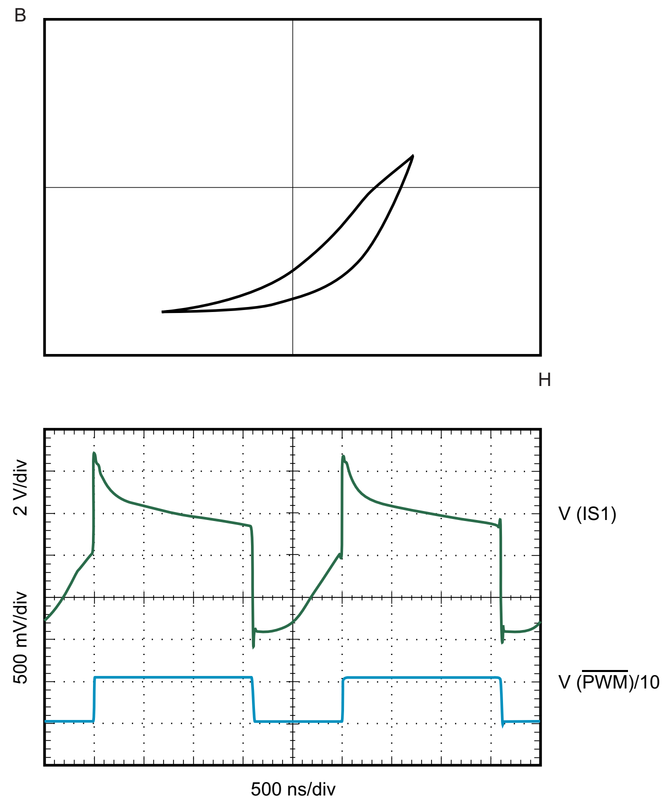


Without an external magnetic field, the hysteresis curve is symmetrical and the probe loop generates 50% duty cycle.

图 37. Magnetic Probe, Hysteresis, and Duty Cycle: No External Magnetic Field

Feature Description (接下页)

If the core material is magnetized in one direction, a long and a short charge time result because the probe current through the inductors generates a field that subtracts or adds to the flux in the probe core, driving the probe core out of saturation or further into saturation, as shown in 图 38. The current into the probe is limited by the voltage drops across the probe driver resistors.



An external magnetic flux (H) generated from the primary current (I_{PRIM}) shifts the hysteresis curve of the magnetic field probe in the H-axis and the probe loop generates a nonsymmetrical duty cycle.

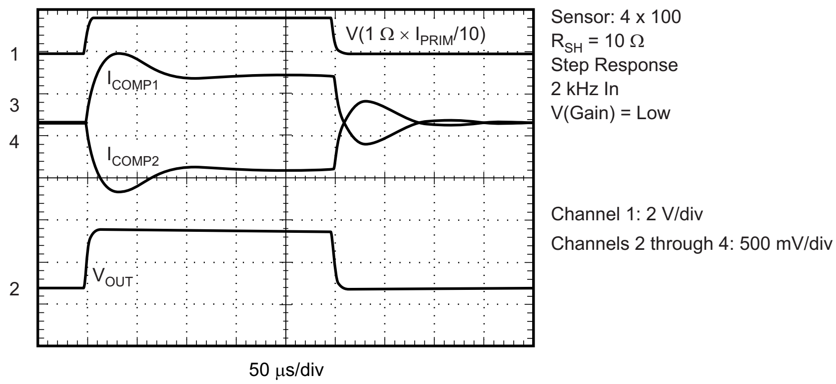
图 38. Magnetic Probe, Hysteresis, and Duty Cycle With External Magnetic Field

The DRV401-Q1 device continuously monitors the logic magnetic flux polarity state. In the case of distortion noise and excessive overload that can fully saturate the probe, the overload control circuit recovers the probe loop. During an overload condition, the probe oscillation frequency increases to approximately 1.6 MHz until limited by the internal timing control.

In an overload condition, the compensation current (I_{COMP}) driver cannot deliver enough current into the sensor secondary winding, so the magnetic flux in the sensor main core becomes uncompensated.

Feature Description (接下页)

The transition from normal operation to overload happens slowly because the inherent sensor transformer characteristics induce the initial primary current step, as shown in 图 39. As the transformer-induced secondary current starts to decay, the compensation feedback driver increases the output voltage to maintain the sensor core flux compensation at zero.



A current pulse of 0 A to 18 A (channel 1) generates the two I_{COMP} signals (channel 3 and channel 4). Channel 2 shows the resulting output signal (V_{OUT}). This test uses the M4645-X030 sensor with no bandwidth limitation, and a 20-sample average.

图 39. Primary Current Step Response

When the system compensation loop reaches the driving limit, the rising magnetic flux causes one of the probe pulse-width modulator (PWM) half-periods to become shorter. The minimum half-period of the probe oscillation is limited by the internal timing to 280 ns, based on the properties of the VAC magnetic sensors. After three consecutive cycles of the same half-period being shorter than 280 ns, the DRV401-Q1 device enters overload-latch mode. The device stores the I_{COMP} driver output signal polarity and continues producing the skewed-duty cycle PWM signal. This action prevents the loss of compensation signal polarity information during strong overloads. In this case, both PWM half-periods are short and approximately equal, because the field probe stays completely in one of the saturated regions.

The overload-latch condition is removed after the primary current goes low enough for the I_{COMP} driver to compensate, and both half-periods of the probe driver oscillation become longer than 280 ns (the field probe comes out of the saturated region).

Peak voltages and currents generate during normal operations and overload conditions. Both probe connection pins are internally protected against coupled energy from the magnetic core. Wiring between probe and device inputs must be short and guarded against interference, as shown in the *Layout Guidelines* section.

For reliable operation, error detection circuits monitor the probe operation:

1. If the probe driver comparator (CMP) output stays low longer than 32 µs, the ERROR flag asserts active, and the compensation current (I_{COMP}) is set to zero.
2. If the probe driver period is less than 275 ns on three consecutive pulses, the ERROR flag asserts active.

See the *Error Conditions* section for more details.

7.3.2 PWM Processing

The PWM and $\overline{\text{PWM}}$ outputs represent the probe output signal as a differential PWM signal. The signal drives external circuitry and is used for synchronous ripple reduction. The PWM signal from the probe excitation and sense stage is internally connected to a high-performance, switched-capacitor integrator followed by an integrating-differentiating filter. The filter converts the PWM signal into a filtered delta signal and prepares the PWM signal to drive the analog compensation coil driver. The gain roll-off frequency of the filter stage provides high dc gain and loop stability. If additional gain is added from external circuitry, the internal gain is reduced by 8 dB, which asserts the GAIN pin high, as shown in the *External Compensation Coil Driver* section.

Feature Description (接下页)

7.3.3 Compensation Driver

The compensation coil driver provides the driving current for the compensation coil. A fully-differential driver stage offers high signal voltages to overcome the wire resistance of the coil with a 5-V supply. The compensation coil is connected between I_{COMP1} and I_{COMP2}, generating an analog voltage across the coil (shown in 图 39) that turns into current from the wire resistance (and eventually from the inductance). The compensation current represents the primary current transformed by the turns ratio. A shunt resistor is connected in this loop and the high-precision difference amplifier translates the voltage from the shunt to an output voltage.

Both compensation driver outputs provide low impedance over a wide frequency range to ensure smooth transitions between the closed-loop compensation frequency range and the high-frequency range, where the primary winding directly couples the primary current into the compensation coil at a rate set by the winding ratio.

The two compensation driver outputs are designed with protection circuitry to handle inductive energy. However, additional external protection diodes may be necessary for high-current sensors.

For reliable operation, a wire break in the compensation circuit can be detected. If the feedback loop is broken, the integrating filter drives the I_{COMP1} and I_{COMP2} outputs to the opposite rails. With one of these pins coming within 300 mV to ground, a comparator tests for a minimum current flowing between I_{COMP1} and I_{COMP2}. If the current stays below the threshold current level for a minimum of 100 μs, the ERROR pin is asserted active (low). The threshold current level for the test is less than 57 mA at 25°C and 65 mA at −40°C if the I_{COMP} pins are fully railed, as shown in the *Typical Characteristics* section.

For sensors with high winding resistance (compensation coil resistance + R_{SHUNT}) or that are connected to an external compensation driver, this function must be disabled by pulling the CCdiag pin low, as shown in 公式 1:

$$R_{MAX} = \frac{V_{OUT}}{65\ \text{mA}} \quad (1)$$

where:

- V_{OUT} equals the peak voltage between I_{COMP1} and I_{COMP2} at a 65-mA drive current; and
- R_{MAX} equals the sum of the coil and the shunt resistance

7.3.4 External Compensation Coil Driver

An external driver for the compensation coil connects to the I_{COMP1} and I_{COMP2} outputs. To prevent a wire break indication, CCdiag must be asserted low.

An external driver provides a higher drive voltage and more drive current. The driver moves the power dissipation to the external transistors, thereby allowing a higher winding resistance in the compensation coil and more current. 图 40 shows a block diagram of an external compensation coil driver. To drive the buffer, one or both of the I_{COMP} outputs may be used. Note, however, that the additional voltage gain can cause instability of the loop. Therefore, the internal gain may be reduced by approximately 8 dB by asserting the GAIN pin high. R_{SHUNT} is connected to GND to allow for a single-ended external compensation driver. The differential amplifier continues to sense the voltage, and is used for the gain and over-range comparator or ERROR flag.

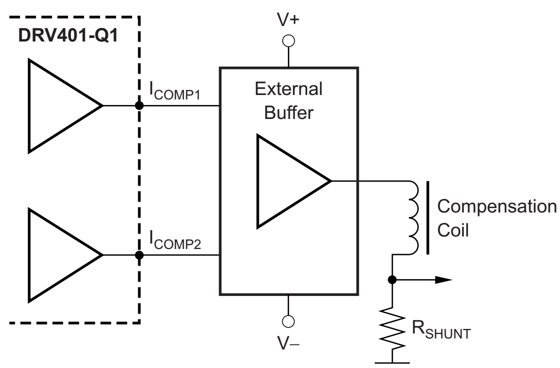


图 40. DRV401-Q1 with External Compensation Coil Driver and R_{SHUNT} Connected to GND

Feature Description (接下页)

7.3.5 Shunt Sense Amplifier

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4 V/V, set by precisely matched and stable internal SiCr resistors.

7.3.6 Over-Range Comparator

High peak current can overload the differential amplifier connected to the shunt. The OVER-RANGE pin, an open-drain output, indicates an over-voltage condition for the differential amplifier by pulling low. The output of this flag is suppressed for 3 µs, preventing unwanted triggering from transients and noise. This pin returns to high when the overload condition is removed (an external pull-up is required to return the pin high).

This ERROR flag provides a warning about a signal clipping condition, but is also a window comparator output for actively shutting off circuits in the system. The value of the shunt resistor defines the operating window for the current. The value of the shunt resistor sets the ratio between the nominal signal and the trip level of the over-range flag. The trip current of this window comparator is calculated using the following example:

With a 5-V supply, the output voltage swing is approximately ±2.45 V (load and supply voltage-dependent).

The gain of 4 V/V allows an input swing of ±0.6125 V.

Thus, the clipping current is I_{MAX} = 0.6125 V / R_{SHUNT}.

See 图 10.

The over-range condition is internally detected when the amplifier exceeds the linear operating range, not merely as a set voltage level. Therefore, the error or the over-range comparator level is reliably indicated in fault conditions such as output shorts, low load or low supply conditions. The flag is activated when the output cannot drive the voltage higher. The configuration is a safety improvement over a voltage level comparator.

注

The internal resistance of the compensation coil may prevent high compensation current from flowing because of I_{COMP} driver overload. Therefore, the differential amplifier may not overload with this current. However, a fast rate of change of the primary current would be transmitted through transformer action and safely trigger the overload flag.

7.3.7 Voltage Reference

The precision 2.5-V reference circuit offers low drift (typically 10 ppm/K), used for internal biasing, and connects to the REF_{OUT} pin. The circuit is intended as the reference point of the output signal to allow a bipolar signal around it. The output is buffered for low impedance and tolerates sink and source currents of ±5 mA. Capacitive loads may be directly connected, but generate ringing on fast load transients. A small series resistor of a few ohms improves the response, especially for a capacitive load in the range of 1 μF. 图 41 illustrates this circuit configuration and the transient load regulation with 1-nF direct load.

The reference source is part of the integrated circuit and referenced to GND2. Large current pulses driving the compensation coil generates a voltage drop in the GND connection that may add on to the reference voltage. Therefore, a low impedance GND layout is critical to handle the currents and the high bandwidth of the device.

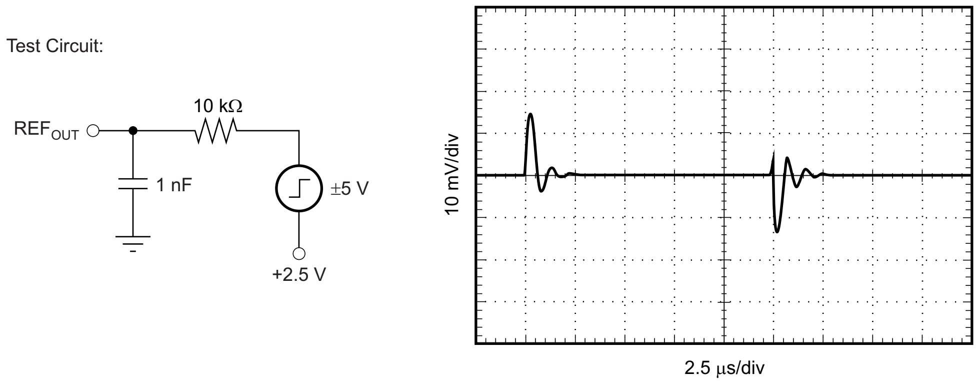


图 41. Pulse Response: Test Circuit and Scope Shot of Reference

7.3.8 Demagnetization

Iron cores are not immune to residual (remanence) magnetism. The residual remanence produces a signal offset error, especially after strong current overload, which goes along with high magnetic field density. Therefore, the DRV401-Q1 device includes a signal generator for a demagnetization cycle. The digital control pin, DEMAG, starts the cycle on demand after the pin is held high for at least 25.6 μs. Shorter pulses are ignored. The cycle lasts for approximately 110 ms. During this time, the ERROR flag is asserted low to indicate that the output is not valid. When DEMAG is high during power-on, a demagnetization cycle immediately initiates (12 μs) after power-on (V_{DD} > 4 V). Holding DEMAG low avoids this cycle at power-up. See the *Power-On and Brownout* section for more information.

The probe circuit is in normal operation and oscillates during the demagnetization cycle. The PWM and $\overline{PWM}$ outputs are active accordingly.

A demagnetization cycle can be aborted by pulling DEMAG low, filtered by 25 μs to ignore glitches, as shown in 图 46. In a typical circuit, the DEMAG pin may be connected to the positive supply, which enables a degauss cycle every time the unit is powered on.

The degauss cycle is based on an internal clock and counter logic. The maximum current is limited by the resistance of the connected coil in series with the shunt resistor. The DEMAG logic input requires a 5-V, CMOS-compatible signal.

7.3.9 Power-On and Brownout

Power-on is detected with the supply voltage going higher than 4 V at V_{DD1}. When DEMAG is high, a degauss cycle is started, as shown in 图 46 through 图 49. During this time the ERROR flag remains low, indicating the *not ready* condition. Maintaining DEMAG low prevents this cycle, and the DRV401-Q1 device starts operation approximately 32 µs after power-up. If no probe error conditions are detected within four full cycles (that is, the probe half-periods are shorter than 32 µs and longer than 280 ns), the compensation driver starts and the ERROR pin indicates the ready condition by going high, typically about 42 µs after power-up.

注

An external pull-up resistor is required to pull the ERROR pin high.

Both supply pins (V_{DD1} and V_{DD2}) must not differ by more than 100 mV for proper device operation. They are normally connected together or separately filtered as shown in *Layout*.

The DRV401-Q1 device tests for low supply voltage with a brownout voltage level of 4 V; proper power conditions must be supplied. Good power-supply and low equivalent series resistance (ESR) bypass capacitors are required to maintain the supply voltage during the large current pulses that the DRV401-Q1 device drives.
A critical voltage level is derived from the proper operation of the probe driver. The probe interface relies on a peak current flowing through the probe to trip the comparator. The probe resistance plus the internal resistance of the driver (see *Probe Coil Loop, Internal Resistor* parameters in the *Electrical Characteristics* table) sets the lower limit for the acceptable supply voltage. Voltage drops lasting less than 31 µs are ignored. The probe error detection activates the ERROR pin when proper oscillation fails for more than 32 µs.

A low supply voltage condition, or brownout, is detected at 4 V. Short and light voltage drops of less than 100 µs are ignored, provided the probe circuit continues to operate. If the probe no longer operates, the ERROR pin goes active. Signal overload recovery is only provided if the probe loop was not discontinued.

A supply drop lasting longer than 100 µs generates power-on reset. A voltage dip down to 1.8 V (for V_{DD1}) initiates a power-on reset.

7.3.10 Error Conditions

In addition to the overrange flag that indicates signal clipping in the output amplifier (differential amplifier), a system error flag is provided. The ERROR flag indicates conditions when the output voltage does not represent the primary current. The ERROR flag is active during a demagnetization cycle, power-fail, or brownout. The ERROR flag becomes active with an open or short-circuit in the probe loop. When the error condition is no longer present and the circuit returns to normal operation, the flag resets.

The ERROR and overrange flags are open-drain logic outputs. The flags connect together for a wired-*OR* and require an external pull-up resistor for proper operation.

The following conditions result in ERROR flag activation (ERROR asserts low):

1. The probe comparator stays low for more than 32 µs. This condition occurs if the probe coil connection is open or if the supply voltage dips to the level where the required saturation current cannot be reached. During the 32-µs timeout, the I_{COMP} driver remains active but goes inactive thereafter. In case of recovery, ERROR is low and the I_{COMP} driver remains in reset for another 3.3 ms.
2. The probe driver pulse-width is less than 280 ns for three consecutive periods. This condition indicates a shorted field probe coil or a fully-saturated sensor at start-up. If this condition persists longer than 25 µs and then recovers, the ERROR flag remains low and I_{COMP} is in reset for another 3.3 ms. If the condition lasts less than 25 µs, the ERROR flag recovers immediately and the I_{COMP} driver is not interrupted.
3. During demagnetization, if the cycle is aborted early by pulling DEMAG low, the ERROR flag stays low for another 3.3 ms (I_{COMP} is disabled during this time).
4. An open compensation coil is detected (longer than 100 µs). This condition indicates that not enough current is flowing in the I_{COMP} driver output; this condition may be the result of a high-resistance compensation coil or the connection of an external driver. Detection of this condition can be disabled by setting the CCdiag pin low.

注

The probe driver, the PWM signal filter, and the I_{COMP} driver continue to function in normal mode. Only the ERROR flag is asserted in the case when an open compensation coil is detected.

5. At power-on after V_{DD1} crosses the 4-V threshold, the ERROR flag is low for approximately 42 μs.
6. A supply voltage low (brownout) condition lasts longer than 100 μs. Recovery is the same as power-up, with or without a demagnetization cycle.

7.3.11 Protection Recommendations

The I_{AIN1} and I_{AIN2} inputs require external protection to limit the voltage swing beyond 10 V of the supply voltage. The driver outputs I_{COMP1} and I_{COMP2} handles high current pulses protected by internal clamp circuits to the supply voltage. If repeated overcurrents of large magnitudes are expected, connect external Schottky diodes to the supply rails. This external protection prevents current flowing into the die.

The IS1 and IS2 probe connections are protected with diode clamps to the supply rails. In normal applications, no external protection is required. The maximum current must be limited to ±75 mA.

All other pins offer standard protection. See the *Absolute Maximum Ratings* table for more information.

7.4 Device Functional Modes

The DRV401-Q1 has a single functional mode and is operational when the power supply voltages, V_{DD1} and V_{DD2}, are between 4.5 V and 5.5 V. For unusual operating conditions where a brownout condition may occur the DRV401-Q1 may perform a power-on reset. See the *Power-On and Brownout* section for a complete description of operation during a brownout.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Functional Principle of Closed-Loop Current Sensors with Magnetic Probe Using the DRV401-Q1 Device

Closed-loop current sensors measure current over wide frequency ranges, including dc. These types of devices offer a contact-free method and an excellent galvanic isolation performance combined with high resolution, accuracy, and reliability.

At dc and in low-frequency ranges, the magnetic field induced from the current in the primary winding is compensated by a current flowing through a compensation winding. A magnetic field probe, located in the magnetic core loop, detects the magnetic flux. This probe delivers the signal to the amplifier that drives the current through the compensation coil, bringing the magnetic flux back to zero. This compensation current is proportional to the primary current, relative to the winding ratio.

In higher-frequency ranges, the compensation winding acts as the secondary winding in the current transformer, while the H-bridge compensation driver is rolled off and provides low output impedance.

A difference amplifier senses the voltage across a small shunt resistor that is connected to the compensation loop. This difference amplifier generates the output voltage that is referenced to REF_{IN} and is proportional to the primary current. The *Functional Block Diagram* shows the DRV401-Q1 device used as a compensation current sensor.

Application Information (接下页)

8.1.2 Basic Connection

The circuit shown in 图 42 offers an example of a fully-connected current sensor system.

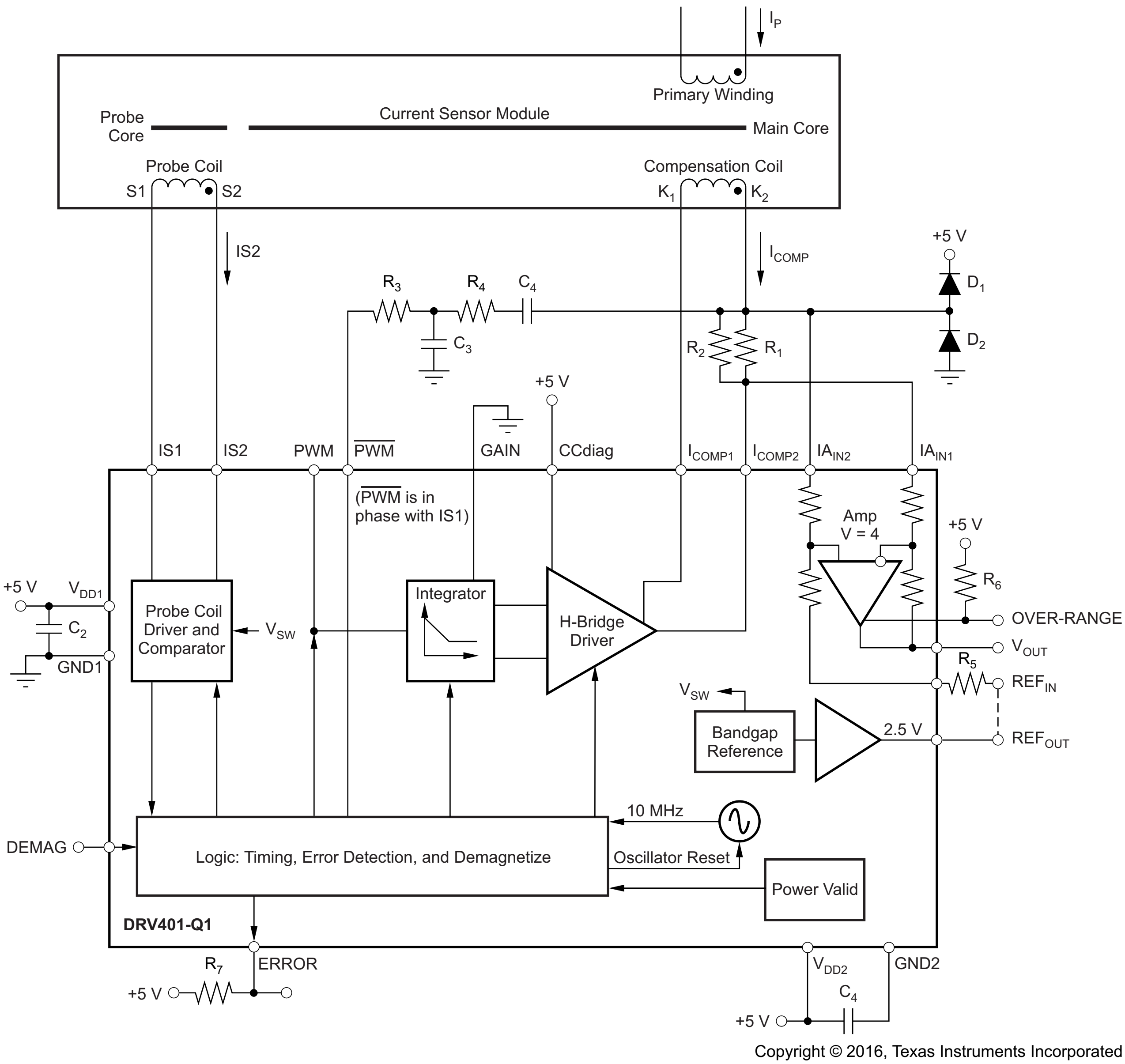


图 42. Basic Connection Circuit

The connection example in 图 42 illustrates the few external components required for optimal performance. Each component is described in the following list:

- I_P is the primary current to be measured; K_1 and K_2 connect to the compensation coil. **S1** and **S2** connect to the magnetic field probe. The dots indicate the winding direction on the sensor main core.
- R_1 and R_2 form the shunt resistor R_{SHUNT}. This resistance is split into two to allow for adjustments to the required R_{SHUNT} value. The accuracy and temperature stability of these resistors are part of the final system performance.
- R_3 and R_4, together with C_3 and C_4, form a network that reduces the remaining probe oscillator ripple in the output signal. The component values depend on the sensor type and are tailored for best results. This network is not required for normal operation.

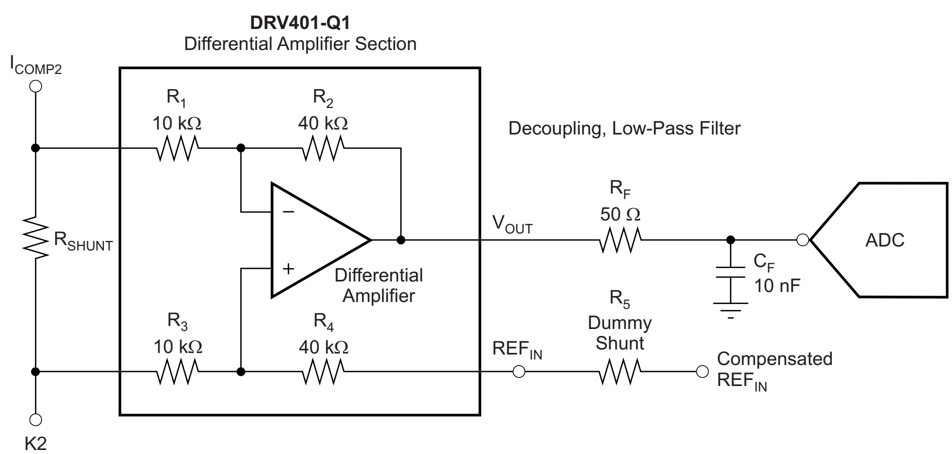
Application Information (接下页)

- **R_5** is the dummy shunt (R_D) resistor used to restore the symmetry of both differential amplifier inputs. $R_5 = 4 \times R_{SHUNT}$, but the accuracy is less important.
- **R_6** and **R_7** are pull-up resistors connected to the logic outputs.
- **C_1** and **C_2** are decoupling capacitors. Use low ESR-type capacitors connected close to the pins. Use low-impedance printed circuit board (PCB) traces, either avoiding vias (plated-through holes) or using multiple vias. A combination of a large (> 1-µF) and a small (< 4.7-nF) capacitor are suggested. When selecting capacitors, make sure to consider the large pulse currents handled from the DRV401-Q1 device.
- **D_1** and **D_2** are protection diodes for the differential amplifier input. They are only needed if the voltage drop at R_{SHUNT} exceeds 10 V at the maximum possible peak current.

8.2 Typical Application

The differential (H-bridge) driver arrangement for the compensation coil requires a differential sense amplifier for the shunt voltage. This differential amplifier offers wide bandwidth and a high slew rate for fast current sensors. Excellent dc stability and accuracy result from an auto-zero technique. The voltage gain is 4 V/V, set by precisely matched and stable internal SiCr resistors.

Both inputs of the differential amplifier are normally connected to the current shunt resistor. The resistor adds to the internal (10-kΩ) resistor, slightly reducing the gain in this leg. For best common-mode rejection (CMR), a dummy shunt resistor (R_5) is placed in series with the REF_{IN} pin to restore matching of both resistor dividers, as shown in 图 43.



R_5 is a dummy shunt resistor equal to $4 \times R_{SHUNT}$ to compensate for R_{SHUNT} and provide optimal CMR.

图 43. Internal Difference Amplifier with an Example of a Decoupling Filter

8.2.1 Design Requirements

- Operate from a single 5-V power supply.
- Measure the compensation coil current with a gain = 4 V/V.
- Maximize the gain accuracy.
- Minimize the common-mode error.

Typical Application (接下页)

8.2.2 Detailed Design Procedure

For gains of 4 V/V, 公式 2 shows the calculation:

$$4 = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_{SHUNT} + R_3} \quad (2)$$

With $R_2 / R_1 = R_4 / R_3 = 4$; $R_5 = R_{SHUNT} \times 4$.

Typically, the gain error resulting from the resistance of R_{SHUNT} is negligible; for 70 dB of common-mode rejection, however, the match of both divider ratios must be better than 1/3000.

The amplifier output may drive close to the supply rails, and is designed to drive the input of a successive-approximation resistance (SAR)-type ADC; adding an RC low-pass filter stage between the DRV401-Q1 device and the ADC is recommended. This filter limits the signal bandwidth and decouples the high-frequency component of the converter input sampling noise from the amplifier output. For R_F and C_F values, see the specific converter recommendations in the specific product data sheet. Empirical evaluation may be necessary to obtain optimum results.

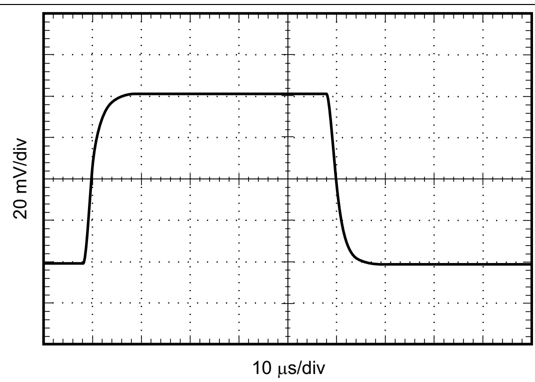
The output drives 100 pF directly and shows 50% overshoot with approximately 1-nF capacitance. Adding R_F allows much larger capacitive loads, as shown in 图 44 and 图 45.

注

Note that with an R_F value of only 20 Ω, the load capacitor must be smaller than 1 nF or larger than 33 nF to avoid overshoot; with an R_F value of 50 Ω, this transient area is avoided.

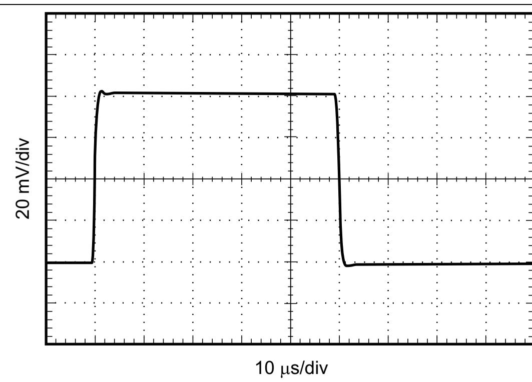
The reference input (REF_{IN}) is the reference node for the exact output signal (V_{OUT}). Connecting REF_{IN} to the reference output (REF_{OUT}) results in a live zero reference voltage of 2.5 V. Using the same reference for REF_{IN} and the ADC avoids mismatch errors that exist between two reference sources.

8.2.3 Application Curves



R_5 = 20 Ω, C_D = 100 nF

图 44. 图 44 Performance (V_{OUT})

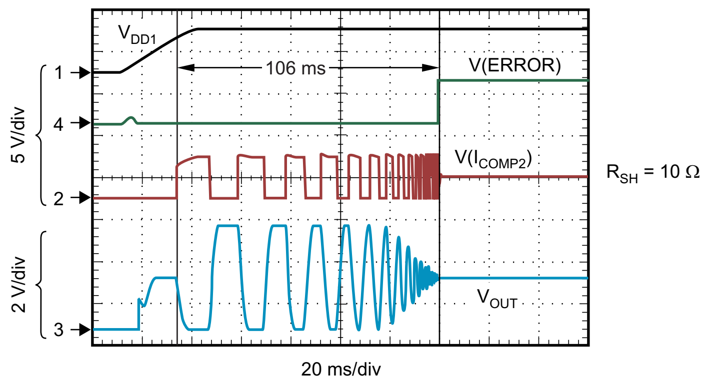


R_5 = 50 Ω, C_D = 10 nF

图 45. 图 45 Performance (V_{OUT})

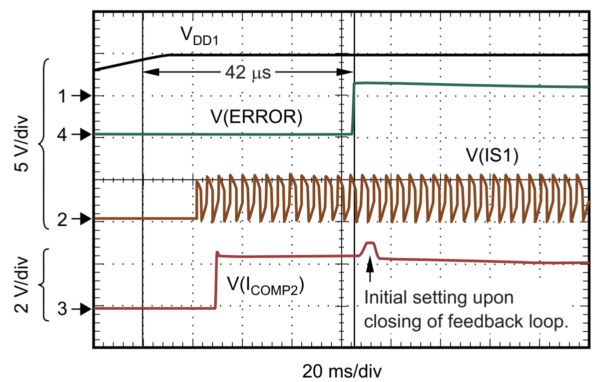
9 Power Supply Recommendations

The DRV401-Q operates from a single power supply, nominally 5 V, and must remain between 4.5 V and 5.5 V for normal operation. See 图 46, 图 47, 图 48, and 图 49 for device power-on behavior.



With power-up, the V_{OUT} across the compensation coil centers around half the supply and then starts the cycle after the 4-V threshold is exceeded. The ERROR flag resets to H after the cycle is completed.

图 46. Demagnetization and Power-On Timing: Demagnetization Cycle on Power-Up



The probe oscillation V(IS1) starts just before ERROR resets—15 µs after the supply voltage crosses the 4-V threshold.

图 47. Demagnetization and Power-On Timing: Power-Up Without Demagnetization

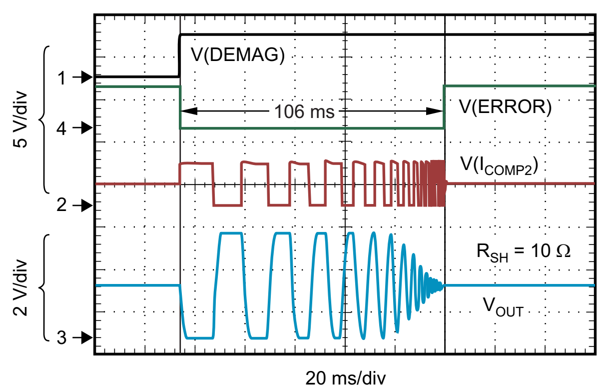
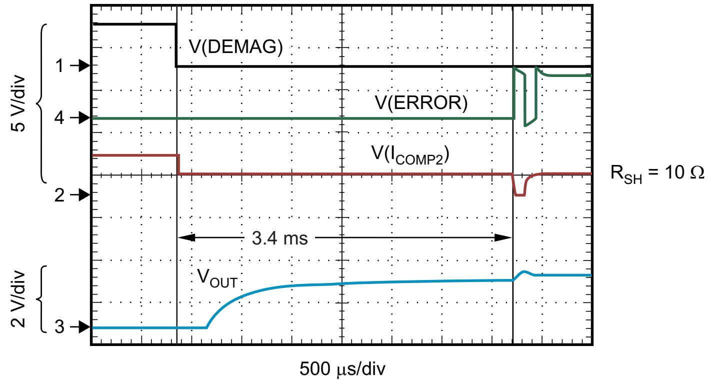


图 48. Demagnetization and Power-On Timing: Demagnetization Cycle On Command



The ERROR flag resets to H (as shown) and the output settles back to normal operation.

图 49. Demagnetization and Power-On Timing: Abort of Demagnetization Cycle

10 Layout

10.1 Layout Guidelines

The typical device configuration is shown in 图 42. The DRV401-Q1 operates with relatively large currents and fast current pulses, and offers wide-bandwidth performance. The device is often exposed to large distortion energy from the primary signal and the operating environment. Therefore, the wiring layout must provide shielding and low-impedance connections between critical points.

Use low-ESR capacitors for power-supply decoupling. Use a combination of a small capacitor and a large capacitor with a 1-µF or larger value. Use low-impedance tracks to connect the capacitors to the pins.

Both grounds must be connected to a local ground plane. Both supplies can be connected together; however, best results are achieved with separate decoupling (to the local GND plane) and ferrite beads in series with the main supply. The ferrite beads decouple the DRV401-Q1 device, reducing interaction with other circuits powered from the same supply voltage source.

The reference output is referred to GND2. A low-impedance, star-type connection is required to avoid the driver current and the probe current modulating the voltage drop on the ground track.

The connection wires of the difference amplifier to the shunt must be low resistance and of equal length. For best accuracy, avoid current in this connection. Consider using a Kelvin Contact-type connection. The required resistance value may be set using two resistors.

Wires and PCB traces for S1 and S2 must be close or twisted. I_{COMP1} and I_{COMP2} must be wired close together. To avoid capacitive coupling, run a ground shield between the S1/S2 and I_{COMP} wire pair or keep them distant from each other.

The compensation driver outputs (I_{COMP}) are low frequency only. However, the primary signal (with high-frequency content present) is coupled into the compensation winding, the shunt, and the difference amplifier. TI recommends a careful layout.

The REF_{OUT} and V_{OUT} output drives some capacitive loads, but avoid large direct capacitive loads; these loads increase internal pulse currents. Given the wide bandwidth of the differential amplifier, isolate any large capacitive load with a small series resistor. A small capacitor (in the pF range) improves the transient response on a high resistive load.

The exposed thermal pad on the bottom of the package must be soldered to GND because the thermal pad is internally connected to the substrate, which must be connected to the most negative potential. Solder the exposed pad to the PCB to provide structural integrity and long-term reliability.

10.2 Layout Example

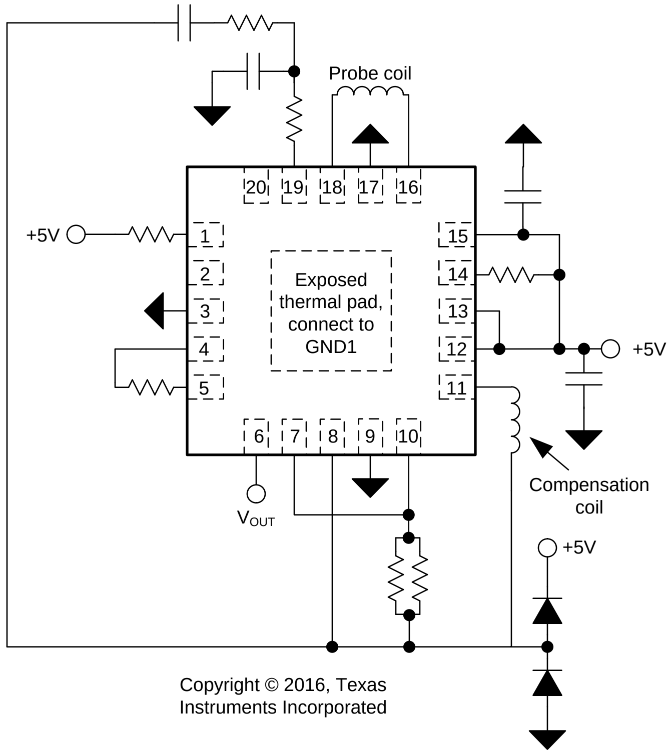


图 50. DRV401-Q1 Layout Example (RGW Package)

10.3 Power Dissipation

Using the thermally-enhanced VQFN package dramatically reduces the thermal impedance from junction to case. This package is constructed using a down-set lead frame that the die is mounted on. This arrangement results in the lead frame exposed as a thermal pad on the underside of the package. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The two outputs (I_{COMP1} and I_{COMP2}) are linear outputs. Therefore, the power dissipation on each output is proportional to the current multiplied by the internal voltage drop on the active transistor. For I_{COMP1} and I_{COMP2}, this internal voltage drop is the voltage drop to V_{DD2} or GND, according to the current-conducting side of the output.

Output short-circuits are particularly critical for the driver because the full supply voltage can be seen across the conducting transistor, and the current is not limited by anything other than the current density limitation of the FET. Permanent damage to the device may occur.

The DRV401-Q1 does not include temperature protection or thermal shutdown.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

器件支持 (接下页)

TINA-TI 可从 WEBENCH® 设计中心免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助WEBENCH 滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来打造最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

使用 DRV401-Q1 器件时，建议参考下列相关文档。除非另外注明，否则这些文档均可从 www.ti.com 下载。

- *《PowerPAD 散热增强型封装》* (SLMA002)
- *《四方扁平无引线逻辑器件封装》*（文献编号：SCBA017）
- *《QFN/SON PCB 连接》*（文献编号：SLUA271）

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

12.1 散热焊盘

散热焊盘外露型封装经专门设计可提供出色的功率耗散，但电路板布局会严重影响总体热耗散。表 1 显示了将外露散热焊盘焊接到常规 PCB 上的种封装的热阻 (θ_{JA})，如*《PowerPAD 散热增强型封装》* (SLMA002) 所述。请参阅 EIA/JEDEC 规范 JESD51-0 至 JESD51-7、*《QFN/SON PCB 连接》* (SLUA271) 和*《方形扁平无引脚逻辑封装》* (SCBA017)。这些文档可从 www.ti.com.cn 下载。

表 **1.** 根据 **EIA/JED51-7** 规范得出的 θ_{JA} 和 θ_{JP} 估算值(1)

参数	VQFN
θ_{JP}	9
θ_{JA}（不通风时）	40
θ_{JA}（强制通风，气流为 150lfm 时）	38

(1) θ_{JA} = 结至环境热阻。

TI 建议测量尽可能靠近散热焊盘处的温度。热阻值 θ_{JP} 相对较低，小于 10°C/W（到 PCB 上的温度测试点具有一些额外热阻），从而可对应用中的结温进行很好的估算。

PCB 上的散热焊盘必须包含九个或更多个适用于 VQFN 封装的通孔。

组件填充、线迹布局、层级和气流均会严重影响热耗散。必须在实际运行环境中测试最差的负载情况，以确保温度条件适当。应最大程度地减小热应力，以实现长期正常运行，并使结温远低于 125°C。

注

所有热模型的精度 ≈ 20%。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV401AQRGWRQ1	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV 401Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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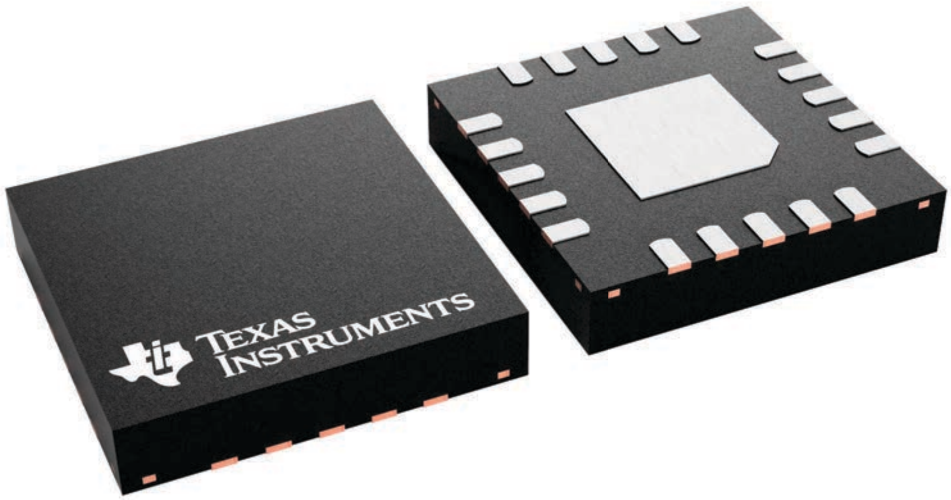
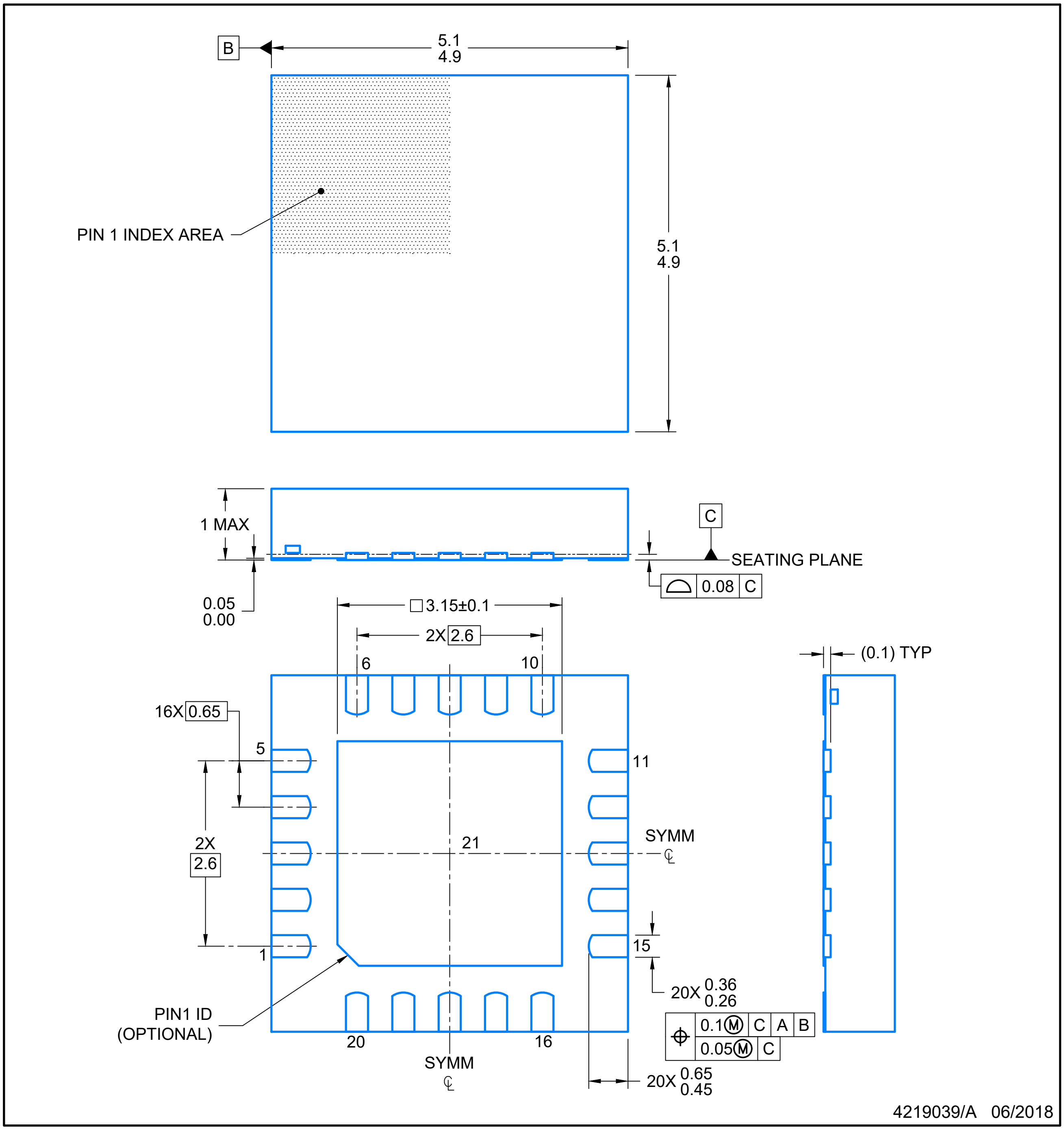
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

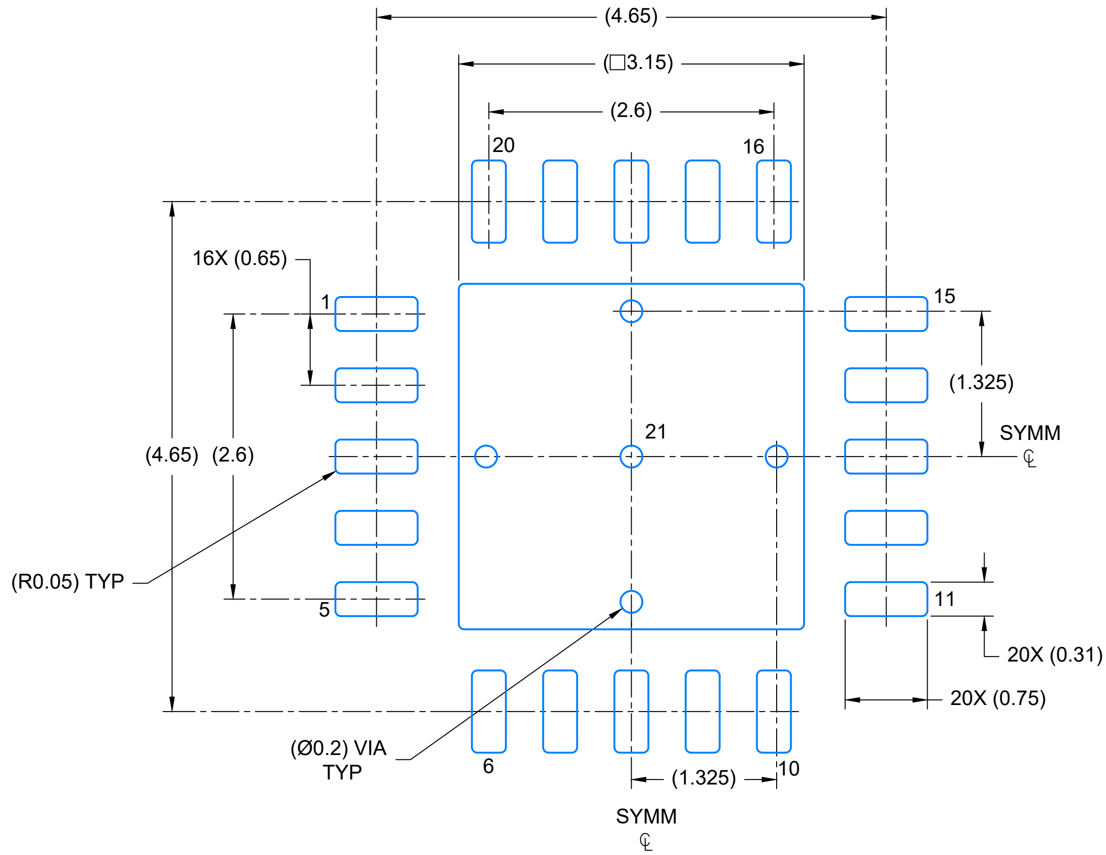


PLASTIC QUAD FLATPACK-NO LEAD

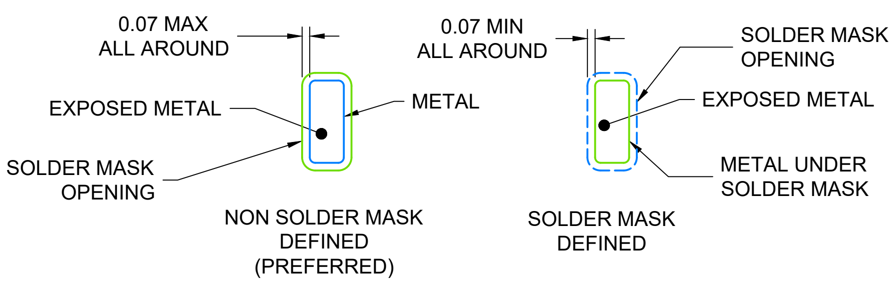


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X



SOLDER MASK DETAILS

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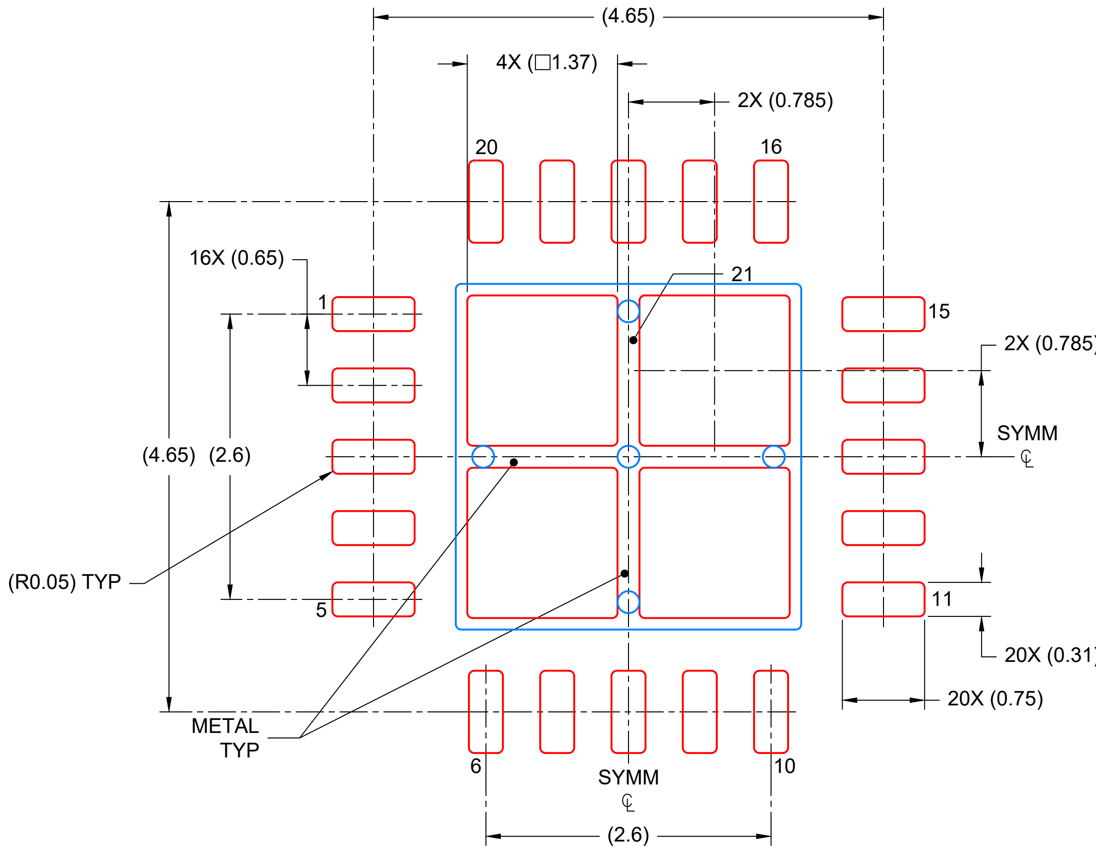
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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