DRV13x Audio-Balanced Line Drivers

1 Features

- Balanced Output
- Low Distortion: 0.0005% at f = 1 kHz
- Wide Output Swing: 17Vrms into 600 Ω
- High Capacitive Load Drive
- High Slew Rate: 15 V/µs
- Wide Supply Range: ±4.5 V to ±18 V
- Low Quiescent Current: ±5.2 mA
- 8-Pin DIP, SO-8, and SOL-16 Packages
- Companion to Audio Differential Line Receivers: INA134 and INA137
- Improved Replacement for SSM2142

2 Applications

- Audio Differential Line Drivers
- Audio Mix Consoles
- Distribution Amplifiers
- Graphic and Parametric Equalizers
- Dynamic Range Processors
- Digital Effects Processors
- Telecom Systems
- Hi-Fi Equipment
- Industrial Instrumentation

3 Description

The DRV134 and DRV135 are differential output amplifiers that convert a single-ended input to a balanced output pair. These balanced audio drivers consist of high performance op amps with on-chip precision resistors. They are fully specified for high performance audio applications and have excellent ac specifications, including low distortion (0.0005% at 1 kHz) and high slew rate (15 V/µs).

The on-chip resistors are laser-trimmed for accurate gain and optimum output common-mode rejection. Wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. They easily drive the large capacitive loads associated with long audio cables. Used in combination with the INA134 or INA137 differential receivers, they offer a complete solution for transmitting analog audio signals without degradation.

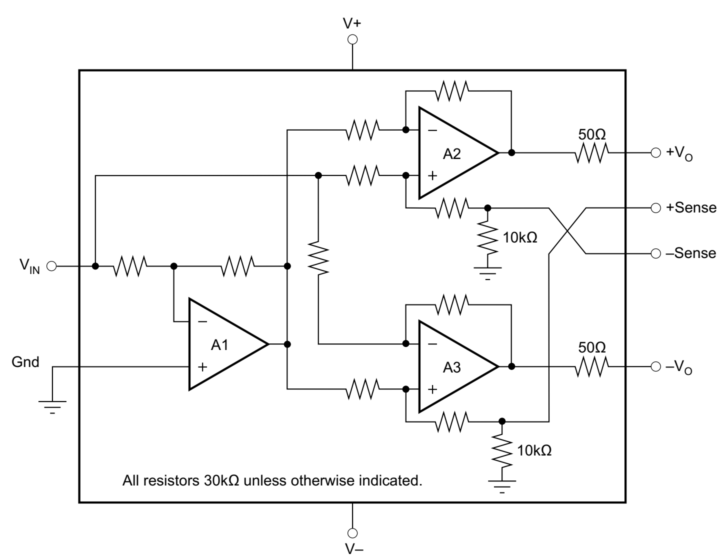
The DRV134 is available in 8-pin DIP and SOL-16 surface-mount packages. The DRV135 comes in a space-saving SO-8 surface-mount package. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C and operate from –55°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV134	SOIC (16)	10.30 mm × 7.50 mm
DRV135	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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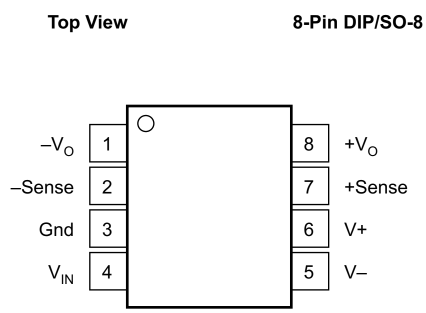
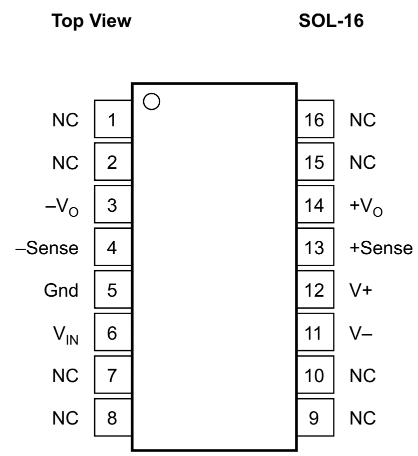
5 Revision History

Changes from Revision A (April 2007) to Revision B — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

6 Pin Configuration and Functions





NOTE: NC - No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DIP-8 and SO-8	SOL-16		
Gnd	3	5	–	Ground
+Sense	7	13	I	Sensing, non-inverting input
–Sense	2	4	I	Sensing, inverting input
V+	6	12	–	Positive supply
V–	5	11	–	Negative supply
V_{IN}	4	6	I	Input
$–V_o$	1	3	O	Inverted, balanced differential output
$+V_o$	8	14	O	Balanced differential output
NC	–	1,2,7,8,9,10,15,16	–	These pins should be left unconnected

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, V+ to V–		40	V
Input voltage range	V–	V+	
Output short-circuit (to ground)		Continuous	
Operating temperature	–55	125	°C
Junction temperature		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_{spe}	Specification temperature range	–40		85	°C
T_A	Operation temperature range	–55		125	°C
V+	Positive supply	4.5	18	18	V
V–	Negative supply	–4.5	–18	–18	V

7.4 Electrical Characteristics

At T_A = +25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total Harmonic Distortion + Noise	f = 20Hz to 20kHz, V_O = 10Vrms		0.001%		
		f = 1kHz, V_O = 10Vrms		0.0005%		
RTO(1)	Noise Floor	20 kHz BW		–98		dBu
RTO(1)	Headroom	THD+N < 1%		27		dBu
INPUT						
Z_{IN}	Input Impedance(2)			10		kΩ
I_{IN}	Input Current	V_{IN} = ±7.07 V	–1000	±700	1000	µA
GAIN						
	Differential	$[(+V_O) – (–V_O)]/V_{IN}$, V_{IN} = ±10V				
	Initial		5.8	6		dB
	Error		–2%	±0.1%	2%	
	Error vs Temperature			±10		ppm/°C
	Single-Ended	V_{IN} = ±5V				
	Initial		5.8	6		dB
	Error		–2%	±0.7%	2%	
	Error vs Temperature			±10		ppm/°C
	Nonlinearity			0.0003		% of FS
OUTPUT						
OCMR	Common-Mode Rejection, f = 1kHz	See Figure 25	46	68		dB
SBR	Signal Balance Ratio, f = 1kHz	See Figure 26	35	54		dB
	Output Offset Voltage					
V_{OCM}(3)	Offset Voltage, Common-Mode	V_{IN} = 0	–250	±50	250	mV
	Offset Voltage, Common-Mode vs Temperature			±150		µV/°C
V_{OD}(4)	Offset Voltage, Differential	V_{IN} = 0	–10	±1	10	mV
	Offset Voltage, Differential vs Temperature			±5		µV/°C
PSRR	Offset Voltage, Differential vs Power Supply	V_S = ±4.5V to ±18V	80	110		dB
	Output Voltage Swing, Positive	No Load(5)	(V+) – 3	(V+) – 2.5		V
	Output Voltage Swing, Negative	No Load(5)	(V–) + 2	(V–) + 1.5		V
	Impedance			50		Ω
C_L	Load Capacitance, Stable Operation	C_L Tied to Ground (each output)		1		µF
I_{SC}	Short-Circuit Current			±85		mA
FREQUENCY RESPONSE						
	Small-Signal Bandwidth			1.5		MHz
SR	Slew Rate			15		V/µs
	Settling Time: 0.01%	V_{OUT} = 10V Step		2.5		µs
	Overload Recovery	Output Overdriven 10%		3		µs
POWER SUPPLY						
V_S	Rated Voltage			±18		V
	Voltage Range		±4.5		±18	V
I_Q	Quiescent Current	I_O = 0	–5.5	±5.2	5.5	mA

(1) dBu = 20log (Vrms /0.7746); RTO = Referred-to-Output.
(2) Resistors are ratio matched but have ±20% absolute value.
(3) $V_{OCM} = [(+V_O) + (–V_O)] / 2$.
(4) $V_{OD} = (+V_O) – (–V_O)$.
(5) Ensures linear operation. Includes common-mode offset.

Electrical Characteristics (continued)

At T_A = +25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE							
	Specification Range			–40		85	°C
	Operation Range			–55		125	°C
	Storage Range			–55		125	°C
θ_{JA}	Thermal Resistance	8-Pin DIP			100		°C/W
		SO-8 Surface mount			150		°C/W
		SOL-16 Surface mount			80		°C/W

7.5 Typical Characteristics

At T_A = 25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

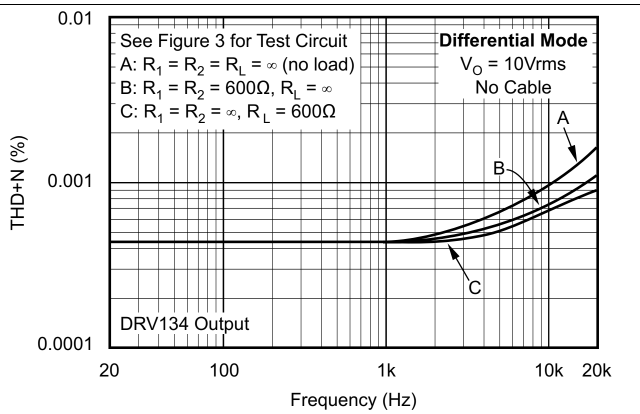


Figure 1. Total Harmonic Distortion + Noise vs Frequency

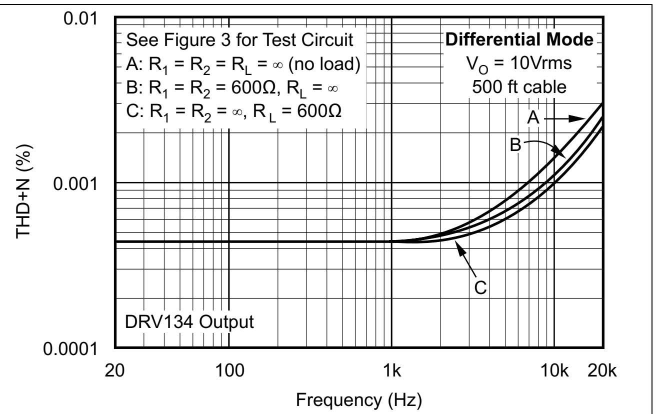


Figure 2. Total Harmonic Distortion + Noise vs Frequency

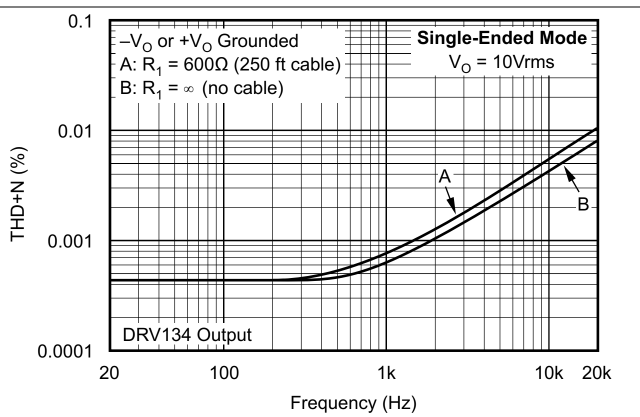


Figure 3. Total Harmonic Distortion + Noise vs Frequency

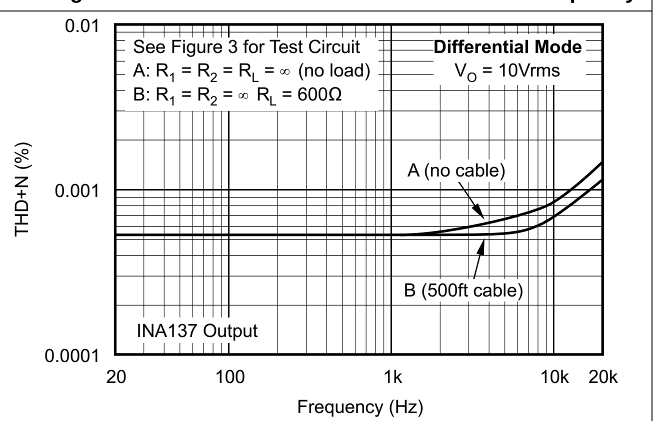


Figure 4. System Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

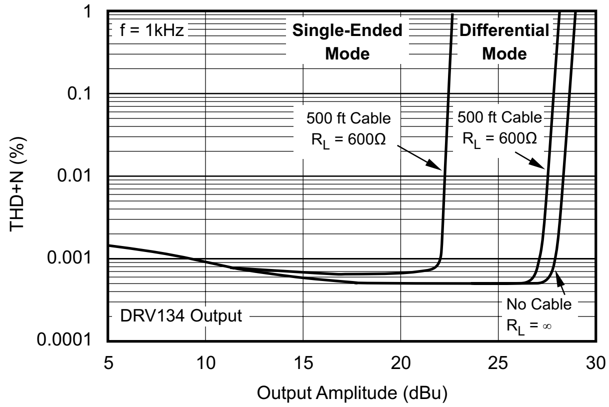


Figure 5. Headroom – Total Harmonic Distortion + Noise vs Output Amplitude

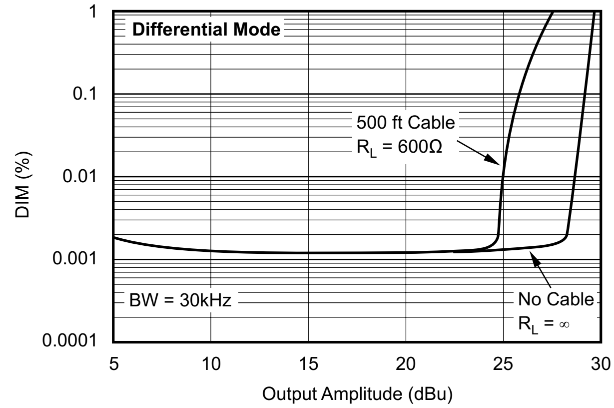


Figure 6. Dim Intermodulation Distortion vs Output Amplitude

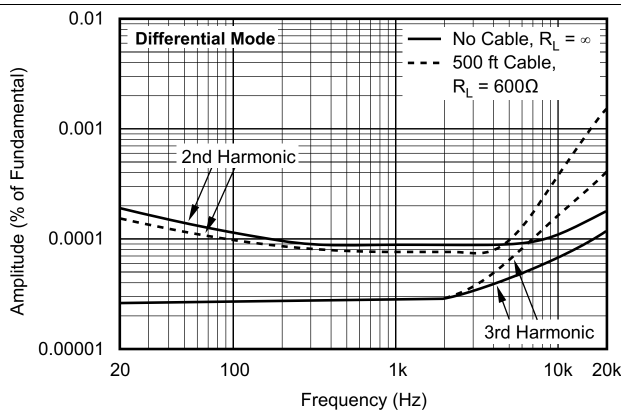


Figure 7. Harmonic Distortion Products vs Frequency

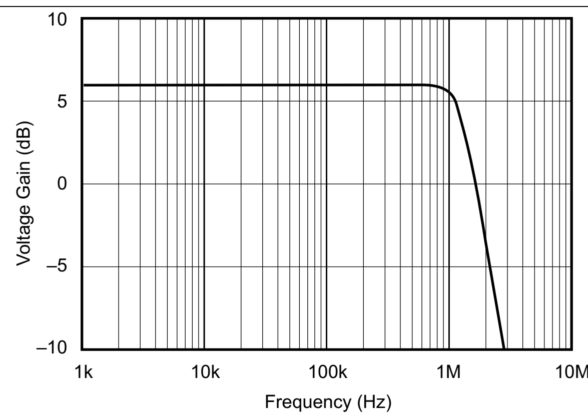


Figure 8. Gain vs Frequency

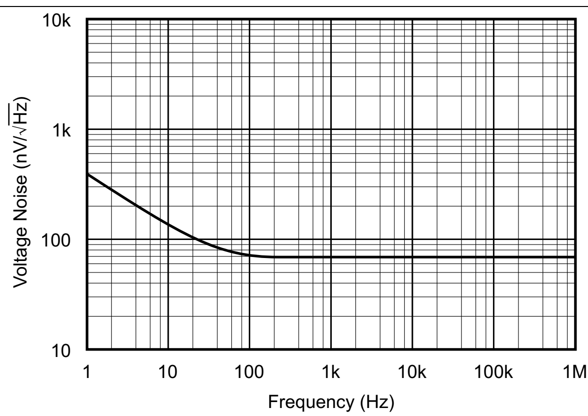


Figure 9. Output Voltage Noise Spectral Density vs Frequency

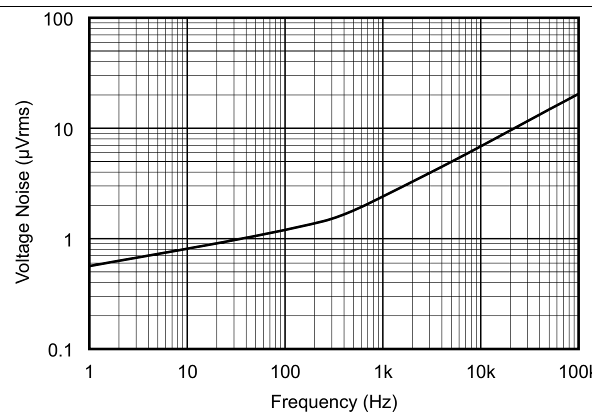


Figure 10. Output Voltage Noise vs Noise Bandwidth

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

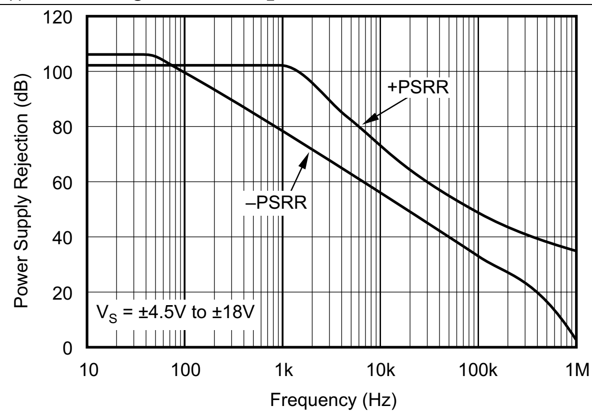


Figure 11. Power Supply Rejection vs Frequency

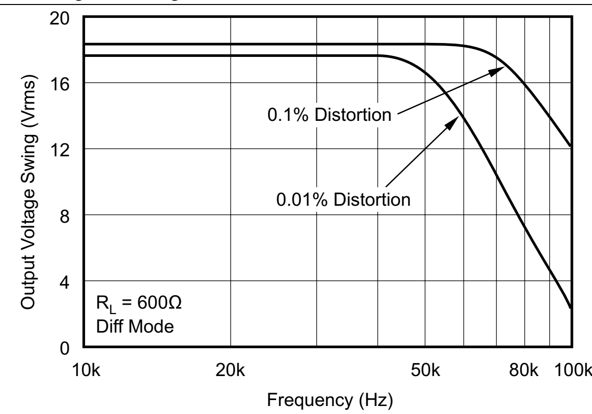


Figure 12. Maximum Output Voltage Swing vs Frequency

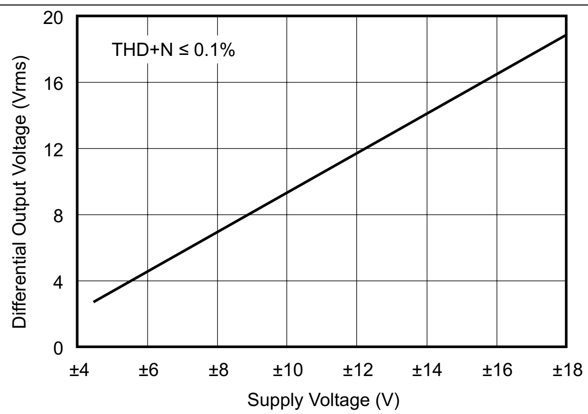


Figure 13. Output Voltage Swing vs Supply Voltage

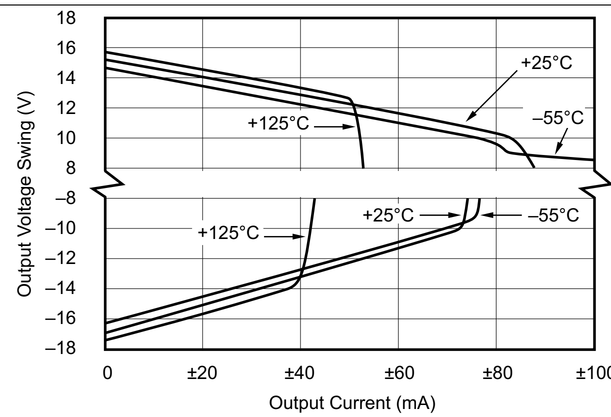


Figure 14. Output Voltage Swing vs Output Current

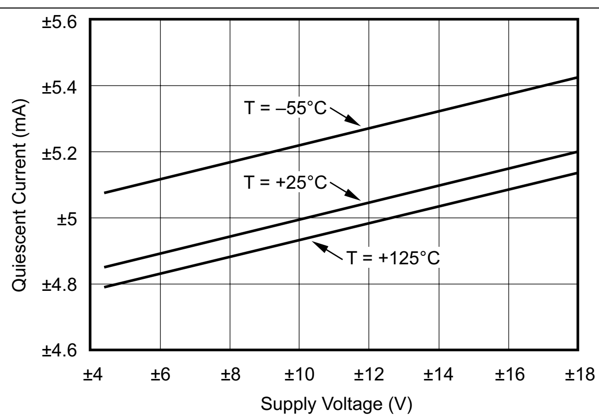


Figure 15. Quiescent Current vs Supply Voltage

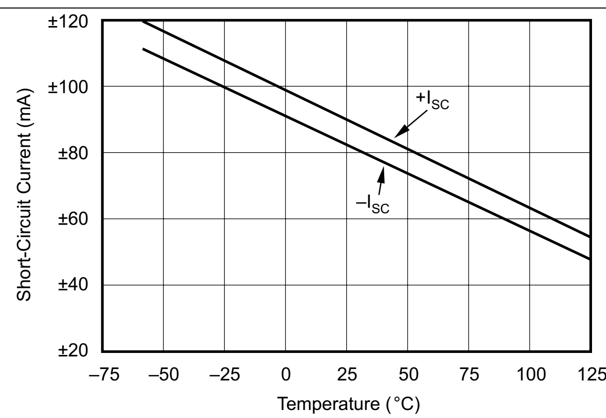


Figure 16. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

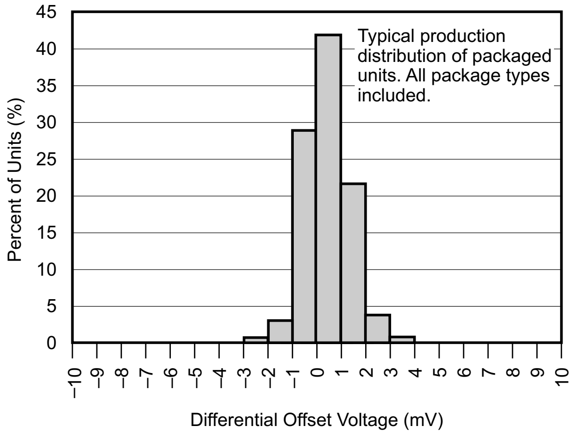


Figure 17. Differential Offset Voltage Production Distribution

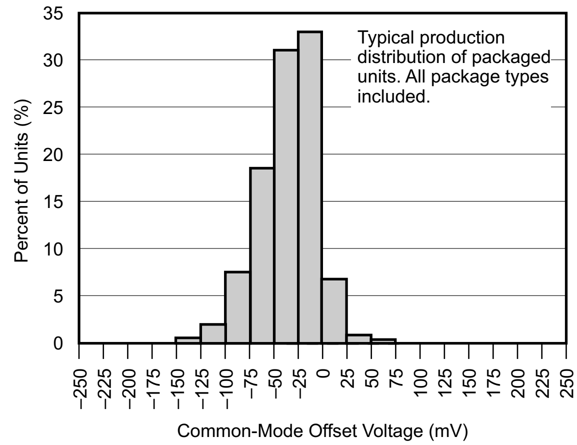
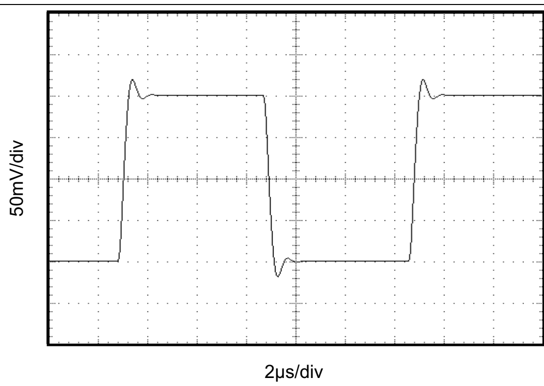
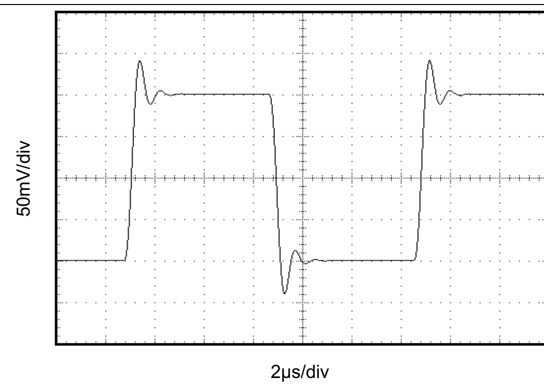


Figure 18. Common-Mode Offset Voltage Production Distribution



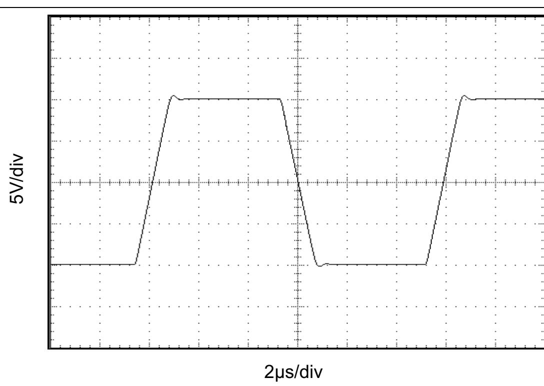
C_L = 100 pF

Figure 19. Small-Signal Step Response



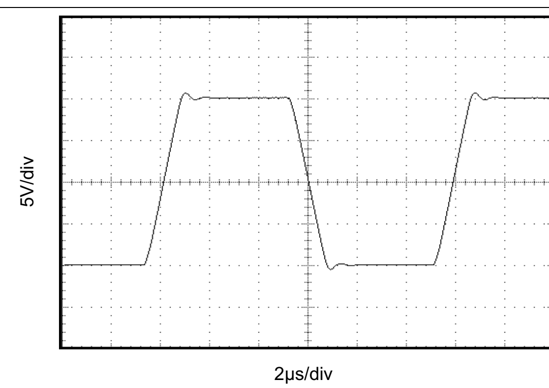
C_L = 1000 pF

Figure 20. Small-Signal Step Response



C_L = 100 pF

Figure 21. Large-Signal Step Response



C_L = 1000 pF

Figure 22. Large-Signal Step Response

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 600 Ω differential connected between $+V_O$ and $–V_O$, unless otherwise noted.

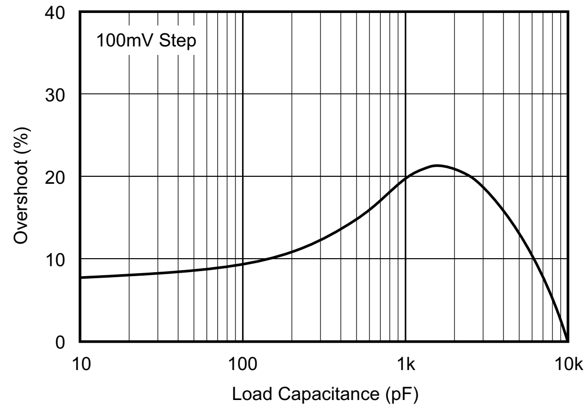


Figure 23. Small-Signal Step Overshoot vs Load Capacitance

8 Detailed Description

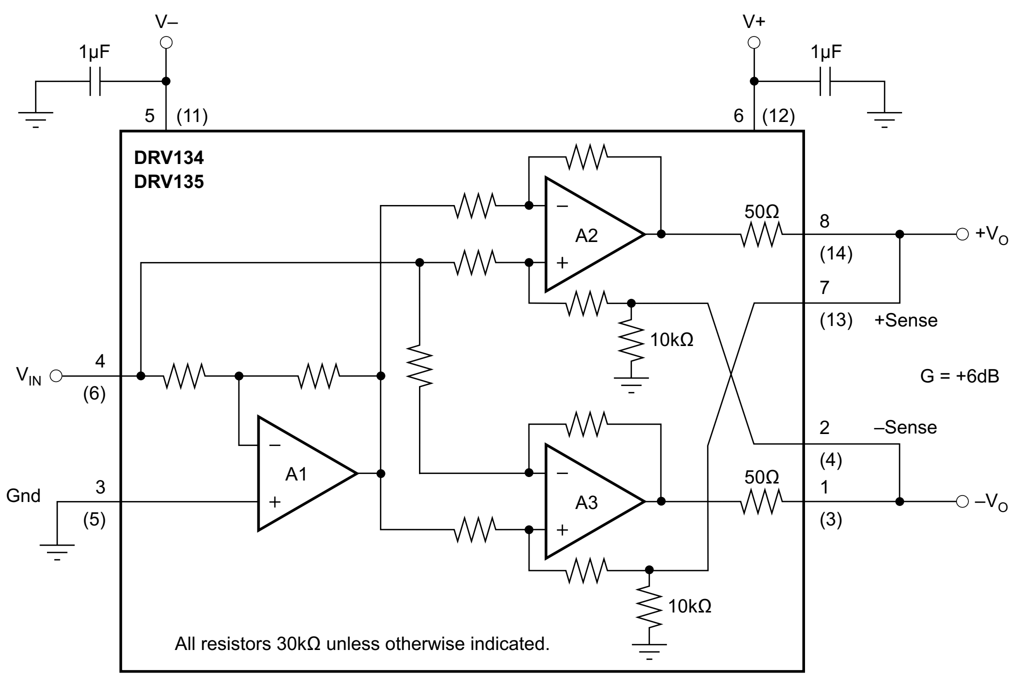
8.1 Overview

The DRV134 and DRV135 consist of an input inverter driving a cross- coupled differential output stage with 50 Ω series output resistors. Characterized by low differential-mode output impedance (50 Ω) and high common-mode output impedance (1.6 kΩ), the DRV134 and DRV135 are ideal for audio applications.

Excellent internal design and layout techniques provide low signal distortion, high output level (27 dBu), and a low noise floor (–98 dBu). Laser trimming of thin film resistors assures excellent output common-mode rejection (OCMR) and signal balance ratio (SBR). In addition, low dc voltage offset reduces errors and minimizes load currents.

The *Functional Block Diagram* section shows a detailed block diagram of the DRV134 and DRV135.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Audio Performance

The DRV134 and DRV135 were designed for enhanced ac performance. Very low distortion, low noise, and wide bandwidth provide superior performance in high quality audio applications. Laser-trimmed matched resistors provide optimum output common-mode rejection (typically 68dB), especially when compared to circuits implemented with op amps and discrete precision resistors. In addition, high slew rate (15 V/μs) and fast settling time (2.5 μs to 0.01%) ensure excellent dynamic response.

The DRV134 and DRV135 have excellent distortion characteristics. As shown in the distortion data provided in the *Typical Characteristics* section, THD+Noise is below 0.003% throughout the audio frequency range under various output conditions. Both differential and single-ended modes of operation are shown. In addition, the optional 10μF blocking capacitors used to minimize V_{OCM} errors have virtually no effect on performance. Measurements were taken with an Audio Precision System One (with the internal 80 kHz noise filter) using the THD test circuit shown in Figure 24.

Feature Description (continued)

Up to approximately 10 kHz, distortion is below the measurement limit of commonly used test equipment. Furthermore, distortion remains relatively constant over the wide output voltage swing range (approximately 2.5 V from the positive supply and 1.5 V from the negative supply). A special output stage topology yields a design with minimum distortion variation from lot-to-lot and unit-to-unit. Furthermore, the small and large signal transient response curves demonstrate the stability under load of the DRV134 and DRV135.

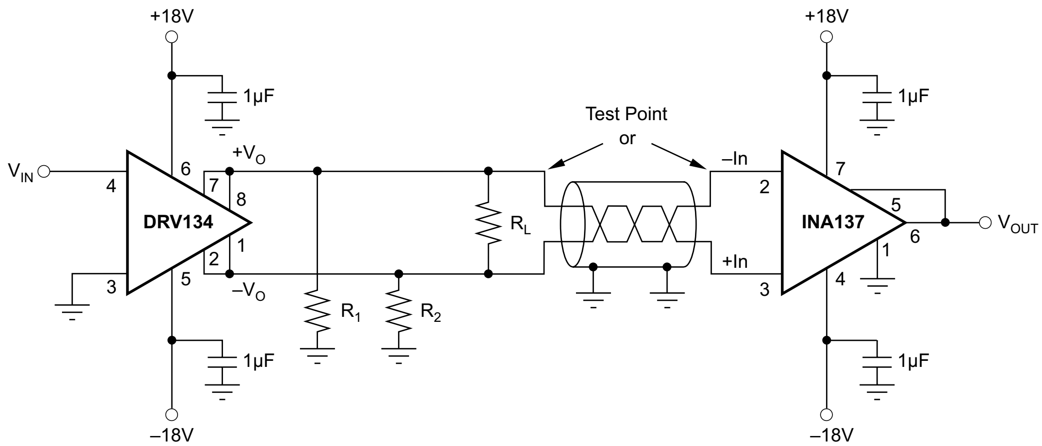


Figure 24. Distortion Test Circuit

8.3.2 Output Common-Mode Rejection

Output common-mode rejection (OCMR) is defined as the change in differential output voltage due to a change in output common-mode voltage. When measuring OCMR, V_{IN} is grounded and a common-mode voltage, VCM, is applied to the output as shown in Figure 25. Ideally no differential mode signal (VOD) should appear. However, a small mode-conversion effect causes an error signal whose magnitude is quantified by OCMR.

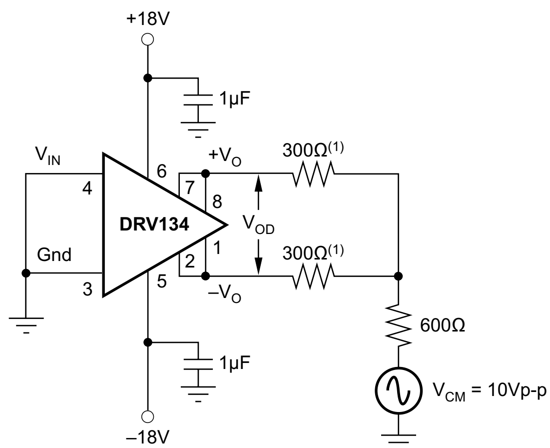


Figure 25. Output Common-Mode Rejection Test Circuit

8.3.3 Signal Balance Ratio

Signal balance ratio (SBR) measures the symmetry of the output signals under loaded conditions. To measure SBR an input signal is applied and the outputs are summed as shown in Figure 26. V_{OUT} should be zero since each output ideally is exactly equal and opposite. However, an error signal results from any imbalance in the outputs. This error is quantified by SBR. The impedances of the DRV134 and DRV135's output stages are closely matched by laser trimming to minimize SBR errors. In an application, SBR also depends on the balance of the load network.

Feature Description (continued)

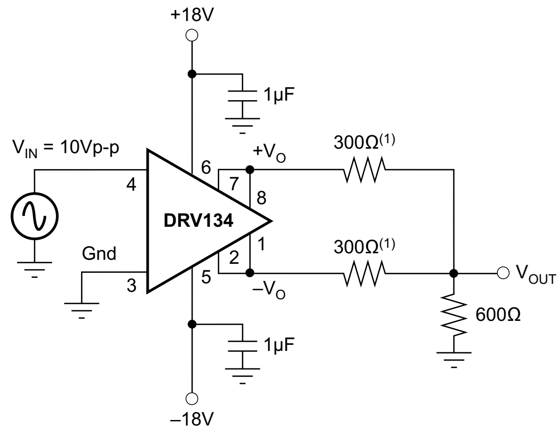


Figure 26. Signal Balance Ratio Test Circuit

8.4 Device Functional Modes

8.4.1 Differential-Output Mode

In differential-output mode, the DRV134 (and DRV135 in SO-8 package) converts a single-ended, ground-referenced input to a floating differential output with +6 dB gain (G = 2). Figure 27 shows the basic connections required for operation in differential-output mode.

Normally, +V_O is connected to +Sense, –V_O is connected to –Sense, and the outputs are taken from these junctions as shown in Figure 27.

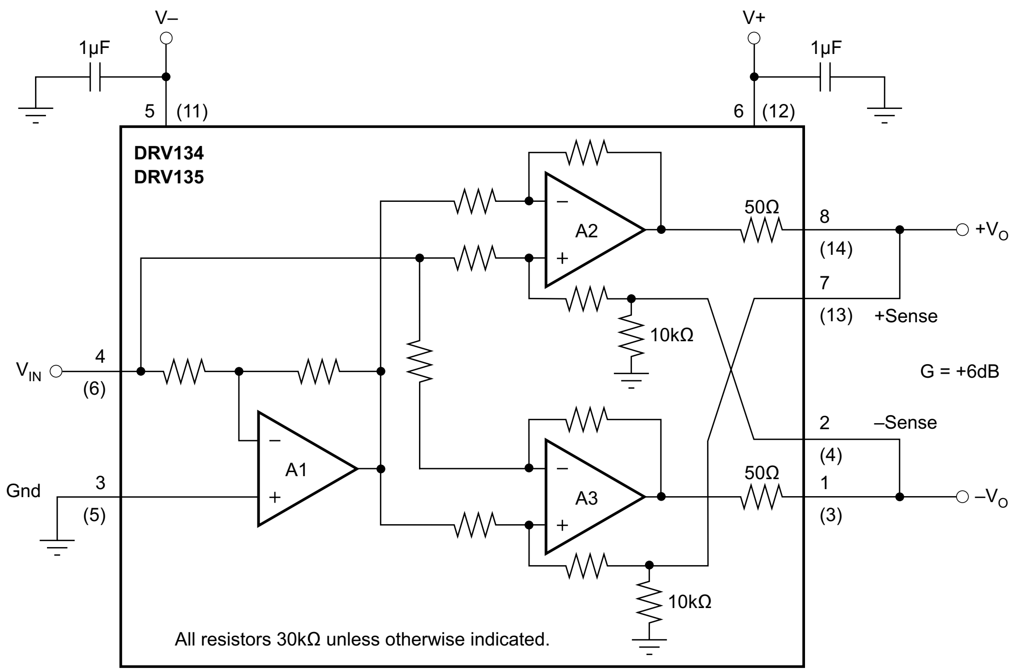


Figure 27. Basic Connections for Differential-Output Mode

Device Functional Modes (continued)

8.4.2 Single-Ended Mode

The DRV134 can be operated in single-ended mode without degrading output drive capability. Single-ended operation requires that the unused side of the output pair be grounded (both the V_O and Sense pins) to a low impedance return path. Gain remains +6 dB. Grounding the negative outputs as shown in Figure 28 results in a non-inverted output signal (G = +2) while grounding the positive outputs gives an inverted output signal (G = –2).

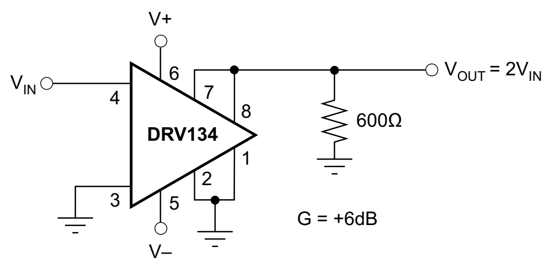


Figure 28. Typical Single-Ended Application

For best rejection of line noise and hum differential mode operation is recommended. However, single-ended performance is adequate for many applications. In general single ended performance is comparable to differential mode (see THD+N typical performance curves), but the common mode and noise rejection inherent in balanced-pair systems is lost.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Decoupling capacitors placed close to the device pins are strongly recommended in applications with noisy or high impedance power supplies.

For best system performance, it is recommended that a high input-impedance difference amplifier be used as the receiver. Used with the INA134 (G = 0 dB) or the INA137 (G = ±6 dB) differential line receivers, the DRV134 forms a complete solution for driving and receiving audio signals, replacing input and output coupling transformers commonly used in professional audio systems (Figure 29). When used with the INA137 (G = –6 dB) overall system gain is unity.

9.2 Typical Application

9.2.1 Cable Driving Application

The DRV134 is capable of driving large signals into 600-Ω loads over long cables. Low impedance shielded audio cables such as the standard Belden 8451 or 9452 (or similar) are recommended, especially in applications where long cable lengths are required.

For applications with large dc cable offset errors, a 10-µF electrolytic nonpolarized blocking capacitor at each sense pin is recommended as shown in Figure 29.

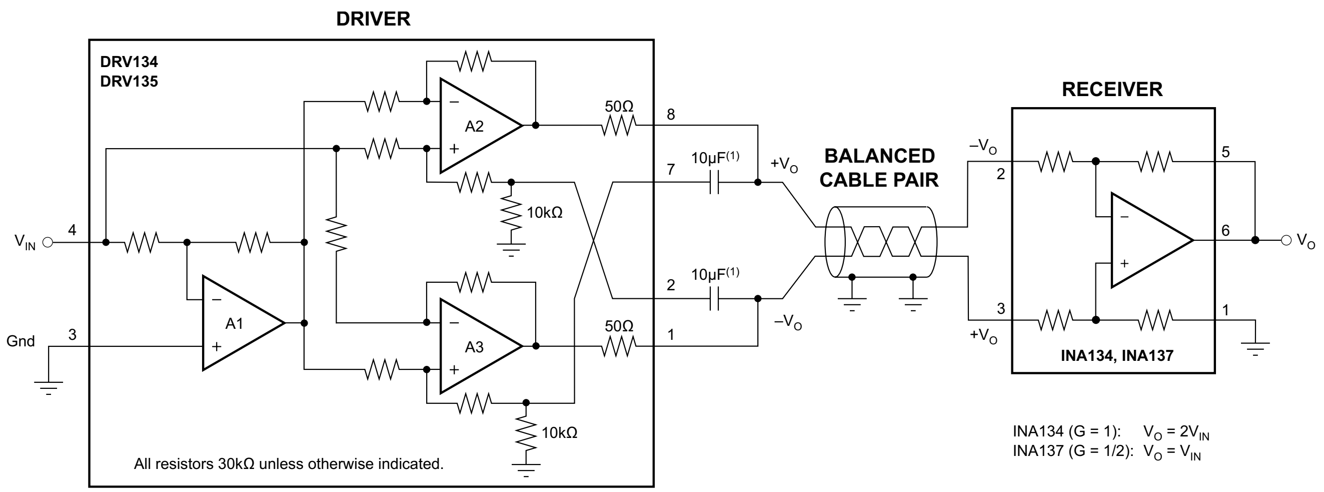


Figure 29. Complete Audio Driver and Receiver Circuit

9.2.1.1 Design Requirements

Consider a design with the goal of differentially transmitting a single ended signal of up to 22.2 dBu through 500 ft of cable with no load at the receiving side. The signal at the end of the cable should have no more than 0.002 percent of total harmonic distortion plus noise (THD+N) at 10 kHz and less than 0.0005 percent of THD+N for frequencies between 20 Hz and 1 kHz.

The system is required to put out a single ended signal 0 dB with respect to the input signal and accommodate inputs with peak to RMS ratios of up to 1.5 for the maximum 22.2 dBu range established above.

Typical Application (continued)

9.2.1.2 Detailed Design Procedure

The dBu is a common unit of measurement for input sensitivity and output level of professional audio equipment. A 0 dBu signal dissipates 1 mW into a 600-Ω resistive load; therefore, a 0 dBu signal corresponds to approximately 0.775 V_{RMS}. Equation 1 shows the relationship between the signal level in dBu (denoted by L_u) and the signal level in V_{RMS} (denoted by x).

$$L_u = 20\log_{10}\left(\frac{x}{0.775}\right) \quad (1)$$

For this design, the single ended input signal of 22.2 dBu corresponds to 9.98 V_{RMS} as shown in Equation 2.

$$V_{IN} = 0.775\left(10^{\frac{L_u}{20}}\right) = 9.98\ V_{RMS} \quad (2)$$

Given that the system must accommodate for 22.2 dBu signals with up to 1.5 of peak to RMS ratio, the maximum peak input signal is 14.97 V_{PEAK} as calculated in Equation 3.

$$V_{IN\_PEAK} = 1.5(9.98) = 14.97\ V_{PEAK} \quad (3)$$

The DRV134 is chosen to convert the single ended input signal into a differential signal and the outputs of the DRV134 will be connected to one end of the 500 ft cable. In order to prevent clipping and distortion of the input signal, the power supply rails for the DRV134 are chosen as 3 V above and below the peak calculated in Equation 3. The 3 V margin is derived from the output voltage swing specification given in the *Electrical Characteristics* table. The supplies selected are 18 V for V+ and –18 V for V–.

Finally, the INA137 is used at the end of the 500 ft cable in order to convert the differential signal output of the DRV134 into a single ended signal that is 0 dB with respect to the input signal.

Figure 30 shows the system diagram.

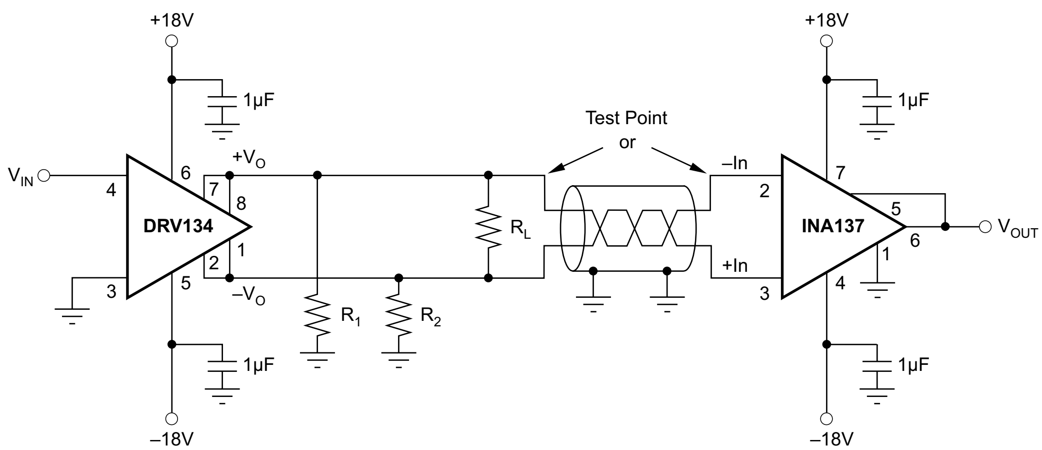


Figure 30. Diagram of System Based on DRV134 and INA137

Typical Application (continued)

9.2.1.3 Application Curve

Figure 31 shows the performance obtained with the system depicted in Figure 30.

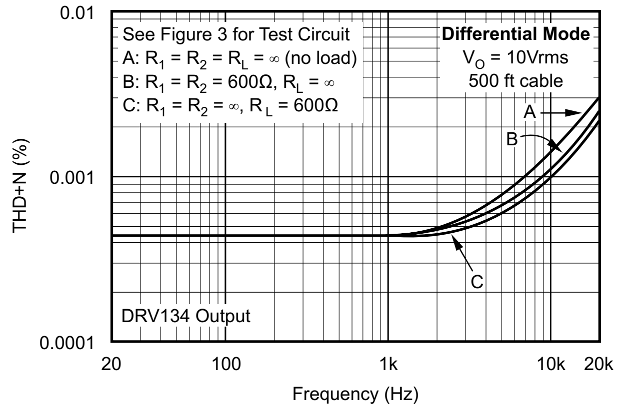


Figure 31. Measured Performance of a System Based on DRV134

10 Power Supply Recommendations

The DRV134 and DRV135 are designed to operate from an input voltage supply range between ±4.5 V and ±18 V. This input supply should be well regulated. If the input supply is located more than a few inches from the DRV134 or DRV135 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

A driver/receiver balanced-pair (such as the DRV134 and INA137) rejects the voltage differences between the grounds at each end of the cable, which can be caused by ground currents, supply variations, etc. In addition to proper bypassing (as shown in Figure 32 and Figure 33), the suggestions below should be followed to achieve optimal OCMR and noise rejection.

- The DRV134 input should be driven by a low impedance source such as an op amp or buffer.
- As is the case for any single-ended system, the source’s common should be connected as close as possible to the DRV134’s ground. Any ground offset errors in the source will degrade system performance.
- Symmetry on the outputs should be maintained.
- Shielded twisted-pair cable is recommended for all applications. Physical balance in signal wiring should be maintained. Capacitive differences due to varying wire lengths may result in unequal noise pickup between the pair and degrade OCMR. Follow industry practices for proper system grounding of the cables.

11.2 Layout Examples

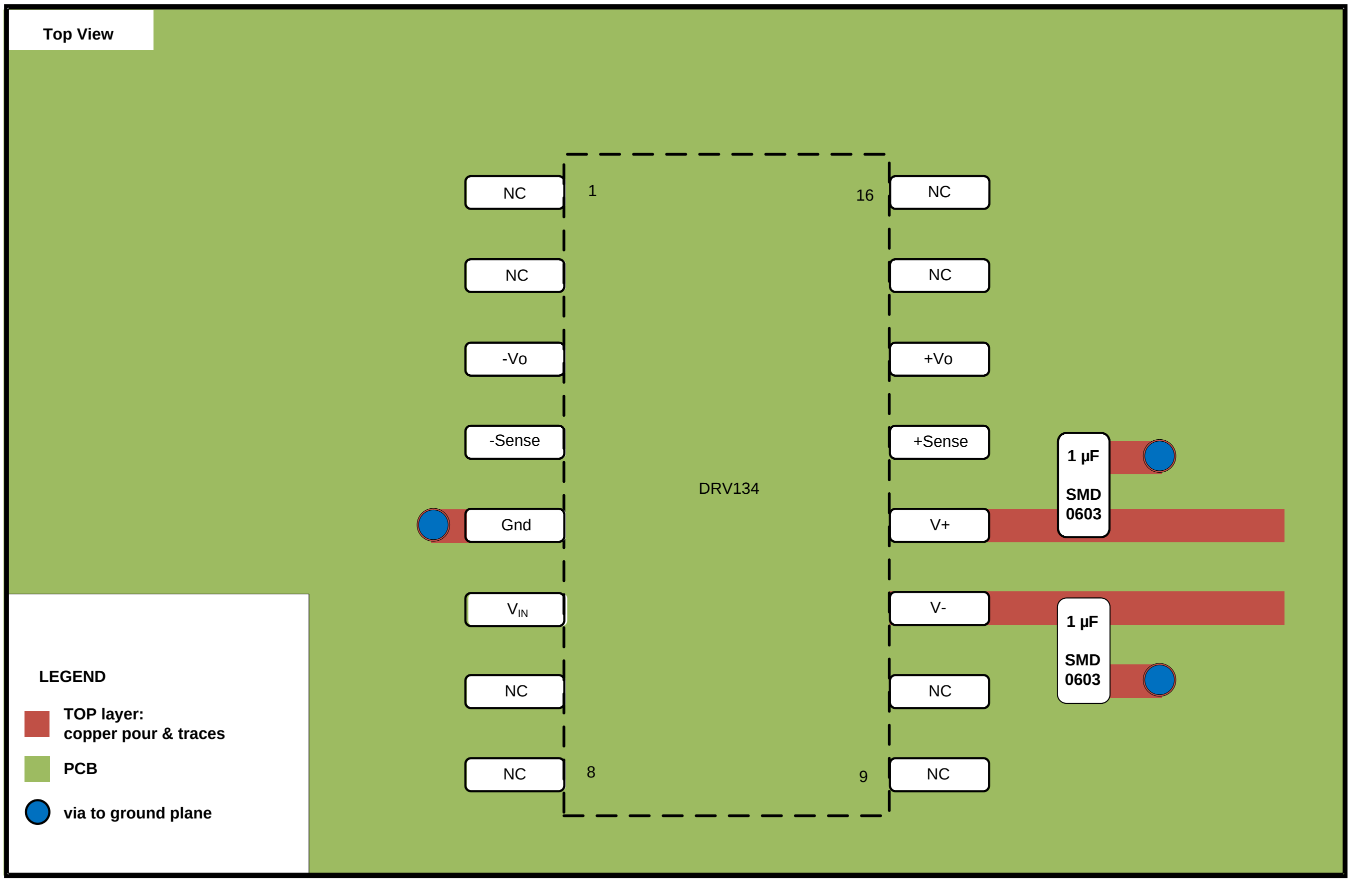


Figure 32. DRV134 Layout Example

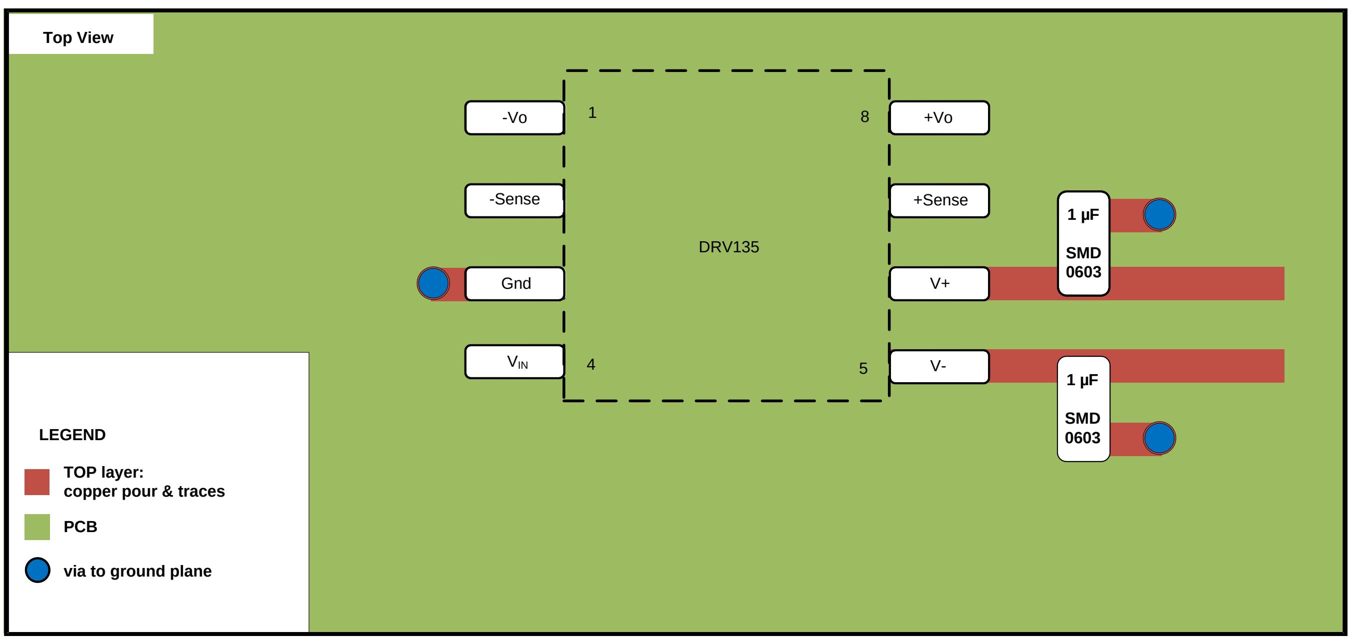


Figure 33. DRV135 Layout Example

11.3 Thermal Performance

The DRV134 and DRV135 have robust output drive capability and excellent performance over temperature. In most applications there is no significant difference between the DIP, SOL-16, and SO-8 packages. However, for applications with extreme temperature and load conditions, the SOL-16 (DRV134UA) or DIP (DRV134PA) packages are recommended. Under these conditions, such as loads greater than 600 Ω or very long cables, performance may be degraded in the SO-8 (DRV135UA) package.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Audio Differential Line Receivers 0dB (G = 1)*, INA134
- *Audio Differential Line Receivers ±6dB (G = 1/2 or 2)*, INA137

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV134	Click here	Click here	Click here	Click here	Click here
DRV135	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV134PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	DRV134PA
DRV134PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	DRV134PA
DRV134UA	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV134UA
DRV134UA.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV134UA
DRV134UA/1K	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV134UA
DRV134UA/1K.A	Active	Production	SOIC (DW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV134UA
DRV135UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV 135UA
DRV135UA.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV 135UA
DRV135UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV 135UA
DRV135UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV 135UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

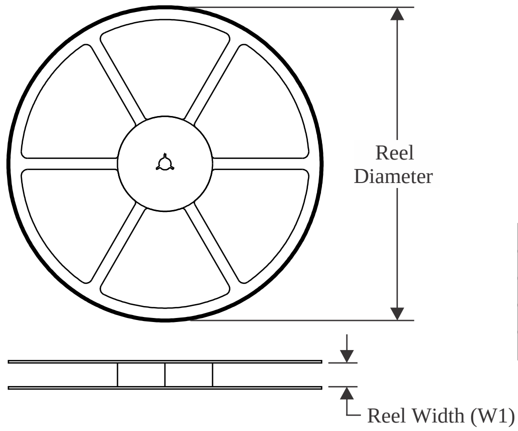
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

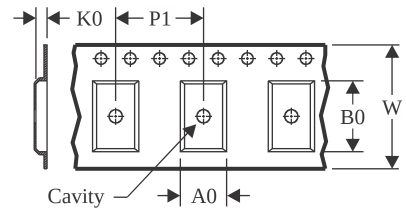
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

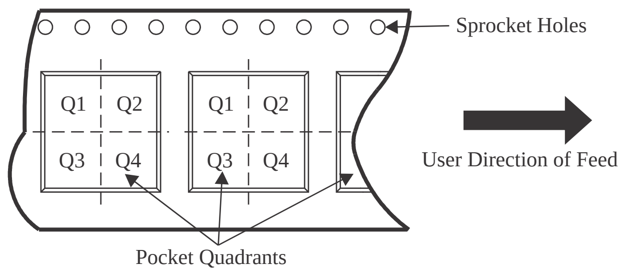


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

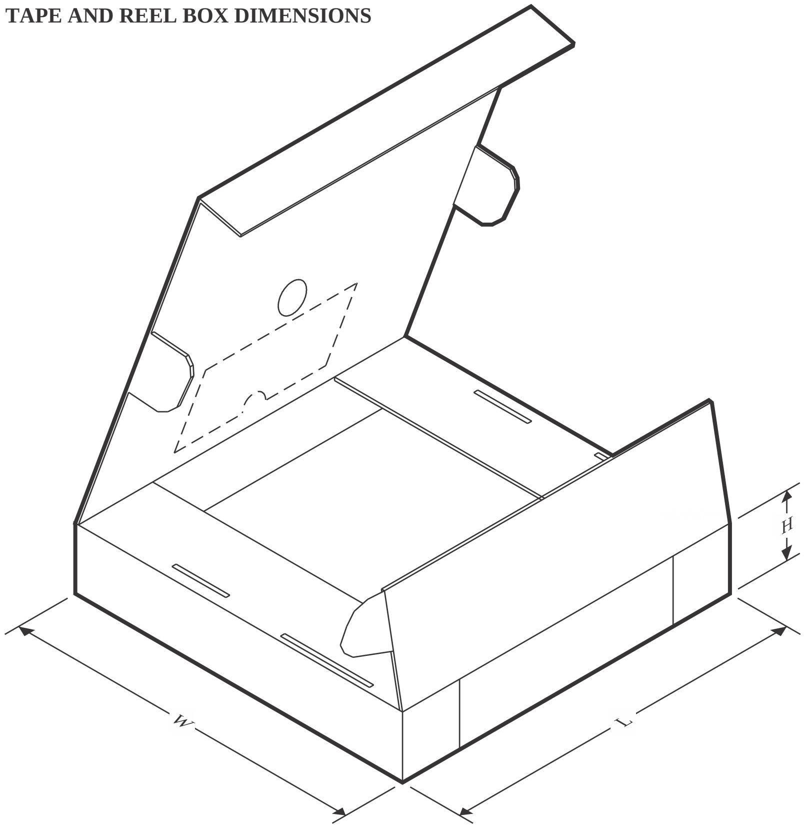
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV134UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
DRV135UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

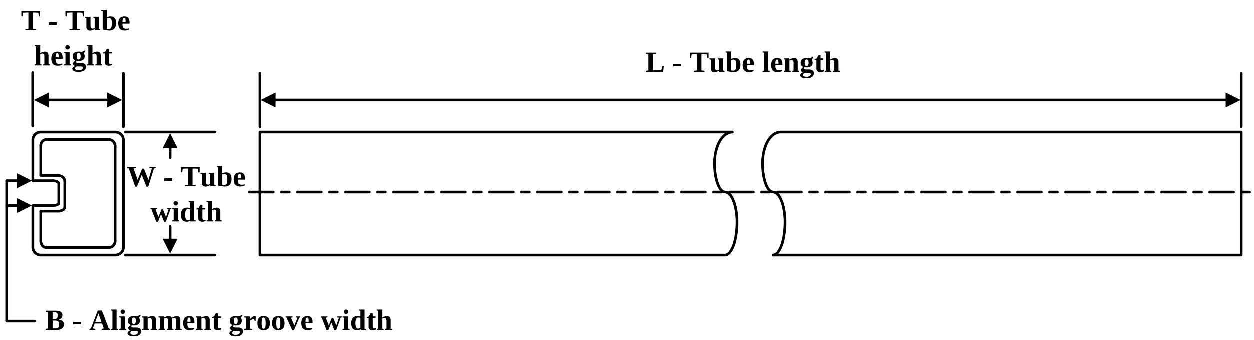
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV134UA/1K	SOIC	DW	16	1000	353.0	353.0	32.0
DRV135UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

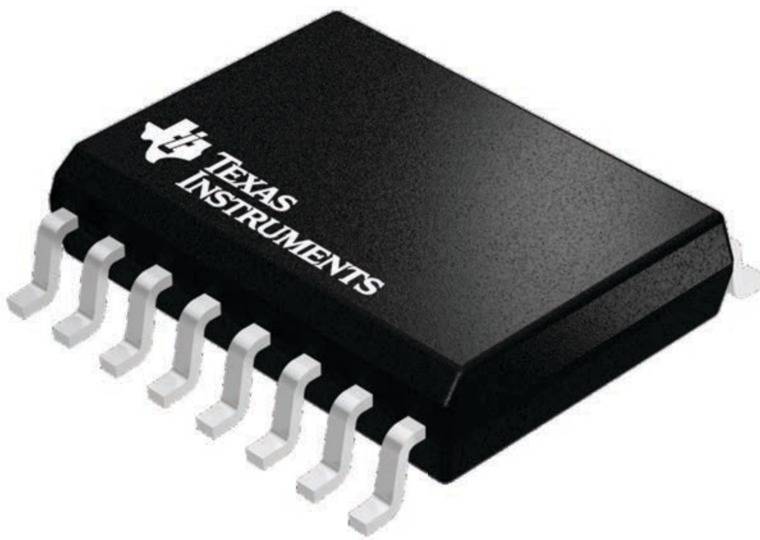
TUBE

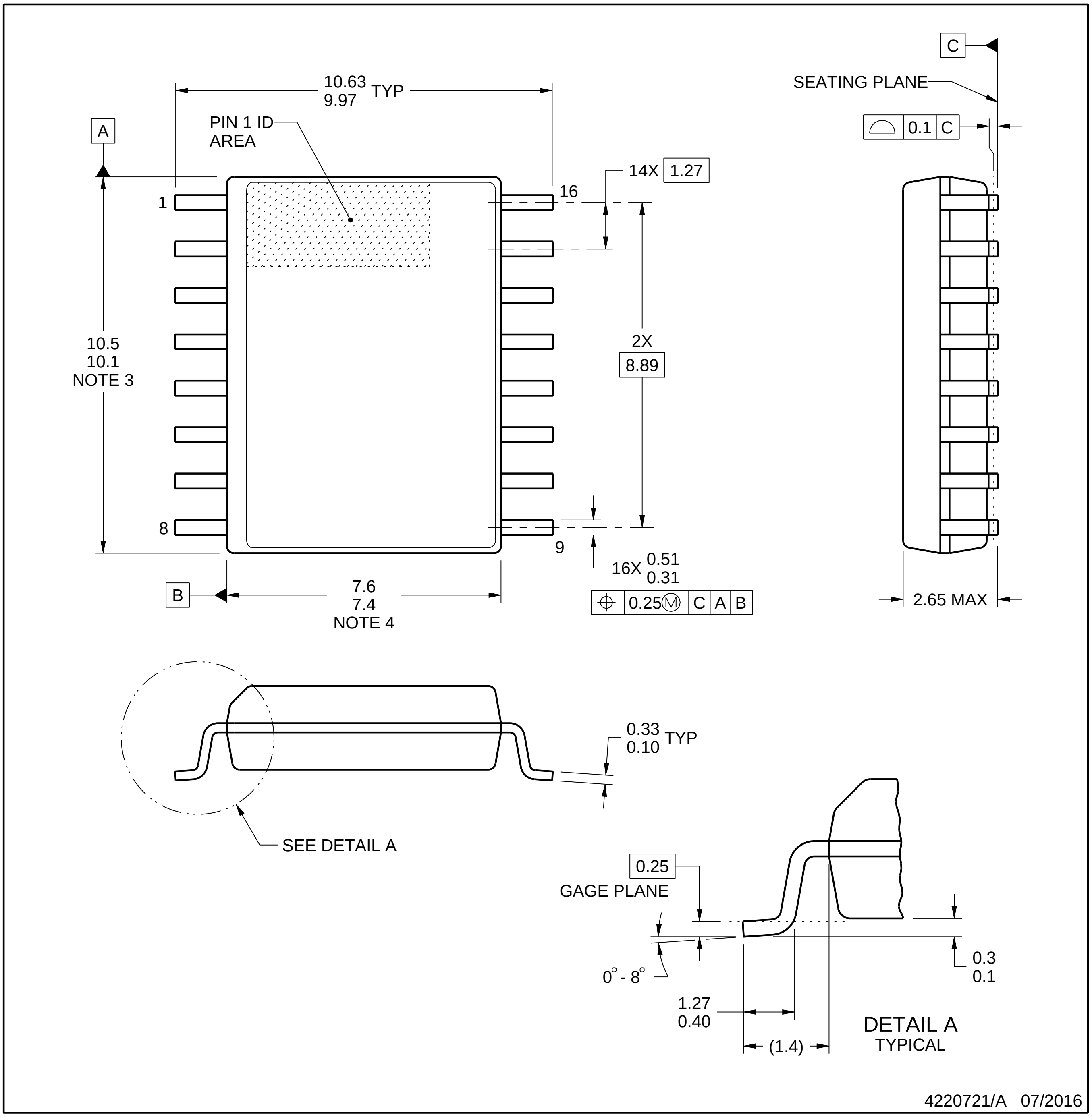


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV134PA	P	PDIP	8	50	506	13.97	11230	4.32
DRV134PA.A	P	PDIP	8	50	506	13.97	11230	4.32
DRV134UA	DW	SOIC	16	40	507	12.83	5080	6.6
DRV134UA.A	DW	SOIC	16	40	507	12.83	5080	6.6
DRV135UA	D	SOIC	8	75	506.6	8	3940	4.32
DRV135UA.A	D	SOIC	8	75	506.6	8	3940	4.32

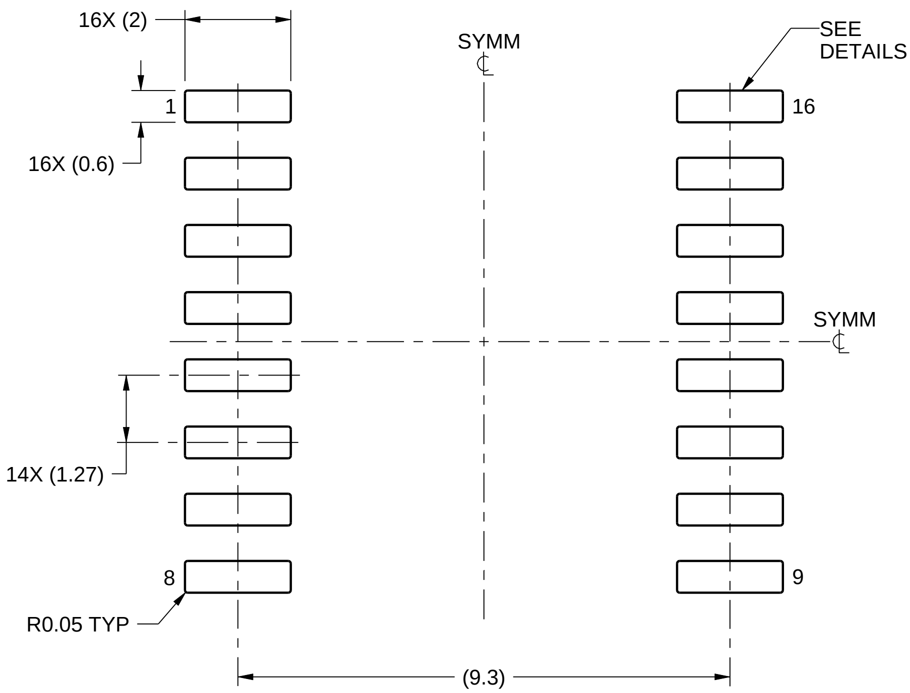
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



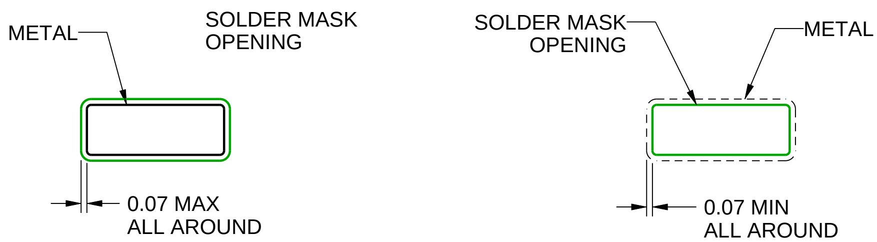


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK DEFINED

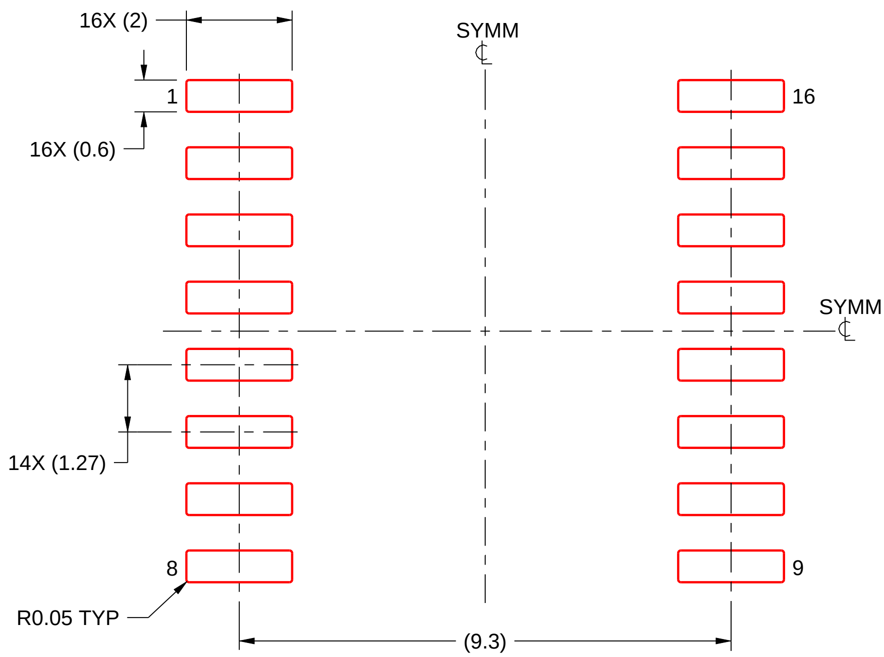
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

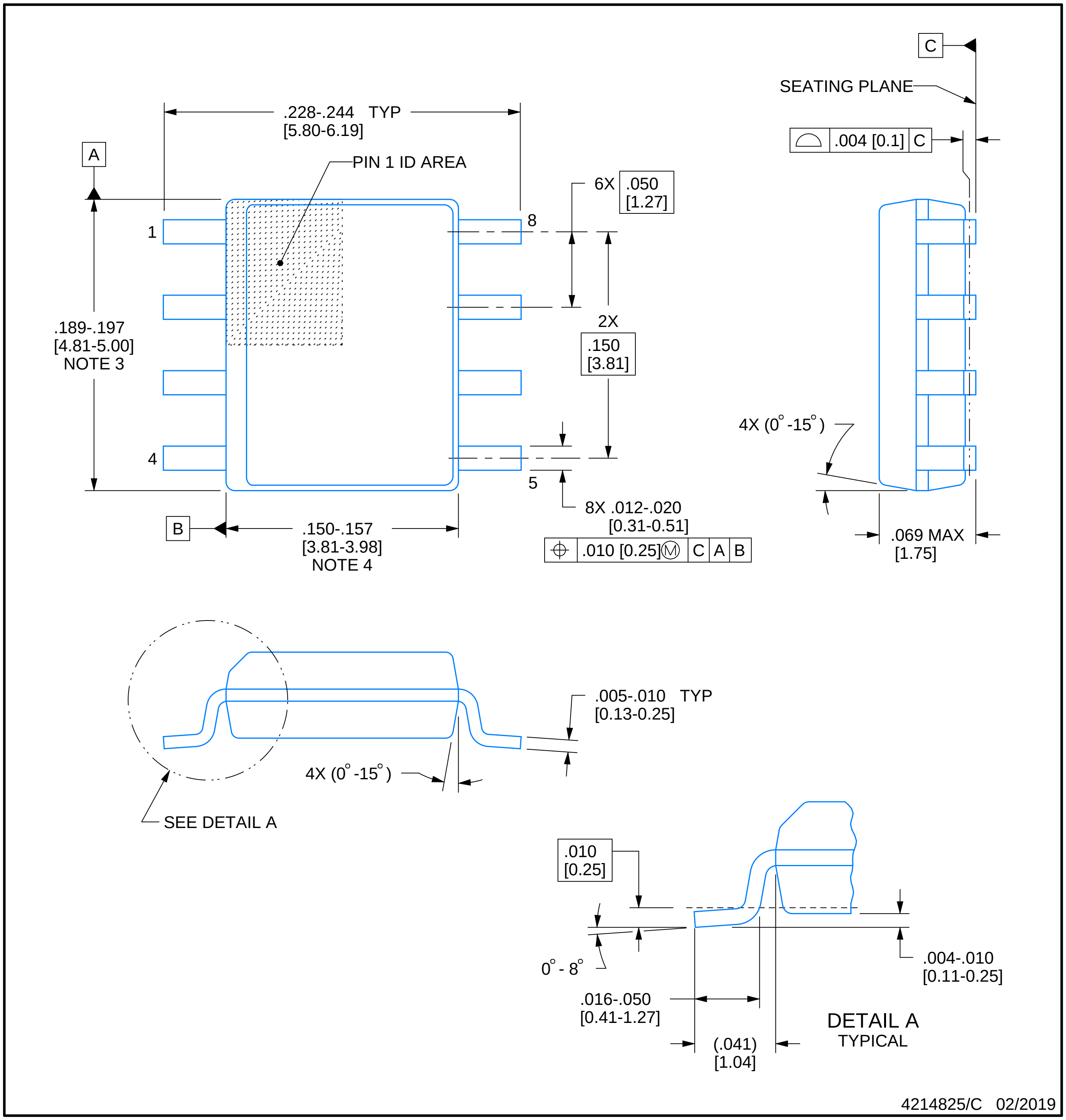


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

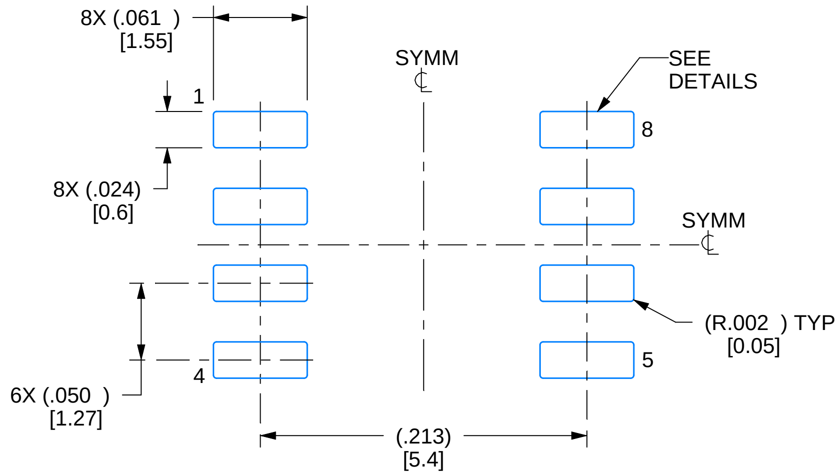
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

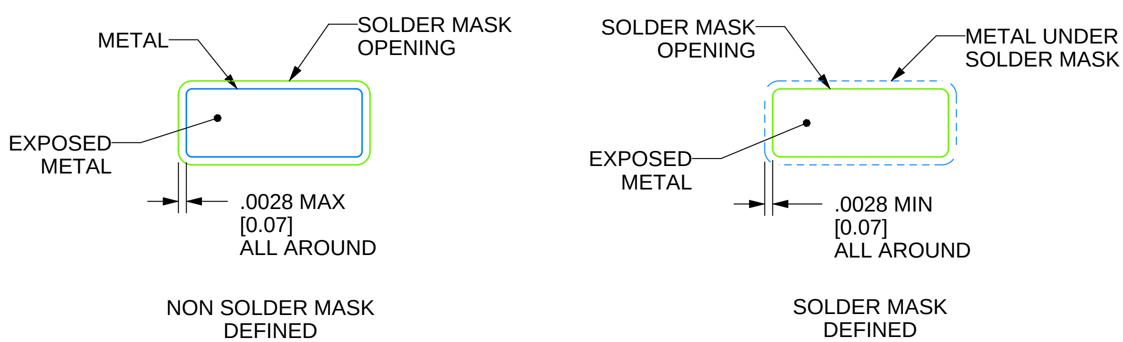


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

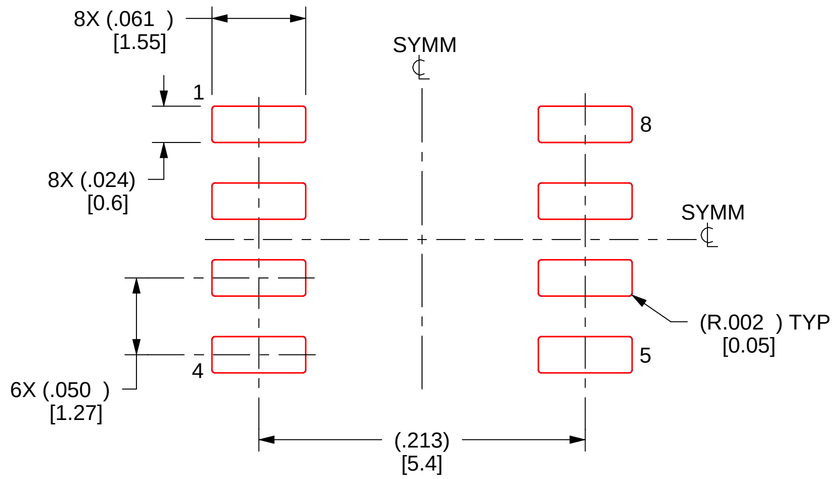
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



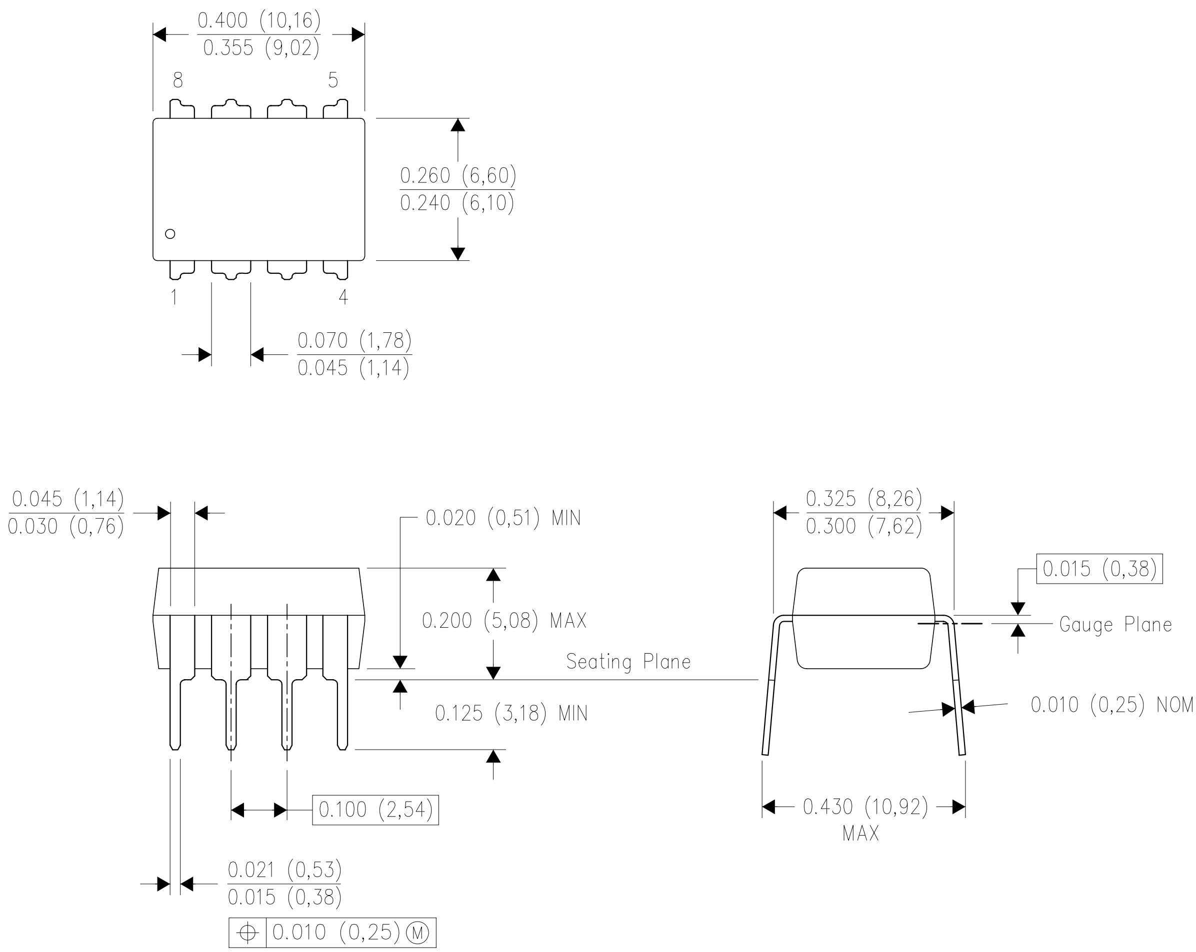
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.