

DLPC6401 DLP® 数据处理器

1 特性

- 提供一个 30 位输入像素接口：
 - YUV, YCrCb 或 RGB 数据格式
 - 每个色彩 8, 9 或 10 位
 - 像素时钟支持高达 150MHz
- 提供一个单通道、基于低压差分信号 (LVDS) 且兼容平板显示 (FPD)-Link 的输入接口：
 - 支持有效像素时钟速率高达 90MHz 的输入源
 - 支持四种经解调的像素映射模式, 适用于 8、9、10 路 YUV、YCrCb 或 RGB 格式的输入
- 支持 45Hz 至 120Hz 的帧速率
- 完全支持 Diamond 0.45 WXGA
- 高速、双倍数据速率 (DDR) 数字微镜器件 (DMD) 接口
- 149.33MHz ARM926™ 微处理器
- 微处理器外设：
 - 可编程脉宽调制 (PWM) 和捕捉定时器
 - 两个 I²C 端口
 - 两个通用异步收发器 (UART) 端口 (只用于调试)
 - 32KB 内部随机存取存储器 (RAM)
 - 专用发光二极管 (LED) PWM 发生器
- 图像处理：
 - 针对标准、宽和黑边缘的自动锁
 - 1D 梯形失真校正
 - 可编程后期色彩校正 (Degamma)
- 屏幕显示 (OSD)
- 初始屏幕显示支持
- 集成型时钟生成电路
 - 运行在单个 32MHz 晶振上

- 集成展频计时

- 集成 64Mb 帧存储器, 无需使用外部高速存储器
- 外部存储器支持: 针对微处理器和 PWM 序列的并行闪存
- 系统控制：
 - DMD 电源和复位驱动器控制
 - DMD 水平和垂直显示图像抖动
- 支持边界扫描测试的 JTAG
- 419 引脚塑料球状引脚栅格阵列封装

2 应用

- 电池供电的移动式附件高清 (HD) 投影仪
- 电池供电的智能 HD 附件
- 无屏幕显示 – 交互式显示器
- 移动电影院
- 游戏显示

3 说明

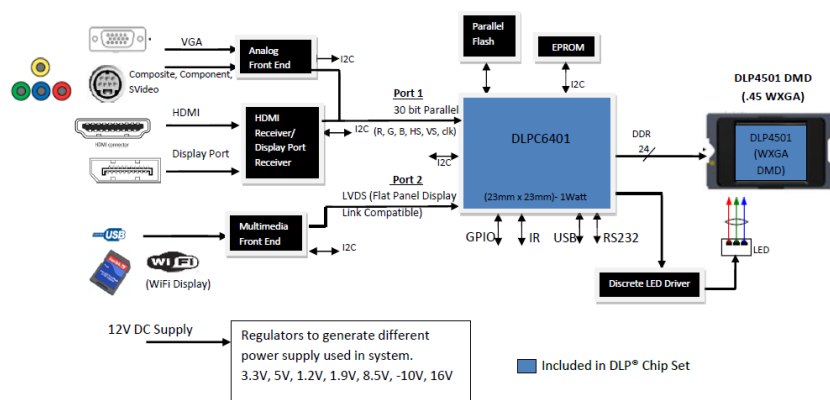
DLPC6401 数字控制器属于 DLP4500 (0.45 WXGA) 芯片组, 用于支持 DLP4500 数字微镜器件 (DMD) 的可靠运行。DLPC6401 控制器在系统电子设备与 DMD 之间提供一个方便的多功能接口, 从而实现了小外形尺寸的高分辨率 HD 显示屏。

器件信息 (1)

部件号	封装	阵列尺寸 (像素)
DLPC6401	BGA (419)	23.00mm x 23.00mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

典型应用图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (June 2015) to Revision C	Page
• 已更新器件标记图。	45

Changes from Revision A (January 2014) to Revision B	Page
• 已添加 ESD 额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
• Removed $V_{(ESD)}$ values from <i>Electrical Characteristics</i> table	13

Changes from Original (December 2013) to Revision A	Page
• 已删除产品预览条	1

5 Pin Configuration and Functions

ZFF PACKAGE 419-PIN BGA TOP VIEW

A22	VSS	B22	VSS	C22	VSS	D22	EPD 28	E22	EPD 28	F22	EPD 38	G22	VDD33	H22	REF 2	J22	REF 3	K22	VSS	L22	VSS	M22	REF 2	N22	REF 2	P22	PL C 6	R22	PL C 4	T22	VDD33	U22	PL C 6	V22	PL B 7	W22	PL B 4	Y22	VDD33	AA22	VDD33	AB22	VSS
A21	VSS	B21	VSS	C21	VSS	D21	EPD 38	E21	EPD 38	F21	EPD 38	G21	REF 2	H21	REF 1	J21	REF 4	K21	EPD 38	L21	REF 2	M21	REF 2	N21	EPD 38	P21	PL C 4	R21	PL C 5	T21	PL C 3	U21	PL B 8	V21	PL B 5	W21	PL B 3	Y21	VSS	AA21	VSS	AB21	VDD33
A20	VDD33	B20	VSS	C20	VSS	D20	VSS	E20	EPD 28	F20	EPD 28	G20	EPD 28	H20	REF 2	J20	REF 3	K20	REF 1	L20	REF 2	M20	REF 2	N20	EPD 28	P20	REF 2	R20	PL C 6	T20	PL C 3	U20	PL B 8	V20	VSS	W20	VSS	Y20	VSS	AA20	PL B 2	AB20	PL A 9
A19	EPD 28	B19	EPD 28	C19	VSS	D19	VSS	E19	VSS	F19	EPD 28	G19	EPD 28	H19	REF 2	J19	REF 3	K19	REF 1	L19	REF 2	M19	REF 2	N19	EPD 28	P19	REF 2	R19	PL C 6	T19	PL C 3	U19	PL B 6	V19	VSS	W19	VSS	Y19	PL B 4	AA19	PL A 8	AB19	PL A 5
A18	EPD 28	B18	EPD 28	C18	EPD 28	D18	EPD 28	E18	VSS	F18	VDDC	G18	RTCK	H18	VDD33	J18	VDD33	K18	VDD33	L18	TDO1	M18	TDO2	N18	VDD33	P18	TDI	R18	TCK	T18	VDD33	U18	VDDC	V18	VSS	W18	PL A 3	Y18	PL A 7	AA18	PL A 4	AB18	PL A 2
A17	EPD 28	B17	EPD 28	C17	EPD 28	D17	VPEM	E17	VDDC	F17	VDDC	G17	VDDC	H17	VDD33	J17	VDD33	K17	REF 2	L17	REF 2	M17	VSS	N17	VDDC	P17	REF 2	R17	REF 2	T17	VDD33	U17	VDDC	V17	REF 2	W17	PL A 6	Y17	PL A 8	AA17	PL A 0	AB17	REF 2
A16	VDD33	B16	EPD 28	C16	EPD 28	D16	EPD 28	E16	REF 2	F16	VDDC																					U16	VDDC	V16	REF 2	W16	PL A 1	Y16	REF 2	AA16	PL B 2	AB16	PL B 3
A15	MOSCIN	B15	REF 2	C15	EPD 28	D15	EPD 28	E15	VDD33	F15	VDD33																					U15	VSS	V15	REF 2	W15	PL A 0	Y15	PL VSS2	AA15	VDD33	AB15	VDD33
A14	MOSC	B14	REF 2	C14	REF 2	D14	REF 2	E14	VSS	F14	VSS					J14	VSS	K14	VSS	L14	VSS	M14	VSS	N14	VSS	P14	VSS				U14	VDD33	V14	VSS	W14	PL A 0	Y14	VSS	AA14	REF 2	AB14	REF 2	
A13	VSS	B13	VSS	C13	REF 2	D13	REF 2	E13	REF 2	F13	REF 2					J13	VSS	K13	VSS	L13	VSS	M13	VSS	N13	VSS	P13	VSS				U13	VDD33	V13	VDD33	W13	REF 2	Y13	REF 2	AA13	VSS	AB13	VSS	
A12	REF 2	B12	REF 2	C12	REF 2	D12	REF 2	E12	VDDC	F12	VDDC					J12	VSS	K12	VSS	L12	VSS	M12	VSS	N12	VSS	P12	VSS				U12	VDD33	V12	VDD33	W12	VSS	Y12	VSS	AA12	REF 2	AB12	REF 2	
A11	REF 2	B11	REF 2	C11	REF 2	D11	REF 2	E11	REF 2	F11	VSS					J11	VSS	K11	VSS	L11	VSS	M11	VSS	N11	VSS	P11	VSS				U11	VDD33	V11	VDD33	W11	REF 2	Y11	REF 2	AA11	VSS	AB11	VSS	
A10	REF 2	B10	REF 2	C10	REF 2	D10	REF 2	E10	REF 2	F10	REF 2					J10	VSS	K10	VSS	L10	VSS	M10	VSS	N10	VSS	P10	VSS				U10	VDD33	V10	VDD33	W10	VSS	Y10	VSS	AA10	REF 2	AB10	REF 2	
A9	REF 2	B9	REF 2	C9	REF 2	D9	REF 2	E9	REF 2	F9	VSS					J9	VSS	K9	VSS	L9	VSS	M9	VSS	N9	VSS	P9	VSS				U9	VDD33	V9	VDD33	W9	REF 2	Y9	REF 2	AA9	VSS	AB9	VDD33	
A8	REF 2	B8	REF 2	C8	REF 2	D8	REF 2	E8	REF 2	F8	REF 2																				U8	VSS	V8	VSS	W8	REF 2	Y8	VSS	AA8	REF 2	AB8	REF 2	
A7	VSS	B7	REF 2	C7	REF 2	D7	REF 2	E7	REF 2	F7	VDDC																				U7	VDDC	V7	REF 2	W7	REF 2	Y7	REF 2	AA7	REF 2	AB7	REF 2	
A6	REF 2	B6	REF 2	C6	REF 2	D6	REF 2	E6	VDDC	F6	VDDC					J6	VDD33	K6	REF 2	L6	REF 2	M6	VDDC	N6	VSS	P6	REF 2	R6	REF 2	T6	VDD33	U6	VDDC	V6	REF 2	W6	REF 2	Y6	REF 2	AA6	REF 2	AB6	REF 2
A5	REF 2	B5	REF 2	C5	REF 2	D5	REF 2	E5	VSS	F5	VDDC					J5	VDD33	K5	VDD33	L5	VDD33	M5	VDDC	N5	VDD33	P5	VDD33	R5	VDD33	T5	VDD33	U5	VDDC	V5	VSS	W5	REF 2	Y5	REF 2	AA5	REF 2	AB5	REF 2
A4	REF 2	B4	VSS	C4	VSS	D4	VSS	E4	VSS	F4	REF 2					J4	REF 2	K4	REF 2	L4	REF 2	M4	REF 2	N4	REF 2	P4	REF 2	R4	REF 2	T4	REF 2	U4	REF 2	V4	VSS	W4	VSS	Y4	REF 2	AA4	REF 2	AB4	REF 2
A3	REF 2	B3	VSS	C3	VSS	D3	VSS	E3	REF 2	F3	REF 2					J3	REF 2	K3	REF 2	L3	REF 2	M3	REF 2	N3	REF 2	P3	REF 2	R3	REF 2	T3	REF 2	U3	REF 2	V3	REF 2	W3	VSS	Y3	VSS	AA3	REF 2	AB3	REF 2
A2	VSS	B2	VSS	C2	VSS	D2	VSS	E2	VSS	F2	VSS					J2	VSS	K2	VSS	L2	VSS	M2	VSS	N2	VSS	P2	VSS	R2	VSS	T2	VSS	U2	VSS	V2	REF 2	W2	VSS	Y2	VSS	AA2	VSS	AB2	REF 2
		B1	REF 2	C1	REF 2	D1	REF 2	E1	VDD33	F1	REF 2					J1	REF 2	K1	REF 2	L1	VDD33	M1	REF 2	N1	REF 2	P1	VSS	R1	REF 2	T1	REF 2	U1	REF 2	V1	VDD33	W1	REF 2	Y1	REF 2	AA1	VSS	AB1	VDD33

Pin Functions

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
CONTROL						
$\overline{\text{EXT_ARST}}$	H20	VDD33	O ₁		Async	External reset output, LOW true. This output is asserted low immediately upon asserting power-up reset (POSENSE) low and remains low while PONSENSE remains low. EXT_ARSTZ continues to be held low after the release of power-up reset (that is, PONSENSE set high) until released by software. EXT_ARSTZ is also asserted low approximately 5 μ s after the detection of a PWRGOOD or any internally-generated reset. In all cases, it remains active for a minimum of 2 ms after the reset condition is released by software. Note, the ASIC contains a software register that can be used to independently drive this output.
PWRGOOD	H19	VDDC	I ₄ H		Async	Power Good is an active-high signal with hysteresis that is generated by an external power supply or voltage monitor. A high value indicates all power is within operating voltage specifications and the system is safe to exit its reset state. A transition from high to low should indicate that the controller or DMD supply voltage will drop below their rated minimum level within the next 0.5 ms (POSENSE must remain active high during this interval). This is an early warning of an imminent power loss condition. This warning is required to enhance long-term DMD reliability. A DMD park sequence, followed by a full controller reset, is performed by the DLPC6401 when PWRGOOD goes low for a minimum of 4 μ s protecting the DMD. This minimum de-assertion time is used to protect the input from glitches. Following this, the DLPC6401 is held in its reset state as long as PWRGOOD is low. PWRGOOD must be driven high for typical operation. The DLPC6401 device acknowledges PWRGOOD as active after it is driven high for a minimum of 625 ns. Uses hysteresis.
POSENSE	G21		I ₄ H		Async	Power-On Sense is an active-high input signal with hysteresis that is generated by an external voltage monitor circuit. PONSENSE must be driven inactive (low) when any of the controller supply voltages are below minimum operating voltage specifications. PONSENSE must be active (high) when all controller supply voltages remain above minimum specifications.
POWER_ON_OFF	N21	VDD33	B ₂		Async	Power On or Power Off is an active-high signal that indicates the power of the system. Power On or Power Off is high when the system is in power-up state, and low when the system is in standby. Power On or Power Off can also be used to power on or off an external power supply.
INIT_DONE	F19	VDD33	B ₂		Async	Prior to transferring part of code from parallel flash content to internal memory, the internal memory is initialized and a memory test is performed. The result of this test (pass or fail) is recorded in the system status. If memory test fails, the initialization process is halted. INIT_DONE is asserted twice to indicate an error situation. See Figure 12 .
I2C_ADDR_SEL	F21	VDD33	B ₂		Async	This signal is sampled during power-up. If the signal is low, the I ² C addresses are 0x34 and 0x35. If the signal is high, the I ² C are 0x3A and 0x3B.
I2C1_SCL	J3	VDD33	B ₂	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 k Ω .	N/A	I ² C clock. Bidirectional, open-drain signal. I ² C slave clock input from the external processor. This bus supports 400 kHz.
I2C1_SDA	J4	VDD33	B ₂	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 k Ω .	I2C1_SCL	I ² C data. Bidirectional, open-drain signal. I ² C slave to accept command or transfer data to and from the external processor. This bus supports 400 kHz.

 (1) For instructions on handling unused pins, see [General Handling Guidelines for Unused CMOS-Type Pins](#).

 (2) I/O Type: I = Input, O = Output, B = Bidirectional, and H = Hysteresis. See [Table 1](#) for subscript explanation.

Pin Functions (continued)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
I2C0_SCL	M2	VDD33	B ₈	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ. This input is not 5-V tolerant.	N/A	I ² C bus 0, clock; I ² C master for on-board peripherals such as temperature sensor. This bus supports 400-kHz, fast-mode operation.
I2C0_SDA	M3	VDD33	B ₈	Requires an external pullup to 3.3 V. The minimum acceptable pullup value is 1 kΩ. This input is not 5-V tolerant.	I2C0_SCL	I ² C bus 0, data; I ² C master for on-board peripherals such as temperature sensor. This bus supports 400-kHz, fast-mode operation.
SYSTEM CLOCK						
MOSC	A14	VDD33	I ₁₀		N/A	System clock oscillator input (3.3-V LVCMOS). Note that the MOSC must be stable a maximum of 25 ms after POSENSE transitions from high to low.
MOSCN	A15	VDD33	O ₁₀		N/A	MOSC crystal return
PORT 1: PARALLEL VIDEO AND GRAPHICS INPUT⁽³⁾⁽⁴⁾⁽⁵⁾						
P1A_CLK	W15	VDD33	I ₄	Includes an internal pulldown	N/A	Port 1 input data pixel write clock 'A'
P1B_CLK	AB17	VDD33	I ₄	Includes an internal pulldown	N/A	Port 1 input data pixel write clock 'B'
P1C_CLK	Y16	VDD33	I ₄	Includes an internal pulldown	N/A	Port 1 input data pixel write clock 'C'
P1_VSYNC	Y15	VDD33	B ₁ H	Includes an internal pulldown	P1A_CLK	Port 1 vertical sync. Uses hysteresis
P1_HSYNC	AB16	VDD33	B ₁ H	Includes an internal pulldown	P1A_CLK	Port 1 horizontal sync. Uses hysteresis
P1_DATEN	AA16	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 data enable
P1_FIELD	W14	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 field sync. Required for interlaced sources only (and not progressive)
P1_A_9	AB20	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 128)
P1_A_8	AA19	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 64)
P1_A_7	Y18	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 32)
P1_A_6	W17	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 16)
P1_A_5	AB19	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 8)
P1_A_4	AA18	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 4)
P1_A_3	Y17	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 2)
P1_A_2	AB18	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 1)
P1_A_1	W16	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 0.5)
P1_A_0	AA17	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 A channel input pixel data (bit weight 0.25)
P1_B_9	U21	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 128)
P1_B_8	U20	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 64)
P1_B_7	V22	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 32)
P1_B_6	U19	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 16)
P1_B_5	V21	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 8)
P1_B_4	W22	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 4)
P1_B_3	W21	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 2)
P1_B_2	AA20	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 1)
P1_B_1	Y19	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 0.5)
P1_B_0	W18	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 B channel input pixel data (bit weight 0.25)
P1_C_9	P21	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 128)
P1_C_8	P22	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 64)

- (3) Port 1 can be used to support multiple source options for a given product (that is, HDMI, BT656). To do so, the data bus from both source components must be connected to the same port 1 pins and control given to the DLPC6401 to tri-state the inactive source. Tying them together like this causes some signal degradation due to reflections on the tri-stated path.
- (4) The A, B, and C input data channels of port 1 can be internally swapped for optimum board layout.
- (5) Sources feeding less than the full 10-bits per color component channel should be MSB justified when connected to the DLPC6401 and LSBs tied off to 0. For example, an 8-bit per color input should be connected to bits 9:2 of the corresponding A, B, or C input channel. BT656 are 8 or 10 bits in width. If a BT656-type input is used, the data bits must be MSB justified as with the other types of input sources on either of the A, B, or C data input channels.

Pin Functions (continued)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
P1_C_7	R19	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 32)
P1_C_6	R20	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 16)
P1_C_5	R21	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 8)
P1_C_4	R22	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 4)
P1_C_3	T21	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 2)
P1_C_2	T20	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 1)
P1_C_1	T19	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 0.5)
P1_C_0	U22	VDD33	I ₄	Includes an internal pulldown	P1A_CLK	Port 1 C channel input pixel data (bit weight 0.25)
PORT 2: FPD-LINK COMPATIBLE VIDEO AND GRAPHICS INPUT⁽⁶⁾						
RCK_IN_P	Y9	VDD33_FPD	I ₅	Includes weak internal pulldown	N/A	Positive differential input signal for clock, FPD-Link receiver
RCK_IN_N	W9	VDD33_FPD	I ₅	Includes weak internal pulldown	N/A	Negative differential input signal for clock, FPD-Link receiver
RA_IN_P	AB10	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel A, FPD-Link receiver
RA_IN_N	AA10	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel A, FPD-Link receiver
RB_IN_P	Y11	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel B, FPD-Link receiver
RB_IN_N	W11	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel B, FPD-Link receiver
RC_IN_P	AB12	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel C, FPD-Link receiver
RC_IN_N	AA12	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel C, FPD-Link receiver
RD_IN_P	Y13	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel D, FPD-Link receiver
RD_IN_N	W13	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel D, FPD-Link receiver
RE_IN_P	AB14	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Positive differential input signal for data channel E, FPD-Link receiver
RE_IN_N	AA14	VDD33_FPD	I ₅	Includes weak internal pulldown	RCK_IN	Negative differential input signal for data channel E, FPD-Link receiver

- (6) Port 2 is a single-channel FPD-Link compatible input interface. FPD-Link is a defacto industry standard FPD interface, which uses the high-bandwidth capabilities of LVDS signaling to serialize video and graphics data down to a couple wires to provide a low-wire count and low-EMI interface. Port 2 supports source rates up to a maximum effective clock of 90 MHz. The port 2 input pixel data must adhere to one of four supported data mapping formats (see [Table 2](#)). Given that port 2 inputs contain weak pulldown resistors, they can be left floating when not used.

Pin Functions (continued)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
DMD INTERFACE						
DMD_D0	A8	VDD_DMD	O ₇		DMD_DCLK	DMD data pins. DMD data pins are DDR signals that are clocked on both edges of DMD_DCLK. All 24 DMD data signals are use to interface to the DLP4500.
DMD_D1	B8					
DMD_D2	C8					
DMD_D3	D8					
DMD_D4	B11					
DMD_D5	C11					
DMD_D6	D11					
DMD_D7	E11					
DMD_D8	C7					
DMD_D9	B10					
DMD_D10	E7					
DMD_D11	D10					
DMD_D12	A6					
DMD_D13	A12					
DMD_D14	B12					
DMD_D15	C12					
DMD_D16	D12					
DMD_D17	B7					
DMD_D18	A10					
DMD_D19	D7					
DMD_D20	B6					
DMD_D21	E9					
DMD_D22	C10					
DMD_D23	C6					
DMD_DCLK	A9	VDD_DMD	O ₇		N/A	DMD data clock (DDR)
DMD_LOADB	B9	VDD_DMD	O ₇		DMD_DCLK	DMD data load signal (active-low)
DMD_SCTRL	C9	VDD_DMD	O ₇		DMD_DCLK	DMD data serial control signal
DMD_TRC	D9	VDD_DMD	O ₇		DMD_DCLK	DMD data toggle rate control
DMD_DRC_BUS	D5	VDD_DMD	O ₇		DMD_SAC_CLK	DMD reset control bus data
DMD_DRC_STRB	C5	VDD_DMD	O ₇		DMD_SAC_CLK	DMD reset control bus strobe
DMD_DRC_OE	B5	VDD_DMD	O ₇	Requires a 30 to 51-kΩ external pullup resistor to VDD_DMD.	Async	DMD reset control enable (active low)
DMD_SAC_BUS	D6	VDD_DMD	O ₇		DMD_SAC_CLK	DMD stepped-address control bus data
DMD_SAC_CLK	A5	VDD_DMD	O ₇		N/A	DMD stepped-address control bus clock
DMD_PWR_EN	G20	VDD_DMD	O ₂		Async	DMD Power Enable control. This signal indicates to an external regulator that the DMD is powered.
EXRES	A3		O		Async	DMD drive strength adjustment precision reference. A ±1% external precision resistor should be connected to this pin.
FLASH INTERFACE						
PM_CS_0	U3	VDD33	O ₂		Async	Reserved for future use. On the PCB, connect to VDD33 through a pullup resistor.
PM_CS_1	U2	VDD33	O ₂		Async	Boot flash (active low). Required for boot memory
PM_CS_2	U1	VDD33	O ₂		Async	Reserved for future use. On the PCB, connect to VDD33 through a pullup resistor.

Pin Functions (continued)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
PM_ADDR_22	V3	VDD33	B ₂		Async	Flash memory address bit
PM_ADDR_21	W1					
PM_ADDR_20	W2					
PM_ADDR_19	Y1					
PM_ADDR_18	AB2					
PM_ADDR_17	AA3					
PM_ADDR_16	Y4					
PM_ADDR_15	W5					
PM_ADDR_14	AB3					
PM_ADDR_13	AA4					
PM_ADDR_12	Y5					
PM_ADDR_11	W6					
PM_ADDR_10	AB4					
PM_ADDR_9	AA5					
PM_ADDR_8	Y6					
PM_ADDR_7	W7					
PM_ADDR_6	AB5					
PM_ADDR_5	AA6					
PM_ADDR_4	Y7					
PM_ADDR_3	AB6					
PM_ADDR_2	W8					
PM_ADDR_1	AA7					
PM_ADDR_0	AB7					
PM_WE	V2	VDD33	O ₂		Async	Write enable (active low)
PM_OE	U4	VDD33	O ₂		Async	Output enable (active low)
PM_BLS_1	AA8	VDD33	O ₂		Async	Upper byte(15:8) enable
PM_BLS_0	AB8	VDD33	O ₂		Async	Lower byte(7:0) enable
PM_DATA_15	M1	VDD33	B ₂		Async	Data bits, upper byte
PM_DATA_14	N1					
PM_DATA_13	N2					
PM_DATA_12	N3					
PM_DATA_11	N4					
PM_DATA_10	P1					
PM_DATA_9	P2					
PM_DATA_8	P3					
PM_DATA_7	P4	VDD33	B ₂		Async	Data bits, lower byte
PM_DATA_6	R2					
PM_DATA_5	R3					
PM_DATA_4	R4					
PM_DATA_3	T1					
PM_DATA_2	T2					
PM_DATA_1	T3					
PM_DATA_0	T4					
LED DRIVER INTERFACE						
LEDR_PWM	K2	VDD33	O ₂		Async	LED red PWM output enable control
LEDG_PWM	K3					LED green PWM output enable control
LEDB_PWM	K4					LED blue PWM output enable control
LEDR_EN	L3	VDD33	O ₂		Async	LED red PWM output
LEDG_EN	L4					LED green PWM output
LEDB_EN	K1					LED blue PWM output

Pin Functions (continued)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
PERIPHERAL INTERFACE						
UART_TXD	L19	VDD33	O ₂		Async	Transmit data output. Reserved for debug messages
UART_RXD	L21	VDD33	I ₄		Async	Receive data input. Reserved for debug messages
UART_RTS	M19	VDD33	O ₂		Async	Ready to send hardware flow control output. Reserved for debug messages
UART_CTS	L20	VDD33	I ₄		Async	Clear to send hardware flow control input. Reserved for debug messages
GENERAL PURPOSE I/O (GPIO)⁽⁷⁾						
GPIO_37	K21	VDD33	B ₂		Async	None
GPIO_36	G1	VDD33	B ₂		Async	None
GPIO_35	H4	VDD33	B ₂		Async	None
GPIO_34	H3	VDD33	B ₂		Async	None
GPIO_33	H2	VDD33	B ₂		Async	None
GPIO_32	F22	VDD33	B ₂		Async	None
GPIO_31	G19	VDD33	B ₂		Async	None
GPIO_29	F20	VDD33	B ₂		Async	None
GPIO_28	E22	VDD33	B ₂		Async	None
GPIO_27	E21	VDD33	B ₂		Async	None
GPIO_25	D22	VDD33	B ₂		Async	None
GPIO_24	E20	VDD33	B ₂		Async	None
GPIO_23	D21	VDD33	B ₂		Async	None
GPIO_21	N20	VDD33	B ₂		Async	None
GPIO_20	N19	VDD33	B ₂		Async	None
GPIO_19	D18	VDD33	B ₂		Async	None
GPIO_18	C18	VDD33	B ₂		Async	None
GPIO_15	B19	VDD33	B ₂		Async	None
GPIO_14	B18	VDD33	B ₂		Async	None
GPIO_13	L2	VDD33	B ₂		Async	None
GPIO_12	M4	VDD33	B ₂		Async	None
GPIO_11	A19	VDD33	B ₂		Async	None
GPIO_10	C17	VDD33	B ₂		Async	None
GPIO_06	A18	VDD33	B ₂		Async	None
GPIO_05	D16	VDD33	B ₂		Async	None
GPIO_04	C16	VDD33	B ₂		Async	None
GPIO_03	B16	VDD33	B ₂		Async	None
GPIO_02	A17	VDD33	B ₂		Async	None
GPIO_00	C15	VDD33	B ₂		Async	None
OTHER INTERFACES						
FAN_LOCKED	B17	VDD33	B ₂		Async	Feedback from fan to indicate fan is connected and running
FAN_PWM	D15	VDD33	B ₂		Async	Fan PWM speed control
BOARD LEVEL TEST AND DEBUG						
TDI	P18	VDD33	I ₄	Includes internal pullup	TCK	JTAG serial data in ⁽⁸⁾
TCK	R18	VDD33	I ₄	Includes internal pullup	N/A	JTAG serial data clock ⁽⁸⁾
TMS1	V15	VDD33	I ₄	Includes internal pullup	TCK	JTAG test mode select ⁽⁸⁾
TDO1	L18	VDD33	O ₁		TCK	JTAG serial data out ⁽⁸⁾

(7) GPIO signals must be configured by software for input, output, bidirectional, or open-drain. Some GPIOs have one or more alternate use modes, which are also software configurable. The reset default for all optional GPIOs is as an input signal. However, any alternate function connected to these GPIO pins with the exception of general-purpose clocks and PWM generation, are reset. An external pullup to the 3.3-V supply is required for each signal configured as open-drain. External pullup or pulldown resistors may be required to ensure stable operation before software is able to configure these ports.

(8) All JTAG signals are LVCMOS-compatible.

Pin Functions (continued)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
$\overline{\text{TRST}}$	V17	VDD33	I ₄ H	Includes internal pullup	Async	JTAG, RESET (active low). This pin should be pulled high (or left unconnected) when the JTAG interface is in use for boundary scan. Connect this pin to ground otherwise. Failure to tie this pin low during normal operation causes startup and initialization problems. ⁽⁸⁾
RTCK	G18	VDD33	O ₂		N/A	JTAG return clock ⁽⁹⁾
ICTSEN	V6	VDD33	I ₄ H	Includes internal pull down. External pulldown recommended for added protection.	Async	IC Tri-State Enable (active high). Asserting high tri-states all outputs except the JTAG interface.

(9) For instructions on handling unused pins, see [General Handling Guidelines for Unused CMOS-Type Pins](#).

Functional Pin Descriptions (Reserved Pins)

PIN ⁽¹⁾		I/O ⁽²⁾		INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.	POWER	TYPE			
RESERVED	V7	VDD33	I ₄ H	Includes internal pulldown	N/A	Connect directly to ground on the PCB.
RESERVED	N22, M22, P19, P20	VDD33	I ₄	Includes an internal pulldown	N/A	Reserved ⁽¹⁾
RESERVED	V16	VDD33	I ₄	Includes an internal pullup	N/A	
RESERVED	D1, J2	VDD33	I ₄		N/A	
RESERVED	F1, F2, G2, G3, G4	VDD33	O ₂	Includes internal pulldown	N/A	Leave these pins unconnected ⁽¹⁾
RESERVED	F3, J1, M21	VDD33	O ₂		N/A	
RESERVED	H20, M18, M20	VDD33	O ₁		N/A	
RESERVED	H21, H22, J19, J20, J21, J22, K19, K20	VDD33	B ₂	Includes internal pulldown	N/A	Reserved ⁽¹⁾
RESERVED	C1, D2, F4	VDD33	B ₂		N/A	
RESERVED	E3, E2	VDD33	—		Async	Reserved

(1) For instructions on handling unused pins, see [General Handling Guidelines for Unused CMOS-Type Pins](#).

(2) I/O Type: I indicates input, O indicates output, B indicates bidirectional, and H indicates hysteresis. See [Table 1](#) for subscript explanation.

Table 1. I/O Type Subscript Definition

SUBSCRIPT	I/O		ESD STRUCTURE
	DESCRIPTION		
1	3.3-V LVCMOS I/O buffer, with 4-mA drive		ESD diode to VDD33 and GND
2	3.3-V LVCMOS I/O buffer, with 8-mA drive		ESD diode to VDD33 and GND
3	3.3-V LVCMOS I/O buffer, with 12-mA drive		ESD diode to VDD33 and GND
4	3.3-V LVCMOS receiver		ESD diode to VDD33 and GND
5	3.3-V LVDS receiver (FPD-Link I/F)		ESD diode to VDD33 and GND
6	None		N/A
7	1.9-V LPDDR output buffer (DMD I/F)		ESD diode to VDD_DMD and GND
8	3.3-V I ² C with 12-mA sink		ESD diode to VDD33 and GND
10	OSC 3.3-V I/O compatible LVCMOS		ESD diode to VDD33 and GND

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating free-air temperature (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
ELECTRICAL				
Supply voltage ⁽²⁾	VDDC (core 1.2-V power)	-0.5	1.7	V
	VDD33 (CMOS I/O)	-0.5	3.8	
	VDD_DMD (DMD driver power)	-0.5	2.3	
	VDD12_FPD (FPD-Link LVDS interface 1.2-V power)	-0.5	1.7	
	VDD33_FPD (FPD-Link LVDS interface 3.3-V power)	-0.5	3.8	
	VDD12_PLLD (DDR clock generator – digital)	-0.5	1.7	
	VDD12_PLLM (master clock generator – digital)	-0.5	1.7	
	VDD_18_PLLD (DDR clock generator – analog)	-0.5	2.3	
	VDD_18_PLLM (master clock generator – analog)	-0.5	2.3	
	V _I Input voltage ⁽³⁾	OSC (BC1850)	-0.3	
LVC MOS (BT3350)		-0.5	3.6	
I ² C (BT3350)		-0.5	3.6	
LVDS (BT3350)		-0.5	3.6	
V _O Output voltage	DMD LPDDR (BC1850)	-0.3	2.0	
	LVC MOS (BT3350)	-0.5	3.6	
	I ² C (BT3350)	-0.5	3.6	
ENVIRONMENTAL				
T _J	Operating junction temperature	0	115	°C
T _{stg}	Storage temperature	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

(3) Applies to external input and bidirectional buffers.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	
	Machine model (MM)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		I/O ⁽¹⁾	MIN	NOM	MAX	UNIT
VDD33	3.3-V supply voltage, I/O		3.135	3.3	3.465	V
VDD_DMD	1.9-V supply voltage, I/O		1.8	1.9	2	V
VDD_18_PLLD	1.8-V supply voltage, PLL analog		1.71	1.8	1.89	V
VDD_18_PLLM	1.8-V supply voltage, PLL analog		1.71	1.8	1.89	V
VDD12	1.2-V supply voltage, core logic		1.116	1.2	1.26	V
VDD12_PLLD	1.2-V supply voltage, PLL digital		1.116	1.2	1.26	V
VDD12_PLLM	1.2-V supply voltage, PLL digital		1.116	1.2	1.26	V
V _I	Input voltage	OSC (10)	0		VDD33	V
		3.3-V LVCMOS (1, 2, 3, 4)	0		VDD33	
		3.3-V I ² C (8)	0		VDD33	
		3.3-V LVDS (5)	0.6		2.2	
V _O	Output voltage	3.3-V LVCMOS (1, 2, 3, 4)	0		VDD33	V
		3.3-V I ² C (8)	0		VDD33	
		1.9-V LPDDR (7)	0		VDD_DMD	
T _A	Operating ambient temperature range	See ⁽²⁾	0		55	°C
T _C	Operating top-center case temperature	See ⁽³⁾⁽⁴⁾	0		104	°C
T _J	Operating junction temperature		0		105	°C

(1) The number inside each parenthesis for the I/O refers to the type defined in the I/O type subscript definition section.

(2) Assumes a minimum 1-m/s airflow along with the JEDEC thermal resistance and associated conditions as listed www.ti.com/packaging. Thus, this is an approximate value that varies with environment and PCB design.

(3) Maximum thermal values assume maximum power of 3 W.

(4) Assume ψ_{JT} equals 0.33 C/W.

6.4 Thermal Information⁽¹⁾

THERMAL METRIC ⁽¹⁾	DLPC6401	UNIT
	ZFF (BGA)	
	419 PINS	
ψ_{JT} Junction-to-top characterization parameter	0.33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*, [SPRA953](http://www.ti.com/lit/zip/Spra953).

6.5 Electrical Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{IH}	High-level input threshold voltage	OSC (10)		2		V	
		3.3-V LVCMOS (1, 2, 3, 4)		2			
		3.3-V I ² C (8)		2.4			
V _{IL}	Low-level input threshold voltage	OSC (10)			0.8	V	
		3.3-V LVCMOS (1, 2, 3, 4)			0.8		
		3.3-V I ² C (8)			1		
R _I	Receiver input impedance	3.3-V LVDS (5)	VDDH = 3.3 V	90	110	132	Ω
V _{id}	Input differential threshold	3.3-V LVDS (5)		-200		200	mV
V _{id}	Absolute input differential voltage	3.3-V LVDS (5)		200		600	mV
VICM	Input common mode voltage range	3.3-V LVDS (5)	At minimum absolute input differential voltage	0.7		2.1	V
		3.3-V LVDS (5)	At max absolute input differential voltage	0.9		1.9	
V _{HYS}	Hysteresis (V _{T+} – V _{T-})	3.3-V LVCMOS (1, 2, 3, 4)			400		mV
		3.3-V I ² C (8)			550		
V _{OH}	High-level output voltage	3.3-V LVCMOS (1, 2, 3)	I _{OH} = Max rated	2.8			V
		1.9-V DMD LPDDR (7)	I _{OH} = -0.1 mA	0.9 × VDD_DMD			
V _{OL}	Low-level output voltage	1.9-V DMD LPDDR (7)	I _{OL} = 0.1 mA			0.1 × VDD_DMD	V
		3.3-V LVCMOS (1, 2, 3)	I _{OL} = Max rated			0.4	
		3.3-V I ² C (8)	I _{OL} = 3-mA sink			0.4	
I _{IH}	High-level input current	OSC (10)				10.0	μA
		3.3-V LVCMOS (1 to 4) (without internal pulldown)	V _{IH} = VDD33			10	
		3.3 V LVCMOS (1 to 4) (with internal pulldown)	V _{IH} = VDD33			200	
		3.3 V I ² C (8)	V _{IH} = VDD33			10	
I _{IL}	Low-level input current	OSC (10)				-10.0	μA
		3.3-V LVCMOS (1 to 4) (without internal pullup)	V _{OH} = VDD33			-10	
		3.3-V LVCMOS (1 to 4) (with internal pullup)	V _{OH} = VDD33			-200	
		3.3-V I ² C (8)	V _{OH} = VDD33			-10	
I _{OH}	High-level output current	1.9-V DMD LPDDR (7)	V _O = 1.5 V			-4	mA
		3.3-V LVCMOS (1)	V _O = 2.4 V			-4	
		3.3-V LVCMOS (2)	V _O = 2.4 V			-8	
		3.3-V LVCMOS (3)	V _O = 2.4 V			-12	
I _{OL}	Low-level output current	1.9-V DMD LPDDR (7)	V _O = 0.4 V			4	mA
		3.3-V LVCMOS (1)	V _O = 0.4 V			4	
		3.3-V LVCMOS (2)	V _O = 0.4 V			8	
		3.3-V LVCMOS (3)	V _O = 0.4 V			12	
		3.3-V I ² C (8)				3	
I _{oz}	High-impedance leakage current	3.3-V LVCMOS (1, 2, 3)				-10	μA
		3.3-V I ² C (8)				-10	
C _I	Input capacitance (including package)	3.3-V LVCMOS (2)		2.8	3.3	4	pF
		3.3-V LVCMOS (4)		2.7	3.4	4.2	
		3.3-V I ² C (8)		3	3.2	3.5	

(1) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

6.6 Electrical Characteristics (Normal Mode)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION ⁽¹⁾	MIN	TYP	MAX ⁽²⁾	UNIT
I _{CC12}	Supply voltage, 1.2-V core power	Normal mode		600	1020	mA
I _{CC19_DMD}	Supply voltage, 1.9-V I/O power (DMD LPDDR)	Normal mode		30	50	mA
I _{CC33}	Supply voltage, 3.3-V (I/O) power	Normal mode		40	70	mA
I _{CC12_FPD}	FPD-Link LVDS I/F supply voltage, 1.2-V power	Normal mode		60	100	mA
I _{CC33_FPD}	FPD-Link LVDS I/F supply voltage, 3.3-V power	Normal mode		50	85	mA
I _{CC12_PLLD}	Supply voltage, PLL digital power (1.2 V)	Normal mode		9	15	mA
I _{CC12_PLLM}	Supply voltage, master clock generator PLL digital power (1.2 V)	Normal mode		9	15	mA
I _{CC18_PLLD}	Supply voltage, PLL analog power (1.8 V)	Normal mode		10	16	mA
I _{CC18_PLLM}	Supply voltage, master clock generator PLL analog power (1.8 V)	Normal mode		10	16	mA
P _{TOT}	Total power	Normal mode		1225	2200	mW

- (1) Normal mode refers to ASIC operation during full functionality, active product operation. Typical values correspond to power dissipated on nominal process devices operating at nominal voltage and 70°C junction temperature (approximately 25°C ambient) displaying typical video-graphics content from a high-frequency source. Maximum values correspond to power dissipated on fast process devices operating at high voltage and 105°C junction temperature (approximately 55°C ambient) displaying typical video-graphics content from a high-frequency source. The increased power dissipation observed on fast process devices operated at maximum recommended temperature is primarily a result of increased leakage current.
- (2) Maximum power values are estimates and may not reflect the actual final power consumption of DLPC6401 ASIC.

6.7 System Oscillators Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
f _{clock}	Clock frequency, MOSC ⁽¹⁾		31.9968	32.0032	MHz
t _c	Cycle time, MOSC ⁽¹⁾		31.188	31.256	ns
t _{w(H)}	Pulse duration ⁽²⁾ , MOSC, high	50% to 50% reference points (signal)	12.5		ns
t _{w(L)}	Pulse duration ⁽²⁾ , MOSC, low	50% to 50% reference points (signal)	12.5		ns
t _t	Transition time ⁽²⁾ , MOSC, t _t = t _f / t _r	20% to 80% reference points (signal)		7.5	ns
t _{jp}	Period jitter ⁽²⁾ , MOSC (that is, the deviation in period from ideal period due solely to high-frequency jitter – not spread spectrum clocking)		–100	100	ps

- (1) The frequency range for MOSC is 32 MHz with ±100 PPM accuracy. (This includes impact to accuracy due to aging, temperature, and trim sensitivity.) The MOSC input cannot support spread spectrum clock spreading.
- (2) Applies only when driven by an external digital oscillator.

6.8 Test and Reset Timing Requirements

			MIN	MAX	UNIT
$t_{W1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)	4		μs
t_{t1}	Transition time, PWRGOOD, $t_{t1} = t_f / t_r$	20% to 80% reference points (signal)		625	μs
$t_{W2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)	500		μs
t_{t2}	Transition time, POSENSE, $t_{t2} = t_f / t_r$	20% to 80% reference points (signal)		1	μs
t_{PH}	Power hold time, POSENSE remains active after PWRGOOD is deasserted	20% to 80% reference points (signal)	500		μs

6.9 JTAG Interface: I/O Boundary Scan Application Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			10	MHz
t_C	Cycle time, TCK		100		ns
$t_{W(H)}$	Pulse duration, high	50% to 50% reference points (signal)	40		ns
$t_{W(L)}$	Pulse duration, low	50% to 50% reference points (signal)	40		ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)		5	ns
t_{SU}	Setup time, TDI valid before TCK \uparrow		8		ns
t_h	Hold time, TDI valid after TCK \uparrow		2		ns
t_{SU}	Setup time, TMS1 valid before TCK \uparrow		8		ns
t_h	Hold time, TMS1 valid after TCK \uparrow		2		ns

6.10 Port 1 Input Pixel Interface Timing Requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency, P1A_CLK, P1B_CLK, P1C_CLK	12	150	MHz
t_c	Cycle time, P1A_CLK, P1B_CLK, P1C_CLK	6.666	83.33	ns
$t_{w(H)}$	Pulse duration, high 50% to 50% reference points (signal)	2.3		ns
$t_{w(L)}$	Pulse duration, low 50% to 50% reference points (signal)	2.3		ns
t_{jp}	Clock period jitter, P1A_CLK, P1B_CLK, P1C_CLK (that is, the deviation in period from ideal period) Max f_{clock}		See ⁽¹⁾	ps
t_t	Transition time, $t_t = t_f / t_r$, P1A_CLK, P1B_CLK, P1C_CLK	20% to 80% reference points (signal)	0.6	2 ns
t_t	Transition time, $t_t = t_f / t_r$, P1_A(9-0), P1_B(9-0), P1_C(9-0), P1_HSYNC, P1_VSYNC, P1_DATEN	20% to 80% reference points (signal)	0.6	3 ns
t_t	Transition time, $t_t = t_f / t_r$, ALF_HSYNC, ALF_VSYNC, ALF_CSYNC ⁽²⁾	20% to 80% reference points (signal)	0.6	3 ns
SETUP AND HOLD TIMES⁽³⁾				
t_{su}	Setup time, P1_A(9-0), valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_A(9-0), valid after P1x_CLK $\uparrow\downarrow$	0.8		ns
t_{su}	Setup time, P1_B(9-0), valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_B(9-0), valid after P1x_CLK $\uparrow\downarrow$	0.8		ns
t_{su}	Setup time, P1_C(9-0), valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_C(9-0), valid after P1x_CLK $\uparrow\downarrow$	0.8		ns
t_{su}	Setup time, P1_VSYNC, valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_VSYNC, valid after P1x_CLK $\uparrow\downarrow$	0.8		ns
t_{su}	Setup time, P1_HSYNC, valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_HSYNC, valid after P1x_CLK $\uparrow\downarrow$	0.8		ns
t_{su}	Setup time, P1_FIELD, valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_FIELD, valid after P1x_CLK $\uparrow\downarrow$	0.8		ns
t_{su}	Setup time, P1_DATEN, valid before P1x_CLK $\uparrow\downarrow$	0.8		ns
t_h	Hold time, P1_DATEN, valid after P1x_CLK $\uparrow\downarrow$	0.8		ns

(1) Use the following formula to obtain the jitter: Maximum clock jitter = $\pm[(1 / f_{\text{clock}}) - 5414 \text{ ps}]$.

(2) ALF_CSYNC, ALF_VSYNC and ALF_HSYNC are asynchronous signals.

(3) Setup and hold times should be considered the same regardless of clock used [P1A_CLK, P1B_CLK, P1C_CLK].

6.11 Port 2 Input Pixel Interface (FPD-Link Compatible LVDS Input) Timing Requirements⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾⁽⁶⁾

		MIN	MAX	UNIT
f_{clock}	Clock frequency, P2_CLK (LVDS input clock)	20	90	MHz
t_c	Cycle time, P2_CLK (LVDS input clock)	11.1	50	ns
t_{slew}	Clock or data slew rate ($f_{\text{pxck}} < 90 \text{ MHz}$)	0.3		V/ns
	Clock or data slew rate ($f_{\text{pxck}} > 90 \text{ MHz}$)	0.5		V/ns
t_{startup}	Link start-up time (internal)		1	ms

(1) Minimize crosstalk and match traces on the PCB as close as possible.

(2) Maintain the common mode voltage as close to 1.2 V as possible.

(3) Maintain the absolute input differential voltage as high as possible.

(4) The LVDS open input detection is related to a low common mode voltage only. It is not related to a low-differential swing.

(5) LVDS power 3.3-V supply (VDD33_FPD) noise level should be below 100 mV_{pp}.

(6) LVDS power 1.2-V supply (VDD12_FPD) noise level should be below 60 mV_{pp}.

6.12 Synchronous Serial Port (SSP) Interface Timing Requirements

		MIN	MAX	UNIT
t_{su}	Setup time, SSP0_RXD valid before SSP0_CLK↓	10		ns
t_h	Hold time, SSP0_RXD valid after SSP0_CLK↓	10		ns
t_t	Transition time ⁽¹⁾ , SSP0_RXD, $t_t = t_f / t_r$		4	ns
t_{su}	Setup time, SSP1_RXD valid before SSP1_CLK↓	10		ns
t_h	Hold time, SSP1_RXD valid after SSP1_CLK↓	10		ns
t_t	Transition time ⁽¹⁾ , SSP1_RXD, $t_t = t_f / t_r$		4	ns

(1) 20% to 80% reference points (signal)

6.13 Programmable Output Clocks Switching Characteristics

over operating free-air temperature range, C_L (min timing) = 5 pF, C_L (max timing) = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock} Clock frequency, OCLKC ⁽¹⁾	N/A	OCLKC	0.7759	48	MHz
t_c Cycle time, OCLKC ⁽¹⁾	N/A	OCLKC	20.83	1288.8	ns
$t_{w(H)}$ Pulse duration, high 50% to 50% reference points (signal)	N/A	OCLKC	$(t_c / 2) - 2$		ns
$t_{w(L)}$ Pulse duration, low ⁽²⁾ 50% to 50% reference points (signal)	N/A	OCLKC	$(t_c / 2) - 2$		ns
f_{clock} Clock frequency, OCLKD ⁽¹⁾	N/A	OCLKD	0.7759	48	MHz
t_c Cycle time, OCLKD	N/A	OCLKD	20.83	1288.8	ns
$t_{w(H)}$ Pulse duration, high ⁽²⁾ 50% to 50% reference points (signal)	N/A	OCLKD	$(t_c / 2) - 2$		ns
$t_{w(L)}$ Pulse duration, low ⁽²⁾ 50% to 50% reference points (signal)	N/A	OCLKD	$(t_c / 2) - 2$		ns
f_{clock} Clock frequency, OCLKE ⁽¹⁾	N/A	OCLKE	0.7759	48	MHz
t_c Cycle time, OCLKE	N/A	OCLKE	20.83	1288.8	ns
$t_{w(H)}$ Pulse duration, high ⁽²⁾ 50% to 50% reference points (signal)	N/A	OCLKE	$(t_c / 2) - 2$		ns
$t_{w(L)}$ Pulse duration, low ⁽²⁾ 50% to 50% reference points (signal)	N/A	OCLKE	$(t_c / 2) - 2$		ns

(1) The frequency of OCLKC through OCLKE is programmable.

(2) The duty cycle of OCLKC through OCLKE is within ± 2 ns of 50%.

6.14 Synchronous Serial Port (SSP) Interface Switching Characteristics

over recommended operating conditions, C_L (min timing) = 5 pF, C_L (max timing) = 35 pF (unless otherwise noted) (see Figure 10)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, SSP0_CLK ⁽¹⁾⁽²⁾	N/A	SSP0_CLK	0.287	9333	kHz
t_c	Cycle time, SSP0_CLK	N/A	SSP0_CLK	0.107	3483	us
$t_{w(H)}$	Pulse duration, high 50% to 50% reference points (signal)	N/A	SSP0_CLK	48		ns
$t_{w(L)}$	Pulse duration, low 50% to 50% reference points (signal)	N/A	SSP0_CLK	48		ns
t_{pd}	Output propagation, clock to Q, SSP0_TXD	SSP0_CLK \uparrow	SSP0_TXD	-5	5	ns
f_{clock}	Clock frequency, SSP1_CLK ⁽¹⁾⁽²⁾	N/A	SSP1_CLK	2.296	74667	kHz
t_c	Cycle time, SSP1_CLK	N/A	SSP1_CLK	0.013	436	us
$t_{w(H)}$	Pulse duration, high 50% to 50% reference points (signal)	N/A	SSP1_CLK	5.85		ns
$t_{w(L)}$	Pulse duration, low 50% to 50% reference points (signal)	N/A	SSP1_CLK	5.85		ns
t_{pd}	Output propagation, clock to Q, SSP1_TXD	SSP1_CLK \uparrow	SSP1_TXD	-2	2	ns

- (1) SSP output timing supports both positive and negative clocking polarity. Figure 10 shows only positive clocking polarity. When the clock polarity is configured through software to be negative, the data is transferred and captured on the opposite edge of the clock shown.
- (2) The maximum rates shown apply to master mode operation only. Slave mode operation is limited to 1/6 of these rates.

6.15 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

Over operating free-air temperature range, C_L (min timing) = 5 pF, C_L (max timing) = 85 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{pd}	Output propagation, clock to Q	TCK \downarrow	TDO1	3	12	ns

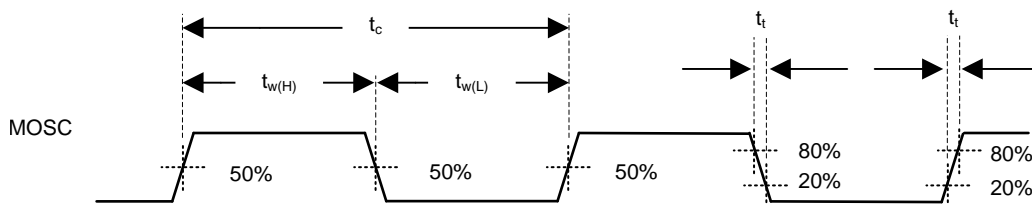
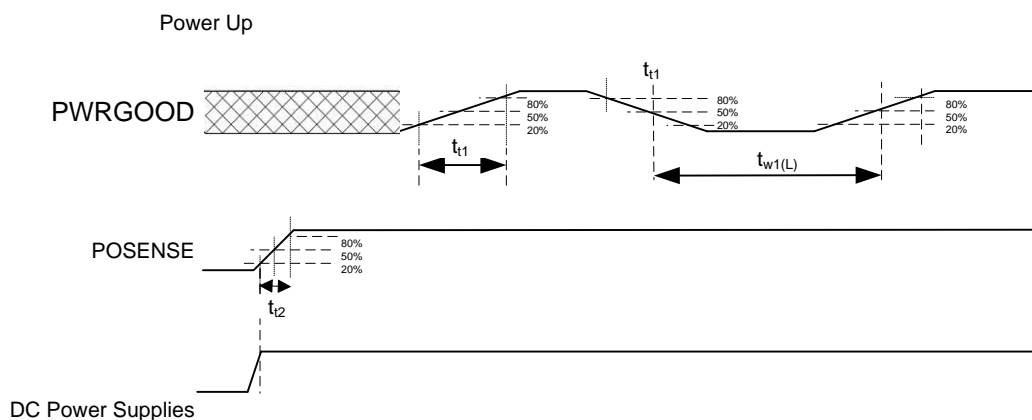


Figure 1. System Oscillators



PWRGOOD has no impact on operation for 60 ms after rising edge of POSENSE.

Figure 2. Power Up

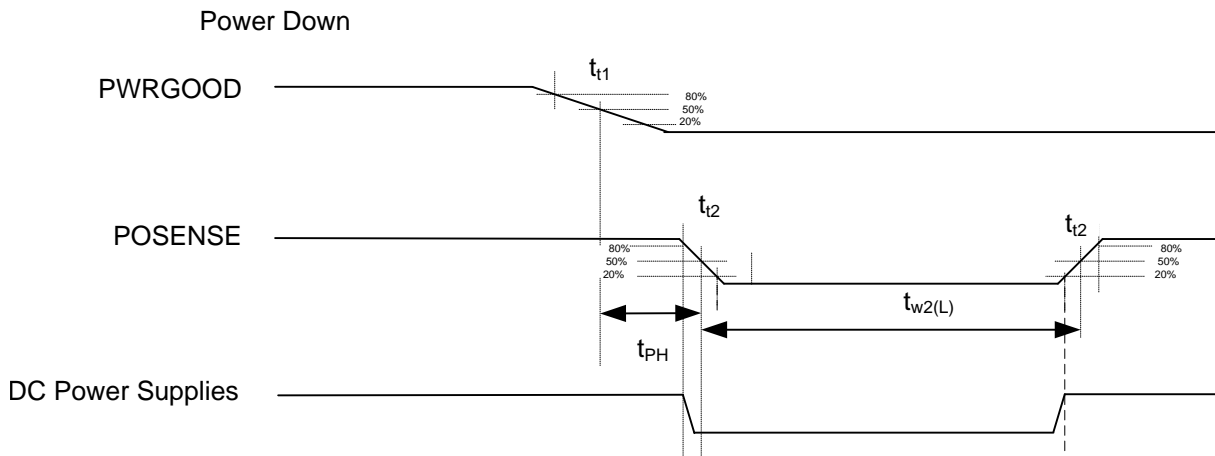


Figure 3. Power Down

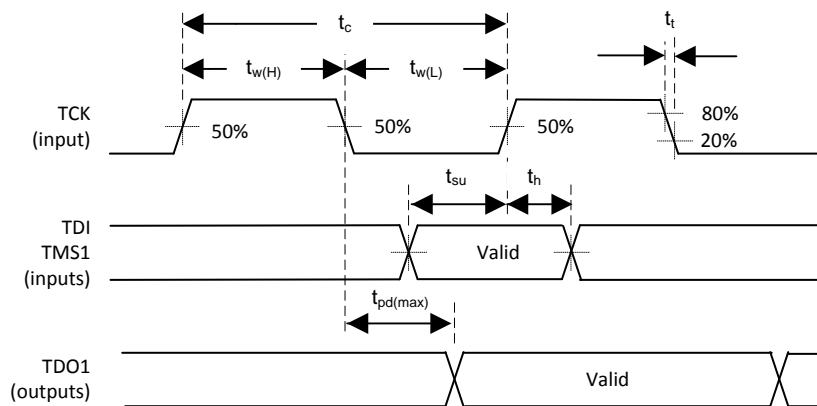


Figure 4. I/O Boundary Scan

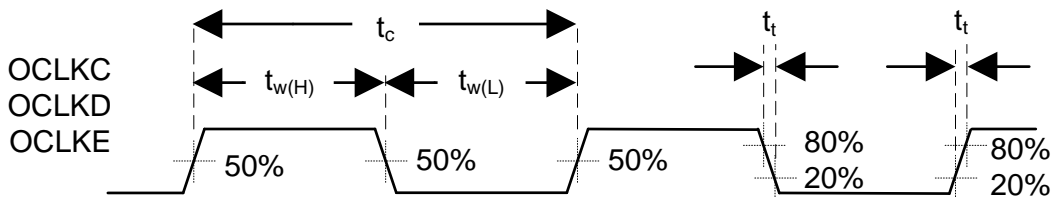


Figure 5. Programmable Output Clocks

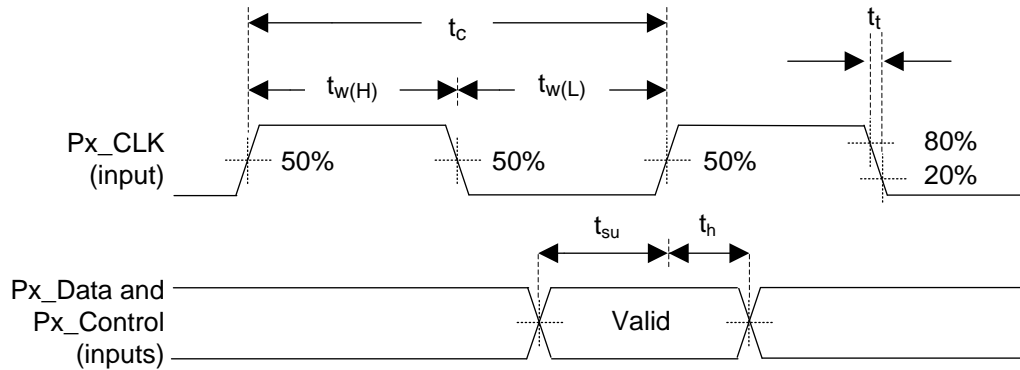


Figure 6. Input Port 1 Interface

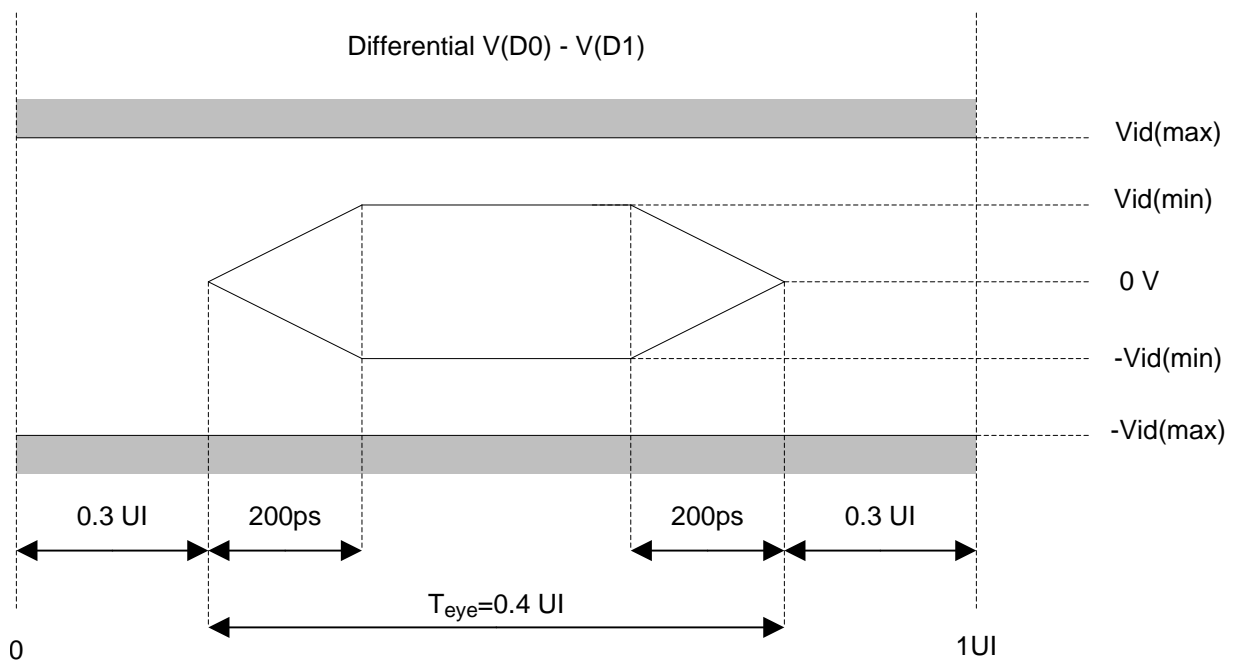


Figure 7. Input Port 2 (LVDS) Interface

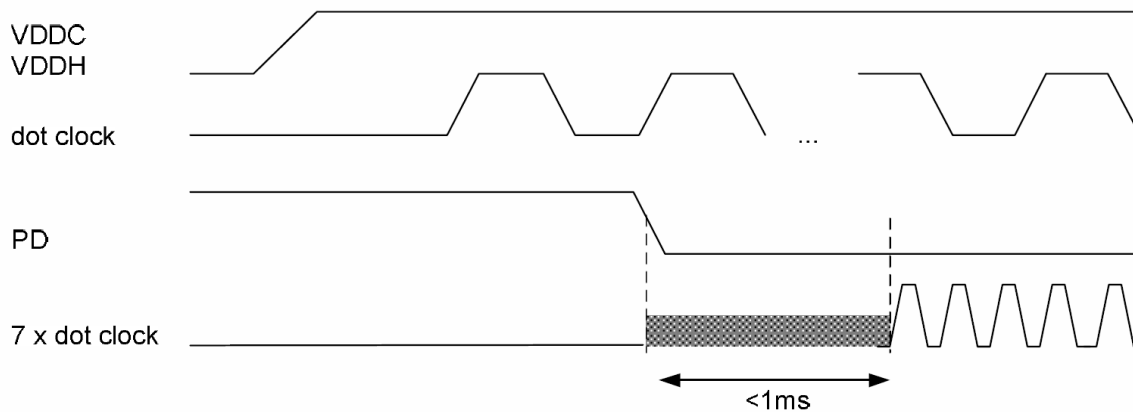


Figure 8. (LVDS) Link Start-Up Timing

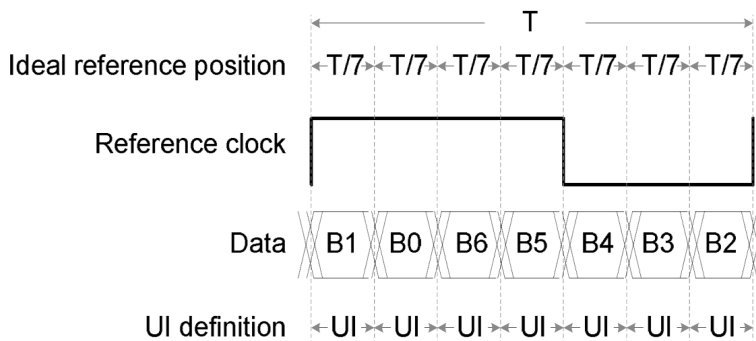


Figure 9. (LVDS) Clock – Data Skew Definition

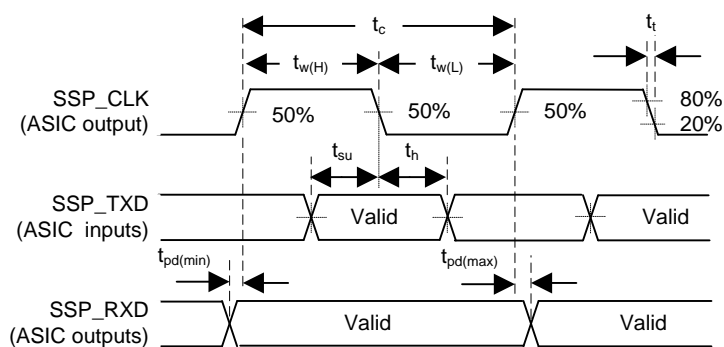


Figure 10. Synchronous Serial Port Interface

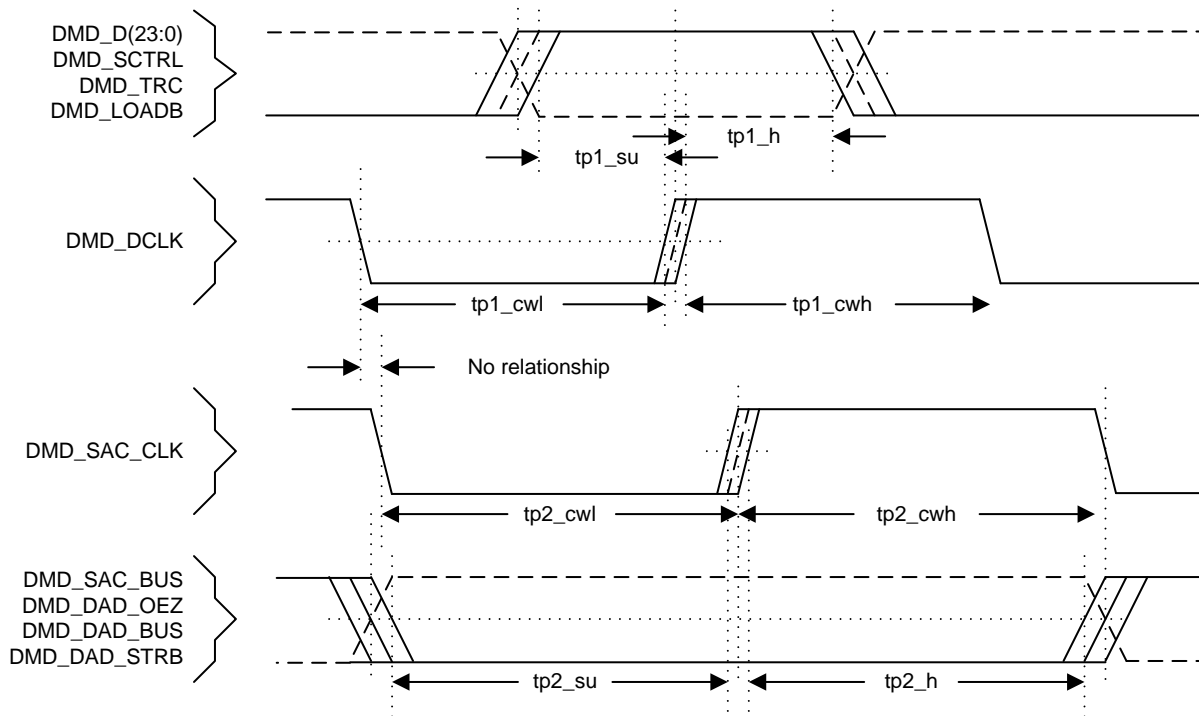


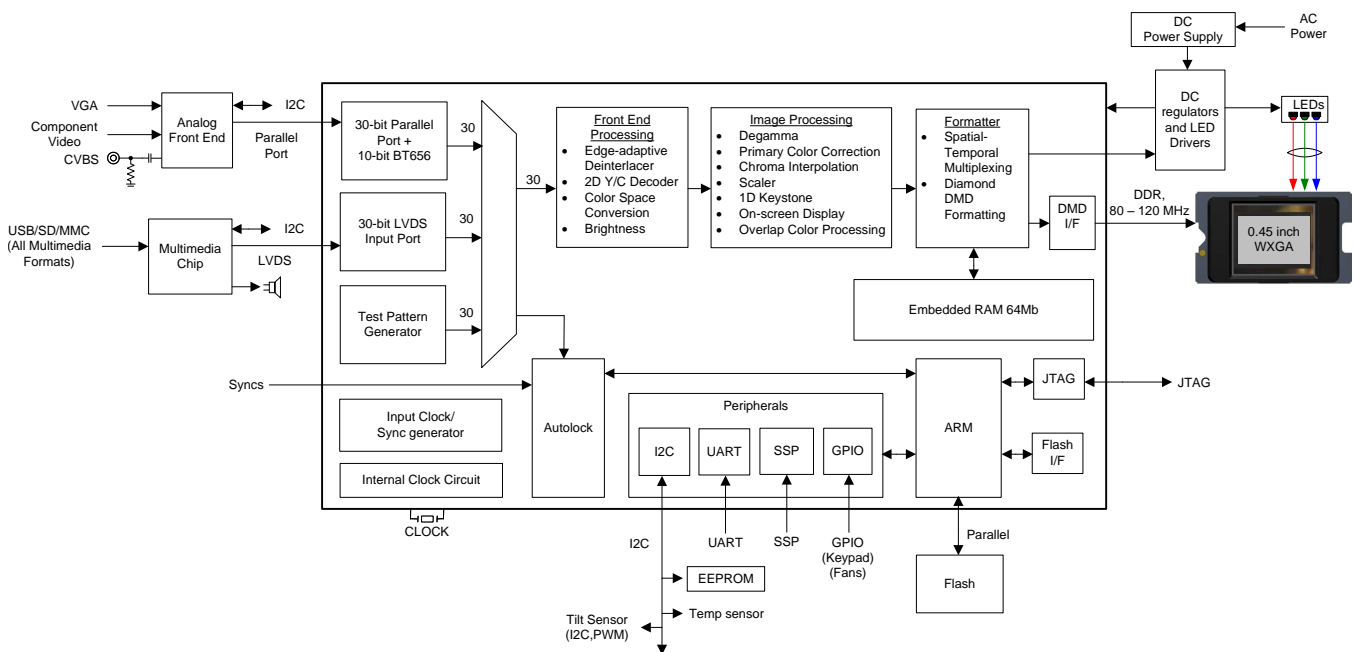
Figure 11. DMD LPDDR Interface

7 Detailed Description

7.1 Overview

The DLPC6401 is the display controller for the DLP4500 (.45 WXGA) DMD. DLPC6401 is part of the chipset comprised of the DLPC6401 controller and DLP4500 (.45 WXGA) DMD. Both the controller and the DMD must be used in conjunction with each other for reliable operation of the DLP4500 (.45 WXGA) DMD. The DLPC6401 display controller provides interfaces and data- and image-processing functions that are optimized for small form factor, high-resolution, and high-brightness display applications. Applications include pico projectors, smart projectors, screenless displays, interactive displays, wearable displays, and digital signage. Standalone projectors must include a separate front-end chip to interface to the outside world (for example, video decoder, HDMI receiver, triple ADC, or USB I/F chip).

7.2 Functional Block Diagram



7.3 Feature Description

Table 2. (LVDS) Receiver Supported Pixel Mapping Modes⁽¹⁾

LVDS RECEIVER INPUT	MAPPING SELECTION 1	MAPPING SELECTION 2	MAPPING SELECTION 3	MAPPING SELECTION 4 ⁽²⁾ [18-Bit Mode]
RA Input Channel				
RDA(6)	Map to GRN(4)	Map to GRN(2)	Map to GRN(0)	Map to GRN(4)
RDA(5)	Map to RED(9)	Map to RED(7)	Map to RED(5)	Map to RED(9)
RDA(4)	Map to RED(8)	Map to RED(6)	Map to RED(4)	Map to RED(8)
RDA(3)	Map to RED(7)	Map to RED(5)	Map to RED(3)	Map to RED(7)
RDA(2)	Map to RED(6)	Map to RED(4)	Map to RED(2)	Map to RED(6)
RDA(1)	Map to RED(5)	Map to RED(3)	Map to RED(1)	Map to RED(5)
RDA(0)	Map to RED(4)	Map to RED(2)	Map to RED(0)	Map to RED(4)
RB Input Channel				
RDB(6)	Map to BLU(5)	Map to BLU(3)	Map to BLU(1)	Map to BLU(5)
RDB(5)	Map to BLU(4)	Map to BLU(2)	Map to BLU(0)	Map to BLU(4)
RDB(4)	Map to GRN(9)	Map to GRN(7)	Map to GRN(5)	Map to GRN(9)
RDB(3)	Map to GRN(8)	Map to GRN(6)	Map to GRN(4)	Map to GRN(8)
RDB(2)	Map to GRN(7)	Map to GRN(5)	Map to GRN(3)	Map to GRN(7)
RDB(1)	Map to GRN(6)	Map to GRN(4)	Map to GRN(2)	Map to GRN(6)
RDB(0)	Map to GRN(5)	Map to GRN(3)	Map to GRN(1)	Map to GRN(5)
RC Input Channel				
RDC(6)	Map to DEN			
RDC(5)	Map to VSYNC			
RDC(4)	Map to HSYNC			
RDC(3)	Map to BLU(9)	Map to BLU(7)	Map to BLU(5)	Map to BLU(9)
RDC(2)	Map to BLU(8)	Map to BLU(6)	Map to BLU(4)	Map to BLU(8)
RDC(1)	Map to BLU(7)	Map to BLU(5)	Map to BLU(3)	Map to BLU(7)
RDC(0)	Map to BLU(6)	Map to BLU(4)	Map to BLU(2)	Map to BLU(6)
RD Input Channel				
RDD(6)	Map to field (option 1 if applicable)			
RDD(5)	Map to BLU(3)	Map to BLU(9)	Map to BLU(7)	No mapping
RDD(4)	Map to BLU(2)	Map to BLU(8)	Map to BLU(6)	No mapping
RDD(3)	Map to GRN(3)	Map to GRN(9)	Map to GRN(7)	No mapping
RDD(2)	Map to GRN(2)	Map to GRN(8)	Map to GRN(6)	No mapping
RDD(1)	Map to RED(3)	Map to RED(9)	Map to RED(7)	No mapping
RDD(0)	Map to RED(2)	Map to RED(8)	Map to RED(6)	No mapping
RE Input Channel				
RDE(6)	Map to field (option 2 if applicable)			
RDE(5)	Map to BLU(1)		Map to BLU(9)	No mapping
RDE(4)	Map to BLU(0)		Map to BLU(8)	No mapping
RDE(3)	Map to GRN(1)		Map to GRN(9)	No mapping
RDE(2)	Map to GRN(0)		Map to GRN(8)	No mapping
RDE(1)	Map to RED(1)		Map to RED(9)	No mapping
RDE(0)	Map to RED(0)		Map to RED(8)	No mapping

(1) Mapping options are selected by software.

(2) If mapping option 4 is the only mapping mode needed, and if, and only if, a 'Field 1' or 'Field 2' input is not needed, then the board layout can leave the LVDS inputs for RD and RE channels floating.

7.3.1 System Reset Operation

7.3.1.1 Power-Up Reset Operation

Immediately following a power-up event, DLPC6401 hardware automatically brings up the master PLL and places the ASIC in normal power mode. It then follows the standard system reset procedure (see [System Reset Operation](#)).

7.3.1.2 System Reset Operation

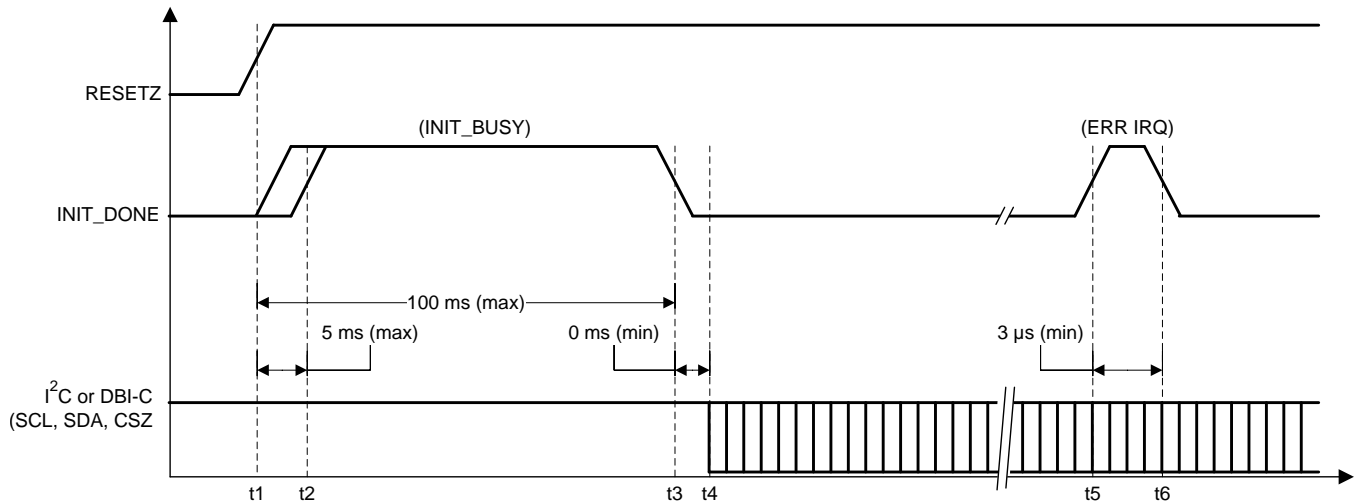
Immediately following any type of system reset (power-up reset, PWRGOOD reset, watchdog timer timeout, and so on), the DLPC6401 device automatically returns to NORMAL power mode and returns to the following state.

- All GPIO tri-state and as a result, all GPIO-controlled voltage switches default to enabling power to all ASIC supply lines. (Assume these outputs are externally pulled-high.)
- The master PLL remains active (it is reset only after a power-up reset sequence) and most of the derived clocks are active. However, only those resets associated with the ARM9 processor and its peripherals are released. (The ARM9 is responsible for releasing all other resets.)
- ARM9 associated clocks default to their *full clock rates*. (Boot-up is a full speed.)
- All front-end derived clocks are disabled.
- The PLL feeding the DDR DMD I/F (PLLD) defaults to its power-down mode and all derived clocks are inactive with corresponding resets asserted. (The ARM9 is responsible for enabling these clocks and releasing associated resets.)
- DMD I/O (except DMD_DAD_OEZ) defaults to its outputs in a logic low state. DMD_DAD_OEZ defaults tri-stated, but should be pulled high through an external 30- to 51-k Ω pullup resistor on the PCB.
- All resets output by the DLPC6401 device remain asserted until released by the ARM9 (after boot-up).
- The ARM9 processor boots-up from external flash.

When the ARM9 boots-up, the ARM9 API:

- Configures the programmable DDR clock generator (DCG) clock rates (that is, the DMD LPDDR I/F rate)
- Enables the DCG PLL (PLLD) while holding divider logic in reset
- When the DCG PLL locks, ARM9 software sets DMD clock rates
- API software then releases DCG divider logic resets, which in turn, enable all derived DCG clocks
- Releases external resets

Application software then typically waits for a wake-up command (through the soft power switch on the projector) from the end user. When the projector is requested to wake-up, the software places the ASIC back in normal mode, re-initialize clocks, and resets as required.



- t2: device drives INIT_DONE high within 5 ms after reset is release. Indicates auto-initialization is busy
- t3: I²C or DBI-C access to DLPC6401 device does not start until the INIT_BUSY flag (on INIT_DONE) goes low. This can occur within 100 ms, but may take several seconds
- t5: an active high pulse on INIT_DONE following the initialization period indicates a detected error condition. The device reports the source of the error in the system status.

Figure 12. Internal Memory Test Diagram

7.3.1.3 Spread Spectrum Clock Generator Support

The DLPC6401 device supports limited, internally-controlled, spread spectrum clock spreading on the DMD interface. The purpose is to frequency spread all signals on the high-speed, external interfaces to reduce EMI emissions. Clock spreading is limited to triangular waveforms. The DLPC6401 device provides modulation options of 0%, ±0.5%, and ±1.0% (center-spread modulation).

7.3.1.4 GPIO Interface

The DLPC6401 device provides 38 software-programmable, general-purpose I/O pins. Each GPIO pin is individually configurable as either input or output. In addition, each GPIO output can be either configured as push-pull or open-drain. Some GPIO have one or more alternate-use modes, which are also software configurable. The reset default for all GPIO is as an input signal. However, any alternate function connected to these GPIO pins, with the exception of general-purpose clocks and PWM generation, will be reset. When configured as open-drain, the outputs must be externally pulled-up (to the 3.3-V supply). External pullup or pulldown resistors may be required to ensure stable operation before software is able to configure these ports.

7.3.1.5 Source Input Blanking

Vertical and horizontal blanking requirements for both input ports are defined as follows (see [视频时序参数定义](#)).

- Minimum port 1 vertical blanking:
 - Vertical back porch: 370 μs
 - Vertical front porch: 2 lines
 - Total vertical blanking: 370 μs + 3 lines
- Minimum port 2 vertical blanking:
 - Vertical back porch: 370 μs
 - Vertical front porch: 0 lines
 - Total vertical blanking: 370 μs + 3 lines
- Minimum port 1 and port 2 horizontal blanking:
 - Horizontal back porch (HBP): 10 pixels
 - Horizontal front porch (HFP): 0 pixels
 - Total horizontal blanking (THB):

- 0.45 WXGA DMD: Roundup (154286 / Source_APPL, 0)
- 0.4 XGA DMD: Roundup (144686 / Source_APPL, 0) pixels

7.3.1.6 Video and Graphics Processing Delay

The DLPC6401 device introduces a fixed number of field and frame delays. For optimum audio and video synchronization, this delay must be matched in the audio path. [Table 3](#) defines the video delay to support audio matching.

Frame and fields in [Table 3](#) refer to source frames and fields.

Table 3. Primary Channel and Video-Graphics Processing Delay

SOURCE	2D VIDEO DECODER	DE-INTERLACING	FORMATTER BUFFER	TOTAL DELAY
10 to 47 Hz Non-interlaced graphics	Disabled {0 frames}	Disabled {0 frames}	Enabled {1 frame}	1 frame
47 to 63 Hz Non-interlaced graphics	Disabled {0 frames}	Disabled {0 frames}	Enabled {1 frame}	1 frame
63 to 120 Hz Non-interlaced graphics	Disabled {0 frames}	Disabled {0 frames}	Enabled {1 frame}	1 frame
100 to 120 Hz Display at native rate graphics	Disabled {0 frames}	Disabled {0 frames}	Enabled {1 frame}	1 frame
50 to 60 Hz interlaced SDTV video (NTSC, PAL, SECAM)	Enabled {0 fields}	Edge adaptive de-interlacing enabled {0 fields}	Enabled {1 field}	1 field
60 Hz interlaced HDTV video (480i, 1080i)	Disabled {0 fields}	Edge adaptive de-interlacing enabled {0 fields}	Enabled {1 field}	1 field
24 to 30 Hz interlaced HDTV video (480i, 1080i)	Disabled {0 fields}	Edge adaptive de-interlacing enabled {0 fields}	Enabled {1 field}	1 field
60 Hz progress HDTV video (480p, 720p)	Disabled {0 frames}	N/A {0 frames}	Enabled {1 frame}	1 frame
24 to 30 Hz Progress HDTV video (480p, 720p)	Disabled {0 frames}	N/A {0 frames}	Enabled {1 frame}	1 frame
63 to 87 Hz Interlaced graphics ≤1280 APPL and ≤75 MHz	Disabled {0 fields}	Edge adaptive de-interlacing enabled {0 fields}	Enabled {1 field}	1 field
63 to 87 Hz Interlaced graphics >1280 APPL or >75 MHz	Disabled {0 fields}	Field-dependent scaling enabled {0 fields}	Enabled {1 field}	1 field

7.3.2 Program Memory Flash/SRAM Interface

The DLPC6401 device provides three external program memory chip selects:

- PM_CSZ_0 – Available for optional SRAM or flash device (≤128 Mb)
- PM_CSZ_1 – Dedicated CS for boot flash device (that is standard NOR-type flash, ≤128 Mb)
- PM_CSZ_2 – Available for optional SRAM or flash device (≤128 Mb)

Flash and SRAM access timing is software programmable up to 31 wait states. Wait state resolution is 6.7 ns in normal mode and 53.57 ns in low-power modes. [Table 4](#) shows wait state program values for typical flash access times.

Table 4. Wait State Program Values for Typical Flash Access Times

	NORMAL MODE ⁽¹⁾	LOW-POWER MODE ⁽¹⁾
Formula to Calculate the Required Wait State Value	= Roundup (Device_Access_Time / 6.7 ns)	= Roundup (Device_Access_Time / 53.57 ns)
Max Supported Device Access Time	207 ns	1660 ns

(1) Assumes a maximum single direction trace length of 75 mm.

Note that when another device such as an SRAM or additional flash is used in conjunction with the boot flash, care must be taken to keep stub length short and located as close as possible to the flash end of the route.

The DLPC6401 device provides enough Program Memory Address pins to support a flash or SRAM device up to 128 Mb. For systems not requiring this capacity, up to two address pins can be used as GPIO instead. Specifically, the two most significant address bits (that is PM_ADDR_22 and PM_ADDR_21) are shared on pins GPIO_16 and GPIO_17 respectively. Like other GPIO pins, these pins float in a high-impedance input state following reset; therefore, if these GPIO pins are to be reconfigured as Program Memory Address pins, they require board-level pulldown resistors to prevent any Flash address bits from floating until software is able to reconfigure the pins from GPIO to Program Memory Address. Also note, that until software reconfigures the pins from GPIO to Program Memory Address, upper portions of flash memory are not accessible.

Table 5 shows typical GPIO_16 and GPIO_17 pin configurations for various flash sizes.

Table 5. Typical GPIO_16 and GPIO_17 Pin Configurations for Various Flash Sizes

FLASH SIZE	GPIO_36 PIN CONFIGURATION	GPIO_35 PIN CONFIGURATION
32 Mb or less	GPIO_17	GPIO_16
64 Mb	GPIO_17	PM_ADDR_21(*) ⁽¹⁾
128 Mb	PM_ADDR_22(*) ⁽¹⁾	PM_ADDR_21(*) ⁽¹⁾

(1) (*) = Board-level pulldown resistor required

7.3.2.1 Calibration and Debug Support

The DLPC6401 device contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pulldown resistor and thus external pullups are used to modify the default test configuration. The default configuration (x00) corresponds to the TSTPT(7:0) outputs being driven low for reduce switching activity during normal operation. For maximum flexibility, TI recommends an option to jumper to an external pullup for TSTPT(0). Note that adding a pullup to TSTPT(7:1) may have adverse affects for normal operation and TI does not recommend it. Note that these external pullups are sampled only after a 0-to-1 transition on POSENSE and thus changing their configuration after reset has been released does not have any affect until the next time reset is asserted and released. Table 6 defines the test mode selection for two programmable scenarios defined by TSTPT_(0):

Table 6. Test Mode Selection

TSTPT(3:0) CAPTURE VALUE	NO SWITCHING ACTIVITY	ARM AHB DEBUG SIGNAL SET
	x0	x1
TSTPT(0)	0	ARM9 HREADY
TSTPT(1)	0	HSEL for all external program memory
TSTPT(2)	0	ARM9 HTRANS ⁽¹⁾
TSTPT(3)	0	PFC HREADY OUT (ARM9 R/W)
TSTPT(4)	0	PFC EMI ⁽²⁾ request (ARM9 R/W)
TSTPT(5)	0	PFC EMI ⁽²⁾ request accept (ARM9 R/W)
TSTPT(6)	0	PFC EMI ⁽²⁾ access done (ARM9 R/W)
TSTPT(7)	0	ARM9 Gate_The_Clk

(1) These are only the default output selections. Software can reprogram the selection at any time.

(2) PFC EMI is the parallel flash controller external memory interface

7.3.2.2 Board-Level Test Support

The in-circuit tri-state enable signal (ICTSEN) is a board-level test control signal. By driving ICTSEN to a logic-high state, all ASIC outputs (except TDO1 and TDO2) are tri-stated.

The DLPC6401 device also provides JTAG boundary scan support on all I/O signals, non-digital I/O, and a few special signals. Table 7 defines these exceptions.

Table 7. DLPC6401 – Signals Not Covered by JTAG

SIGNAL NAME	PKG BALL
TDO2	M18
TMS2	V16
MOSC	A14
MOSCN	A15
VPGM	D17
EXRES	A3
RA_IN_P	AB10
RA_IN_N	AA10
RB_IN_P	Y11
RB_IN_N	W11
RC_IN_P	AB12
RC_IN_N	AA12
RD_IN_P	Y13
RD_IN_N	W13
RE_IN_P	AB14
RE_IN_N	AA14
RCK_IN_P	Y9
RCK_IN_N	W9

7.4 Device Functional Modes

DLPC6401 has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the projector automatically powers up and an image is projected from the DMD.
- When pin PROJ_ON is set low, the projector automatically powers down to save power.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLCP6401 controller is required to be coupled with DLP4500 DMD to provide a reliable display solution for various data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLCP6401. Applications of interest include accessory projectors, smart projectors, screenless display, embedded in display devices like notebooks, laptops, tablets, and hot spots. Other applications include wearable (near-eye or head mounted) displays, interactive displays, low-latency gaming displays, and digital signage.

8.2 Typical Application

A common application when using the DLCP6401 is for creating a pico-projector that can be used as an accessory to a smartphone, tablet, or laptop. The DLCP6401 in the pico-projector receives images from a multimedia front-end within the product as shown in Figure 13.

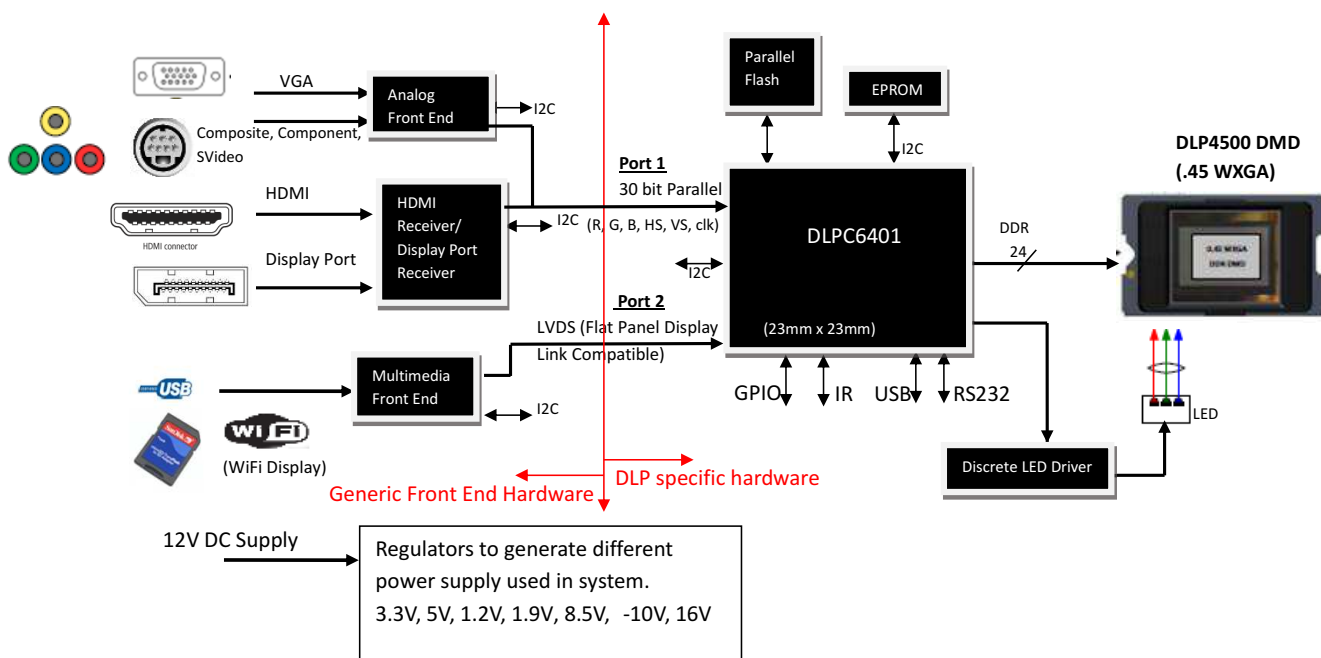


Figure 13. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

A pico-projector is created by using a DLP chipset comprised of DLP4500 DMD and a DLPC6401 controller. The DLPC6401 controller does the digital image processing and the DLP4500 DMD is the display device for producing the projected image. In addition to these DLP chips in the chipset, other chips may be needed. Typically a Flash part is needed to store the software and firmware. Additionally, a discrete LED driver solution is required to provide the LED driver functionality for LED illumination. The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector. DLPC6401 controller provides either parallel- or LVDS-interface to connect the DLPC6401 controller to the multimedia front-end for receiving images and video.

8.2.1.1 Recommended MOSC Crystal Oscillator Configuration

Table 8. Crystal Port Characteristics

PARAMETER	NOMINAL	UNIT
MOSC to GND capacitance	3.9	pF
MOSCZ to GND capacitance	3.8	pF

Table 9. Recommended Crystal Configuration⁽¹⁾

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	32	MHz
Crystal frequency temperature stability	±30	PPM
Overall crystal frequency tolerance (including accuracy, stability, aging, and trim sensitivity)	±100	PPM
Crystal ESR	50 (max)	Ω
Crystal load	10	pF
Crystal shunt load	7 (max)	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1	MΩ
CL1 external crystal load capacitor (MOSC)	See ⁽¹⁾	pF
CL2 external crystal load capacitor (MOSCN)	See ⁽¹⁾	pF
PCB layout	TI recommends a ground isolation ring around the crystal.	

(1) Typical drive level with the TCX 9C32070001 crystal (ESR_{max} = 30 Ω) = 160 μW

C_L = Crystal load capacitance (Farads)
 $C_{L1} = 2 * (C_L - C_{Stray-MOSC})$
 $C_{L2} = 2 * (C_L - C_{Stray-MOSCN})$
 $C_{Stray-MOSC}$ = Sum of Package & PCB capacitance at the crystal pin associated with ASIC signal MOSC.
 $C_{Stray-MOSCN}$ = Sum of Package & PCB capacitance at the crystal pin associated with ASIC signal MOSCN.

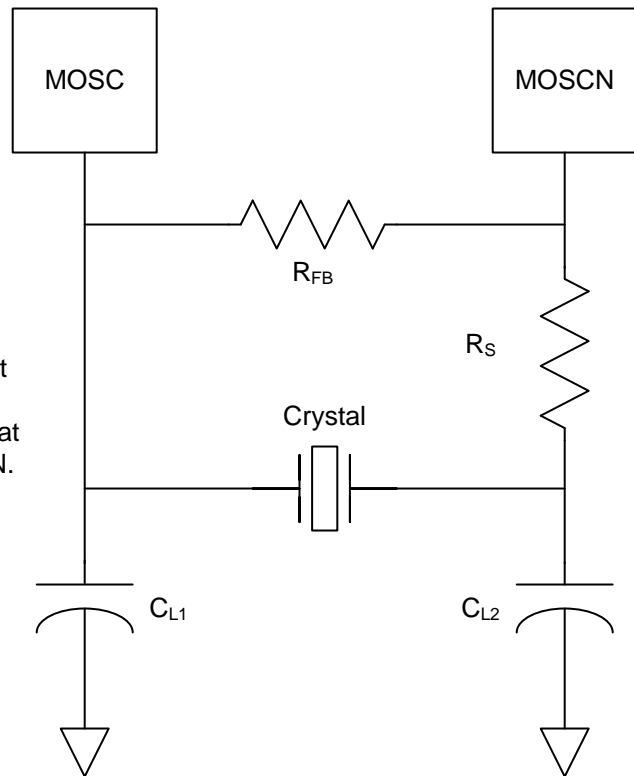


Figure 14. Recommended Crystal Oscillator Configuration

It is assumed that the external crystal oscillator will stabilize within 50 ms after stable power is applied.

8.2.2 Detailed Design Procedure

For connecting the DLPC6401 controller and the DLP4500 DMD together, see the reference design schematic. Layout guidelines should be followed to achieve a reliable projector. To complete the DLP system, an optical module or light engine is required that contains the DLP4500 DMD, associated illumination sources, optical elements, and necessary mechanical components.

8.2.3 Application Curve

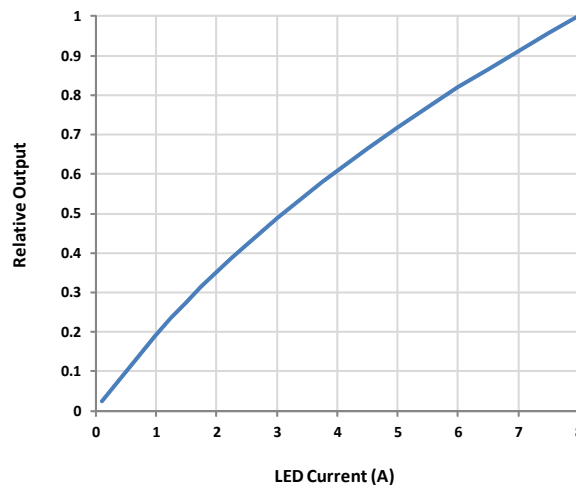


Figure 15. Relative Output vs LED Current

9 Power Supply Recommendations

9.1 System Power Regulation

Table 10 shows the recommended power delivery budget for DC offset and AC noise as observed at the corresponding DLPC6401 power pins.

Table 10. Recommended Power Delivery Budget for DC Offset and AC Noise

ASIC POWER RAIL	USAGE	NOMINAL VOLTAGE	TOTAL SUPPLY MARGIN ⁽¹⁾
VDDC	ASIC core	1.2 V	±5%
VDD12_PLLM/ VDD12_PLLD	Internal PLLs	1.2 V	±5%
VDD_18_PLLM/ VDD18_PLLD	Internal PLLs	1.8 V	±5% ⁽²⁾
VDD_DMD	DMD LPDDR I/O	1.9 V	±5%
VDD33	LVC MOS I/O	3.3 V	±5%
VDD12_FPD	FPD-Link LVDS I/F	1.2 V	±5%
VDD33_FPD	FPD-Link LVDS I/F	3.3 V	±5%

(1) Total supply margin = DC offset budget + AC noise budget

(2) When possible, TI suggests that a tighter supply tolerance (±3%) be used for the 1.8-V power to the PLLs to improve system noise immunity

TI strongly recommends that the VDD_18_PLLM and VDD_18_PLLD power feeding internal PLLs be derived from an isolated linear regulator to minimize the AC noise component. It is acceptable for VDD12_PLLM and VDD12_PLLD to be derived from the same regulator as the core VDD12, but they should be filtered.

9.2 System Power-Up Sequence

Although the DLPC6401 device requires an array of power supply voltages (1.2 V, 1.8 V, 1.9 V, and 3.3 V), there are no restrictions regarding the relative order of power supply sequencing. This is true for both power-up and power-down scenarios. Similarly, there is no minimum time between powering-up and powering-down the different supplies feeding the DLPC6401 device. However, note that it is not uncommon for there to be power-sequencing requirements for the devices that share the supplies with the DLPC6401 device. For example:

- 1.2-V core power should be applied whenever any I/O power is applied. This ensures the state of the associated I/O that are powered are controlled to a known state. Thus, TI recommends to apply core power first. Other supplies should be applied only after the 1.2-V ASIC core has ramped up.
- All ASIC power should be applied before POSENSE is asserted to ensure proper power-up initialization is performed. 1.8-V PLL power, 1.9-V I/O power, and 3.3-V I/O power should remain applied as long as 1.2-V core power is applied and POSENSE is asserted.

It is assumed that all DLPC6401 device power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC6401 device in system reset during power-up (that is, POSENSE = 0). It should continue to assert system reset until *all* ASIC voltages have reached minimum specified voltage levels. During this time, all ASIC I/O are either tri-stated or driven low. The master PLL (PLLM) is released from reset upon the low-to-high transition of POSENSE, but the DLPC6401 device keeps the rest of the ASIC in reset for an additional 100 ms to allow the PLL to lock and stabilize its outputs. After this 100-ms delay, ARM9-related internal resets are de-asserted, causing the microprocessor to begin its boot-up routine.

Figure 16 shows the recommended DLPC6401 system power-up sequence.

System Power-Up Sequence (continued)

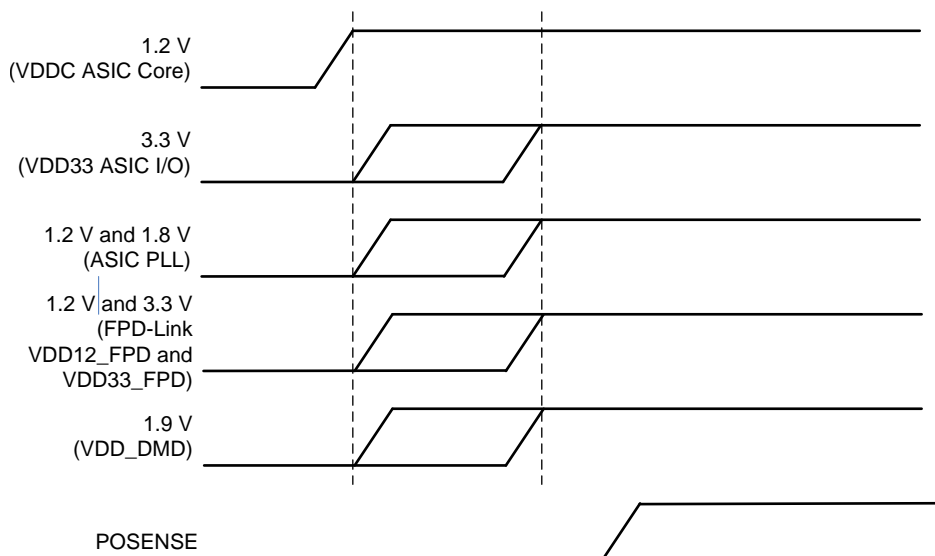


Figure 16. System Power-Up Sequence

9.3 Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the ASIC minimum supply voltage specification. Thus for practical reasons, TI recommends that the external power monitor generating POSENSE target its threshold to 90% of the minimum supply voltage specifications and ensure that POSENSE remain low a sufficient amount of time for all supply voltages to reach minimum ASIC requirements and stabilize. Note that the trip voltage for detecting the loss of power is not critical for POSENSE and thus may be as low as 50% of rated supply voltages. In addition, the reaction time to respond to a low voltage condition is not critical for POSENSE; however, PWRGOOD does have much more critical requirements in these areas.

9.4 System Environment and Defaults

9.4.1 DLPC6401 System Power-Up and Reset Default Conditions

Following system power-up, the DLPC6401 device performs a power-up initialization routine that defaults the ASIC to its normal power mode, in which ARM9-related clocks are enabled at their full rate and associated resets are released. Most other clocks default to disabled state with associated resets asserted until released by the processor. These same defaults are also applied as part of all system reset events (watch dog timer timeout, and so on) that occur without removing or cycling power.

Following power-up or system reset initialization, the ARM9 boots from an external flash memory after which it enables the rest of the ASIC clocks. When system initialization is complete, application software determines if and when to enter low-power mode.

9.4.2 1.2-V System Power

The DLPC6401 device can support a power delivery system with a single 1.2-V power source derived from a switching regulator. The DLPC6401 main core should receive 1.2-V power directly from the regulator output and the internal ASIC PLLs (**VDDC**, **VDD12_PLLD**, and **VDD12_PLLM**) should receive individually-filtered versions of this 1.2-V power. For specific filter recommendations, see [PCB Layout Guidelines for Internal ASIC Power](#).

9.4.3 1.8-V System Power

A single 1.8-V power source should be used to supply both DLPC6401 internal PLLs. To keep this power as clean as possible, TI recommends that this power be sourced by a linear regulator that is individually filtered for each PLL (**VDD_18_PLLD** and **VDD_18PLL**). For specific filter recommendations, see [PCB Layout Guidelines for Internal ASIC Power](#).

System Environment and Defaults (continued)

9.4.4 1.9-V System Power

To maximize signal integrity, TI recommends to use an independent linear regulator to source the 1.9-V supply that supports the DMD interface (**VDD_DMD**). To achieve maximum performance, this supply must be tightly regulated to operating within a 1.9-V ± 0.1 V range.

9.4.5 3.3-V System Power

The DLPC6401 device can support a power delivery system with a single 3.3-V power sources derived from a switching regulator. This 3.3-V power supplies all of the LVCMOS I/O. 3.3-V power should remain active in all power modes (**VDD33**) for which 1.2-V core power is applied.

9.4.6 FPD-Link Input LVDS System Power

The DLPC6401 device supports an FPD-Link compatible, LVDS input for an additional method of inputting video or graphics data for display. This interface has some special ASIC power considerations that are separate from the other ASIC 1.2- or 3.3-V power rails. [Figure 17](#) shows a FPD-Link 1.2-V power pin (**VDD12_FPD**) configuration example.

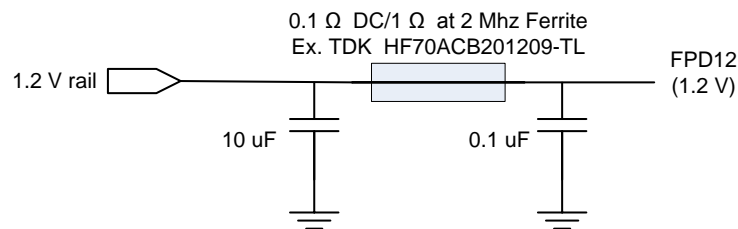


Figure 17. FPD-Link

In addition, TI recommends to place 0.1- μ F low equivalent series resistor (ESR) capacitors to ground as close to the FPD-Link lower pins of the ASIC as possible. FPD-Link 3.3-V power pins (**FPD33**) should also use external capacitors in the same manner as for **VDD12_FPD** pins.

When FPD-Link is not used, the user can omit the previously mentioned filtering. However, the corresponding voltages must still be provided to avoid potential long-term reliability issues.

9.4.7 Power Good (PWRGOOD) Support

The PWRGOOD signal is defined as an early warning signal that alerts the ASIC 500 μ s before DC supply voltages drop below specifications. This allows the ASIC to park the DMD ensuring the integrity of future operation. For practical reasons, TI recommends that the monitor sensing PWRGOOD be on the input side of supply regulators.

9.4.8 5-V Tolerant Support

The DLPC6401 device does not support any 5-V tolerant I/O. However, note that source signals ALF_HSYNC, ALF_VSYNC, and I²C typically have 5-V requirements and special measures must be taken to support them. TI recommends the use of a 5- to 3.3-V level shifter.

10 Layout

10.1 Layout Guidelines

TI recommends 2-ounce copper (2.6-mil) power and ground planes in the PCB design to achieve needed thermal connectivity.

10.1.1 PCB Layout Guidelines for Internal ASIC Power

TI recommends the following guidelines to achieve desired ASIC performance relative to internal PLLs:

- The DLPC6401 device contains two PLLs (PLL M and PLL D), each of which has a dedicated 1.2-V digital and 1.8-V analog supply. These 1.2-V PLL pins should be individually isolated from the main 1.2-V system supply through a ferrite bead. The impedance of the ferrite bead should be much greater than that of the capacitor at frequencies where noise is expected. Specifically the impedance of the ferrite bead must be less than 0.5 Ω in the frequency range of 100 to 300 kHz and greater than 10 Ω in the frequency range >100 MHz.
- As a minimum, 1.8-V analog PLL power and ground pins should be isolated using an LC-filter with a ferrite serving as the inductor and a 0.1-μF capacitor on the ASIC side of the ferrite. TI recommends that this 1.8-V PLL power be supplied from a dedicated linear regulator and each PLL should be individually isolated from the regulator. The same ferrite recommendations described for the 1.2-V digital PLL supply apply to the 1.8-V analog PLL supplies.
- When designing the overall supply filter network, take care to ensure no resonance occurs. Particularly take care around the 1- to 2-mHz band, as this coincides with the PLL natural loop frequency.

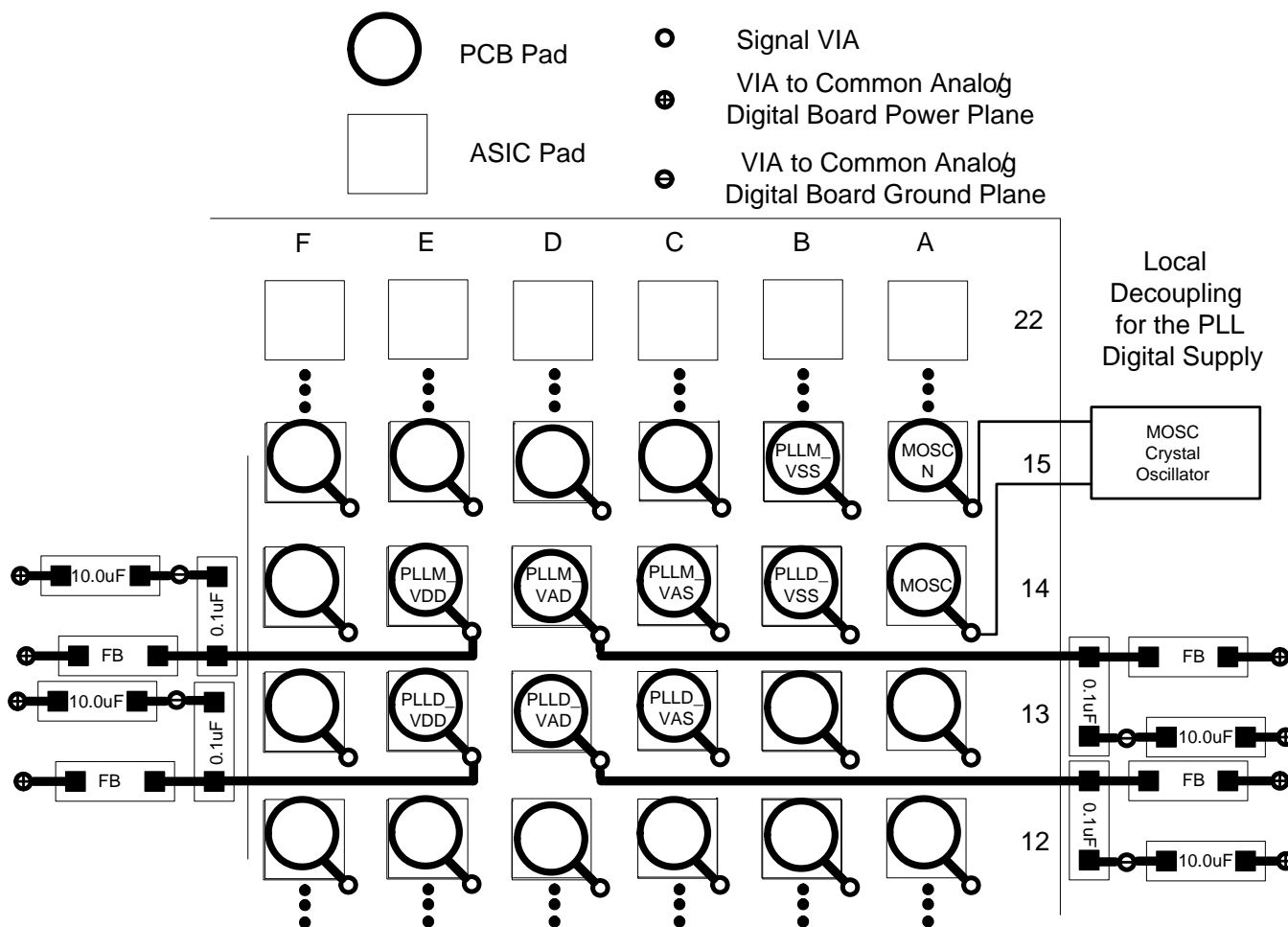


Figure 18. PLL Filter Layout

Layout Guidelines (continued)

High-frequency decoupling is required for both 1.2-V and 1.8-V PLL supplies and should be provided as close as possible to each of the PLL supply package pins. TI recommends placing decoupling capacitors under the package on the opposite side of the board. Use high-quality, low-ESR, monolithic, surface mount capacitors. Typically 0.1 μF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting, and thus, where possible, there should be no trace, allowing the via to butt up against the land itself. Additionally, the connecting trace should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design. Typically, a good ceramic capacitor in the 10- μF range is adequate.

10.1.2 PCB Layout Guidelines for Quality Auto-Lock Performance

One of the most important factors in getting good performance from Auto-Lock is to design the PCB with the highest-quality signal integrity possible. TI recommends the following:

- Place the ADC chip as close to the VESA/video connectors as possible.
- Avoid crosstalk to the analog signals by keeping them away from digital signals.
- Do not place the digital ground or power planes under the analog area between the VESA connector to the ADC chip.
- Avoid crosstalk onto the RGB analog signals. Separate them from the VESA Hsync and Vsync signals.
- Analog power should not be shared with the digital power directly.
- Try to keep the trace lengths of the RGB as equal as possible.
- Use good quality (1%) termination resistors for the RGB inputs to the ADC.
- If the green channel must be connected to more than the ADC green input and ADC sync-on-green input, provide a good-quality high-impedance buffer to avoid adding noise to the green channel.

10.1.3 DMD Interface Considerations

The DMD interface is modeled after the low-power DDR memory (LPDDR) interface. To minimize power dissipation, the LPDDR interface is defined to be unterminated. This makes good PCB signal integrity management imperative. In particular, impedance control and crosstalk mitigation is critical to robust operation. LPDDR board design recommendations include 3x design rules (that is, trace spacing = 3x trace width), $\pm 10\%$ impedance control, and signal routing directly over a neighboring reference plane (ground or 1.9-V plane).

DMD interface performance is also a function of trace length, so even with good board design, the length of the line limits performance. The DLPC6401 device works over a very-narrow range of DMD signal routing lengths at 120 MHz only. The device provides the option to reduce the interface clock rate to facilitate a longer interface (this includes 106.7-MHz, 96-MHz, 87.7-MHz, and 80-MHz programming options). However, note that reducing the interface clock rate has the impact of increasing DMD load time, which in turn reduces image quality. Even with a clock reduction, the edge rates required to achieve the fastest clock rates still exist and cause overshoot and undershoot issues if there is excessive crosstalk, or the line is too short. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

$$\text{Setup margin} = (\text{DLPC6401 output setup}) - (\text{DMD input setup}) - (\text{PCB routing mismatch}) - (\text{PCB SI degradation}) \quad (1)$$

$$\text{Hold-time margin} = (\text{DLPC6401 output hold}) - (\text{DMD input hold}) - (\text{PCB routing mismatch}) - (\text{PCB SI degradation}) \quad (2)$$

Where *PCB SI degradation* is signal integrity degradation due to PCB effects, which include simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI). The DLPC6401 I/O timing parameters can be found in their corresponding tables. Similarly, *PCB routing mismatch* can be budgeted and met through controlled PCB routing. However, PCB SI degradation is not so straightforward.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

Layout Guidelines (continued)

PCB design:

- Configuration: Asymmetric dual stripline
- Signal routing layer thickness (T): 1.0-oz copper (1.2 mil)
- Single-ended signal impedance controlled: 50 Ω (±10%)
- Differential signal impedance controlled: 100-Ω differential (±10%)

PCB Stackup:

- Reference plane 1 is assumed to be a ground plane for proper return path.
- Reference plane 2 is assumed to be the 1.9-V DMD I/O power plane or another ground plane.
- Dielectric FR4, (Er): 4.3 at 1 GHz (nominal)
- Signal trace distance to reference plane 1 (H1): 5 mil (nominal)
- Signal trace distance to reference plane 2 (H2): 30.4 mil (nominal)
- If additional routing layers are required, ensure they are adjacent to one of these reference planes

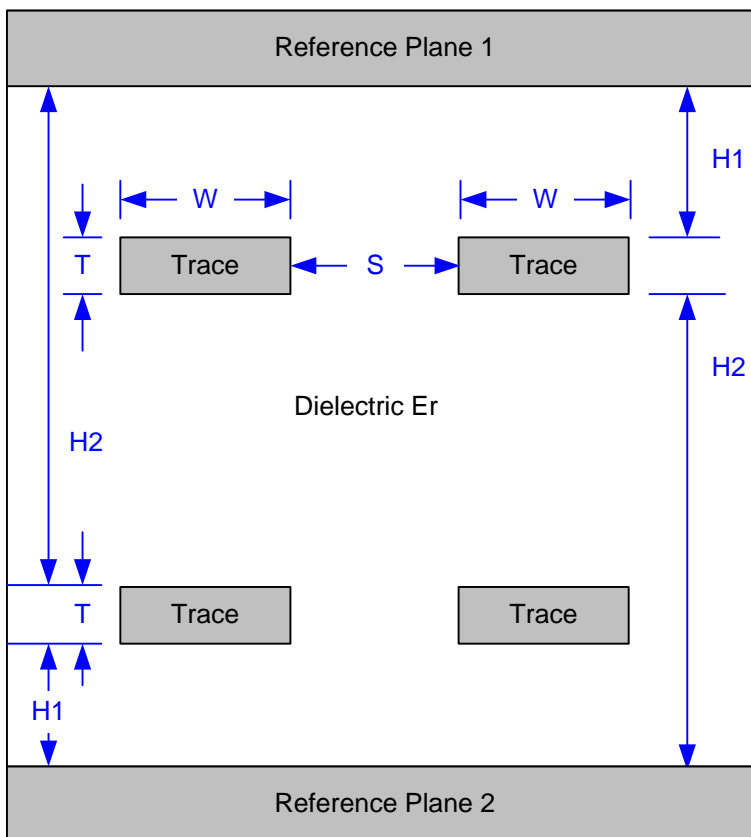


Figure 19. PCB Stackup Geometries

Flex design:

- Configuration: 2-layer microstrip
- The reference plane is assumed to be a ground plane for proper return path.
- Vias: Max 2 per signal

Layout Guidelines (continued)

- Single trace width: 4 mil (min)
- Signal routing layer thickness (T): 0.5-oz copper (0.6 mil)
- Single-ended signal impedance controlled: 50 Ω (±10%)

Table 11. General PCB Routing (Applies to All Corresponding PCB Signal)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	REQUIREMENT	UNIT
Line width (W) ⁽¹⁾	Escape routing in ball field	4 (0.1)	Minimum	mil (mm)
	PCB etch data or control	5 (0.13)	Minimum	mil (mm)
	PCB etch clocks	7 (0.18)	Minimum	mil (mm)
Minimum Line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	Minimum	mil (mm)
	PCB etch data or control	2x the line width ⁽²⁾	Minimum	mil (mm)
	PCB etch clocks	3x the line width	Minimum	mil (mm)

- (1) Line width is expected to be adjusted to achieve impedance requirements
(2) 3x line spacing is recommended for all signals to help achieve the desired signal integrity

Table 12. DMD I/F, PCB Interconnect Length Matching Requirements⁽¹⁾⁽²⁾

SIGNAL GROUP LENGTH MATCHING				
I/F	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (DDR)	DMD_TRC, DMD_SCTRL, DMD_LOADB DMD_D(23:0)	DMD_DCLK	±200 (±5.08)	mil (mm)
DMD (SDR)	DMD_SAC_BUS, DMD_DAD_OEZ, DMD_DAD_STRB, DMD_DAD_BUS	DMD_SAC_CLK	±200 (± 5.08)	mil (mm)

- (1) These values apply to the PCB routing only. They do not include any internal package routing mismatch associated with the DLPC6401 or the DMD. Additional margin can be attained if internal DLPC6401 package skew is taken into account.
(2) To minimize EMI radiation, serpentine routes added to facilitate matching should be implemented on signal layers only, and *between* reference planes.

Table 13. DMD I/F, PCB⁽¹⁾ Interconnect Min and Max Length Limitations (Note Operating Frequency Dependencies)⁽²⁾

BUS	SIGNAL GROUP	SIGNAL ROUTING LENGTH				UNIT	
		MIN ⁽³⁾	MAX ⁽³⁾⁽⁴⁾				
			120 MHz	106.7 MHz	96 MHz		87.7 MHz
DMD (DDR)	DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB DMD_D(23:0)	2480 (63)	2953 (75)	3465 (88)	3937 (100)	3937 (100)	mil (mm)

- (1) Signal lengths below the stated minimum likely result in excessive overshoot or undershoot (at any frequency).
(2) PCB layout assumes 2x design rules (that is, line spacing = 2x line width). However, 3x design rules reduce crosstalk and significantly help performance.
(3) Minimum and maximum signal routing length includes escape routing.
(4) DMD-DDR maximum signal length is a function of the DMD_DCLK rate.

Table 13. DMD I/F, PCB⁰ Interconnect Min and Max Length Limitations (Note Operating Frequency Dependencies)⁰ (continued)

BUS	SIGNAL GROUP	SIGNAL ROUTING LENGTH				UNIT
		MIN ⁽³⁾	MAX ⁽³⁾⁽⁴⁾			
			120 MHz	106.7 MHz	96 MHz	
DMD (SDR)	DMD_SAC_CLK, DMD_SAC_BUS, DMD_DAD_OEZ, DMD_DAD_STRB, DMD_DAD_BUS	512 (13)	5906 (150)			mil (mm)

- Number of layer changes:
 - Minimize layer changes
- Stubs:
 - Stubs should be avoided

Termination requirements:

DMD DDR data:	Specifically: DMD_D(23-0) External [5-Ω] series termination (at the transmitter)
DMD DDR clock	Specifically: DMD_DCLK External [5-Ω] series termination
DMD TRC, SCTRL, load:	Specifically: DMD_TRC, DMD_SCTRL, DMD_LOADB External [5-Ω] series termination (at the transmitter)
DMD SAC and miscellaneous control:	Specifically: DMD_SAC_CLK, DMD_SAC_BUS, DMD_DAD_STRB, DMD_DAD_BUS External [5-Ω] series termination (at the transmitter)
DAD output enable:	Specifically: DMD_DAD_OEZ External [0-Ω] series termination Instead this signal must be externally pulled-up to VDD_DMD through a 30- to 51-kΩ resistor.

However, note that both the DLPC6401 output timing parameters and the DMD input timing parameters include timing budget to account for their respective internal package routing skew. Thus, additional system margin can be attained by comprehending the package variations and compensating for them in the PCB layout. To increase system timing margin, TI recommends that DLPC6401 package variation be compensated for (by signal group), but it may not be desirable to compensate for DMD package skew. Because, each DMD has a different skew profile making the PCB layout DMD specific. Thus, if an OEM wants to use a common PCB design for different DMDs, TI recommends that either the DMD package skew variation not be compensated for on the PCB or the package lengths for all applicable DMDs be considered. [Table 14](#) provides the DLPC6401 package output delay at the package ball for each DMD I/F signal. DMD internal routing skew data is contained in the DMD data sheet.

Table 14. DLPC6401 DMD I/F Package Routing Length

SIGNAL	TOTAL DELAY (ps)	PACKAGE BALL	SIGNAL	TOTAL DELAY (ps)	PACKAGE BALL
DMD_D0	25.9	A8	DMD_D14	19	B12
DMD_D1	19.6	B8	DMD_D15	11.7	C12
DMD_D2	13.4	C8	DMD_D16	4.7	D12
DMD_D3	7.4	D8	DMD_D17	21.5	B7
DMD_D4	18.1	B11	DMD_D18	24.8	A10
DMD_D5	11.1	C11	DMD_D19	8.3	D7
DMD_D6	4.4	D11	DMD_D20	23.9	B6

Table 14. DLPC6401 DMD I/F Package Routing Length (continued)

SIGNAL	TOTAL DELAY (ps)	PACKAGE BALL	SIGNAL	TOTAL DELAY (ps)	PACKAGE BALL
DMD_D7	0	E11	DMD_D21	1.6	E9
DMD_D8	14.8	C7	DMD_D22	10.7	C10
DMD_D9	18.4	B10	DMD_D23	16.7	C6
DMD_D10	6.4	E7	DMD_DCLK	24.8	A9
DMD_D11	4.8	D10	DMD_LOADB	18	B9
DMD_D12	29.8	A6	DMD_SCTRL	11.4	C9
DMD_D13	25.7	A12	DMD_TRC	4.6	D9

10.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with an internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown, unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line.

Unused output-only pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate resistor.

10.2 Layout Example

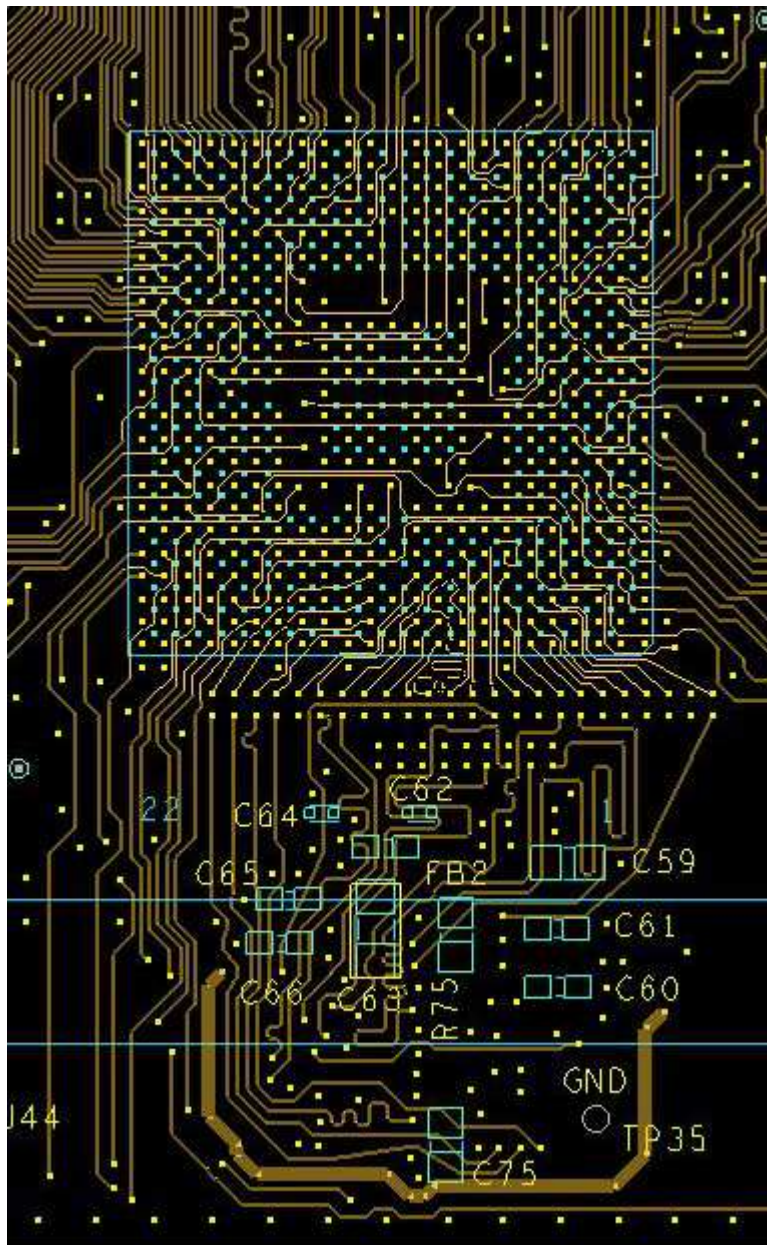
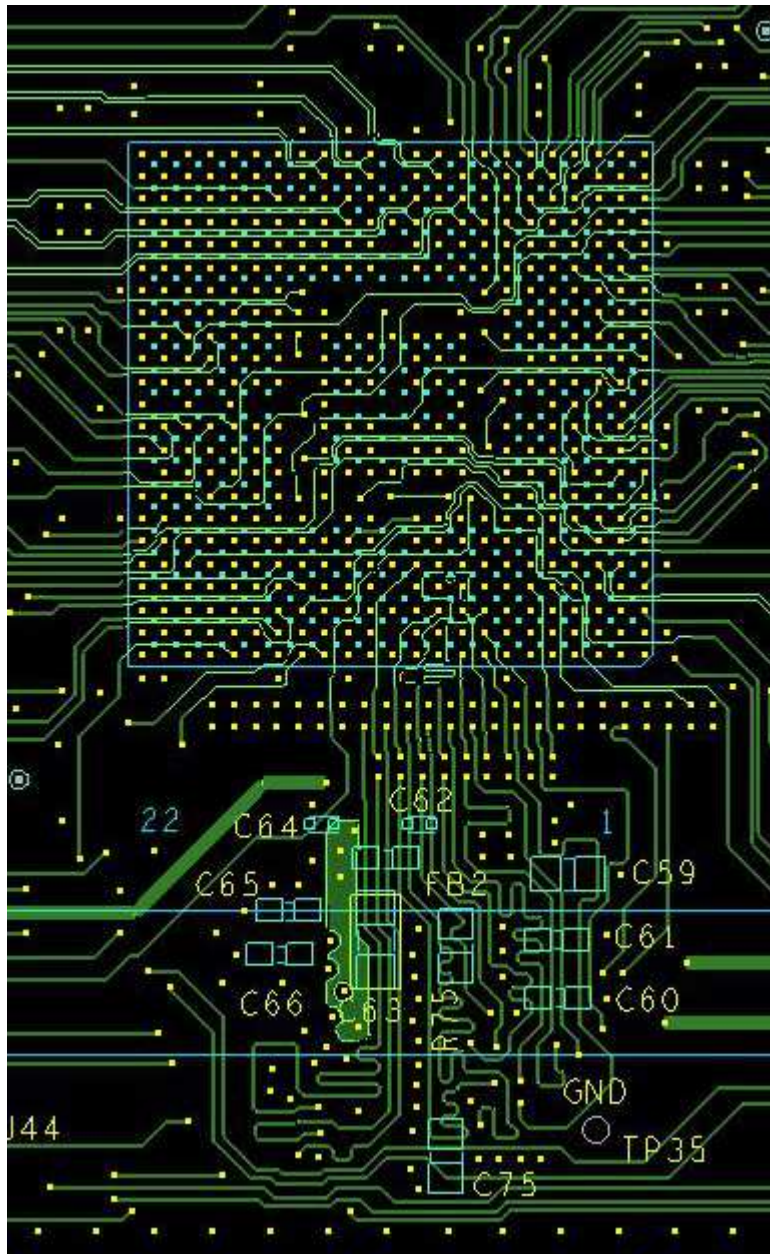


Figure 20. Layer 3

Layout Example (continued)

Figure 21. Layer 4
10.3 Thermal Considerations

The underlying thermal limitation for the DLPC6401 device is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the [Recommended Operating Conditions](#)). This temperature depends on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC6401 device, and power dissipation of surrounding components. The DLPC6401 package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

Thermal Considerations (接下页)

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC6401 power dissipation and $R_{\theta JA}$ at 1 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC-defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC6401 PCB, and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommends that thermal performance be measured and validated.

To do this, the top-center case temperature should be measured under the worst-case product scenario (maximum power dissipation, maximum voltage, and maximum ambient temperature) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured ϕ_{JT} for the DLPC6401 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40-gauge) thermocouple. The bead and the thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally-conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

11.1.1.1 视频时序参数定义

每帧有效扫描行数 (**ALPF**) 定义一帧中包含可显示数据的行数: **ALPF** 是每帧总行数 (**TLPF**) 的子集。

每行有效像素 (**APPL**) 定义包含可显示数据的一行中的像素时钟数: **APPL** 是每行总像素 (**TPPL**) 的子集。

水平后沿 (**HBP**) 消隐 水平同步之后, 第一个有效像素之前的消隐像素时钟数量。注意: **HBP** 时间以各自同步信号的前缘 (有效) 边沿为基准。

水平前沿 (**HFP**) 消隐 最后一个有效时钟之后, 水平同步之前的消隐像素时钟的数量。

水平同步 (**HS**) 定义水平间隔 (行) 开始的时序基准点。绝对基准点由 **HS** 信号的有效边沿定义。有效边沿 (源定义的上升沿或下降沿) 是测量所有水平消隐参数的基准。

每帧总行数 (**TLPF**) 以行数定义垂直扫描时间 (帧时间): **TLPF** = 每帧总行数 (有效和无效行)

每行总像素 (**TPPL**) 以像素时钟数定义水平行扫描时间: **TPPL** = 每行总像素时钟数 (有效和无效像素时钟)

垂直后沿 (**VBP**) 消隐 垂直同步后, 第一个有效行之前的消隐行的数量。

垂直前沿 (**VFP**) 消隐 最后有效行之后, 垂直同步前的消隐行的数量。

垂直同步 (**VS**) 定义垂直间隔 (帧) 开始的时序基准点。这个绝对基准点由 **VS** 信号的有效边沿定义。有效边沿 (源定义的上升沿或下降沿) 是测量所有垂直消隐参数的基准。

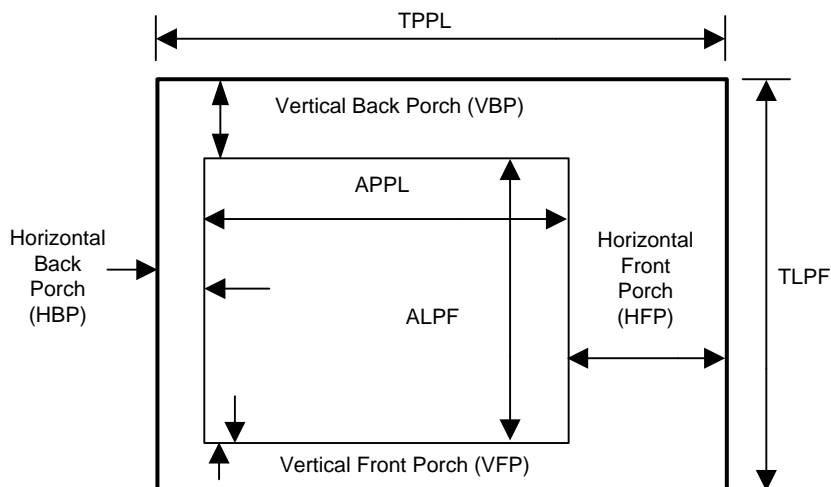
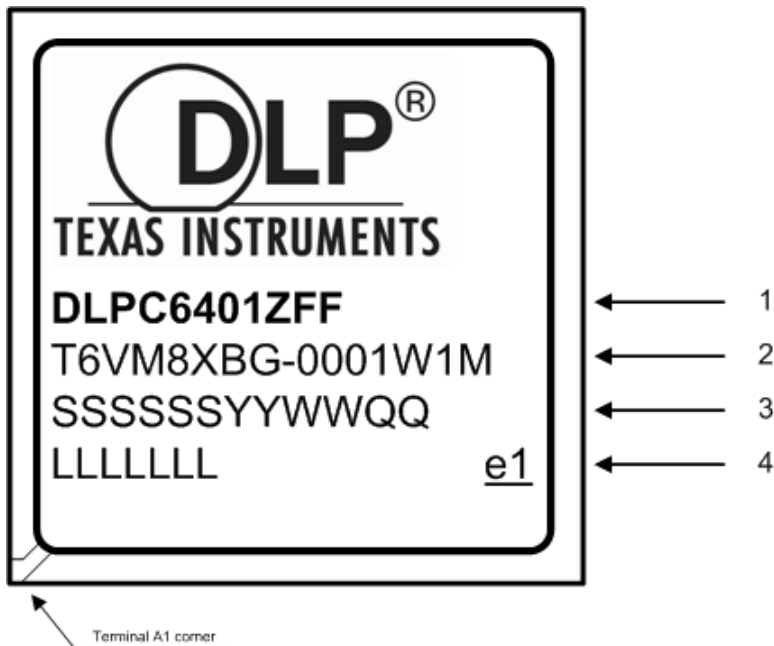


图 22. 时序参数图

器件支持 (接下页)

11.1.1.2 器件标记



标记定义:

第 1 行: DLP®设备名称

第 2 行: 铸造部件号

第 3 行: SSSSSSYWW-QQ: 封装组件信息

SSSSSS: 制造工厂

YYWW: 日期代码 (YY = 年 :: WW = 周)

QQ: 合格等级选项 – 工程样品在此处以 **ES** 后缀标记。

例如, TAIWAN1324-ES 表示在台湾制造的工程样品, 制造日期是 2013 年第 24 周

第 4 行: LLLLLLL e1: 半导体晶圆的铸造批次代码以及无铅焊锡球标记

LLLLLLL: 铸造批次代码

e1: 表示含 SnAgCu 的无铅焊锡球

11.2 社区资源

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TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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DLP is a registered trademark of Texas Instruments.

ARM926 is a trademark of ARM.

All other trademarks are the property of their respective owners.

11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPC6401ZFF	Active	Production	BGA (ZFF) 419	60 JEDEC TRAY (5+1)	Yes	Call TI	Call TI	0 to 55	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

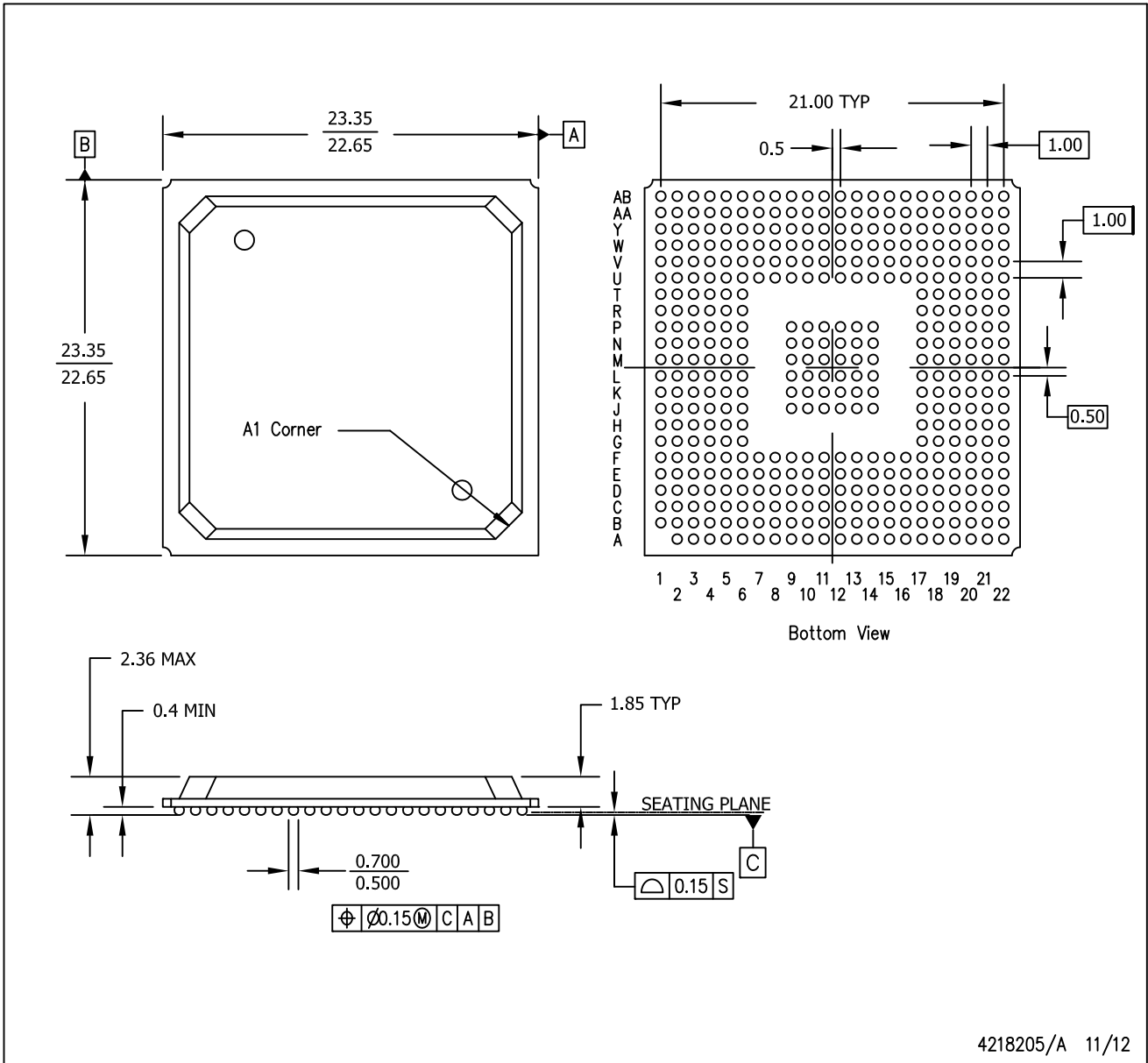
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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ZFF (S-PBGA-N419)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. This package is Pb-free.

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