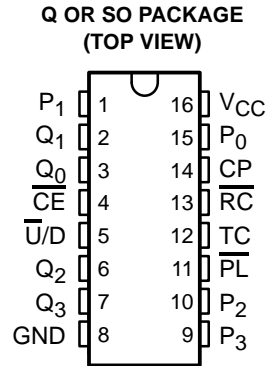


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- 64-mA Output Sink Current  
32-mA Output Source Current



### description

The CY74FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the CY74FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple-clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**PIN DESCRIPTION**

NAME	DESCRIPTION
$\overline{CE}$	Count enable input (active low)
CP	Clock pulse input (active rising edge)
P	Parallel data inputs
$\overline{PL}$	Asynchronous parallel load input (active low)
$\overline{U/D}$	Up/down count control input
Q	Flip-flop outputs
$\overline{RC}$	Ripple clock output (active low)
TC	Terminal count output



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# CY74FCT191T

## 4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001



### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6.2	CY74FCT191CTQCT	FT191-3
	SOIC – SO	Tube	6.2	CY74FCT191CTSOC	FCT191C
		Tape and reel	6.2	CY74FCT191CTSOCT	
	SOIC – SO	Tube	7.8	CY74FCT191ATSOC	FCT191A
		Tape and reel	7.8	CY74FCT191ATSOCT	


† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### Function Tables

#### $\overline{RC}$ FUNCTION

INPUTS		OUTPUTS	
$\overline{CE}$	CP	TC†	$\overline{RC}$
L		H	
H	X	X	H
X	X	L	H

H = High logic level, L = Low logic level,

X = Don't care,  = Low pulse

† TC is generated internally.

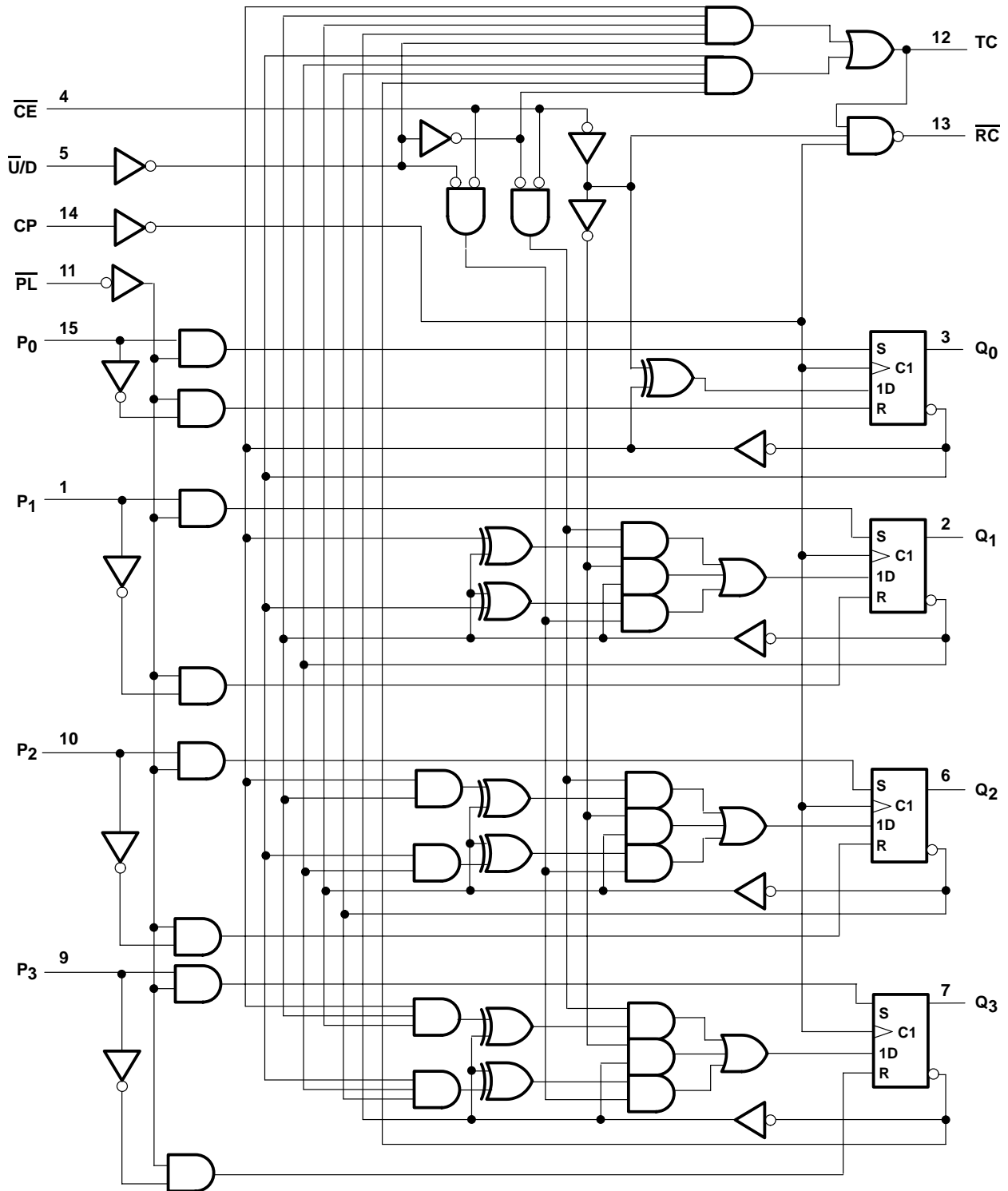
#### MODE SELECT

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	↑	Count up
H	L	H	↑	Count down
L	X	X	X	Preset (asynchronous)
H	H	X	X	No change (hold)

H = High logic level, L = Low logic level, X = Don't care,

↑ = Low-to-high clock transition

**logic diagram (positive logic)**



CY74FCT191T  
4-BIT UP/DOWN BINARY COUNTER

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absolute maximum rating over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, $T_A$	–65°C to 135°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–32	mA
$I_{OL}$ Low-level output current			64	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V <sub>IK</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>IN</sub> = −18 mA		−0.7	−1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = −32 mA	2			V	
	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = −15 mA	2.4	3.3			
V <sub>OL</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 64 mA		0.3	0.55	V	
V <sub>H</sub>	All inputs			0.2		V	
I <sub>I</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = V <sub>CC</sub>			5	μA	
I <sub>IH</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 2.7 V			±1	μA	
I <sub>IL</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 0.5 V			±1	μA	
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0 V	−60	−120	−225	mA	
I <sub>off</sub>	V <sub>CC</sub> = 0 V,	V <sub>OUT</sub> = 4.5 V			±1	μA	
I <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V			0.1	0.2	mA	
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open			0.5	2	mA	
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.25 V, One bit switching at 50% duty cycle, Preset mode, Outputs open, MR = V <sub>CC</sub> = SR, PL = CE = U/D = CP = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2 V			0.06	0.12	mA/MHz	
I <sub>C</sub> #	V <sub>CC</sub> = 5.25 V, Preset mode, Outputs open, PL = CE = U/D = CP = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> = V <sub>CC</sub> or GND		0.4	0.8	mA
			V <sub>IN</sub> = 3.4 V or GND		0.7	1.8	mA
		Four bits switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> = V <sub>CC</sub> or GND		1.3	2.6	mA
			V <sub>IN</sub> = 3.4 V or GND		2.3	6.6	mA
C <sub>i</sub>				5	10	pF	
C <sub>o</sub>				9	12	pF	

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

# CY74FCT191T

## 4-BIT UP/DOWN BINARY COUNTER

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

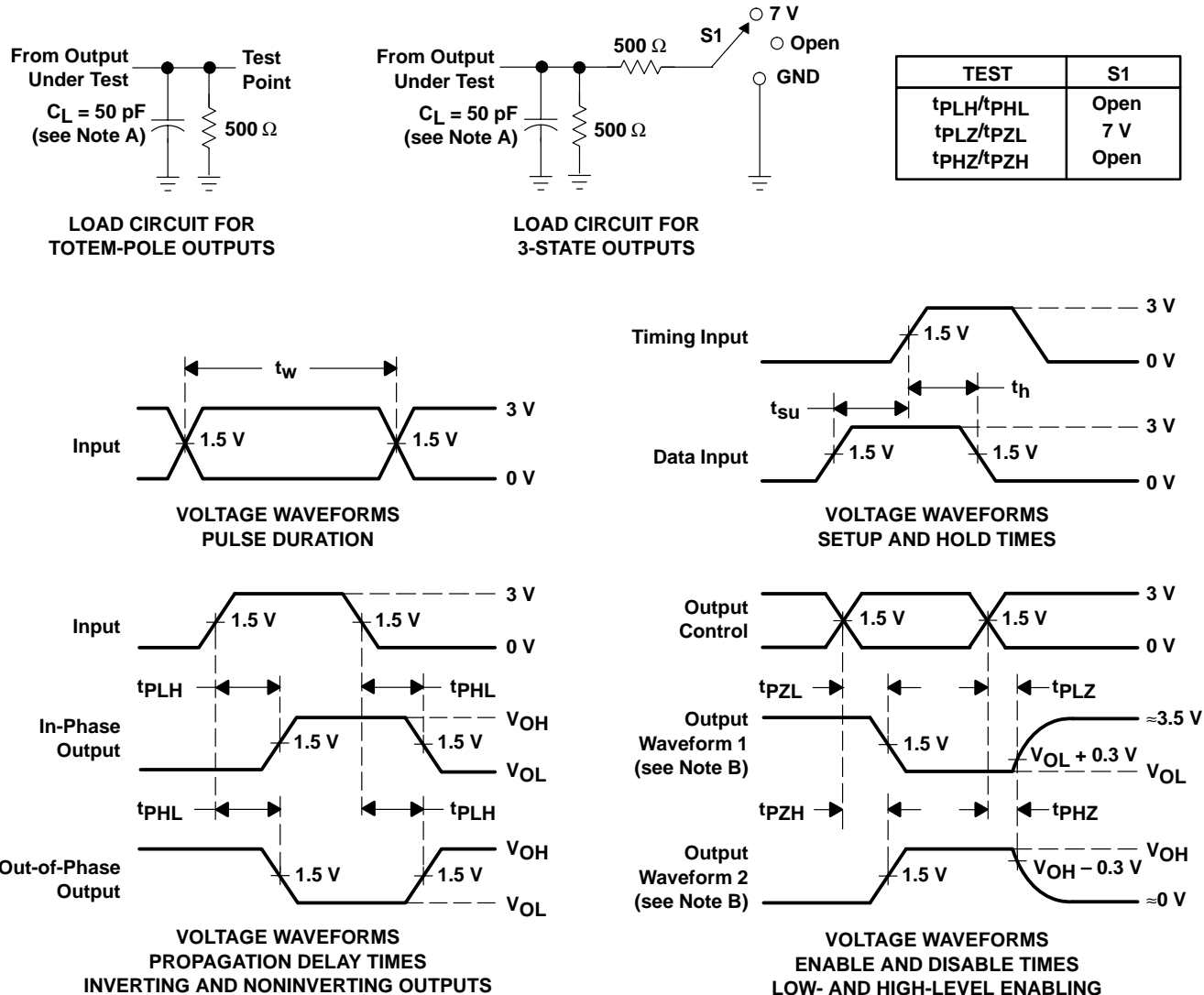
PARAMETER			CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
$t_w$ Pulse duration	CP	High or Low	4		4		ns
	$\overline{PL}$ low		5.5		5		
$t_{su}$ Setup time	Data before $\overline{PL}\downarrow$	High or Low	4		3.5		ns
	$\overline{CE}$ before $CP\uparrow$	Low	9		7.2		
	$\overline{U/D}$ before $CP\uparrow$	High or Low	10		8		
$t_h$ Hold time	Data after $\overline{PL}\downarrow$	High or Low	1.5		1		ns
	$\overline{CE}$ after $CP\uparrow$	Low	0		0		
	$\overline{U/D}$ after $CP\uparrow$	High or Low	0		0		
$t_{rec}$ Recovery time	$\overline{PL}$ after $CP\uparrow$		5		4.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	$Q_n$	1.5	7.8	1.5	6.2	ns
$t_{PHL}$			1.5	7.8	1.5	6.2	
$t_{PLH}$	CP	TC	1.5	11.8	1.5	9.4	ns
$t_{PHL}$			1.5	11.8	1.5	9.4	
$t_{PLH}$	CP	$\overline{RC}$	1.5	8.5	1.5	6.8	ns
$t_{PHL}$			1.5	8.5	1.5	6.8	
$t_{PLH}$	CE	$\overline{RC}$	1.5	7.2	1.5	6	ns
$t_{PHL}$			1.5	7.2	1.5	6	
$t_{PLH}$	$\overline{U/D}$	$\overline{RC}$	1.5	13	1.5	11	ns
$t_{PHL}$			1.5	13	1.5	11	
$t_{PLH}$	$\overline{U/D}$	TC	1.5	7.2	1.5	6.1	ns
$t_{PHL}$			1.5	7.2	1.5	6.1	
$t_{PLH}$	$P_n$	$Q_n$	1.5	9.1	1.5	7.7	ns
$t_{PHL}$			1.5	9.1	1.5	7.7	
$t_{PLH}$	$\overline{PL}$	$Q_n$	2	8.5	2	7.2	ns
$t_{PHL}$			2	8.5	2	7.2	



### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CY74FCT191ATSOC</a>	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191A
CY74FCT191ATSOC.B	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191A
<a href="#">CY74FCT191CTQCT</a>	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT191-3
CY74FCT191CTQCT.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT191-3
<a href="#">CY74FCT191CTSOC</a>	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C
CY74FCT191CTSOC.B	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C
CY74FCT191CTSOCG4	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C
CY74FCT191CTSOCG4.B	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT191CTQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT191CTQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT191ATSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT191ATSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT191CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT191CTSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT191CTSOCG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT191CTSOCG4.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



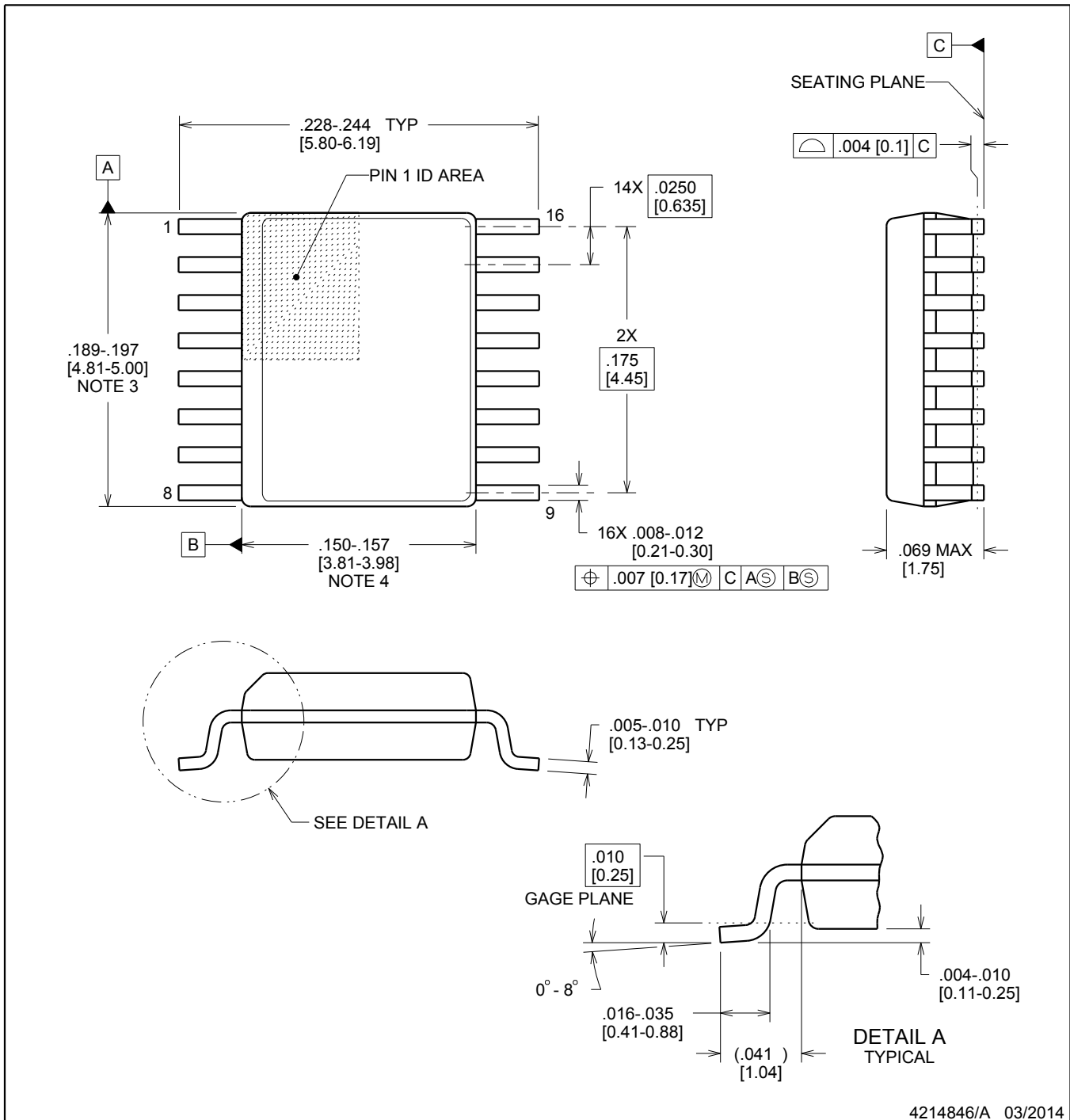


**DBQ0016A**

## PACKAGE OUTLINE

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

### NOTES:

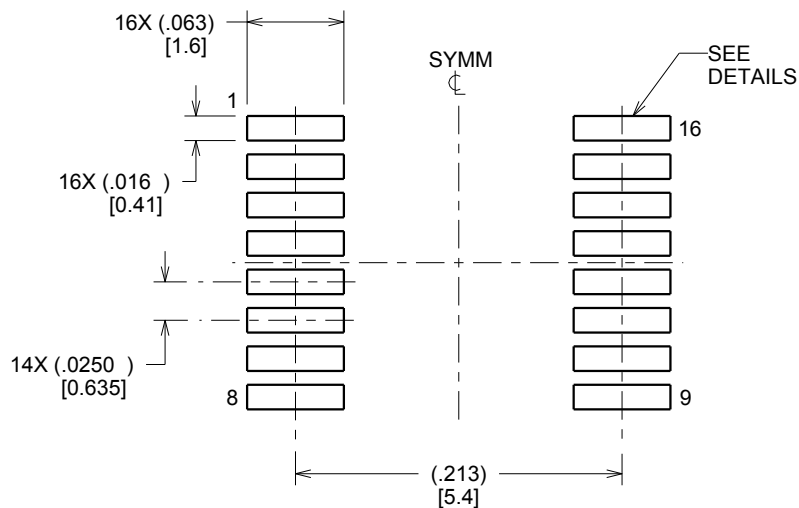
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

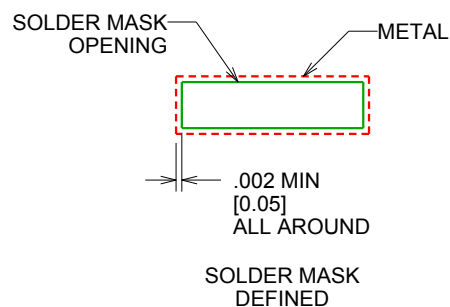
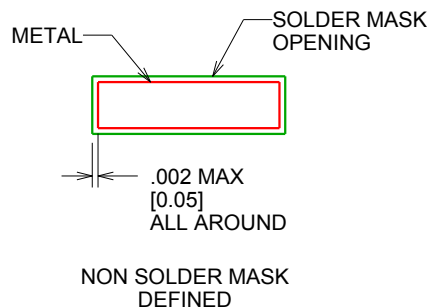
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

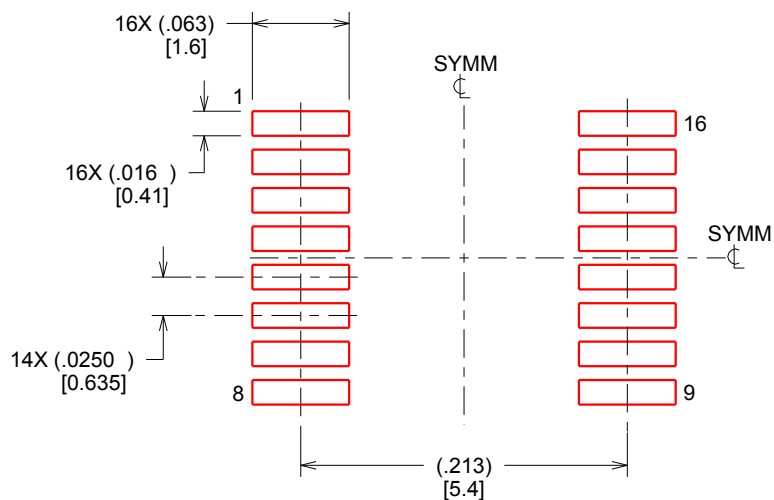
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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