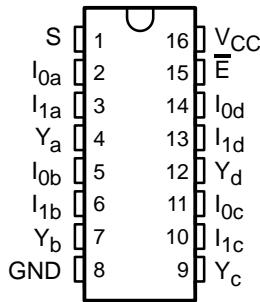
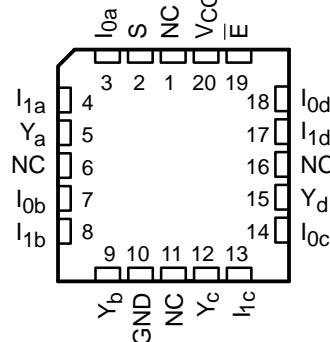


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- CY54FCT157T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT157T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

**CY74FCT157T . . . Q OR SO PACKAGE  
(TOP VIEW)**



**CY54FCT157T . . . L PACKAGE  
(TOP VIEW)**



NC – No internal connection

### description

The 'FCT157T devices are quad two-input multiplexers that select four bits of data from two sources under the control of a common data-select (S) input. The output-enable ( $\bar{E}$ ) input is active low. When  $\bar{E}$  is high, all of the outputs (Y) are forced low, regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the 'FCT157T devices. The state of S determines the particular register from which the data comes. It also can be used as a function generator. These devices are useful for implementing highly irregular logic by generating any 4 of the 16 different functions of 2 variables, with 1 variable common.

The 'FCT157T devices are logic implementations of a four-pole, two-position switch, where the position of the switch is determined by the logic levels at S.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**CY54FCT157T, CY74FCT157T  
QUAD 2-INPUT MULTIPLEXERS  
WITH 3-STATE OUTPUTS**

SCCS014B – MAY 1994 – REVISED NOVEMBER 2001

**PIN DESCRIPTION**

NAME	DESCRIPTION
S	Common select input
$\bar{E}$	Enable inputs (active low)
$I_0$	Data inputs from source 0
$I_1$	Data inputs from source 1
Y	Noninverted outputs

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>†</sup>		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	QSOP – Q	Tape and reel	4.3	CY74FCT157CTQCT	FT157-3
	SOIC – SO	Tube	4.3	CY74FCT157CTSOC	FCT157C
		Tape and reel	4.3	CY74FCT157CTSOCT	
	QSOP – Q	Tape and reel	5	CY74FCT157ATQCT	FT157-1
	SOIC – SO	Tube	5	CY74FCT157ATSOC	FCT157A
		Tape and reel	5	CY74FCT157ATSOCT	
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	LCC – L	Tube	5.8	CY54FCT157ATLMB	

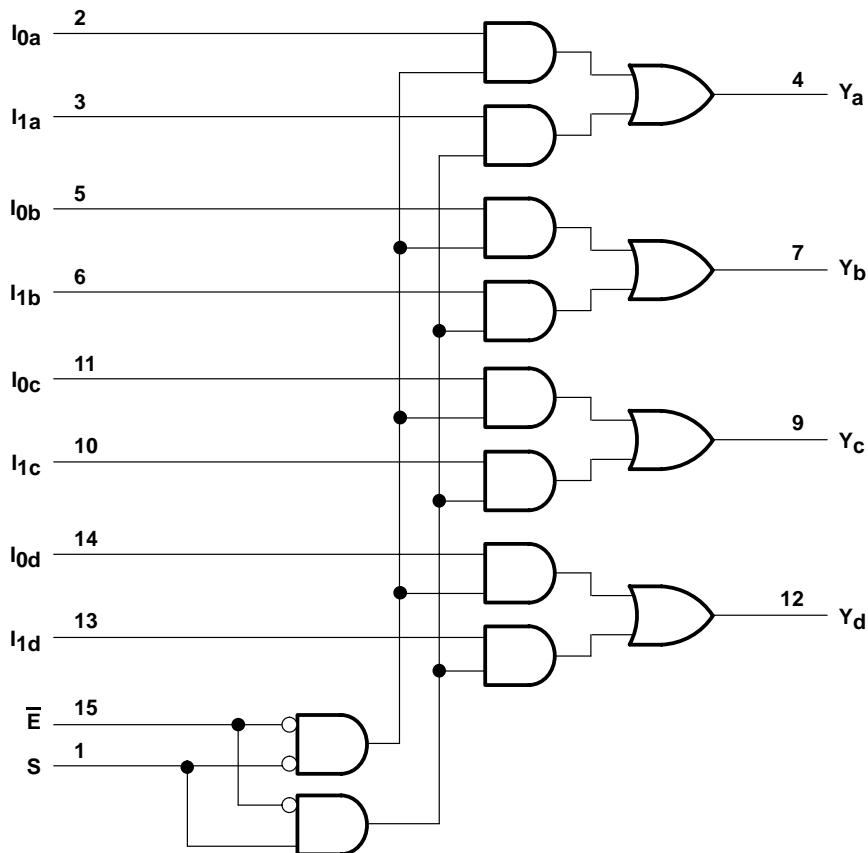
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

INPUTS				OUTPUT Y
$\bar{E}$	S	$I_0$	$I_1$	
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High logic level, L = Low logic level,  
X = Don't care

## logic diagram (positive logic)



Pin numbers shown are for the Q and SO packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51-7.

**CY54FCT157T, CY74FCT157T  
QUAD 2-INPUT MULTIPLEXERS  
WITH 3-STATE OUTPUTS**

SCCS014B – MAY 1994 – REVISED NOVEMBER 2001

**recommended operating conditions (see Note 2)**

		CY54FCT157T			CY74FCT157T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-32	mA
I <sub>OL</sub>	Low-level output current			32			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	CY54FCT157T			CY74FCT157T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-0.7	-1.2				V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7		-1.2	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -32 mA				2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA	0.3	0.55					V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs		0.2			0.2		V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>		5					µA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>					5		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V		±1					µA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V					±1		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V		±1					µA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V					±1		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V		10					µA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V				10			
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V		-10					µA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V				-10			
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V		±1			±1		µA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1	0.2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open	0.5	2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open				0.5	2		

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS			CY54FCT157T			CY74FCT157T			UNIT	
				MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX		
I <sub>CCD</sub> <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\bar{E}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V			0.06 0.12						mA/ MHz	
	V <sub>CC</sub> = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\bar{E}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V						0.06 0.12				
I <sub>C</sub> <sup>#</sup>	V <sub>CC</sub> = 5.5 V, Outputs open, $\bar{E}$ = GND	One input switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	0.7 1.4						mA	
			V <sub>IN</sub> = 3.4 V or GND	1 2.4							
		Four bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V	0.7 1.4							
			V <sub>IN</sub> = 3.4 V or GND	1.7 5.4							
	V <sub>CC</sub> = 5.25 V, Outputs open, $\bar{E}$ = GND	One input switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.7 1.4				
			V <sub>IN</sub> = 3.4 V or GND				1 2.4				
		Four bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.7 1.4				
			V <sub>IN</sub> = 3.4 V or GND				1.7 5.4				
C <sub>i</sub>				5 10			5 10			pF	
C <sub>o</sub>				9 12			9 12			pF	

<sup>†</sup> Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>¶</sup> This parameter is derived for use in total power-supply calculations.

$$\# I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$$

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

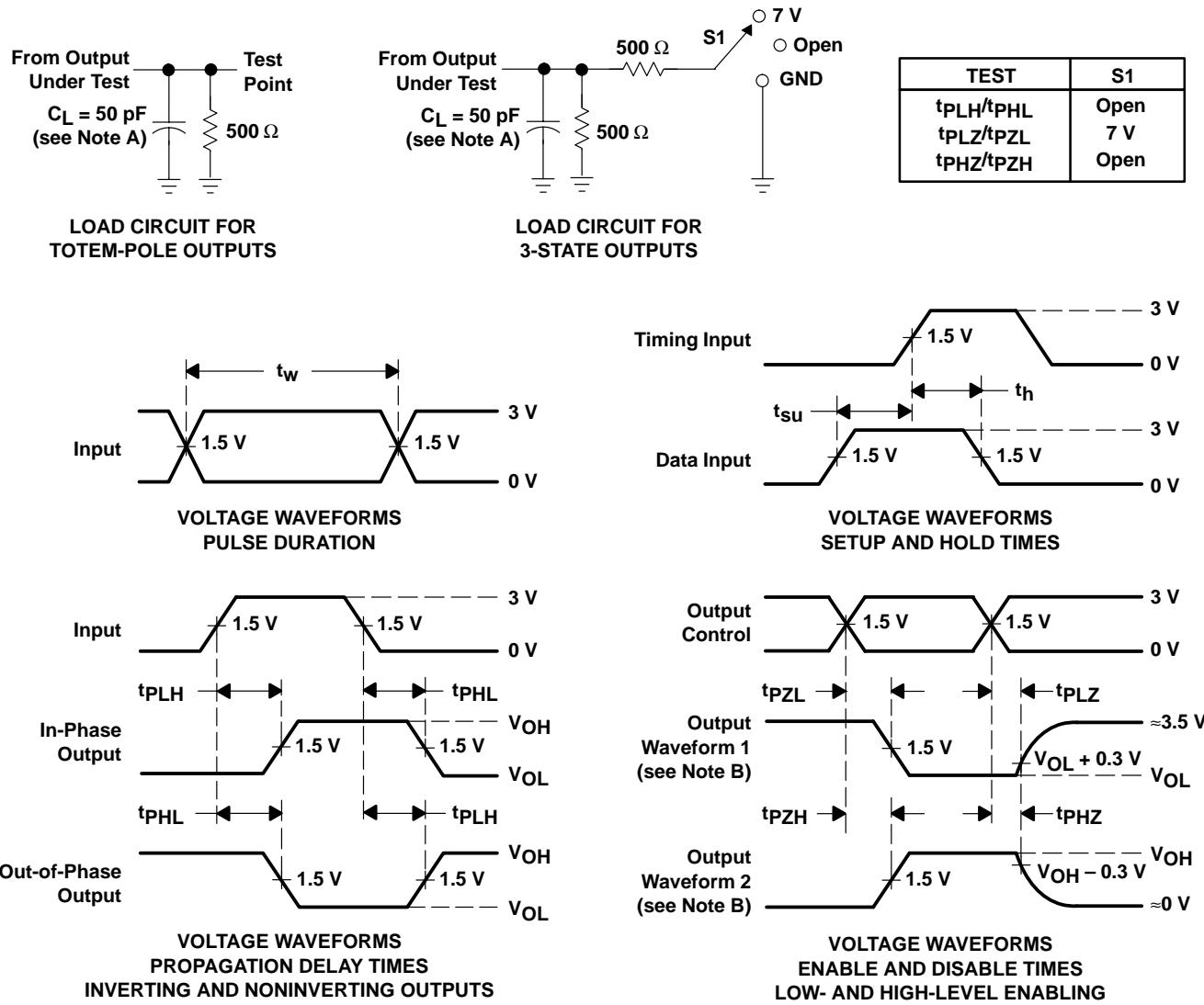
All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT157AT		CY74FCT157AT		CY74FCT157CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	I	Y	1.5	5.8	1.5	5	1.5	4.3	ns
t <sub>PHL</sub>			1.5	5.8	1.5	5	1.5	4.3	
t <sub>PLH</sub>	E	Y	1.5	7.4	1.5	6	1.5	4.8	ns
t <sub>PHL</sub>			1.5	7.4	1.5	6	1.5	4.8	
t <sub>PLH</sub>	S	Y	1.5	8.1	1.5	7	1.5	5.2	ns
t <sub>PHL</sub>			1.5	8.1	1.5	7	1.5	5.2	

## PARAMETER MEASUREMENT INFORMATION



**Figure 1. Load Circuit and Voltage Waveforms**

NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. The outputs are measured one at a time with one input transition per measurement.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9220803M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220803M2A
<a href="#">CY74FCT157ATDR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157AT
CY74FCT157ATDR.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157AT
<a href="#">CY74FCT157ATSOC</a>	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157A
CY74FCT157ATSOC.B	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157A
<a href="#">CY74FCT157CTD</a>	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157CT
CY74FCT157CTD.B	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157CT
<a href="#">CY74FCT157CTQCT</a>	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT157-3
CY74FCT157CTQCT.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT157-3
<a href="#">CY74FCT157CTSOC</a>	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157C
CY74FCT157CTSOC.B	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157C
<a href="#">CY74FCT157CTSOCT</a>	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157C
CY74FCT157CTSOCT.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT157C

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

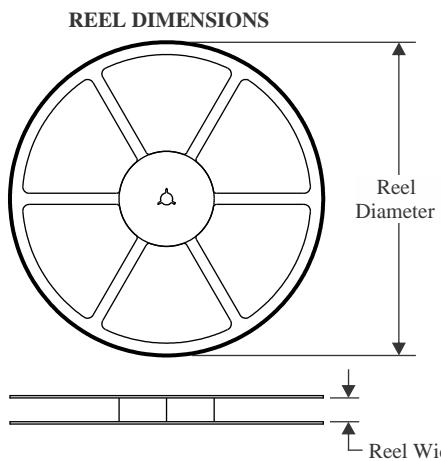
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

---

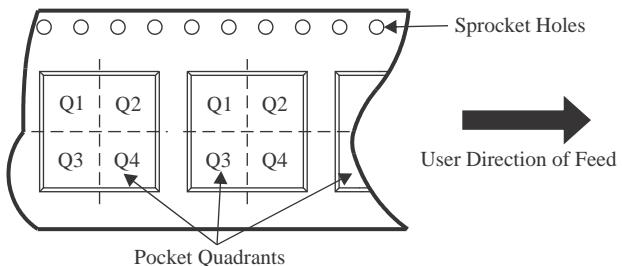
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


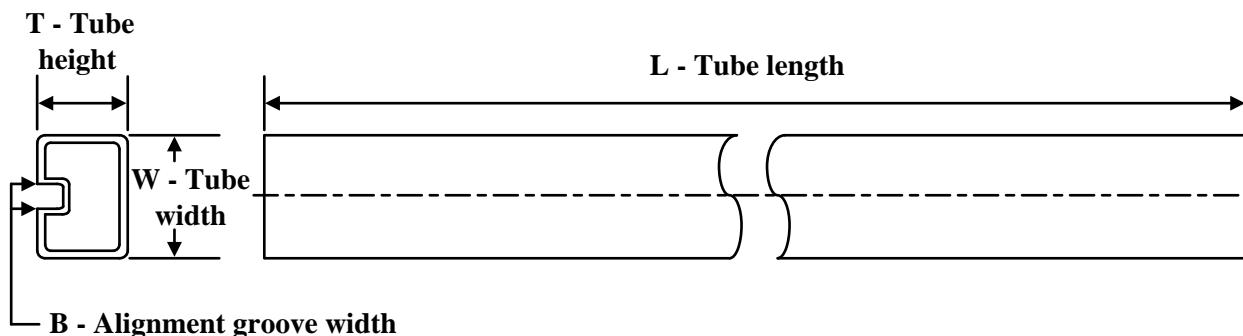
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT157ATDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CY74FCT157CTQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
CY74FCT157CTSOCT	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT157ATDR	SOIC	D	16	2500	340.5	336.1	32.0
CY74FCT157CTQCT	SSOP	DBQ	16	2500	353.0	353.0	32.0
CY74FCT157CTSOCT	SOIC	DW	16	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9220803M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT157ATSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT157ATSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT157CTD	D	SOIC	16	40	507	8	3940	4.32
CY74FCT157CTD.B	D	SOIC	16	40	507	8	3940	4.32
CY74FCT157CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT157CTSOC.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025