

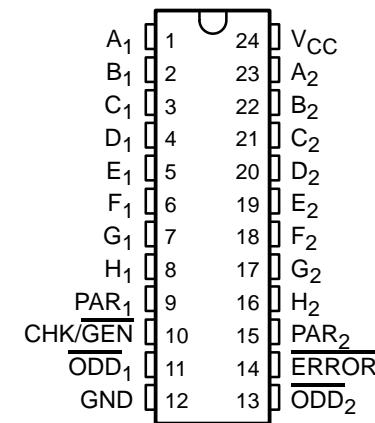
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- Two 8-Bit Parity Generators/Checkers
- Open-Drain Active-Low Parity-Error Output
- Expandable for Larger Word Widths
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- CY54FCT480T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT480T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current

### description

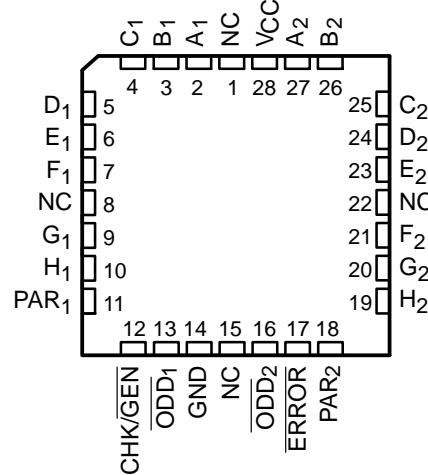
The 'FCT480T devices are high-speed, dual, 8-bit parity generators/checkers. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a sum and parity-error (ERROR) output. These devices can be used in odd-parity systems. ERROR is an open-drain output designed for easy expansion of the word width by a wired-OR connection of several 'FCT480T devices. Because no additional logic is needed, the parity-generation or parity-checking times remain the same as for an individual 'FCT480T device.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**CY74FCT480T . . . P, Q, OR SO PACKAGE  
(TOP VIEW)**



**CY54FCT480T . . . L PACKAGE  
(TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CY54FCT480T, CY74FCT480T DUAL 8-BIT PARITY GENERATORS/CHECKERS

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## ORDERING INFORMATION

| TA             | PACKAGE <sup>†</sup> |               | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|------------|-----------------------|------------------|
| -40°C to 85°C  | DIP – P              | Tube          | 6.1        | CY74FCT480BTPC        | CY74FCT480BTPC   |
|                | QSOP – Q             | Tape and reel | 6.1        | CY74FCT480BTQCT       | FCT480B          |
|                | SOIC – SO            | Tube          | 6.1        | CY74FCT480BTSOC       | FCT480B          |
|                |                      | Tape and reel | 6.1        | CY74FCT480BTSOCT      |                  |
|                | DIP – P              | Tube          | 7.5        | CY74FCT480ATPC        | CY74FCT480ATPC   |
| -55°C to 125°C | QSOP – Q             | Tape and reel | 7.5        | CY74FCT480ATQCT       | FCT480A          |
|                | LCC – L              | Tube          | 7          | CY54FCT480BTLMB       |                  |

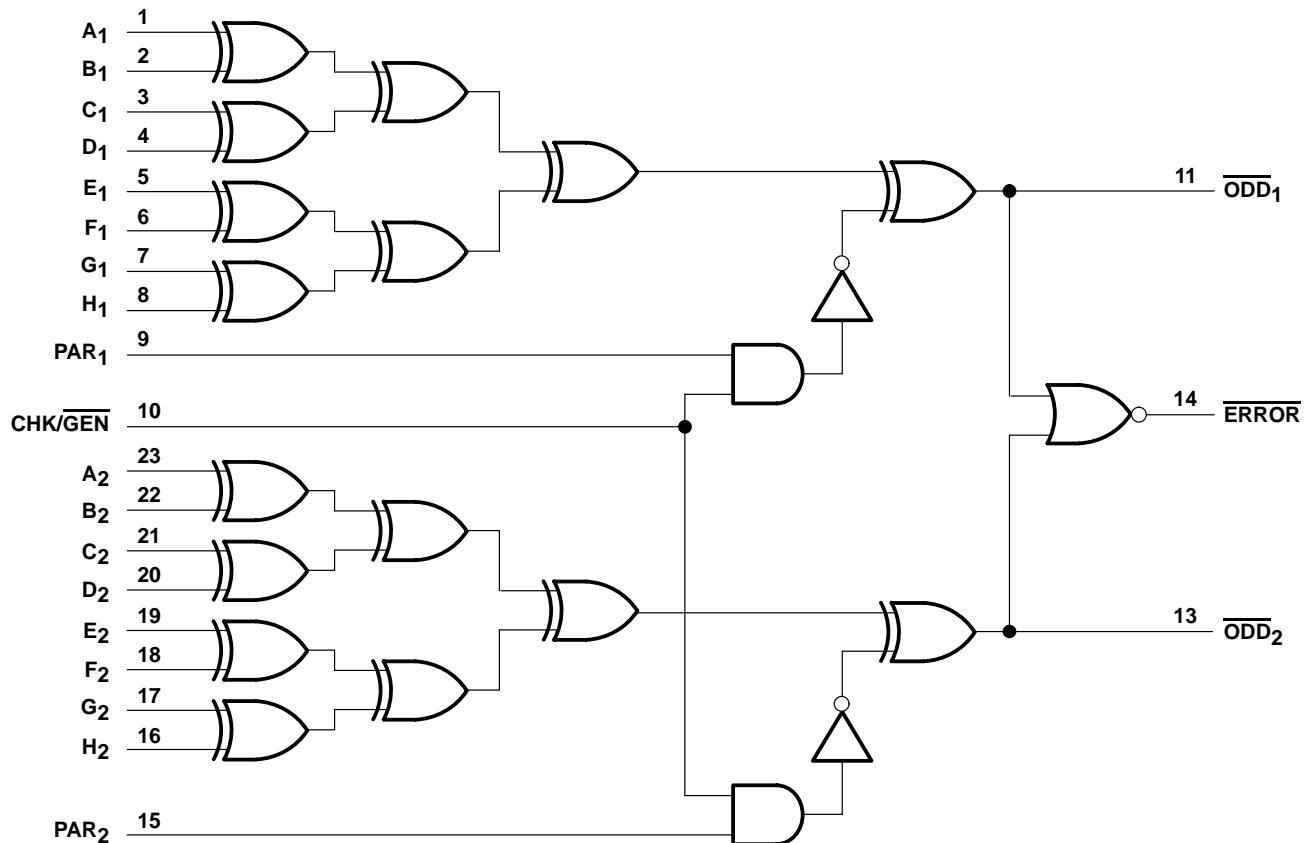
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

|   |   | INPUTS  |                  |                  | OUTPUTS          |                  |       |
|---|---|---------|------------------|------------------|------------------|------------------|-------|
| A <sub>1</sub> –H <sub>1</sub>                                | A <sub>2</sub> –H <sub>2</sub>                                | CHK/GEN | PAR <sub>1</sub> | PAR <sub>2</sub> | ODD <sub>1</sub> | ODD <sub>2</sub> | ERROR |
| Number of A <sub>1</sub> –H <sub>1</sub> inputs, high is even | Number of A <sub>2</sub> –H <sub>2</sub> inputs, high is even | H       | H                | H                | L                | L                | H     |
|   |   | H       | L                | H                | H                | L                | L     |
|   |   | H       | H                | L                | L                | H                | L     |
|   |   | H       | L                | L                | H                | H                | L     |
|   |   | L       | X                | X                | H                | H                | L     |
|   | Number of inputs A <sub>2</sub> –H <sub>2</sub> , high is odd | H       | H                | H                | L                | H                | L     |
|   |   | H       | L                | H                | H                | H                | L     |
|   |   | H       | H                | L                | L                | L                | H     |
|   |   | H       | L                | L                | H                | L                | L     |
|   |   | L       | X                | X                | H                | L                | L     |
| Number of A <sub>1</sub> –H <sub>1</sub> inputs, high is odd  | Number of A <sub>2</sub> –H <sub>2</sub> inputs, high is even | H       | H                | H                | H                | L                | L     |
|   |   | H       | L                | H                | L                | L                | H     |
|   |   | H       | H                | L                | H                | H                | L     |
|   |   | H       | L                | L                | L                | H                | L     |
|   |   | L       | X                | X                | L                | H                | L     |
|   | Number of A <sub>2</sub> –H <sub>2</sub> inputs, high is odd  | H       | H                | H                | H                | H                | L     |
|   |   | H       | L                | H                | L                | H                | L     |
|   |   | H       | H                | L                | H                | L                | L     |
|   |   | H       | L                | L                | L                | L                | H     |
|   |   | L       | X                | X                | L                | L                | H     |

H = High logic level, L = Low logic level, X = Don't care

## logic diagram



Pin numbers shown are for the P, Q, and SO packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

|                 |                                | CY54FCT480T |     |     | CY74FCT480T |     |      | UNIT |
|-----------------|--------------------------------|-------------|-----|-----|-------------|-----|------|------|
|                 |                                | MIN         | NOM | MAX | MIN         | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5         | 5   | 5.5 | 4.75        | 5   | 5.25 | V    |
| V <sub>IH</sub> | High-level input voltage       |             | 2   |     | 2           |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage        |             |     | 0.8 |             |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current      |             |     | -12 |             |     | -32  | mA   |
| I <sub>OL</sub> | Low-level output current       |             |     | 32  |             |     | 64   | mA   |
| T <sub>A</sub>  | Operating free-air temperature | -55         |     | 125 | -40         |     | 85   | °C   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS  | CY54FCT480T |       |      | CY74FCT480T |       |      | UNIT |
|-------------------|--|-------------|-------|------|-------------|-------|------|------|
|                   |  | MIN         | TYPT† | MAX  | MIN         | TYPT† | MAX  |      |
| V <sub>IK</sub>   | V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA  |             | -0.7  | -1.2 |             |       |      | V    |
|                   | V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA   |             |       |      |             | -0.7  | -1.2 |      |
| V <sub>OH</sub>   | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA  | 2.4         | 3.3   |      |             |       |      | V    |
|                   | V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -15 mA   |             |       |      | 2.4         | 3.3   |      |      |
| V <sub>OL</sub>   | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA   | 0.3         | 0.55  |      |             |       |      | V    |
|                   | V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA  |             |       |      | 0.3         | 0.55  |      |      |
| V <sub>hys</sub>  | All inputs   | 0.2         |       |      | 0.2         |       |      | V    |
| I <sub>I</sub>    | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>                                   |             | 5     |      |             |       |      | µA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>                                  |             |       |      |             |       | 5    |      |
| I <sub>IH</sub>   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V   |             | ±1    |      |             |       |      | µA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V  |             |       |      |             |       | ±1   |      |
| I <sub>IL</sub>   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V   |             | ±1    |      |             |       |      | µA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V  |             |       |      |             |       | ±1   |      |
| I <sub>off</sub>  | V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V  |             | ±1    |      |             | ±1    |      | µA   |
| I <sub>OS</sub> ‡ | V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V  | -60         | -120  | -225 |             |       |      | mA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V   |             |       |      | -60         | -120  | -225 |      |
| I <sub>OZH</sub>  | V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V  |             | 10    |      |             |       |      | µA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V   |             |       |      |             |       | 10   |      |
| I <sub>OZL</sub>  | V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V  |             | -10   |      |             |       |      | µA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V   |             |       |      |             |       | -10  |      |
| I <sub>CC</sub>   | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V  | 0.1         | 0.2   |      |             |       |      | mA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V |             |       |      | 0.1         | 0.2   |      |      |
| ΔI <sub>CC</sub>  | V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open          | 0.5         | 2     |      |             |       |      | mA   |
|                   | V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open         |             |       |      | 0.5         | 2     |      |      |

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

| PARAMETER          | TEST CONDITIONS   | CY54FCT480T   |   |     | CY74FCT480T |      |         | UNIT       |
|--------------------|---|---|---|-----|-------------|------|---------|------------|
|                    |   | MIN   | TYP†  | MAX | MIN         | TYP† | MAX     |            |
| I <sub>CCD</sub> † | V <sub>CC</sub> = 5.5 V, Outputs open,<br>One bit switching at 50% duty cycle,<br>V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V  | 0.06 0.12   |   |     |             |      |         | mA/<br>MHz |
|                    | V <sub>CC</sub> = 5.25 V, Outputs open,<br>One bit switching at 50% duty cycle,<br>V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V |   |   |     | 0.06 0.12   |      |         |            |
| I <sub>C</sub> ‡   | V <sub>CC</sub> = 5.5 V,<br>f <sub>0</sub> = 0 MHz,<br>Outputs open   | One bit<br>switching<br>at f <sub>1</sub> = 2.5 MHz<br>at 50% duty<br>cycle | V <sub>IN</sub> ≤ 0.2 V or<br>V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V |     | 0.7         | 1.4  |         | mA         |
|                    |   |   | V <sub>IN</sub> = 3.4 V or GND  |     | 1           | 2.4  |         |            |
|                    |   | 16 bits<br>switching<br>at f <sub>1</sub> = 2.5 MHz<br>at 50% duty<br>cycle | V <sub>IN</sub> ≤ 0.2 V or<br>V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V |     | 2.5         | 5    |         |            |
|                    |   |   | V <sub>IN</sub> = 3.4 V or GND  |     | 6.5         | 21   |         |            |
|                    | V <sub>CC</sub> = 5.25 V,<br>f <sub>0</sub> = 0 MHz,<br>Outputs open  | One bit<br>switching<br>at f <sub>1</sub> = 2.5 MHz<br>at 50% duty<br>cycle | V <sub>IN</sub> ≤ 0.2 V or<br>V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V |     |             |      | 0.7 1.4 | mA         |
|                    |   |   | V <sub>IN</sub> = 3.4 V or GND  |     |             |      | 1 2.4   |            |
|                    |   | 16 bits<br>switching<br>at f <sub>1</sub> = 2.5 MHz<br>at 50% duty<br>cycle | V <sub>IN</sub> ≤ 0.2 V or<br>V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V |     |             |      | 2.5 5   |            |
|                    |   |   | V <sub>IN</sub> = 3.4 V or GND  |     |             |      | 6.5 21  |            |
| C <sub>i</sub>     |   |   | 5   | 10  |             | 5    | 10      | pF         |
| C <sub>o</sub>     |   |   | 9   | 12  |             | 9    | 12      | pF         |

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ This parameter is derived for use in total power-supply calculations.

# I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.

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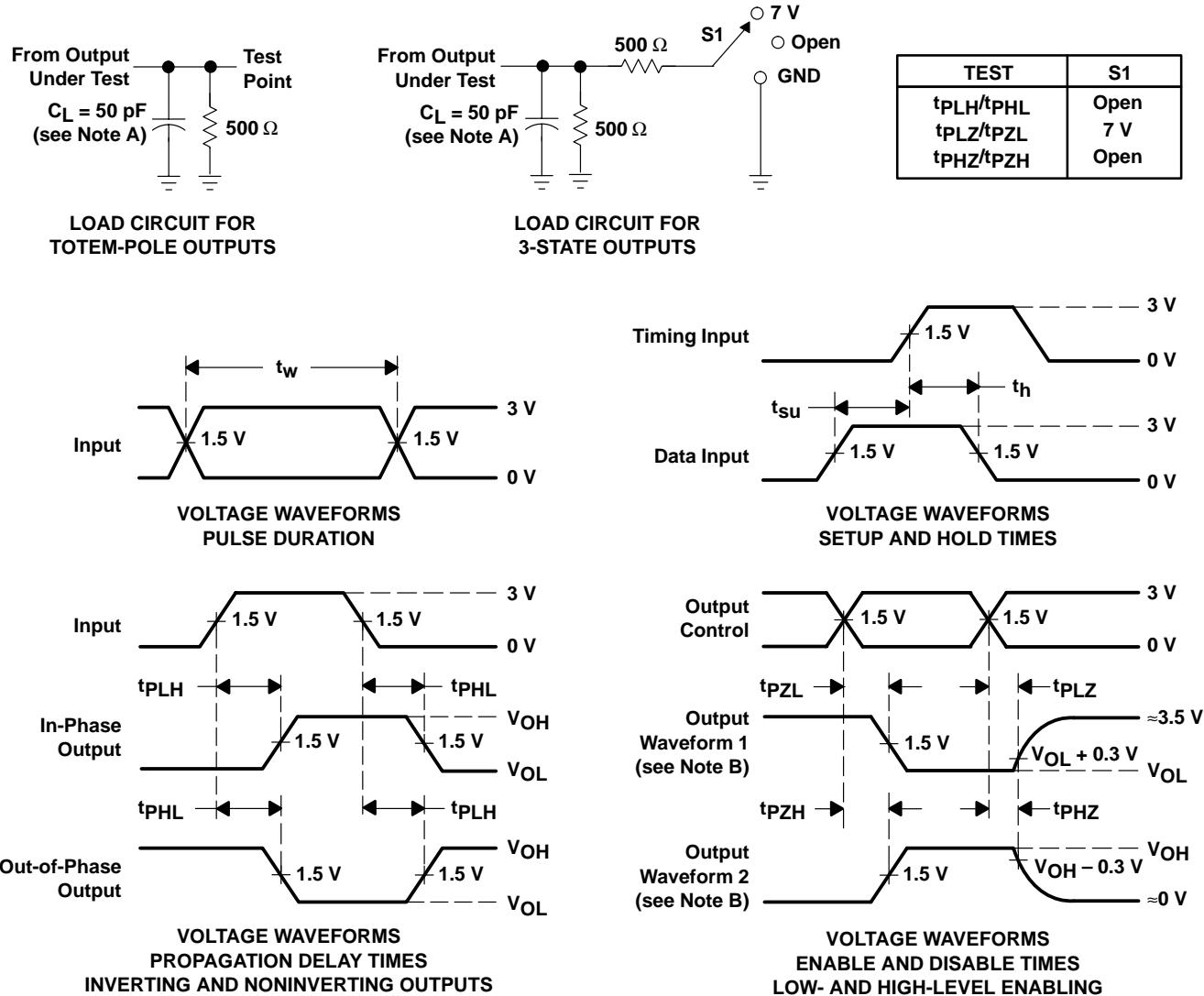
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## switching characteristics over operating free-air temperature range (see Figure 1)

| PARAMETER                     | FROM<br>(INPUT) | TO<br>(OUTPUT)                 | CY74FCT480AT |     | CY54FCT480BT |     | CY74FCT480BT |     | UNIT |
|-------------------------------|-----------------|--------------------------------|--------------|-----|--------------|-----|--------------|-----|------|
|                               |                 |                                | MIN          | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>PLH</sub>              | A               | <u>ODD</u><br>(see Figure 1)   |              | 7.5 |              | 7   |              | 6.1 | ns   |
| t <sub>PHL</sub>              |                 |                                |              | 7   |              | 6.6 |              | 6.1 |      |
| t <sub>PLH</sub>              | CHK/GEN         | <u>ODD</u><br>(see Figure 1)   |              | 6.5 |              | 6.3 |              | 5.9 | ns   |
| t <sub>PHL</sub>              |                 |                                |              | 7.5 |              | 7.4 |              | 5.9 |      |
| t <sub>PLH</sub> <sup>†</sup> | A               | <u>ERROR</u><br>(see Figure 2) |              | 7   |              | 7   |              | 6.1 | ns   |
| t <sub>PHL</sub>              |                 |                                |              | 8.5 |              | 8.1 |              | 6.5 |      |
| t <sub>PLH</sub>              | CHK/GEN         | <u>ERROR</u><br>(see Figure 2) |              | 7.5 |              | 7.1 |              | 5.7 | ns   |
| t <sub>PHL</sub>              |                 |                                |              | 7   |              | 6.9 |              | 5.5 |      |

<sup>†</sup>t<sub>PLH</sub> is measured up to V<sub>OUT</sub> = V<sub>OL</sub> + 0.3 V.

PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

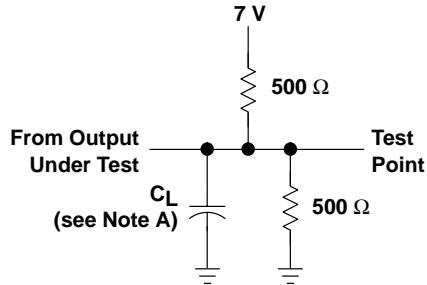
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

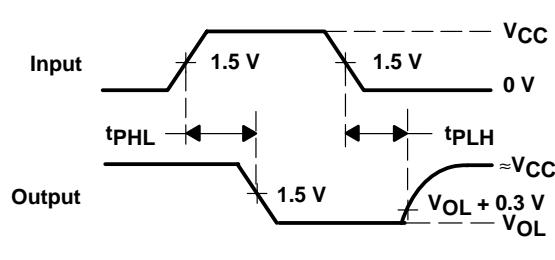
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## PARAMETER MEASUREMENT INFORMATION FOR OPEN-DRAIN OUTPUTS



LOAD CIRCUIT FOR  
OPEN-DRAIN OUTPUTS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CY54FCT480BTLM        | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CY54FCT<br>480BTLM  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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