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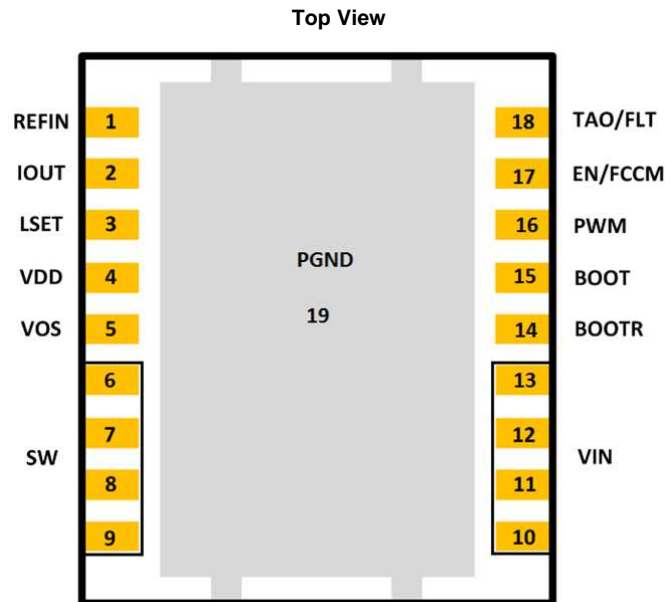
## 4 Revision History

### Changes from Original (June 2017) to Revision A

**Page**

•	更正了特性部分和器件信息表中的封装类型 .....	<b>1</b>
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
REFIN	1	External reference voltage input for current sensing amplifier.
IOUT	2	Output of current sensing amplifier. $V(IOUT) - V(REFIN)$ is proportional to the phase current.
LSET	3	A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.
VDD	4	Supply voltage for gate drivers and internal circuitry.
VOS	5	Output voltage sensing pin for the internal current sensing circuitry.
SW	6-9	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
VIN	10-13	Input voltage pin. Connect input capacitors close to this pin.
BOOTR	14	Return path for HS gate driver. It is connected to VSW internally.
BOOT	15	Bootstrap capacitor connection. Connect a minimum 0.1- $\mu$ F, 16-V, X5R ceramic cap from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
PWM	16	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time ( $t_{3HT}$ ).
EN/FCCM	17	This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, Diode Emulation Mode is enabled for sync FET. When the pin is high, device operates in Forced Continuous Conduction Mode. When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.
TAO/FAULT	18	Temperature Amplifier Output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown, LSOC, or HSS detection circuit is tripped.
PGND	19	Power ground.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)<sup>(1)</sup>

	MIN	MAX	UNIT
$V_{IN}$ to $P_{GND}$	-0.3	20	V
$V_{IN}$ to $V_{SW}$	-0.3	20	V
$V_{IN}$ to $V_{SW}$ (10 ns)		23	V
$V_{SW}$ to $P_{GND}$	-0.3	20	V
$V_{SW}$ to $P_{GND}$ (10 ns)	-7	23	V
$V_{DD}$ to $P_{GND}$	-0.3	7	V
EN/FCCM, TAO/FLT, LSET to $P_{GND}$ <sup>(2)</sup>	-0.3	$V_{DD} + 0.3$	V
IOUT, VOS, PWM to $P_{GND}$	-0.3	7	V
REFIN	-0.3	3.6	V
BOOT to BOOTR <sup>(2)</sup>	-0.3	$V_{DD} + 0.3$	V
BOOT to $P_{GND}$	-0.3	30	V
$T_J$ Operating junction temperature	-55	150	$^\circ\text{C}$
$T_{stg}$ Storage temperature	-55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Should not exceed 7 V.

### 6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM)	$\pm 2000$
	Charged-device model (CDM)	$\pm 500$

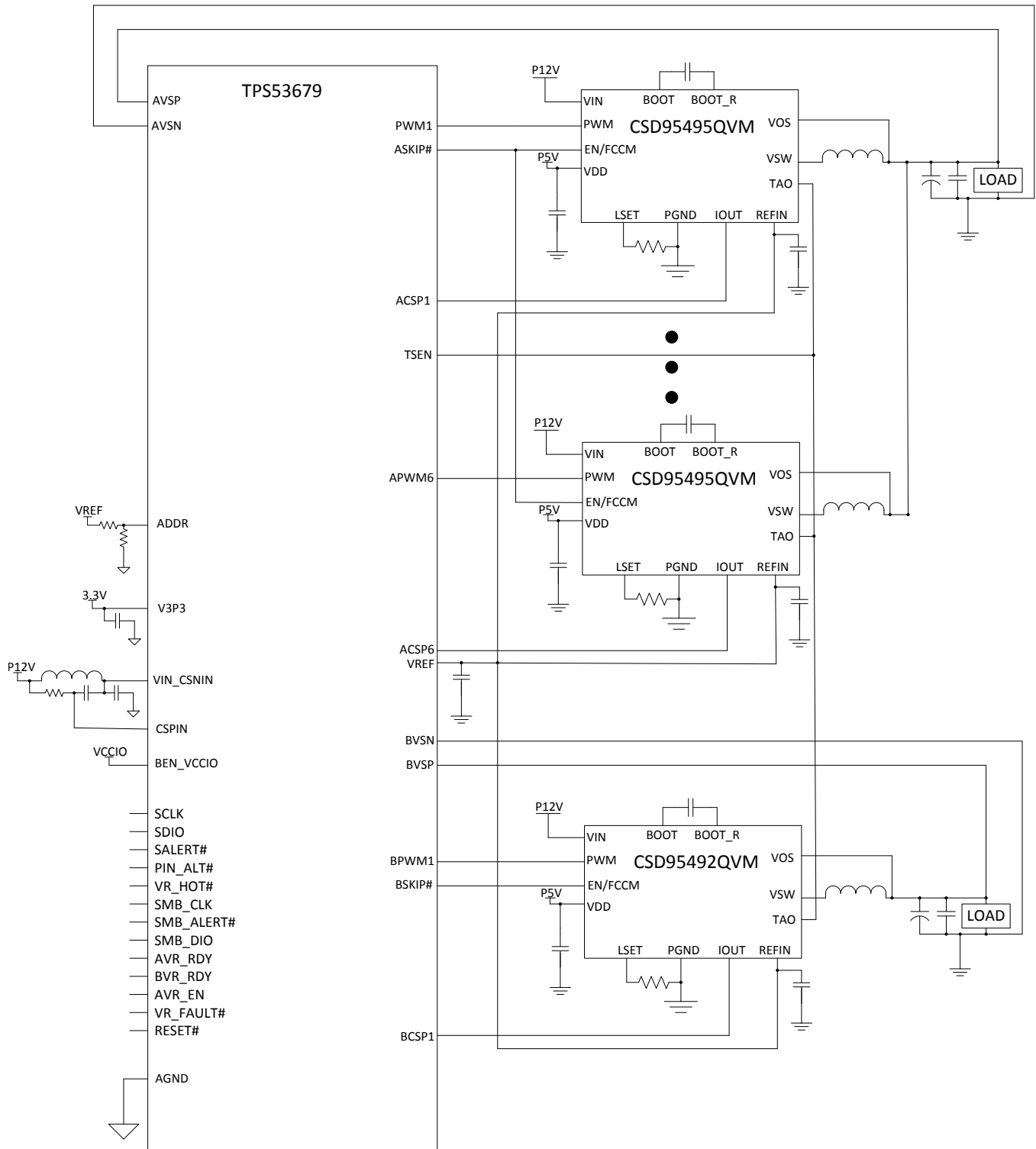
### 6.3 Recommended Operating Conditions

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

	MIN	MAX	UNIT
$V_{DD}$ Driver supply voltage	4.5	5.5	V
$V_{IN}$ Input supply voltage <sup>(1)</sup>	4.5	16	V
$V_{OUT}$ Output voltage		5.5	V
PWM PWM to $P_{GND}$		$V_{DD}$	V
$I_{OUT}$ Continuous output current	$V_{IN} = 12\text{ V}$ , $V_{DD} = 5\text{ V}$ , $V_{OUT} = 1.2\text{ V}$ , $f_{SW} = 500\text{ kHz}$ <sup>(2)</sup>	50	A
$I_{OUT-PK}$ Peak output current <sup>(3)</sup>		75	A
$f_{SW}$ Switching frequency	$C_{BST} = 0.1\ \mu\text{F}$ (min), $V_{OUT} = 2.5\text{ V}$ (max)	1250	kHz
On-time duty cycle	$f_{SW} = 1\text{ MHz}$	85%	
Minimum PWM on-time		20	ns
Operating junction temperature		-40	$^\circ\text{C}$

- (1) Operating at high  $V_{IN}$  can create excessive AC voltage overshoots on the switch node ( $V_{SW}$ ) during MOSFET switching transients. For reliable operation, the switch node ( $V_{SW}$ ) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
- (2) Measurement made with six 10- $\mu\text{F}$  (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across  $V_{IN}$  to  $P_{GND}$  pins.
- (3) System conditions as defined in Note 2. Peak output current is applied for  $t_p = 50\ \mu\text{s}$ .

## 7 Application Schematic



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**Figure 1. Application Schematic**

Note: The schematic in [Figure 1](#) is a conceptual drawing only. Actual designs may require additional components not shown.

## 8 器件和文档支持

### 8.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com](http://TI.com) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。

### 8.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 8.3 商标

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### 8.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 8.5 Glossary

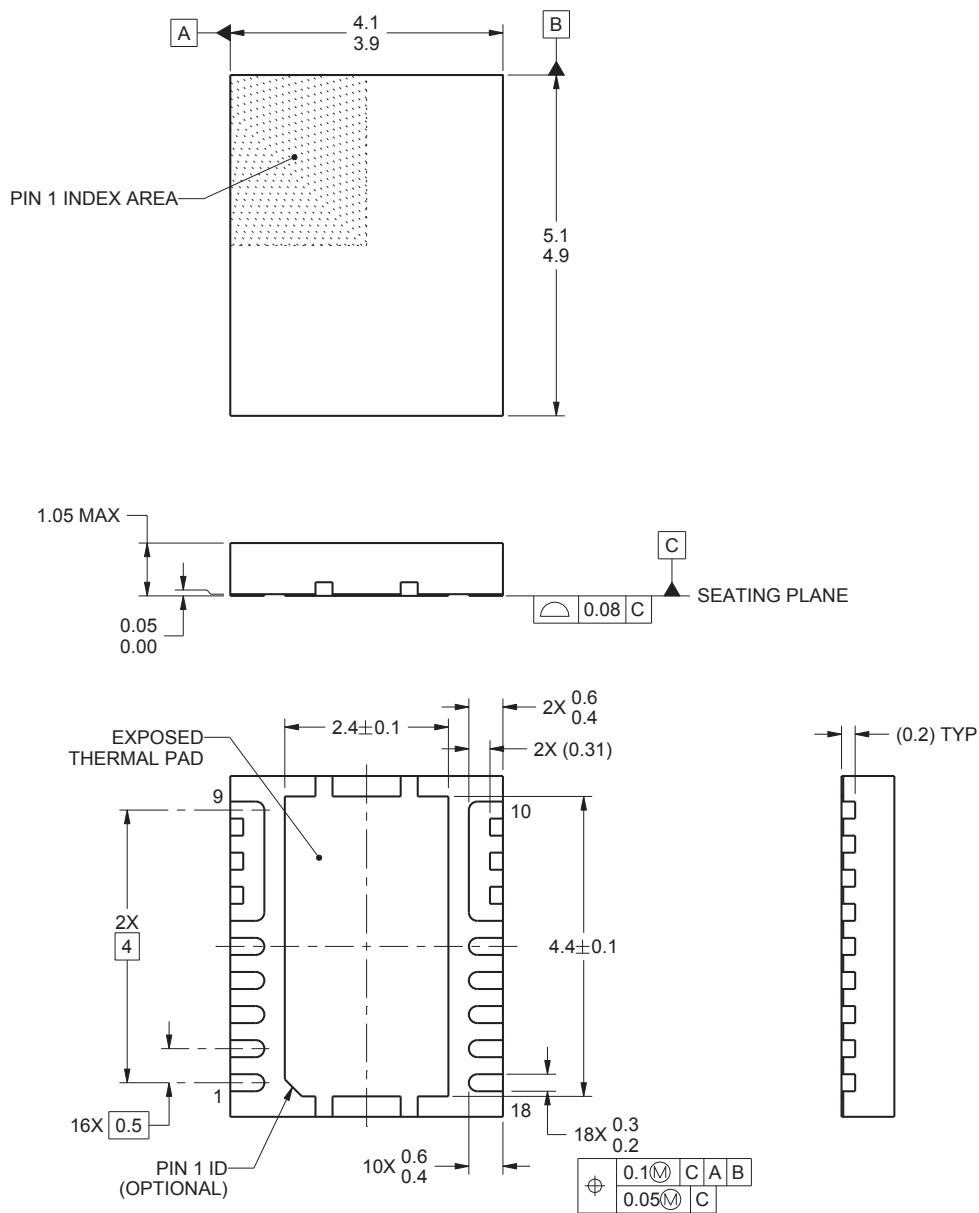
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 机械、封装和可订购信息

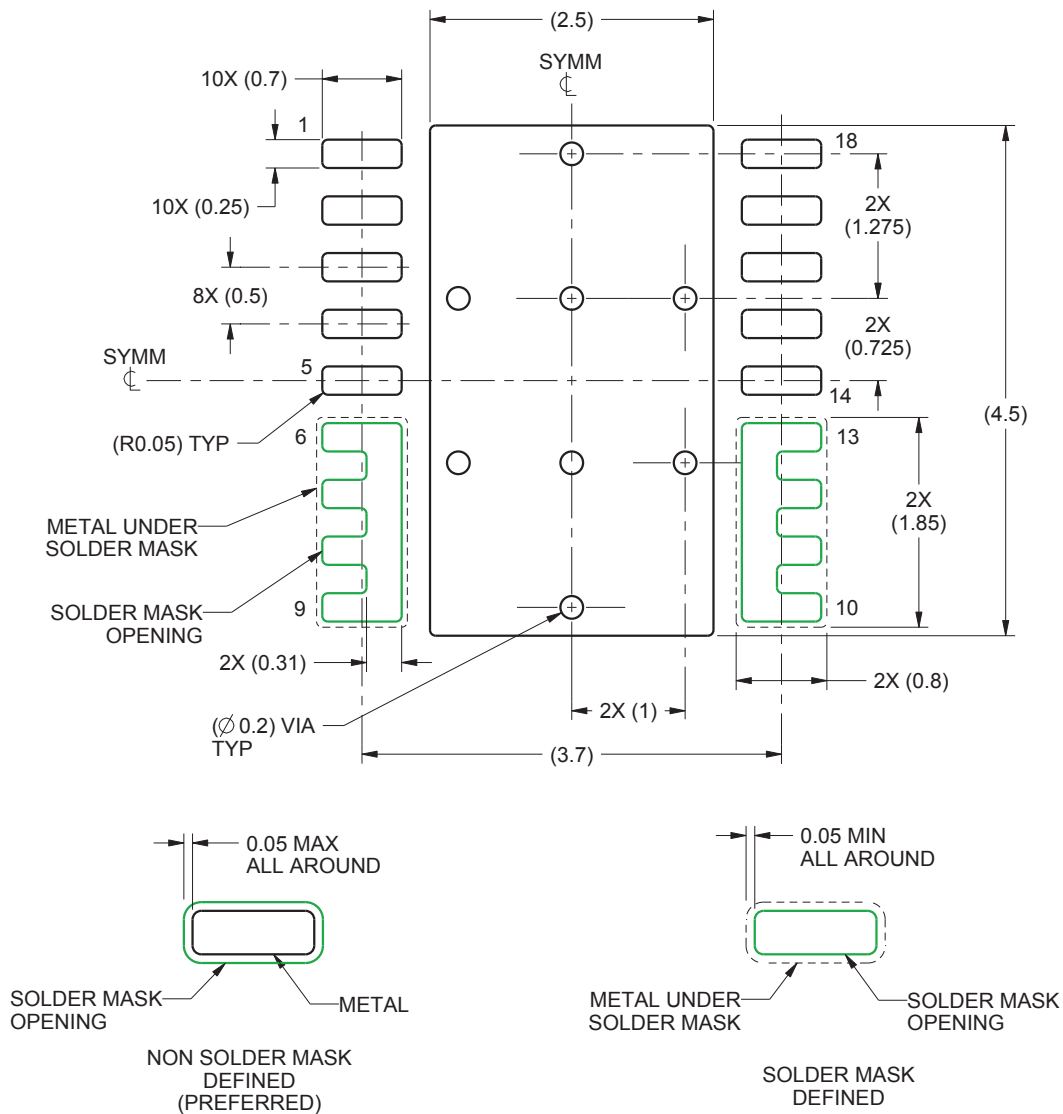
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

### 9.1 机械制图



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 必须在印刷电路板上焊接封装散热焊盘，以获得良好的散热和机械性能。

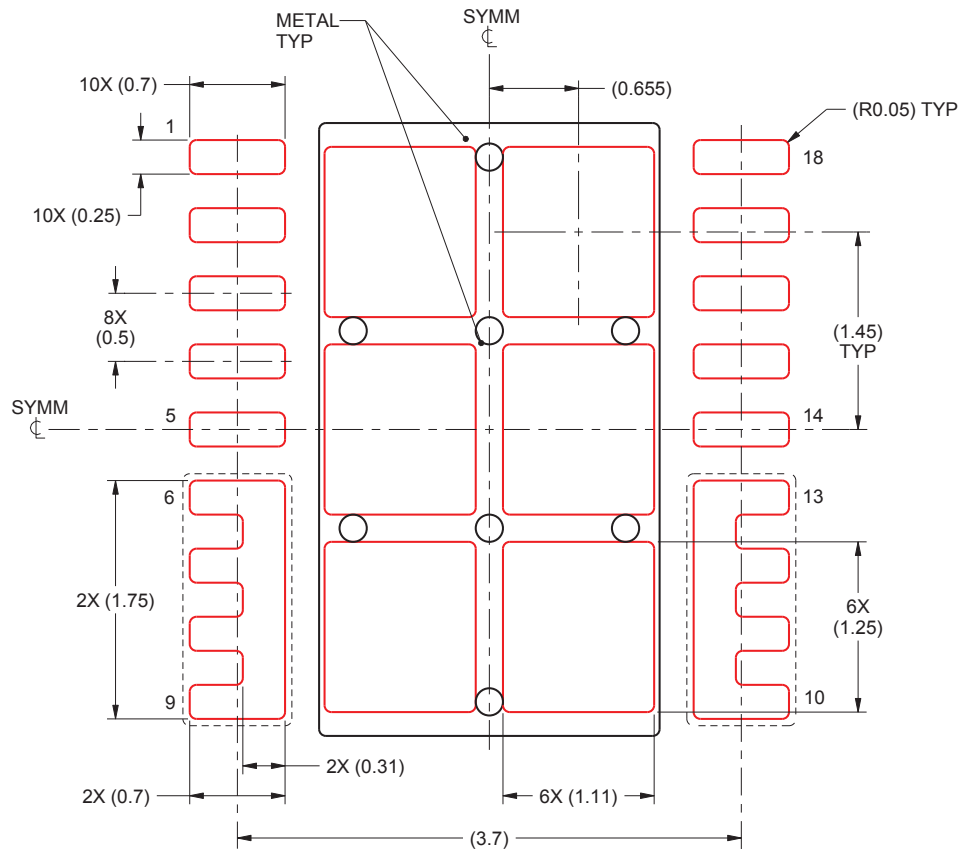
## 9.2 推荐 PCB 焊盘图案



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 此封装设计用于焊接到电路板的散热焊盘上。有关更多信息，请参阅《[QFN/SON PCB 连接](#)》(SLUA271)。



### 9.3 建议模版开孔



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95495QVM	ACTIVE	VSON-CLIP	DMH	18	2500	RoHS-Exempt & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-55 to 150	95495QM	<a href="#">Samples</a>
CSD95495QVMT	ACTIVE	VSON-CLIP	DMH	18	250	RoHS-Exempt & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-55 to 150	95495QM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95495QVM	VSON-CLIP	DMH	18	2500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
CSD95495QVMT	VSON-CLIP	DMH	18	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
CSD95495QVMT	VSON-CLIP	DMH	18	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95495QVM	VSON-CLIP	DMH	18	2500	346.0	346.0	33.0
CSD95495QVMT	VSON-CLIP	DMH	18	250	210.0	185.0	35.0
CSD95495QVMT	VSON-CLIP	DMH	18	250	213.0	191.0	35.0

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