

## CSD86360Q5D 同步降压 NexFET™ 电源块

### 1 特性

- 半桥电源块
- 25A 电流下系统效率高达 91%
- 运行电流高达 50A
- 高频工作（高达 1.5MHz）
- 高密度 SON 5mm × 6mm 封装
- 针对 5V 栅极驱动进行了优化
- 开关损耗较低
- 超低电感封装
- 符合 RoHS 标准
- 无卤素
- 无铅引脚镀层

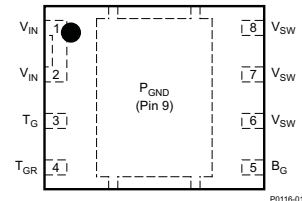
### 2 应用

- 同步降压转换器
  - 高频应用
  - 高电流、低占空比应用
- 多相位同步降压转换器
- 负载点 (POL) 直流/直流转换器
- IMVP、VRM 和 VRD 应用

### 3 说明

CSD86360Q5D NexFET™ 电源块是面向同步降压应用的优化设计方案，能够以 5mm × 6mm 的小巧外形提供高电流、高效率以及高频率性能。该产品针对 5V 栅极驱动应用进行了优化，在与外部控制器/驱动器的任一 5V 栅极驱动配套使用时，可提供一套灵活的解决方案来实现高密度电源。

图 1. 俯视图

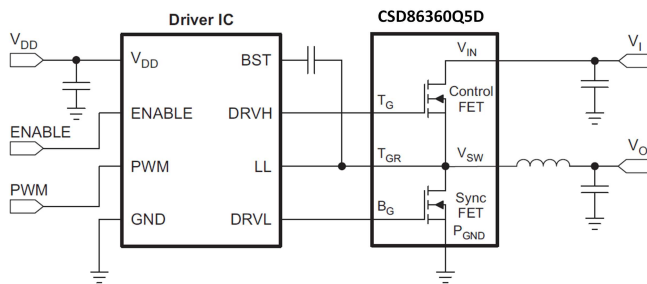


器件信息(1)

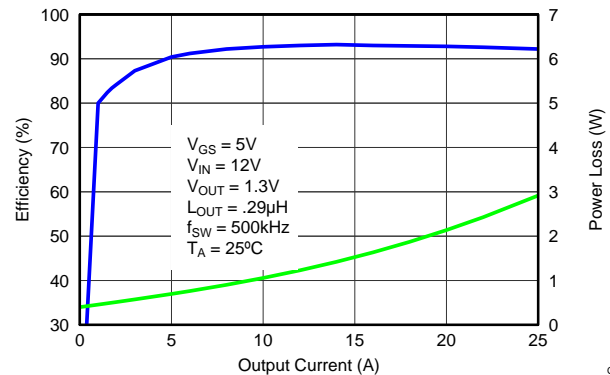
器件	介质	数量	封装	配送
CSD86360Q5D	13 英寸卷带	2500	5.00mm × 6.00mm SON 塑料封装	卷带封装

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型电路



典型电源块效率与功率损耗



G001



## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	<b>7</b>	<b>Layout</b> .....	<b>16</b>
<b>2</b>	<b>应用</b> .....	<b>1</b>	7.1	Layout Guidelines .....	16
<b>3</b>	<b>说明</b> .....	<b>1</b>	7.2	Layout Example .....	17
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	<b>8</b>	<b>器件和文档支持</b> .....	<b>18</b>
<b>5</b>	<b>Specifications</b> .....	<b>3</b>	8.1	文档支持 .....	18
5.1	Absolute Maximum Ratings .....	3	8.2	接收文档更新通知 .....	18
5.2	Recommended Operating Conditions .....	3	8.3	社区资源 .....	18
5.3	Power Block Performance .....	3	8.4	商标 .....	18
5.4	Thermal Information .....	3	8.5	静电放电警告 .....	18
5.5	Electrical Characteristics .....	4	8.6	术语表 .....	18
5.6	Typical Power Block Device Characteristics .....	6	<b>9</b>	<b>机械、封装和可订购信息</b> .....	<b>19</b>
5.7	Typical Power Block MOSFET Characteristics .....	8	9.1	Q5D 封装尺寸 .....	19
<b>6</b>	<b>Application and Implementation</b> .....	<b>11</b>	9.2	焊盘布局建议 .....	20
6.1	Application Information .....	11	9.3	模版建议 .....	21
6.2	Typical Application .....	14	9.4	Q5D 卷带信息 .....	21

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (May 2013) to Revision B	Page
• Changed Recommended PCB Design Overview section to <i>Layout</i> section .....	16
• 已添加 器件和文档支持部分 .....	18
• 已更改 将机械数据部分更改为机械、封装和可订购信息 部分 .....	19
• 更新了 Q5D 封装尺寸 部分 .....	19
• 更新了焊盘图案建议 图 .....	20
• 更新了模版建议 图 .....	21

Changes from Original (September 2012) to Revision A	Page
• Changed the footnote notations in the THERMAL INFORMATION table .....	3
• Updated <a href="#">Figure 7</a> .....	6
• Updated <a href="#">Figure 8</a> .....	6
• Updated <a href="#">Figure 9</a> .....	6
• Updated <a href="#">Figure 10</a> .....	6

## 5 Specifications

### 5.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	$V_{IN}$ to $P_{GND}$		25	V
	$V_{SW}$ to $P_{GND}$		25	
	$V_{SW}$ to $P_{GND}$ (10 ns)		27	
	$T_G$ to $T_{GR}$	–8	10	
	$B_G$ to $P_{GND}$	–8	10	
Pulsed current rating, $I_{DM}$ <sup>(2)</sup>			120	A
Power dissipation, $P_D$ <sup>(3)</sup>			13	W
Avalanche energy, $E_{AS}$	Sync FET, $I_D = 110\text{ A}$ , $L = 0.1\text{ mH}$		605	mJ
	Control FET, $I_D = 61\text{ A}$ , $L = 0.1\text{ mH}$		186	
Operating junction, $T_J$		–55	150	$^\circ\text{C}$
Storage temperature, $T_{STG}$		–55	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Pulse duration  $\leq 50\text{ }\mu\text{s}$ . Duty cycle  $\leq 0.01\%$ .

(3)  $T_{PCB} \leq 95^\circ\text{C}$ .

### 5.2 Recommended Operating Conditions

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{GS}$ Gate drive voltage		4.5	8	V
$V_{IN}$ Input supply voltage			22	V
$f_{SW}$ Switching frequency	$C_{BST} = 0.1\text{ }\mu\text{F}$ (min)	200	1500	kHz
Operating current			50	A
$T_J$ Operating temperature			125	$^\circ\text{C}$

### 5.3 Power Block Performance

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{LOSS}$ Power loss <sup>(1)</sup>	$V_{IN} = 12\text{ V}$ , $V_{GS} = 5\text{ V}$ , $V_{OUT} = 1.3\text{ V}$ , $I_{OUT} = 25\text{ A}$ , $f_{SW} = 500\text{ kHz}$ , $L_{OUT} = 0.3\text{ }\mu\text{H}$ , $T_J = 25^\circ\text{C}$		2.6		W
$I_{QVIN}$ $V_{IN}$ quiescent current	$T_G$ to $T_{GR} = 0\text{ V}$ $B_G$ to $P_{GND} = 0\text{ V}$		10		$\mu\text{A}$

(1) Measurement made with six 10- $\mu\text{F}$  (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across  $V_{IN}$  to  $P_{GND}$  pins and using a high current 5-V driver IC.

### 5.4 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) <sup>(1)</sup>			102	$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance (max Cu) <sup>(1)(2)</sup>			50	

(1)  $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in  $\times$  1.5-in (3.81-cm  $\times$  3.81-cm), 0.06-in (1.52-mm) thick FR4 board.  $R_{\theta JC}$  is specified by design while  $R_{\theta JA}$  is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>) Cu.

## Thermal Information (continued)

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

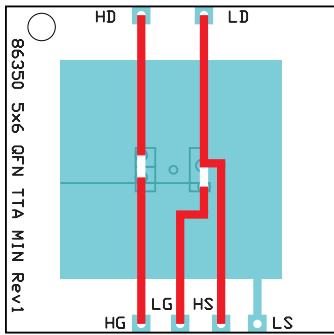
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) <sup>(1)</sup>			20	$^\circ\text{C/W}$
	Junction-to-case thermal resistance ( $P_{GND}$ pin) <sup>(1)</sup>			2	

## 5.5 Electrical Characteristics

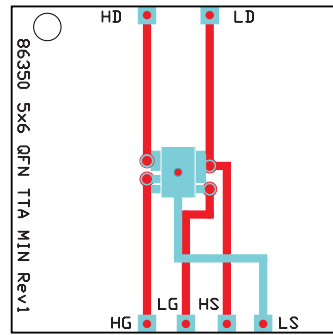
 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			
			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS									
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>DS</sub> = 250 μA	25			25		V	
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V			1			1 μA	
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +10 / −8 V			100			100 nA	
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = 250 μA	1		2.1	0.75		1.15 V	
Z <sub>DS(on)</sub>	Drain-to-source on-impedance	V <sub>IN</sub> = 12 V, V <sub>DD</sub> = 5 V, V <sub>OUT</sub> = 1.3 V I <sub>OUT</sub> = 25 A, f <sub>SW</sub> = 500 kHz, L <sub>OUT</sub> = 0.3 μH	3.7			0.7		mΩ	
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 10 V, I <sub>DS</sub> = 20 A	113			169		S	
DYNAMIC CHARACTERISTICS									
C <sub>ISS</sub>	Input capacitance <sup>(1)</sup>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 12.5 V, f = 1 MHz		1590	2060		3910	5080 pF	
C <sub>OSS</sub>	Output capacitance <sup>(1)</sup>			840	1090		1970	2560 pF	
C <sub>RSS</sub>	Reverse transfer capacitance <sup>(1)</sup>			42	54		53	69 pF	
R <sub>G</sub>	Series gate resistance <sup>(1)</sup>	V <sub>DS</sub> = 12.5 V, I <sub>DS</sub> = 20 A		1.2	2.5		1.1	2.2 Ω	
Q <sub>g</sub>	Gate charge total (4.5 V) <sup>(1)</sup>			9.7	12.6		23	30 nC	
Q <sub>gd</sub>	Gate charge gate-to-drain			2.3			3.6	nC	
Q <sub>gs</sub>	Gate charge gate-to-source			3.5			6.0	nC	
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			1.9			3.5	nC	
Q <sub>OSS</sub>	Output charge	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 0 V		15.1			33	nC	
t <sub>d(on)</sub>	Turnon delay time	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 4.5 V, I <sub>DS</sub> = 20 A, R <sub>G</sub> = 2 Ω		8.4			9.5	ns	
t <sub>r</sub>	Rise time			20.4			14.8	ns	
t <sub>d(off)</sub>	Turnoff delay time			14.5			29.3	ns	
t <sub>f</sub>	Fall time			4.3			6.6	ns	
DIODE CHARACTERISTICS									
V <sub>SD</sub>	Diode forward voltage	I <sub>DS</sub> = 20 A, V <sub>GS</sub> = 0 V		0.85	1		0.75	0.82 V	
Q <sub>rr</sub>	Reverse recovery charge	V <sub>dd</sub> = 12 V, I <sub>F</sub> = 20 A, di/dt = 300 A/μs		27			50	nC	
t <sub>rr</sub>	Reverse recovery time			22			34	ns	

(1) Specified by design.



Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
(6.45 cm<sup>2</sup>) of 2-oz  
(0.071-mm) thick Cu.



Max  $R_{\theta JA} = 102^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz (0.071-mm) thick  
Cu.

## 5.6 Typical Power Block Device Characteristics

$T_J = 125^\circ\text{C}$ , unless stated otherwise.

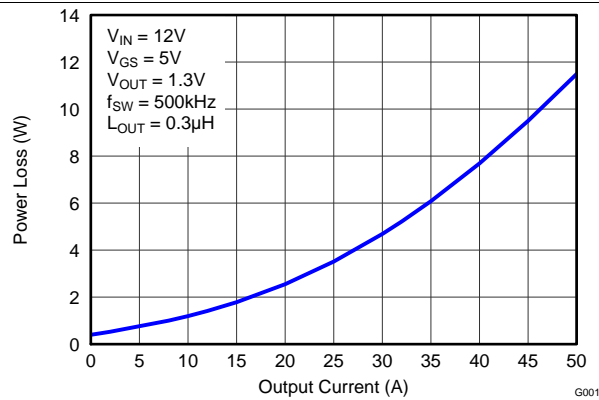


Figure 2. Power Loss vs Output Current

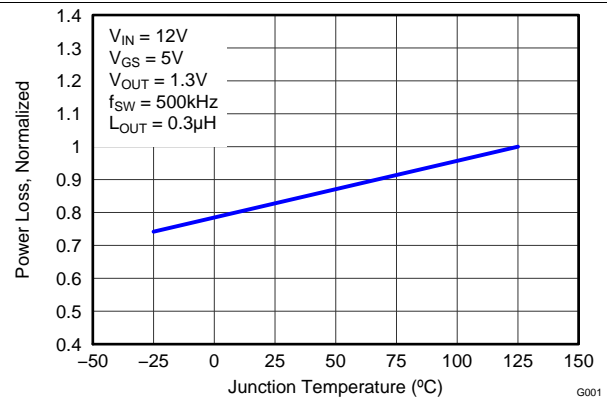


Figure 3. Normalized Power Loss vs Temperature

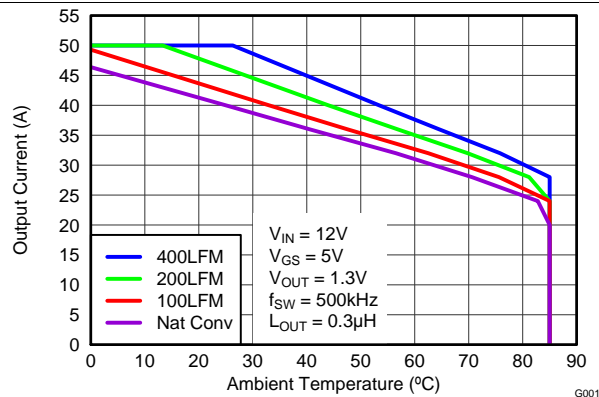


Figure 4. Safe Operating Area – PCB Vertical Mount (1)

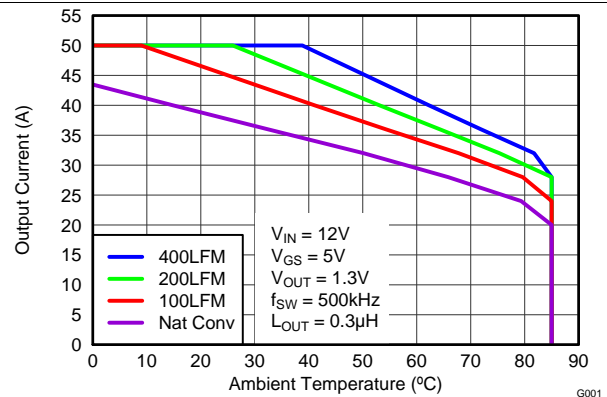


Figure 5. Safe Operating Area – PCB Horizontal Mount (1)

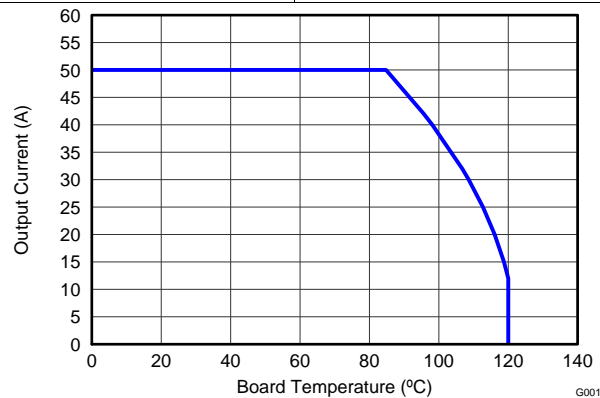
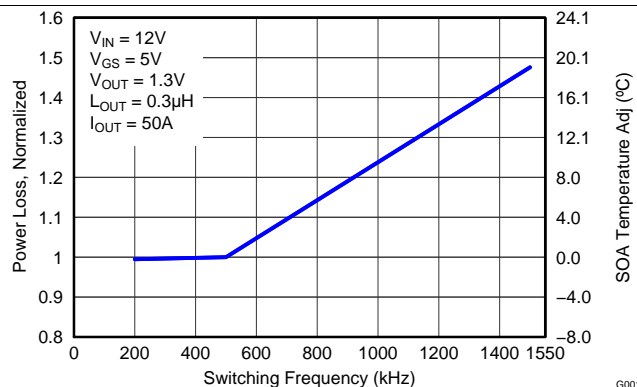


Figure 6. Typical Safe Operating Area(1)

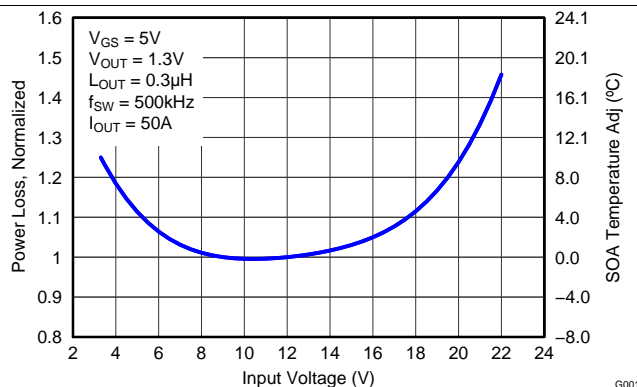
- (1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See [Application and Implementation](#) section for detailed explanation.

## Typical Power Block Device Characteristics (continued)

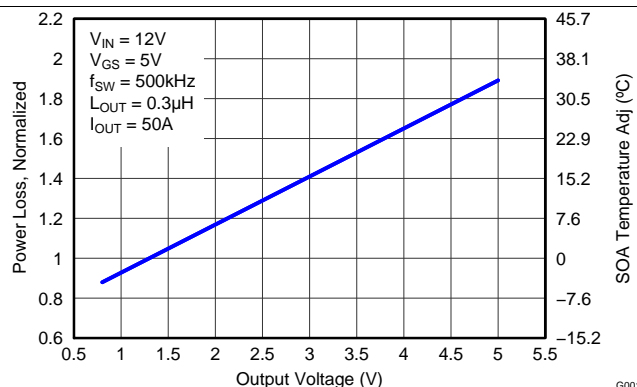
$T_J = 125^\circ\text{C}$ , unless stated otherwise.



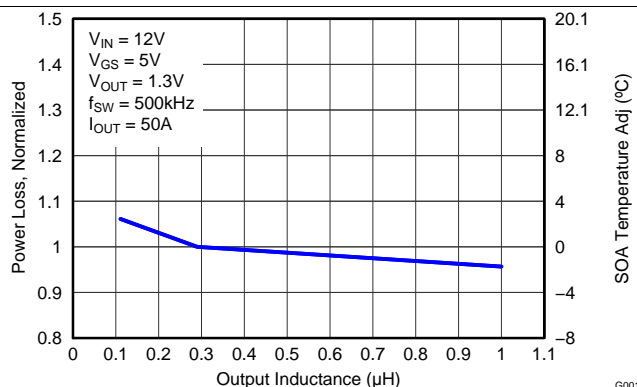
**Figure 7. Normalized Power Loss vs Switching Frequency**



**Figure 8. Normalized Power Loss vs Input Voltage**



**Figure 9. Normalized Power Loss vs Output Voltage**



**Figure 10. Normalized Power Loss vs Output Inductance**

## 5.7 Typical Power Block MOSFET Characteristics

$T_A = 25^\circ\text{C}$ , unless stated otherwise.

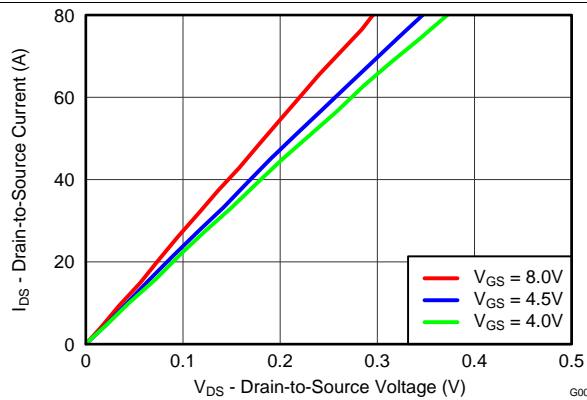


Figure 11. Control MOSFET Saturation

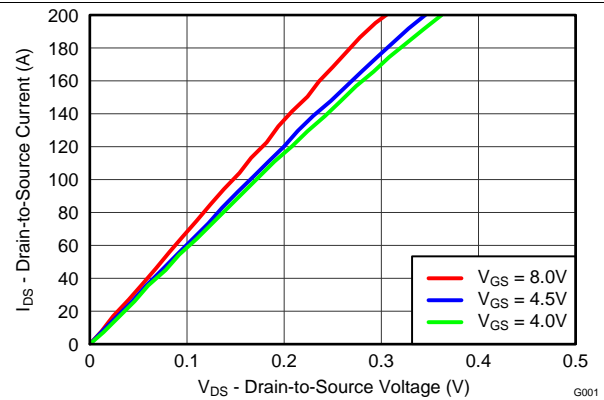


Figure 12. Sync MOSFET Saturation

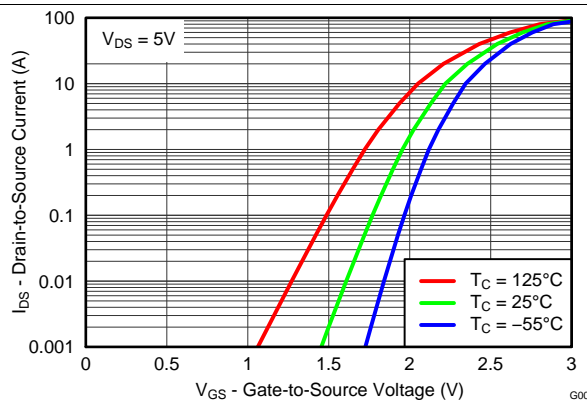


Figure 13. Control MOSFET Transfer

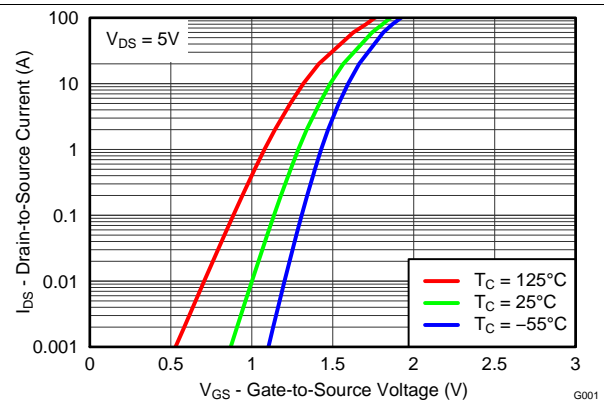


Figure 14. Sync MOSFET Transfer

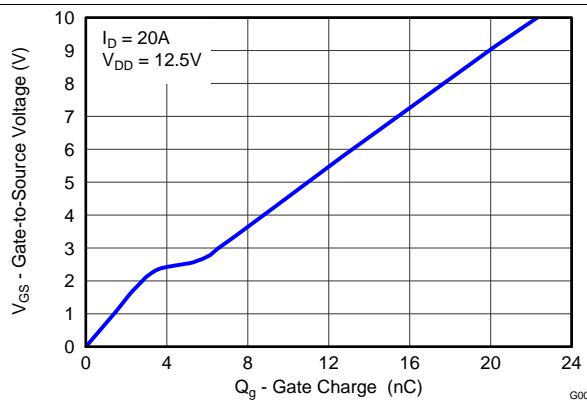


Figure 15. Control MOSFET Gate Charge

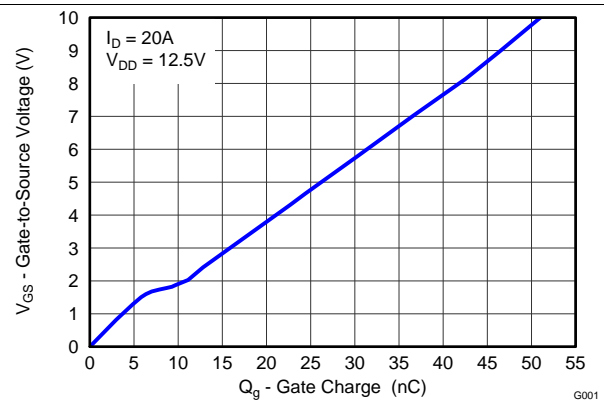


Figure 16. Sync MOSFET Gate Charge



## Typical Power Block MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ , unless stated otherwise.

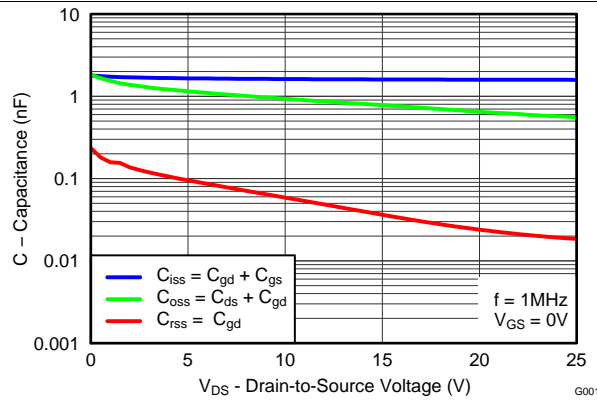


Figure 17. Control MOSFET Capacitance

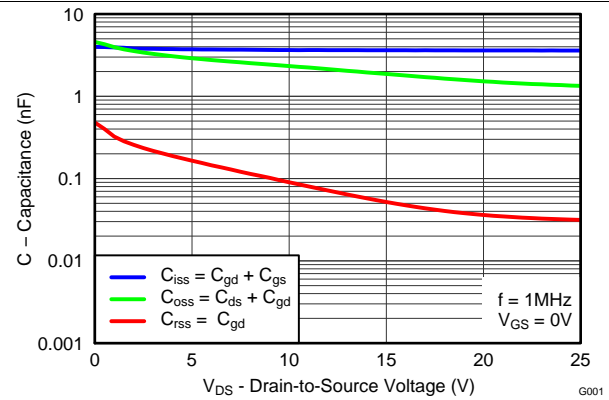


Figure 18. Sync MOSFET Capacitance

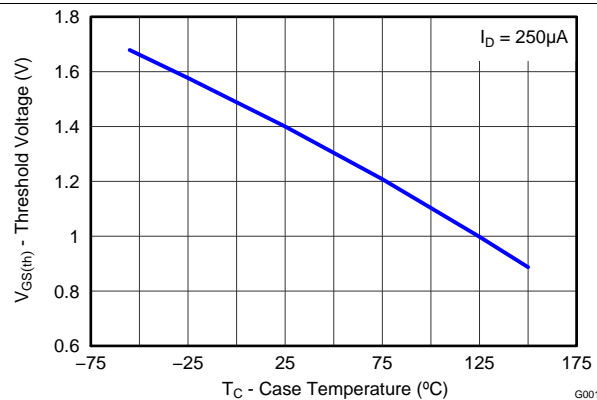


Figure 19. Control MOSFET  $V_{GS(th)}$

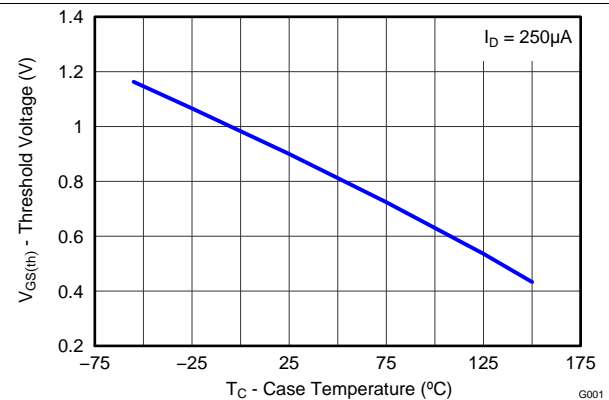


Figure 20. Sync MOSFET  $V_{GS(th)}$

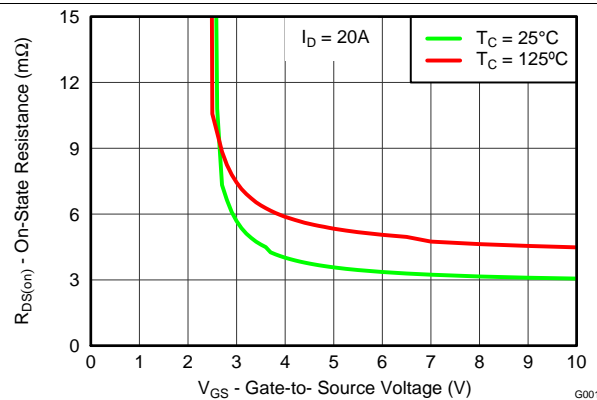


Figure 21. Control MOSFET  $R_{DS(on)}$  vs  $V_{GS}$

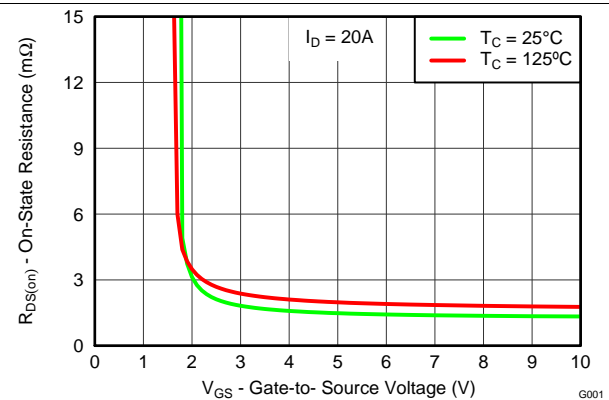


Figure 22. Sync MOSFET  $R_{DS(on)}$  vs  $V_{GS}$

## Typical Power Block MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ , unless stated otherwise.

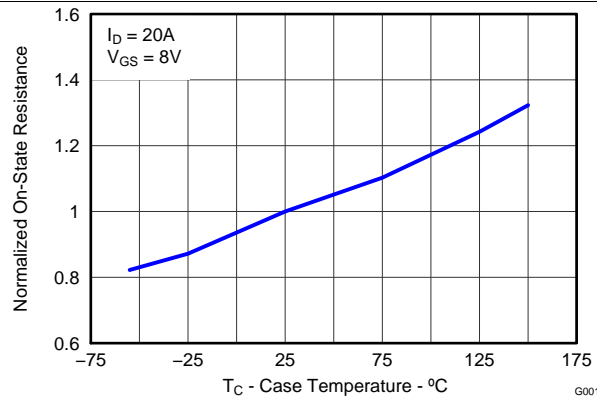


Figure 23. Control MOSFET Normalized  $R_{DS(on)}$

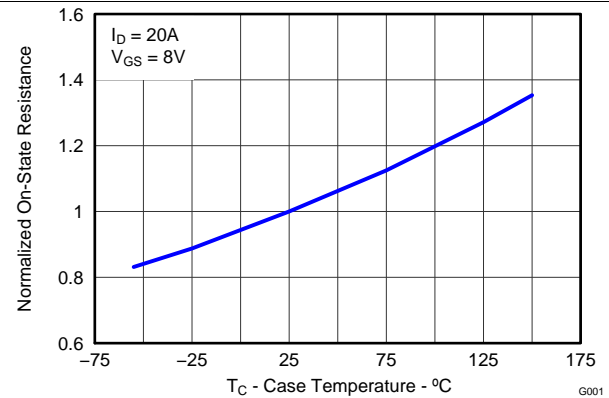


Figure 24. Sync MOSFET Normalized  $R_{DS(on)}$

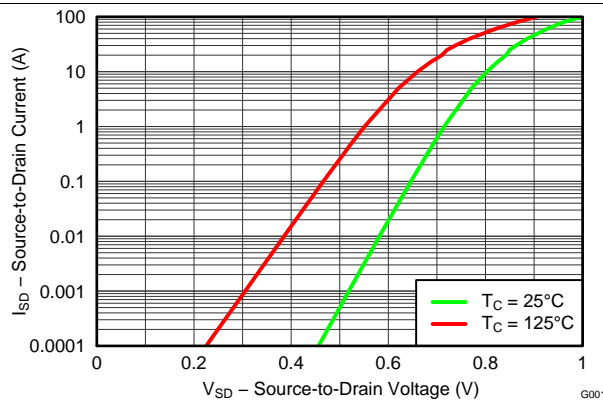


Figure 25. Control MOSFET Body Diode

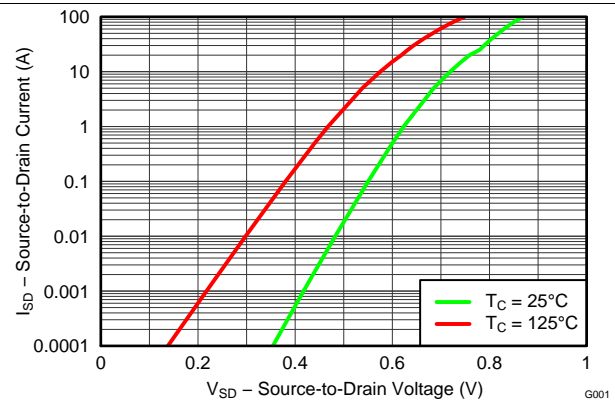


Figure 26. Sync MOSFET Body Diode

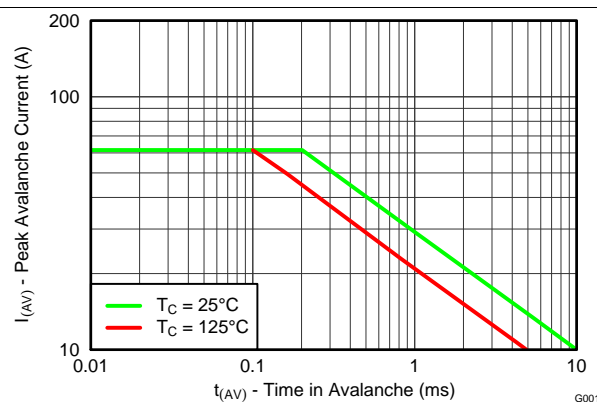


Figure 27. Control MOSFET Unclamped Inductive Switching

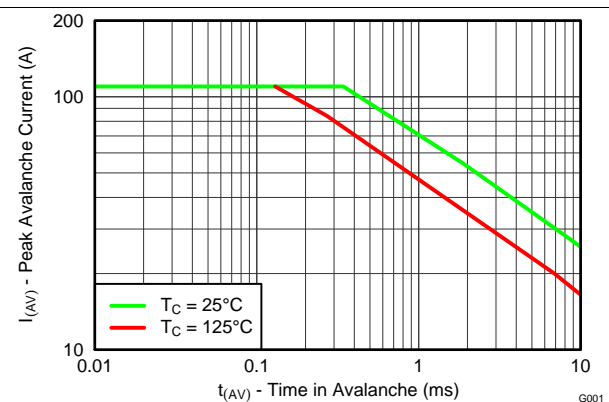


Figure 28. Sync MOSFET Unclamped Inductive Switching

## 6 Application and Implementation

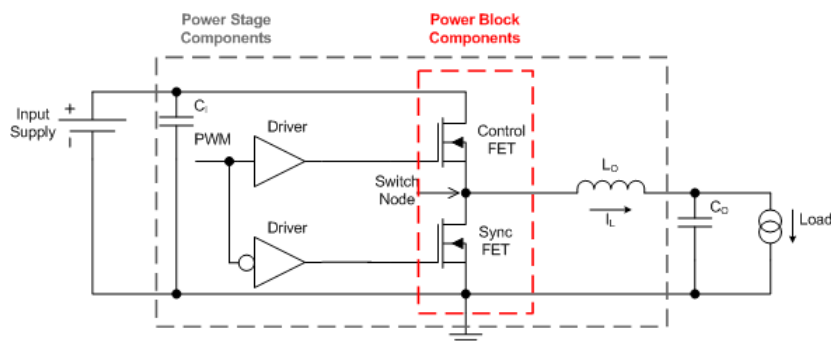
### NOTE

Information in the following Application section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI customers are responsible for determining suitability of components selection for their designs. Customers should validate and test their design implementation to confirm system functionality.

### 6.1 Application Information

#### 6.1.1 Equivalent System Performance

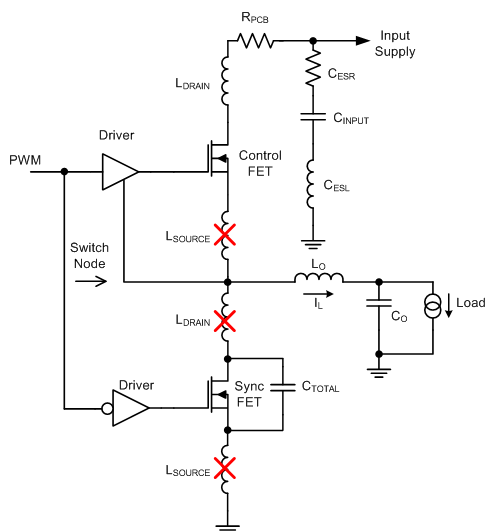
Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see Figure 29). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing  $R_{DS(ON)}$ .



**Figure 29. Equivalent System Schematic**

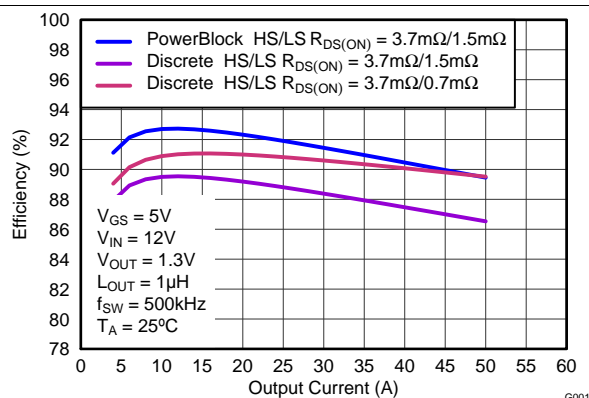
The CSD86360Q5D is part of TI's power block product family, which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon, which has been optimized for switching performance, as well as minimizing losses associated with  $Q_{GD}$ ,  $Q_{GS}$ , and  $Q_{RR}$ . Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see Figure 30). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET, which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in [Power Loss Calculation With CSI Consideration for Synchronous Buck Converters](#) (SLPA009).

### Application Information (continued)

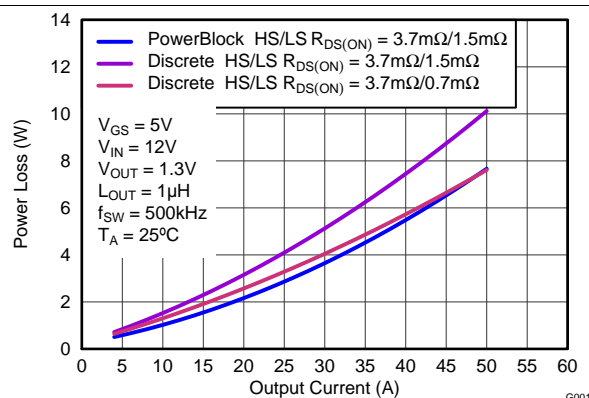


### Figure 30. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar  $R_{DS(ON)}$  and MOSFET chipsets with lower  $R_{DS(ON)}$ . [Figure 31](#) and [Figure 32](#) compare the efficiency and power loss performance of the CSD86360Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD86360Q5D clearly highlights the importance of considering the effective AC on-impedance ( $Z_{DS(ON)}$ ) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET  $R_{DS(ON)}$  specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.



**Figure 31. Efficiency Comparison for Discrete Parts vs Power Block**



**Figure 32. Power Loss Comparison for Discrete Parts vs Power Block**

## Application Information (continued)

**Table 1** below compares the traditional DC measured  $R_{DS(ON)}$  of CSD86360Q5D versus its  $Z_{DS(ON)}$ . This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured  $R_{DS(ON)}$  values that are equivalent to CSD86360Q5D's  $Z_{DS(ON)}$  value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

**Table 1. Comparison of  $R_{DS(ON)}$  vs  $Z_{DS(ON)}$**

PARAMETER	HS		LS	
	TYP	MAX	TYP	MAX
Effective AC on-impedance $Z_{DS(ON)}$ ( $V_{GS} = 5\text{ V}$ )	3.7	—	0.7	—
DC measured $R_{DS(ON)}$ ( $V_{GS} = 4.5\text{ V}$ )	3.7	4.5	1.5	1.9

The CSD86360Q5D NexFET™ power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed, which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

### 6.1.2 Power Loss Curves

MOSFET centric parameters such as  $R_{DS(ON)}$  and  $Q_{gd}$  are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. **Figure 2** plots the power loss of the CSD86360Q5D as a function of load current. This curve is measured by configuring and running the CSD86360Q5D as it would be in the final application (see **Figure 33**). The measured power loss is the CSD86360Q5D loss and consists of both input conversion loss and gate drive loss. **Equation 1** is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power loss} \quad (1)$$

The power loss curve in **Figure 2** is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

### 6.1.3 Safe Operating Area (SOA) Curves

The SOA curves in the CSD86360Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. **Figure 4** to **Figure 6** outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

### 6.1.4 Normalized Curves

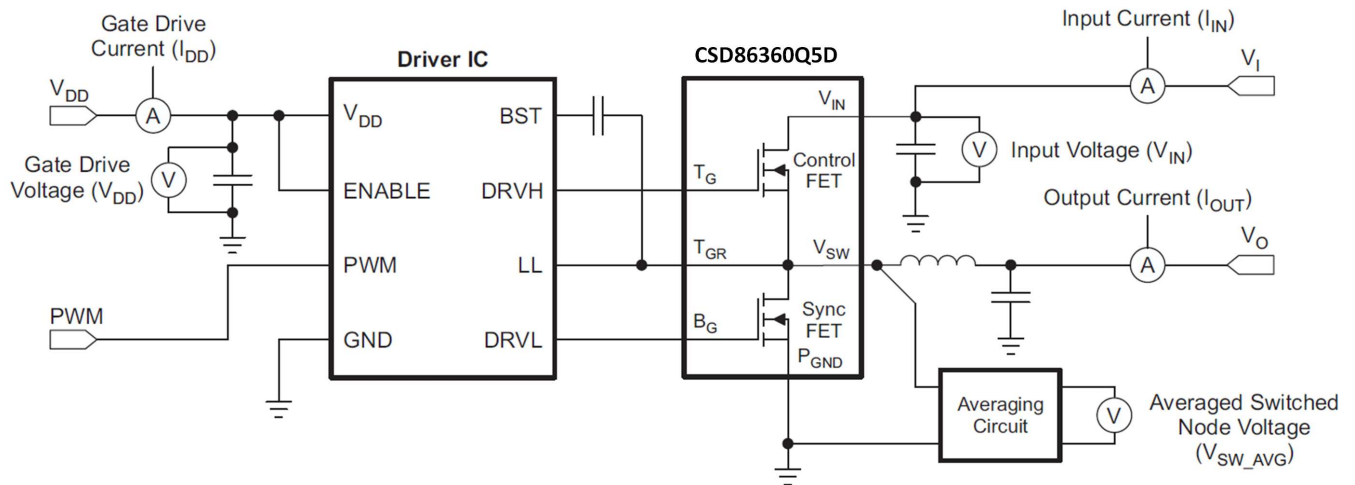
The normalized curves in the CSD86360Q5D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

## CSD86360Q5D

ZHCSAE5B – SEPTEMBER 2012 – REVISED APRIL 2018

[www.ti.com.cn](http://www.ti.com.cn)

### 6.2 Typical Application



**Figure 33. Typical Application**

## Typical Application (continued)

### 6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see [Operating Conditions](#) section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

#### 6.2.1.1 Operating Conditions

- Output current = 25 A
- Input voltage = 7 V
- Output voltage = 1 V
- Switching frequency = 800 kHz
- Inductor = 0.2  $\mu$ H

#### 6.2.1.2 Calculating Power Loss

- Power loss at 25 A = 3.5 W ([Figure 2](#))
- Normalized power loss for input voltage  $\approx 1.03$  ([Figure 8](#))
- Normalized power loss for output voltage  $\approx 0.90$  ([Figure 9](#))
- Normalized power loss for switching frequency  $\approx 1.15$  ([Figure 7](#))
- Normalized power loss for output inductor  $\approx 1.03$  ([Figure 10](#))
- **Final calculated power loss =  $3.5 \text{ W} \times 1.03 \times 0.90 \times 1.15 \times 1.03 \approx 3.84 \text{ W}$**

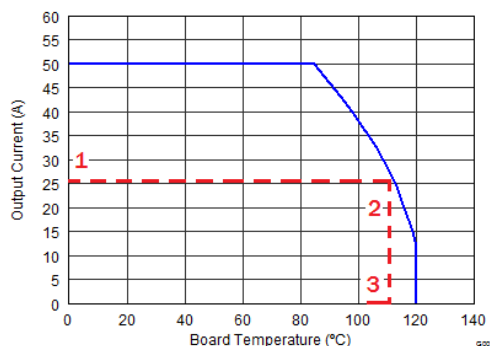
#### 6.2.1.3 Calculating SOA Adjustments

- SOA adjustment for input voltage  $\approx 1.3^\circ\text{C}$  ([Figure 8](#))
- SOA adjustment for output voltage  $\approx -2.5^\circ\text{C}$  ([Figure 9](#))
- SOA adjustment for switching frequency  $\approx 6.0^\circ\text{C}$  ([Figure 7](#))
- SOA adjustment for output inductor  $\approx 1.3^\circ\text{C}$  ([Figure 10](#))
- **Final calculated SOA adjustment =  $1.3 + (-2.5) + 6.0 + 1.3 \approx 6.1^\circ\text{C}$**

In the design example above, the estimated power loss of the CSD86360Q5D would increase to 3.84 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by  $6.1^\circ\text{C}$ . [Figure 34](#) graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of  $6.1^\circ\text{C}$ . In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.



**Figure 34. Power Block SOA**

## 7 Layout

### 7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

#### 7.1.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/μs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see [Figure 35](#)). The example in [Figure 35](#) uses 6 × 10-μF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T<sub>G</sub> and B<sub>G</sub> should connect to the outputs of the driver IC. The T<sub>GR</sub> pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Please refer to TI App Note [Snubber Circuits: Theory, Design and Application](#) (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the VSW node and PGND see [Figure 35](#) <sup>(1)</sup>

#### 7.1.2 Thermal Performance

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in [Figure 35](#) uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla



## 7.2 Layout Example

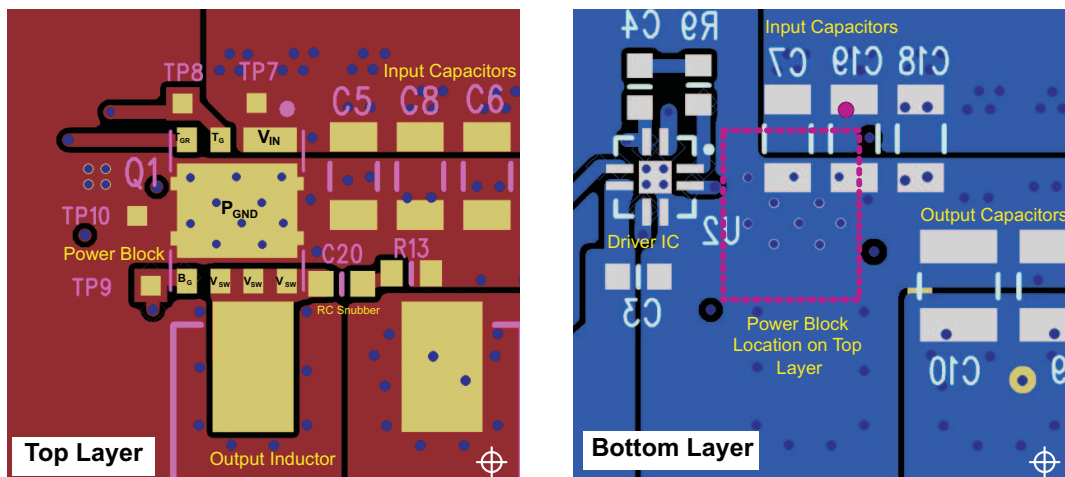


Figure 35. Recommended PCB Layout (Top Down View)

## 8 器件和文档支持

### 8.1 文档支持

#### 8.1.1 相关文档

请参阅如下相关文档：

- [针对同步降压转换器的功率损耗计算（包含共源电感注意事项）\(SLPA009\)](#)
- [阻尼器电路：理论、设计和应用 \(SLUP100\)](#)

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** **TI 的工程师对工程师 (E2E) 社区。**此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 8.4 商标

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 8.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 8.6 术语表

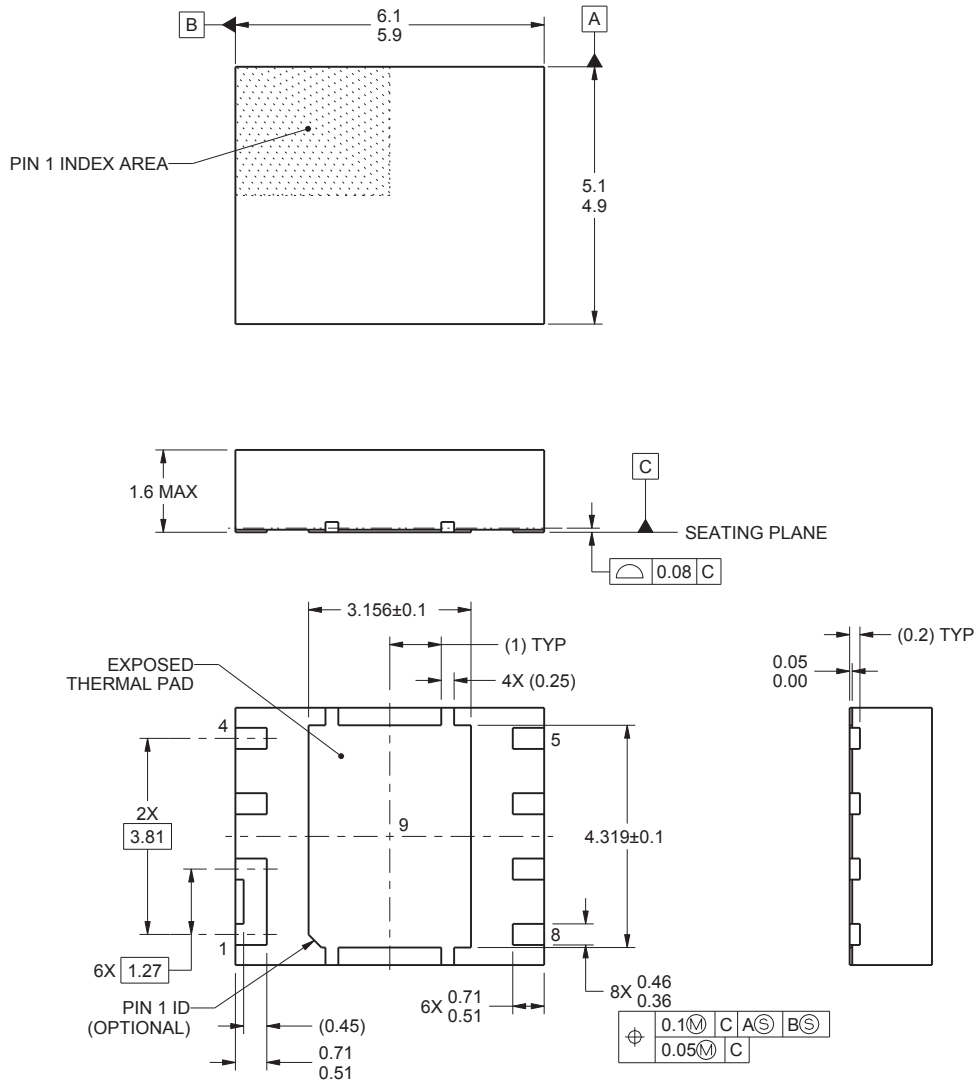
**SLYZ022** — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

### 9.1 Q5D 封装尺寸



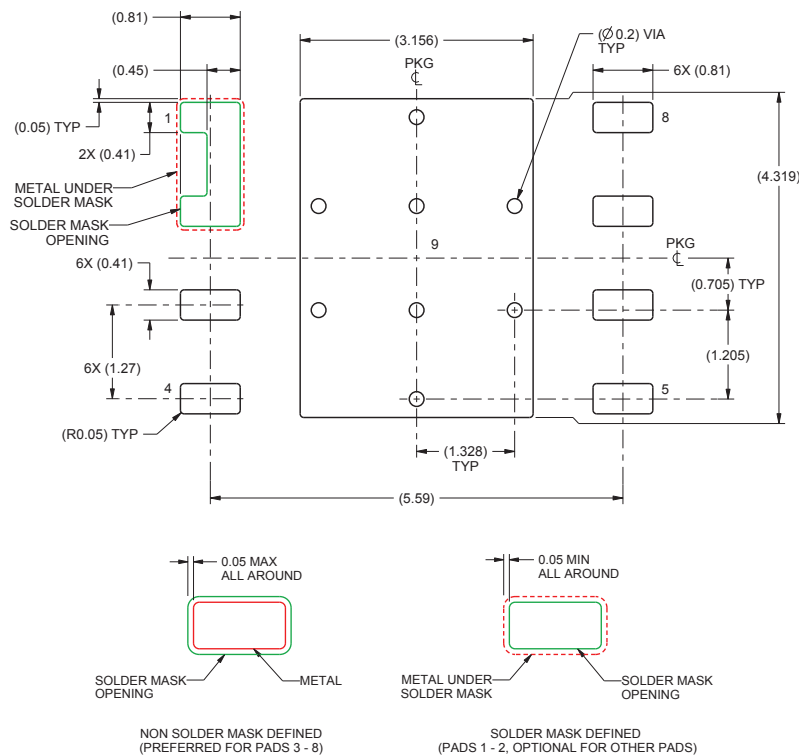
4222206/A 01/2016

1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 必须在印刷电路板上焊接封装散热焊盘，以获得良好的散热和机械性能。

## Q5D 封装尺寸 (接下页)

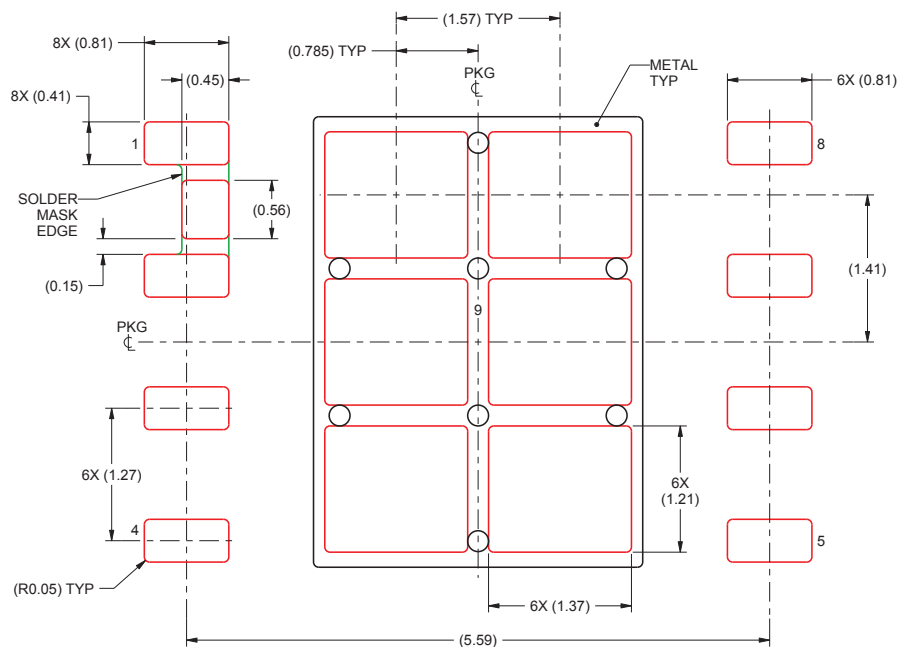
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 典型值		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

## 9.2 焊盘布局建议



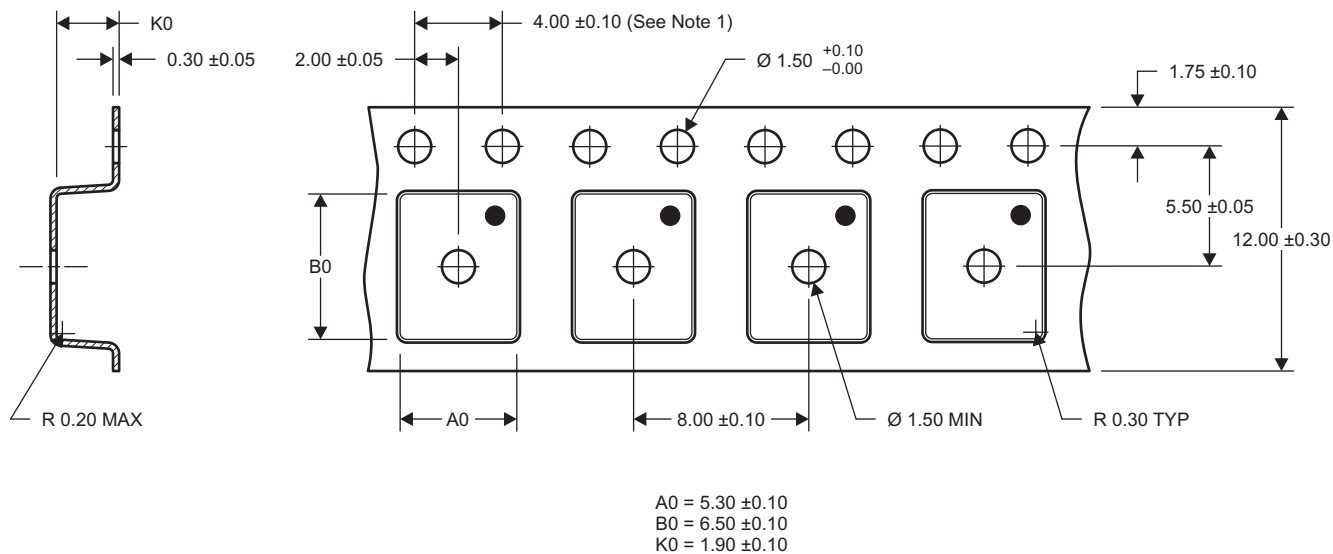
1. 此封装设计用于焊接到电路板的散热焊盘上。有关更多信息，请参阅《[QFN/SON PCB 连接](#)》(SLUA271)。
2. 根据应用决定是否选用过孔，详情请参见器件数据表。如果实现了部分或全部过孔，则会显示建议的过孔位置。

### 9.3 模版建议



1. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。要获得与 PCB 设计相关的建议电路布局，请参阅《通过 PCB 布局技巧来减少振铃》(SLPA005)。

### 9.4 Q5D 卷带信息



NOTES: 1. 10 链轮孔距累积容差为 ±0.2

2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸单位为 mm，除非另外注明。
5. 厚度：0.3 ± 0.05mm。
6. 符合 MSL1 260°C（红外和对流）PbF 回流焊要求。

M0191-01

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD86360Q5D</a>	Active	Production	LSON-CLIP (DQY)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	86360D
CSD86360Q5D.B	Active	Production	LSON-CLIP (DQY)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	86360D
CSD86360Q5DG4	Active	Production	LSON-CLIP (DQY)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	86360D
CSD86360Q5DG4.B	Active	Production	LSON-CLIP (DQY)   8	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	86360D

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD86360Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD86360Q5DG4	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

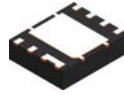


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD86360Q5D	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0
CSD86360Q5DG4	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0



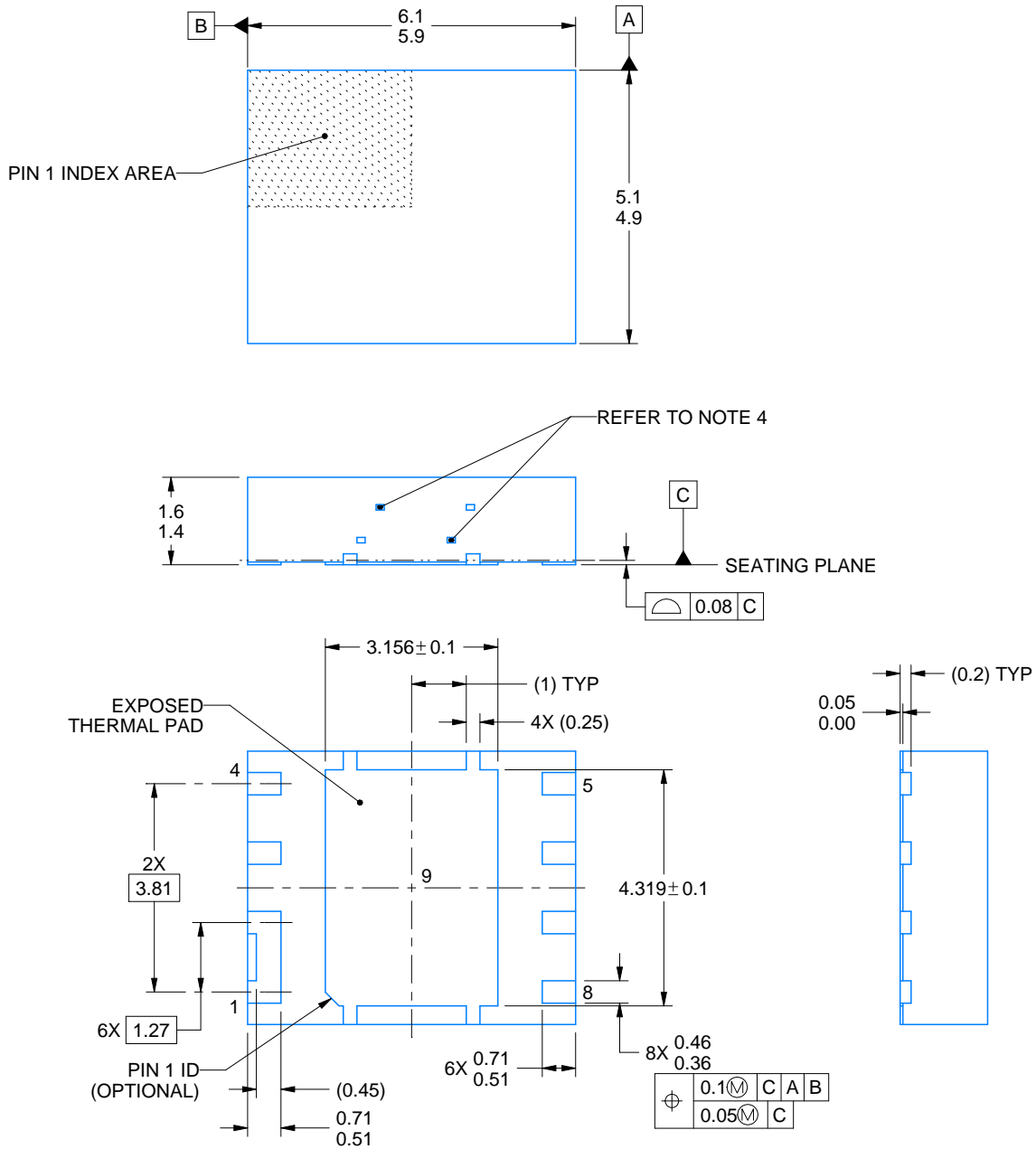
DQY0008A



# PACKAGE OUTLINE

## LSON-CLIP - 1.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218872/B 11/2024

### NOTES:

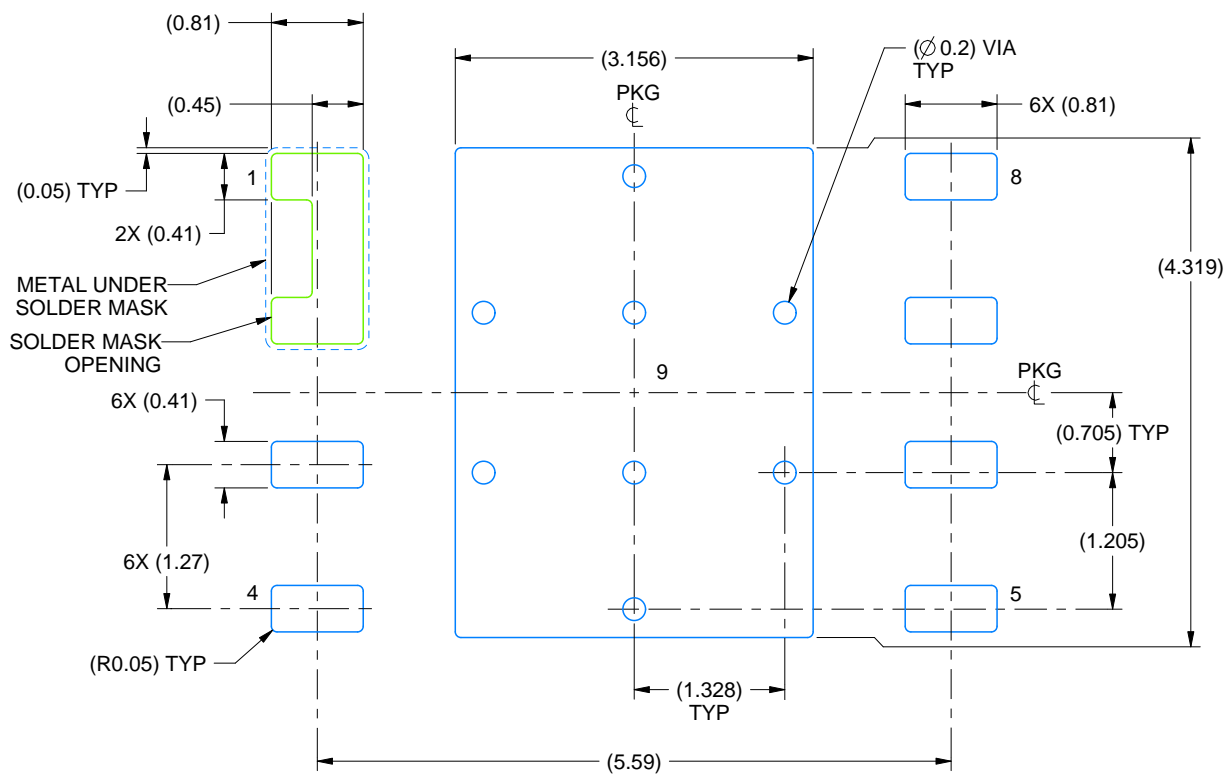
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed metals on side wall may vary or not visible

# EXAMPLE BOARD LAYOUT

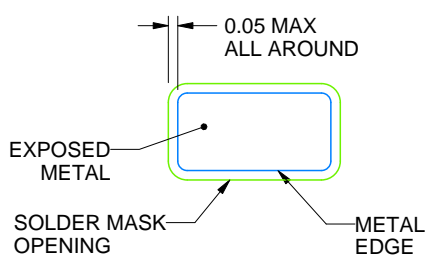
DQY0008A

LSON-CLIP - 1.6 mm max height

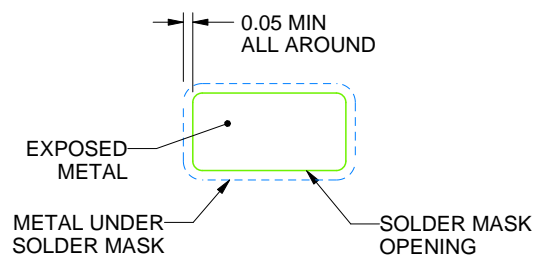
PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK DEFINED  
(PREFERRED FOR PADS 3 - 8)



SOLDER MASK DEFINED  
(PADS 1 - 2, OPTIONAL FOR OTHER PADS)

## SOLDER MASK DETAILS

4218872/B 11/2024

NOTES: (continued)

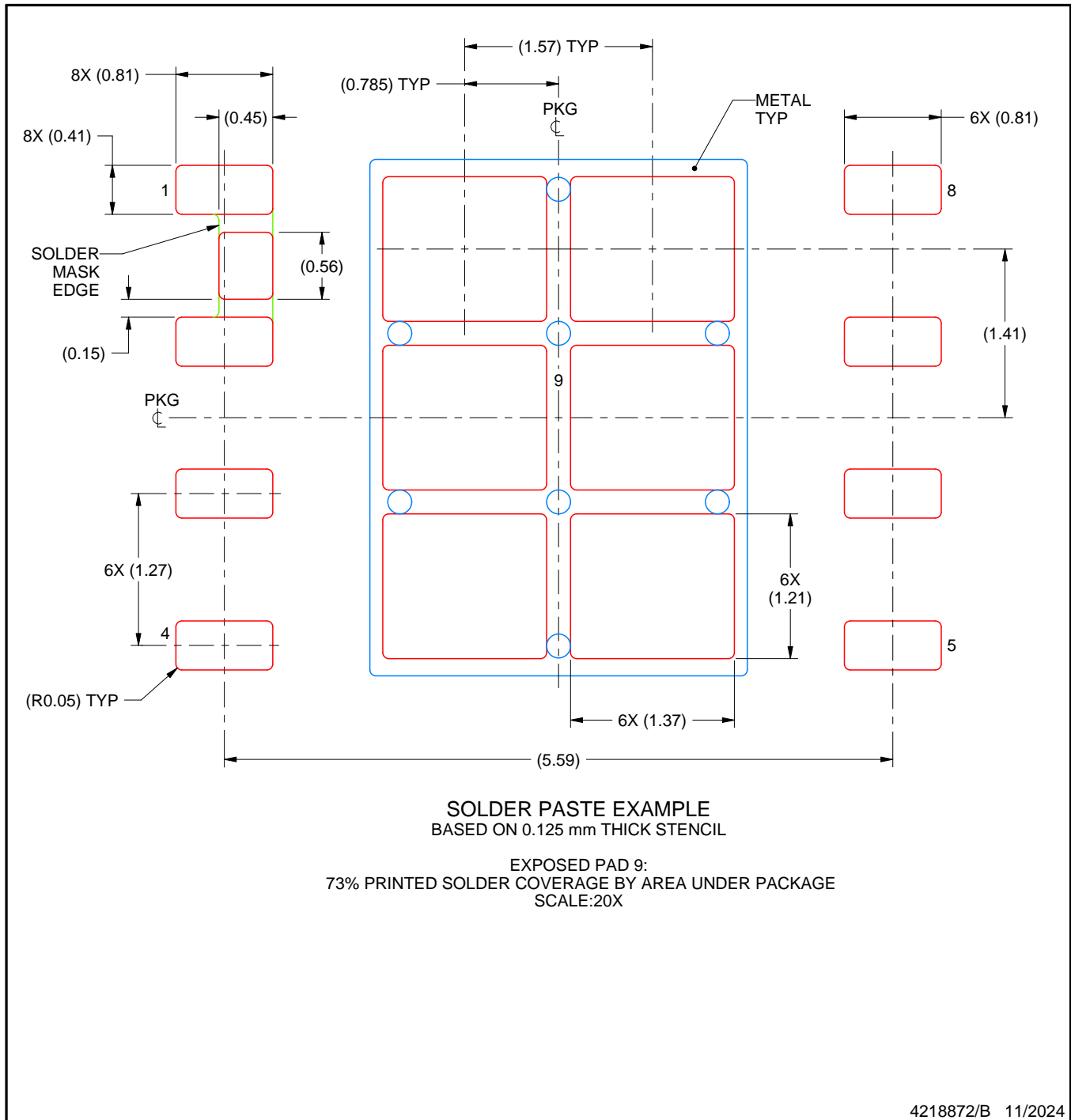
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DQY0008A

LSON-CLIP - 1.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月