

CSD25310Q2 20V P 沟道 NexFET™ 功率 MOSFET

1 特性

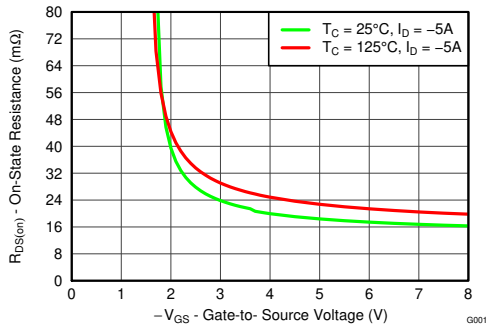
- 超低 Q_g 和 Q_{gd}
- 低导通电阻
- 低热阻
- 无铅
- 符合 RoHS
- 无卤素
- SON 2mm × 2mm 塑料封装

2 应用

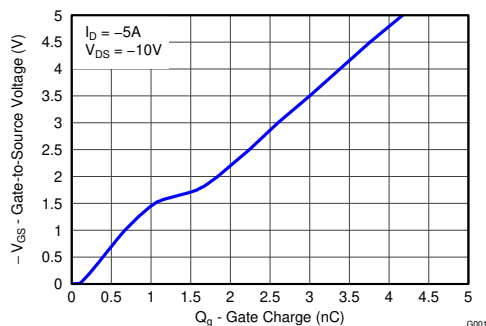
- 电池管理
- 负载管理
- 电池保护

3 说明

这款 19.9mΩ、-20V P 沟道器件旨在以超薄且具有出色散热特性的极小封装提供更高的导通电阻和栅极电荷。该器件将低导通电阻与 SON 2mm × 2mm 塑料封装的极小封装尺寸融为一体，堪称电池供电型空间受限应用的理想之选。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

产品概要

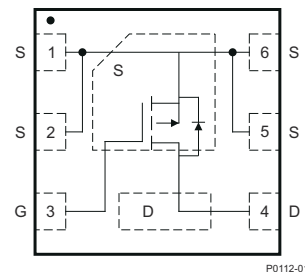
$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	-20	V
Q_g	栅极电荷总量 (-4.5V)	3.6	nC
Q_{gd}	栅漏栅极电荷	0.5	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = -1.8\text{V}$	59.0 mΩ
		$V_{GS} = -2.5\text{V}$	27.0 mΩ
		$V_{GS} = -4.5\text{V}$	19.9 mΩ
$V_{GS(th)}$	阈值电压	-0.85	V

订购信息

器件	介质	数量	封装	运输
CSD25310Q2	7 英寸卷带	3000	SON 2mm x 2mm 塑料封装	卷带包装
CSD25310Q2T	7 英寸卷带	250		

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	±8	V
I_D	持续漏极电流 (受封装限制)	-20	A
	持续漏极电流(1)	-9.6	A
I_{DM}	脉冲漏极电流(2)	48	A
P_D	功率耗散	2.9	W
	1. $R_{\theta JA} = 43^\circ\text{C/W}$, 这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 平方英寸 (2 盎司) 覆铜上测得的典型值。		
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C



顶视图



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4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$, unless otherwise specified

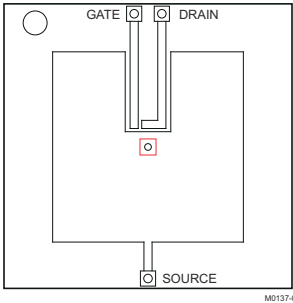
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0V, I _D = - 250 μ A	- 20			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0V, V _{DS} = - 16V	- 1			μ A
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0V, V _{GS} = - 8V	- 100			nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = - 250 μ A	- 0.55	- 0.85	- 1.10	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = - 1.8V, I _{DS} = - 5A	59.0		89.0	mΩ
		V _{GS} = - 2.5V, I _{DS} = - 5A	27.0		32.5	mΩ
		V _{GS} = - 4.5V, I _{DS} = - 5A	19.9		23.9	mΩ
g _{fs}	Transconductance	V _{DS} = - 16V, I _{DS} = - 5A	34			S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = - 10V, f = 1MHz	504		655	pF
C _{OSS}	Output Capacitance		281		365	pF
C _{RSS}	Reverse Transfer Capacitance		16.7		21.7	pF
R _g	Series Gate Resistance		1.9			Ω
Q _g	Gate Charge Total (- 4.5 V)	V _{DS} = - 10V, I _{DS} = - 5A	3.6		4.7	nC
Q _{gd}	Gate Charge Gate to Drain		0.5			nC
Q _{gs}	Gate Charge Gate to Source		1.1			nC
Q _{g(th)}	Gate Charge at V _{th}		0.6			nC
Q _{OSS}	Output Charge	V _{DS} = - 10V, V _{GS} = 0V	5.0			nC
t _{d(on)}	Turn On Delay Time	V _{DS} = - 10V, V _{GS} = - 4.5V, I _{DS} = - 5A R _G = 2Ω	8			ns
t _r	Rise Time		15			ns
t _{d(off)}	Turn Off Delay Time		15			ns
t _f	Fall Time		5			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{DS} = - 5A, V _{GS} = 0V	- 0.8		- 1.0	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = - 10V, I _F = - 5A, di/dt = 200A/ μ s	9.2			nC
t _{rr}	Reverse Recovery Time		13			ns

4.2 Thermal Information

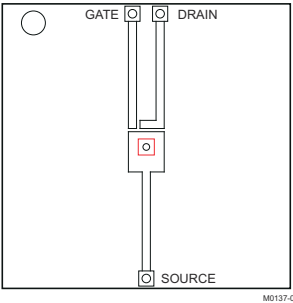
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			4.5	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ^{(1) (2)}			55	

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45cm²), 2oz. (0.071mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81cm × 3.81cm), 0.06 inch (1.52mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user’ s board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45cm²), 2oz. (0.071mm thick) Cu.



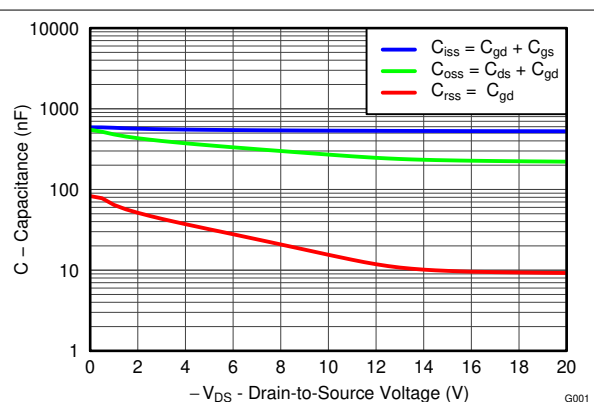
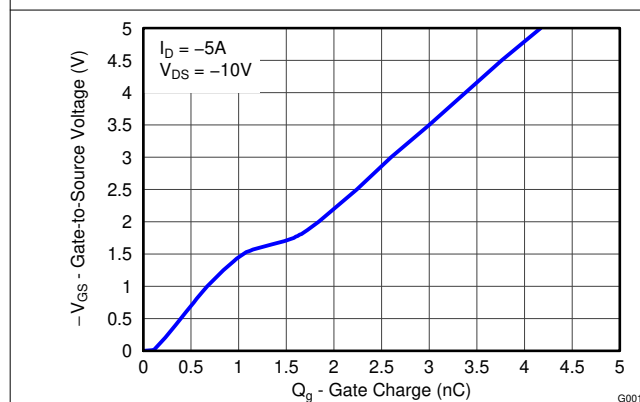
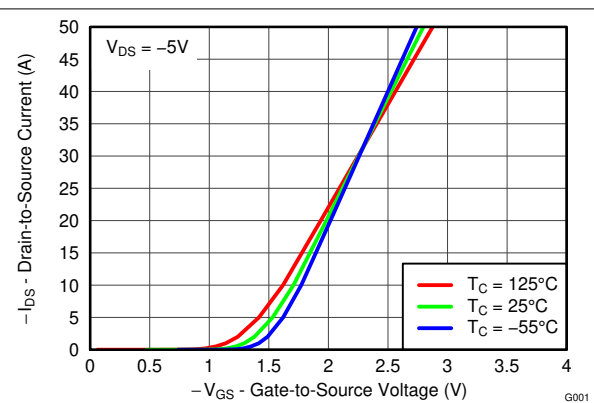
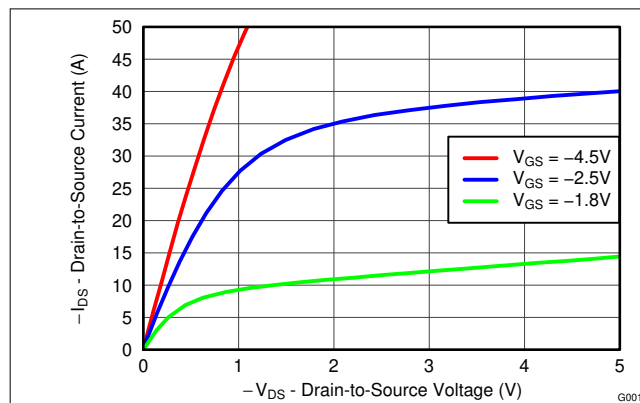
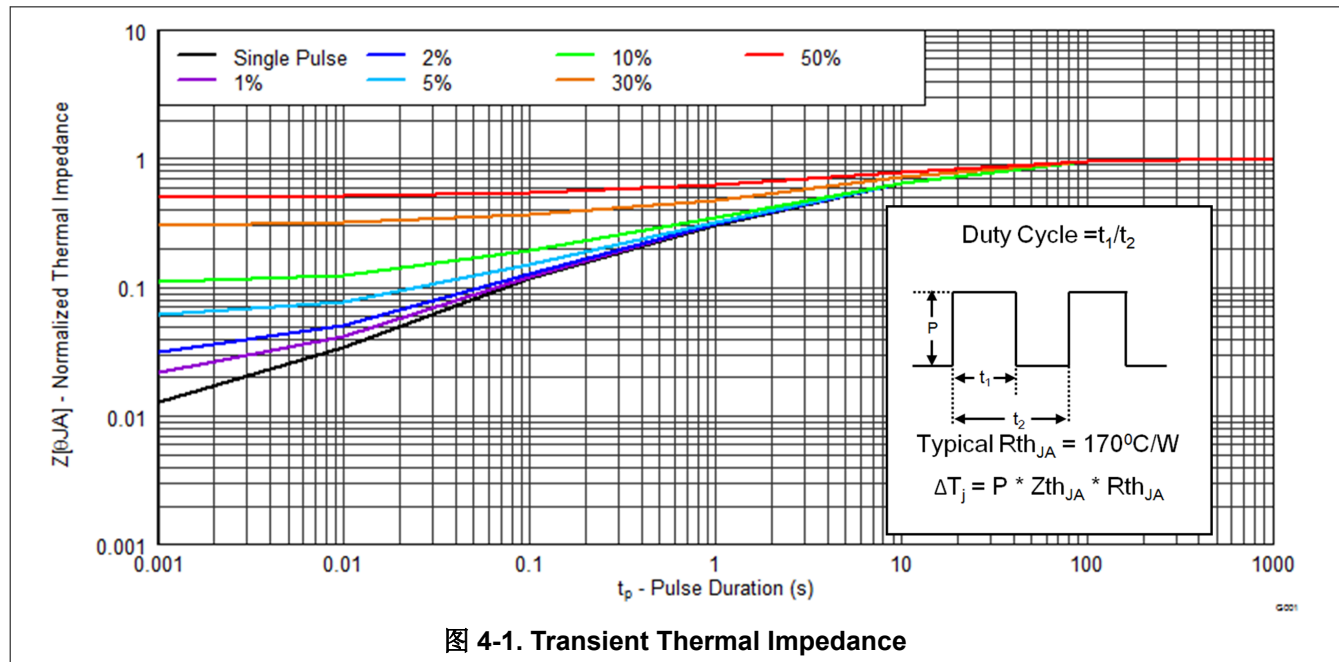
Max R_{θJA} = 55 when
mounted on 1 inch²
(6.45cm²) of 2oz. (0.071mm
thick) Cu.



Max R_{θJA} = 215 when
mounted on minimum pad
area of 2oz. (0.071mm thick)
Cu.

4.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



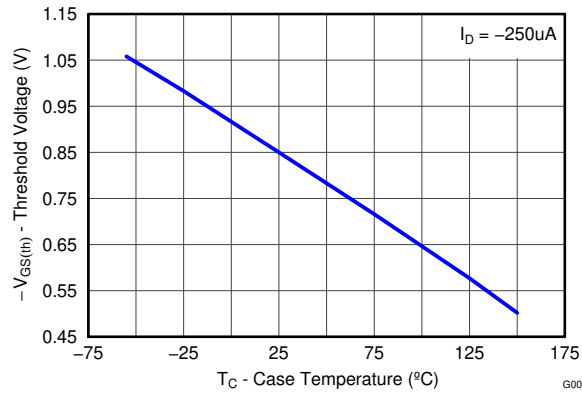


图 4-6. Threshold Voltage vs Temperature

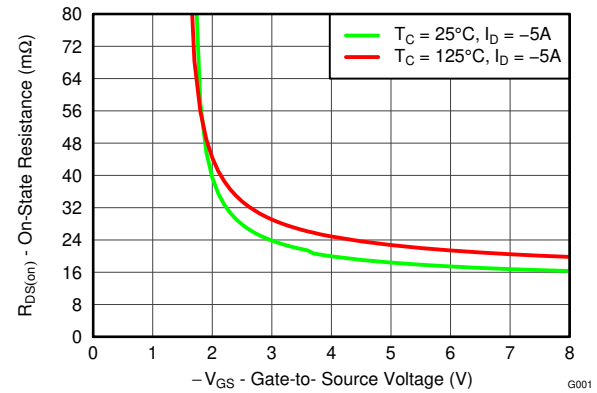


图 4-7. On-State Resistance vs Gate-to-Source Voltage

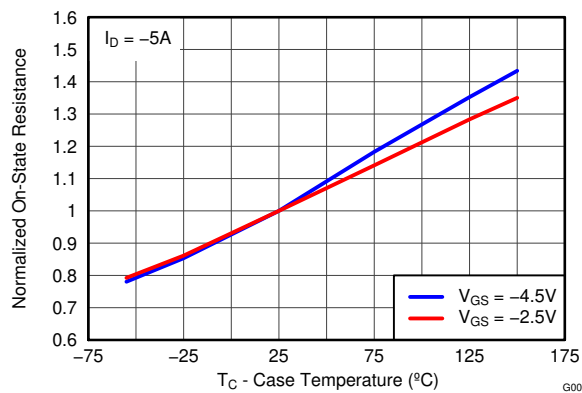


图 4-8. Normalized On-State Resistance vs Temperature

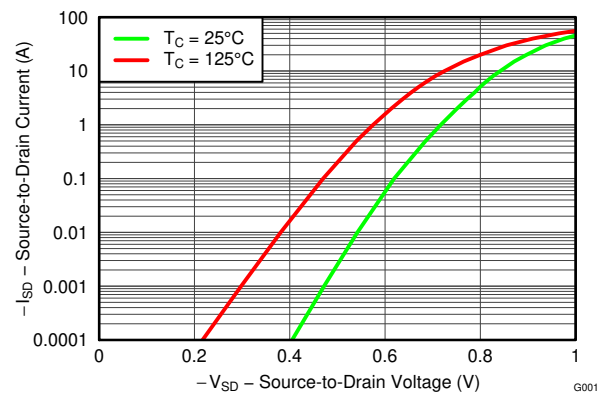


图 4-9. Typical Diode Forward Voltage

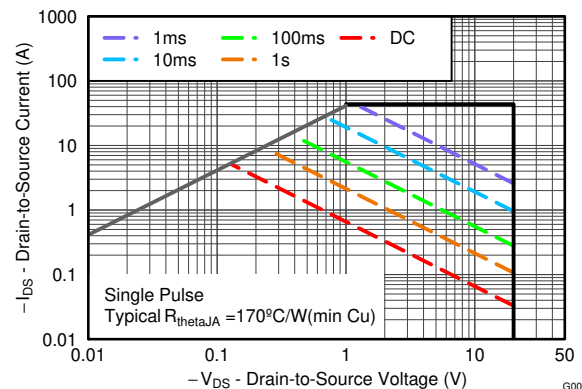


图 4-10. Maximum Safe Operating Area

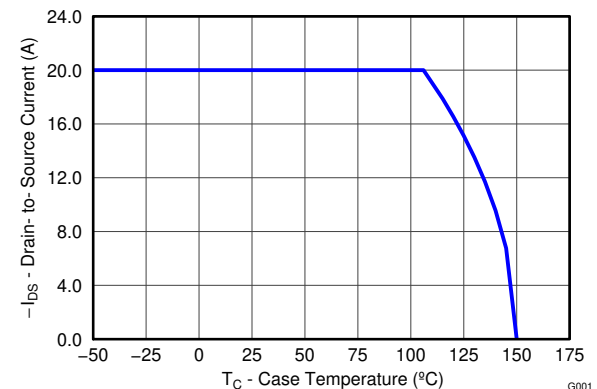


图 4-11. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 第三方产品免责声明

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5.2 Documentation Support

5.2.1 Related Documentation

5.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

5.5 Trademarks

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5.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

Changes from Revision B (March 2022) to Revision C (February 2025) Page

- 更新了整个文档中的表格、图和交叉参考的编号格式..... 1

Changes from Revision A (June 2014) to Revision B (March 2022) Page

- Updated drain and source connection images..... 4

Changes from Revision * (January 2014) to Revision A (June 2014) Page

- 已将“无铅端子镀层”修改为唯一状态“无铅” 1
- 在订购信息表中添加了小卷带选项..... 1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25310Q2	Active	Production	WSO (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530
CSD25310Q2.B	Active	Production	WSO (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530
CSD25310Q2G4.B	Active	Production	WSO (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530
CSD25310Q2T	Active	Production	WSO (DQK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530
CSD25310Q2T.B	Active	Production	WSO (DQK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

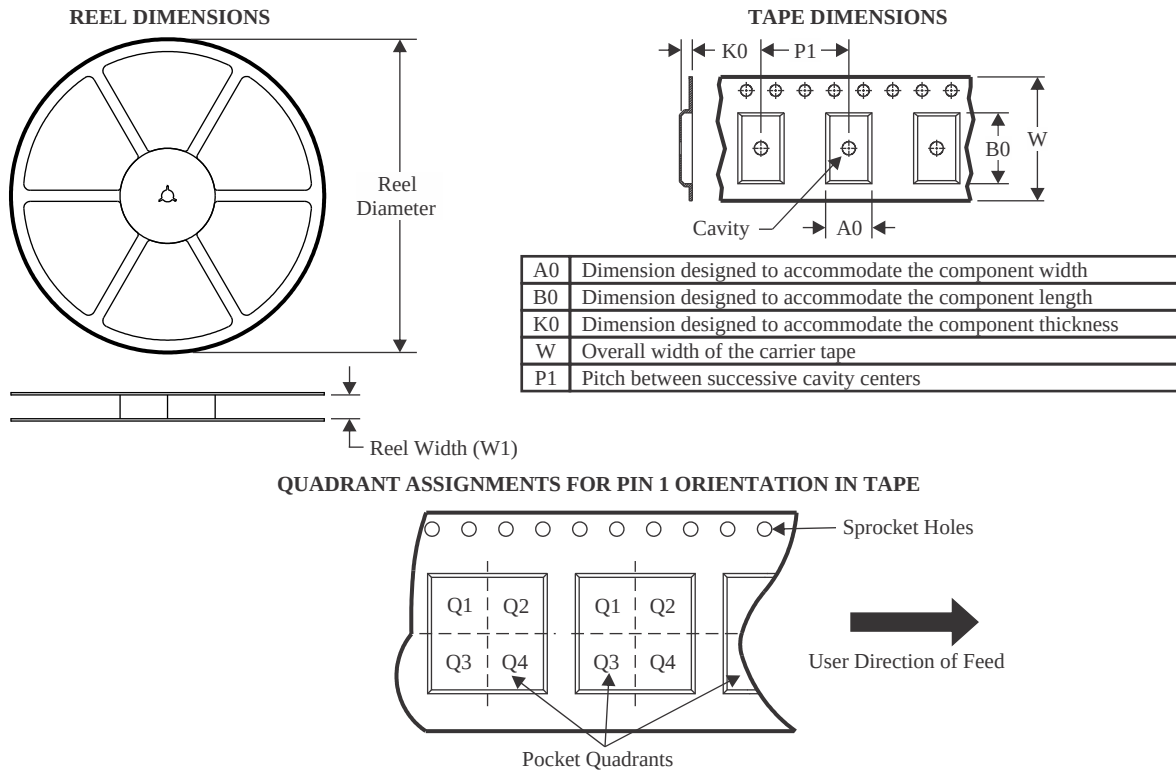
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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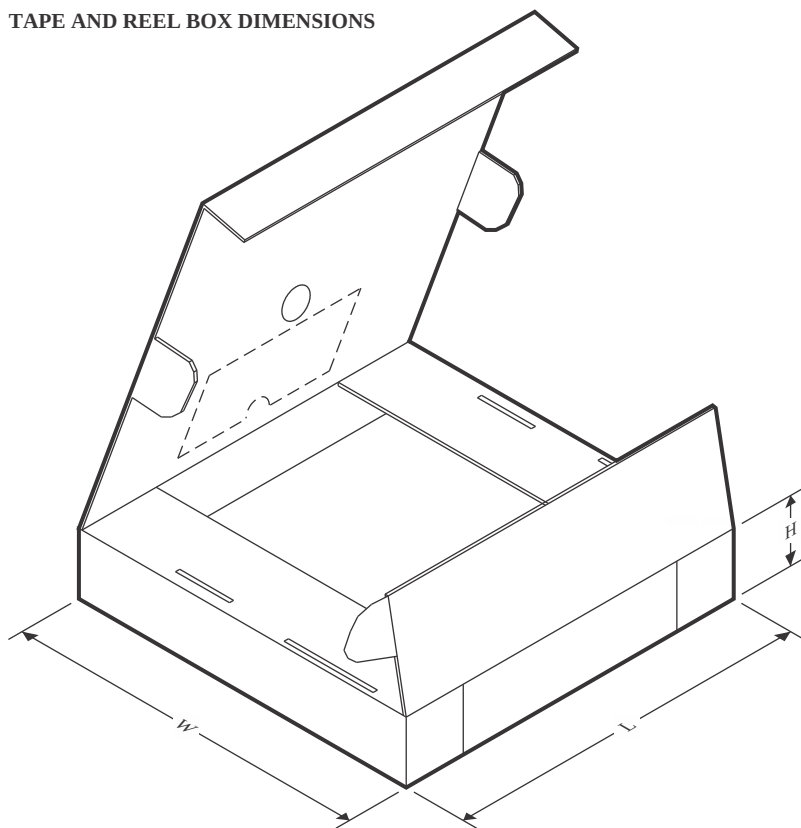
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25310Q2	WS0N	DQK	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD25310Q2T	WS0N	DQK	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25310Q2	WSO	DQK	6	3000	189.0	185.0	36.0
CSD25310Q2T	WSO	DQK	6	250	189.0	185.0	36.0

GENERIC PACKAGE VIEW

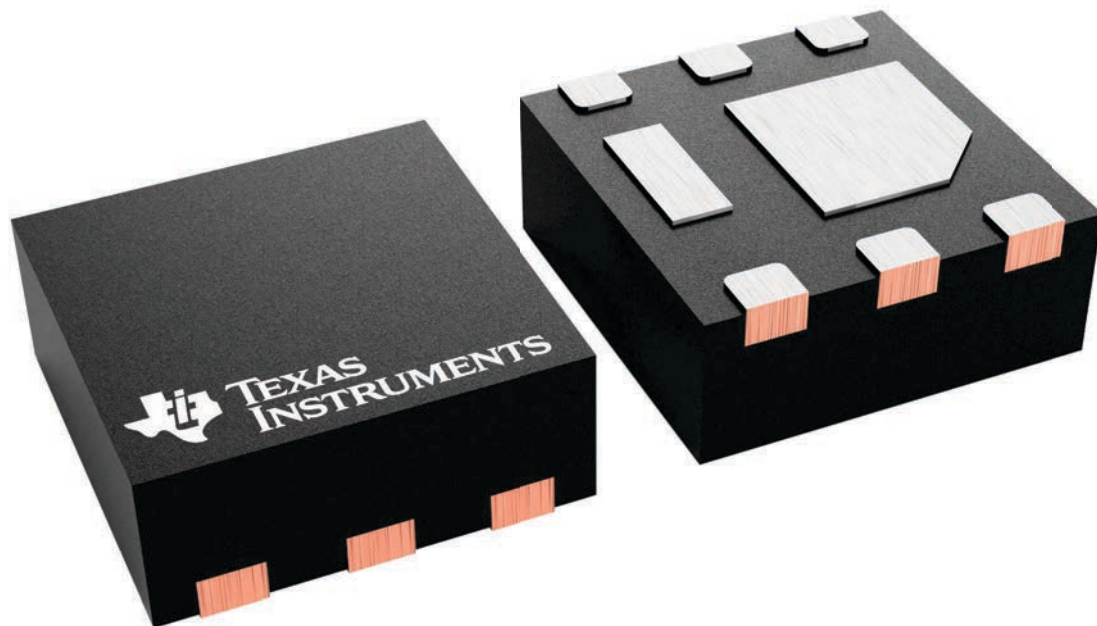
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

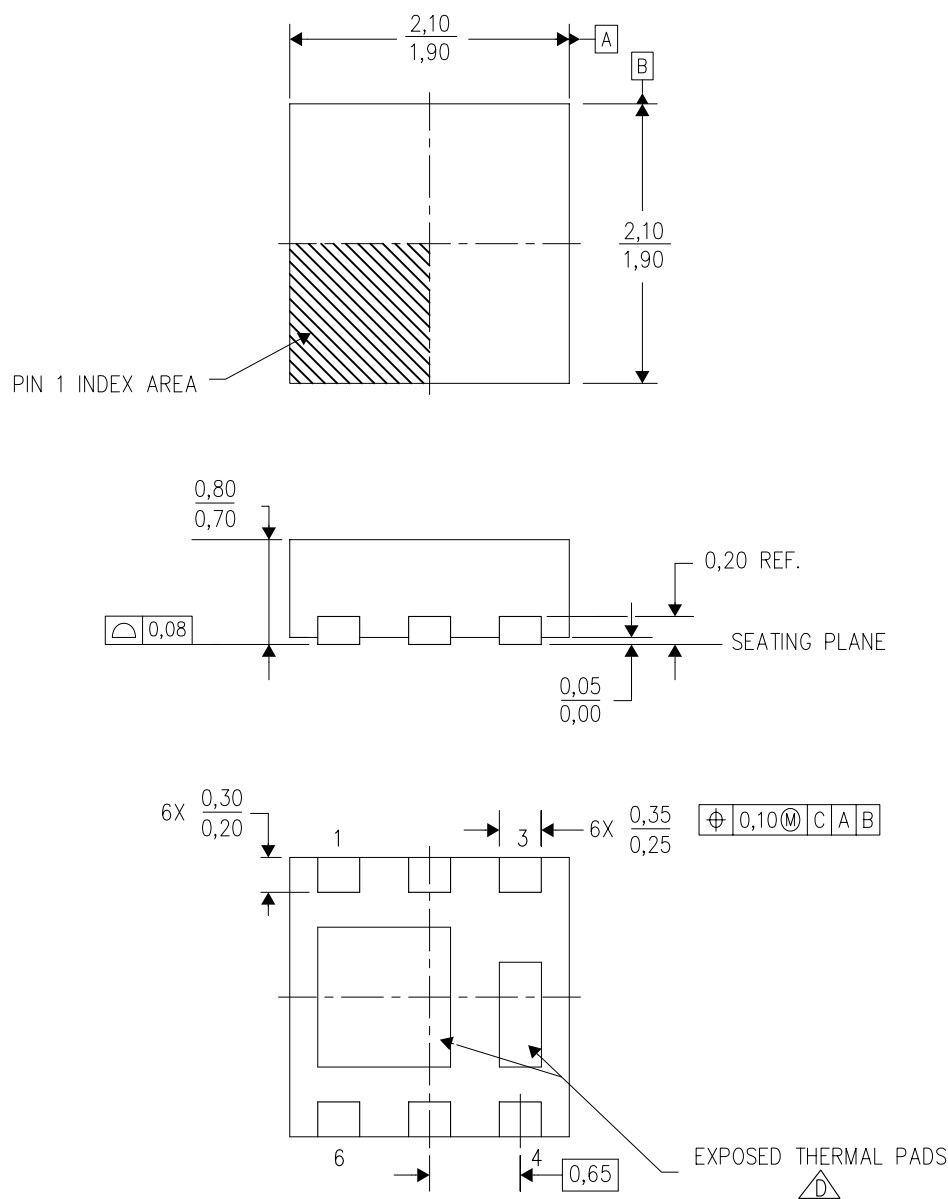
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229807/A

DQK (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4210192/B 01/10

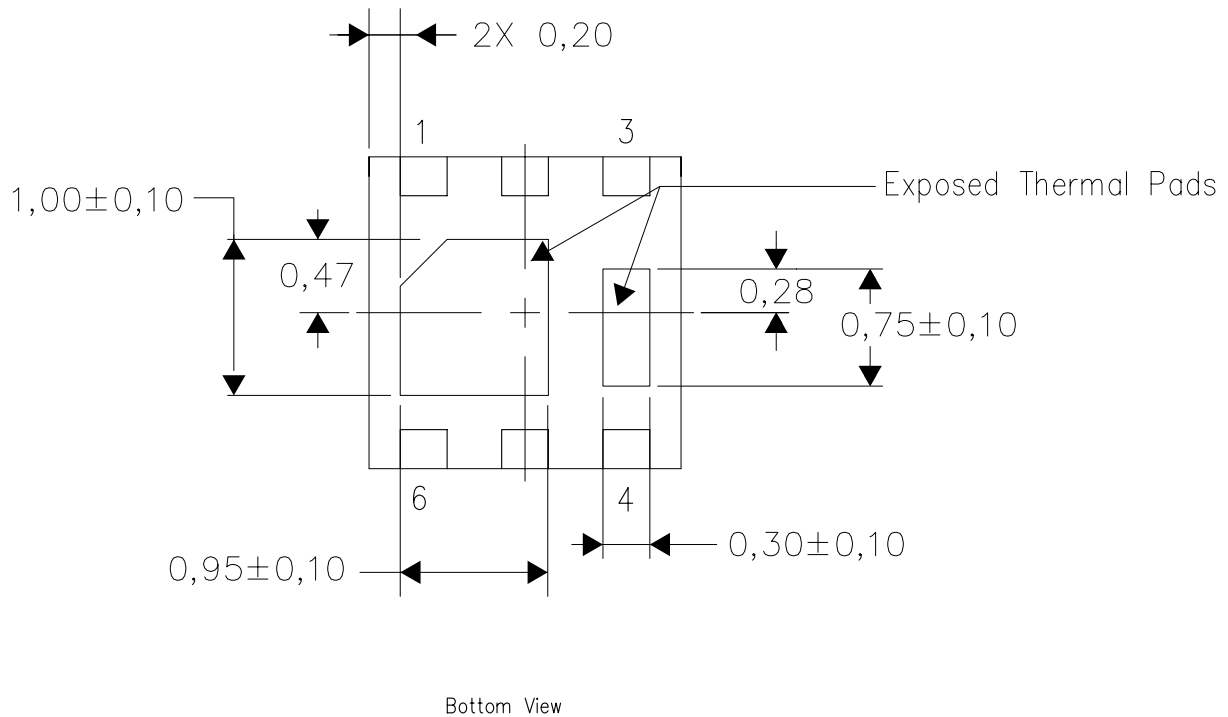
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

重要通知和免责声明

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