CSD23285F5 -12V P 沟道 FemtoFET™ MOSFET

1 特性

- 低导通电阻
- 低 Q_g 和 Q_{gd}
- 超小尺寸
  - 1.53mm x 0.77mm
  - 0.50mm 焊盘间距
- 薄型封装
  - 厚度为 0.36mm
- 集成型 ESD 保护二极管
  - 额定值 > 4kV 人体放电模式 (HBM)
  - 额定值 > 2kV 组件充电模式 (CDM)
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对工业负载开关应用进行了优化
- 针对通用开关应用进行了优化

3 说明

该 29mΩ、-12V N 沟道 FemtoFET™ MOSFET 技术经过设计和优化，能够最大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。

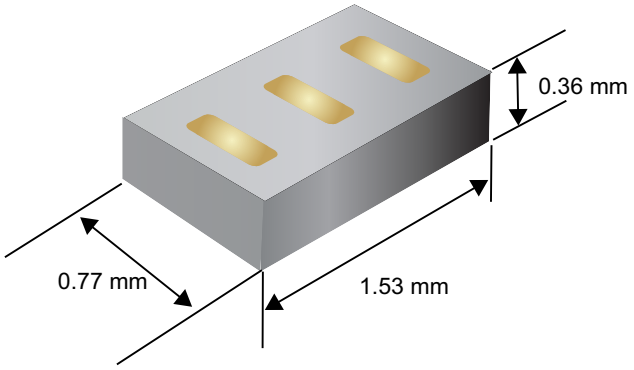


图 3-1. 典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-12		V
Q_g	栅极电荷总量 (-4.5V)	3.2		nC
Q_{gd}	栅极电荷 (栅极到漏极)	0.48		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.5V	64	mΩ
		V_{GS} = -1.8V	49	
		V_{GS} = -2.5V	38	
		V_{GS} = -4.5V	29	
$V_{GS(th)}$	阈值电压	-0.65		V

器件信息(1)

器件	数量	介质	封装	配送
CSD23285F5	3000	7 英寸卷带	Femto 1.53mm × 0.77mm 无引线 SMD	卷带式
CSD23285F5T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-12	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	-3.3	A
	持续漏极电流(2)	-5.4	
I_{DM}	脉冲漏极电流(1) (3)	-31	A
P_D	功率耗散(1)	0.5	W
	功率耗散(2)	1.4	
$V_{(ESD)}$	人体放电模型 (HBM)	4000	V
	充电器件模型 (CDM)	2000	
T_J、T_{stg}	工作结温、贮存温度	-55 至 150	°C

(1) $R_{\theta JA}$ = 245°C/W (覆铜面积最小时的典型值) 。
(2) $R_{\theta JA}$ = 90°C/W (覆铜面积最大时的典型值) 。
(3) 脉冲持续时间 ≤ 100 µs，占空比 ≤ 1%。

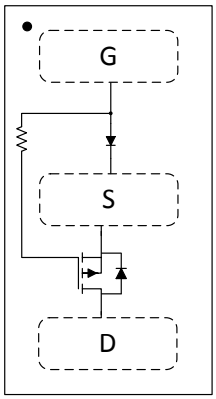


图 3-2. 顶视图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision A (July 2017) to Revision B (February 2022)	Page
• 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm	1
• 将超薄型封装图片中的厚度从 0.35mm 更新为 0.36mm	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm	8
• Added FemtoFET Surface Mount Guide note	9

Changes from Revision * (August 2016) to Revision A (July 2017)	Page
• Added 表 7-1 to the *节 7.1* section	8

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –9.6 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –5 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.40	–0.65	–0.95	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_{DS} = –1 A		64	130	mΩ
		V_{GS} = –1.8 V, I_{DS} = –1 A		49	80	
		V_{GS} = –2.5 V, I_{DS} = –1 A		38	47	
		V_{GS} = –4.5 V, I_{DS} = –1 A		29	35	
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_{DS} = –1 A		8.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –6 V, f = 1 MHz		483	628	pF
C_{oss}	Output capacitance			305	397	pF
C_{rss}	Reverse transfer capacitance			37	48	pF
R_G	Series gate resistance			17		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –6 V, I_{DS} = –1 A		3.2	4.2	nC
Q_{gd}	Gate charge gate-to-drain			0.48		nC
Q_{gs}	Gate charge gate-to-source			0.66		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.40		nC
Q_{oss}	Output charge	V_{DS} = –6 V, V_{GS} = 0 V		4.8		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_{DS} = –1 A, R_G = 2 Ω		15		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			30		ns
t_f	Fall time			13		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –1 A, V_{GS} = 0 V		–0.73	–1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		245		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

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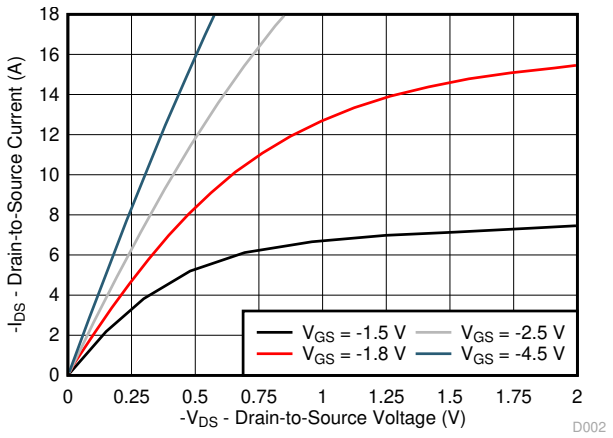
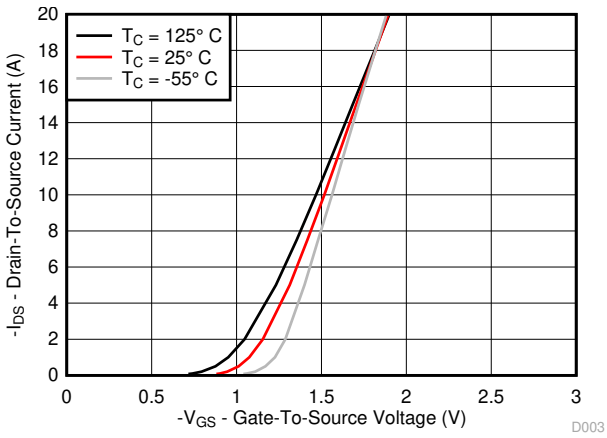


图 5-1. Saturation Characteristics



VDS = – 5 V

图 5-2. Transfer Characteristics

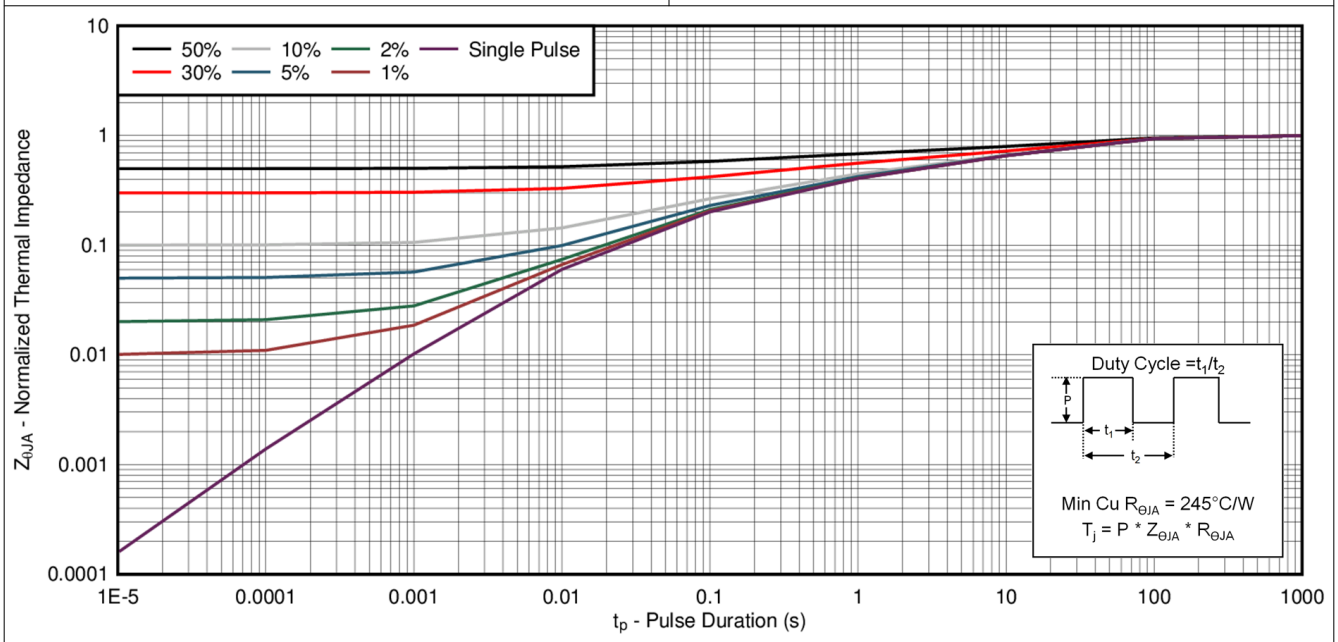
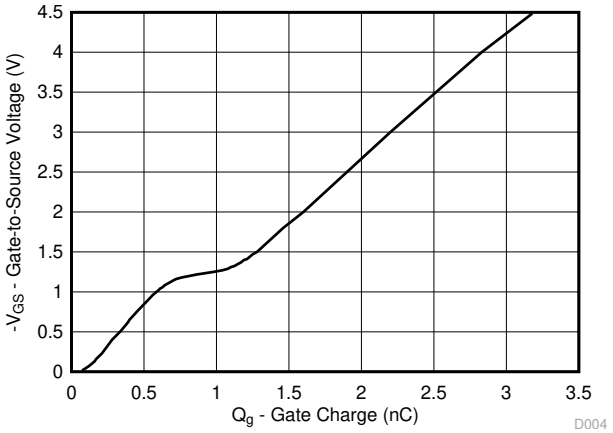


图 5-3. Transient Thermal Impedance

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I_D = –1 A V_{DS} = –6 V

图 5-4. Gate Charge

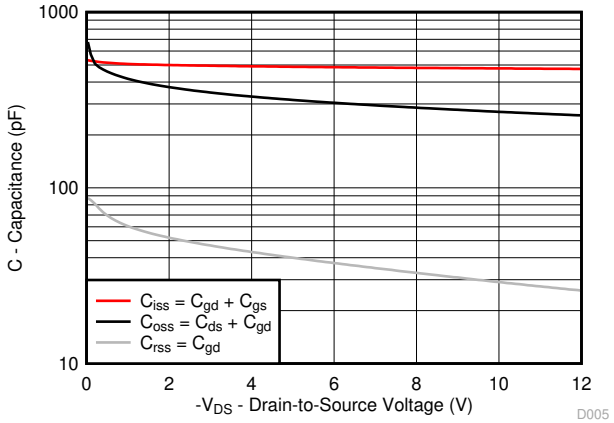
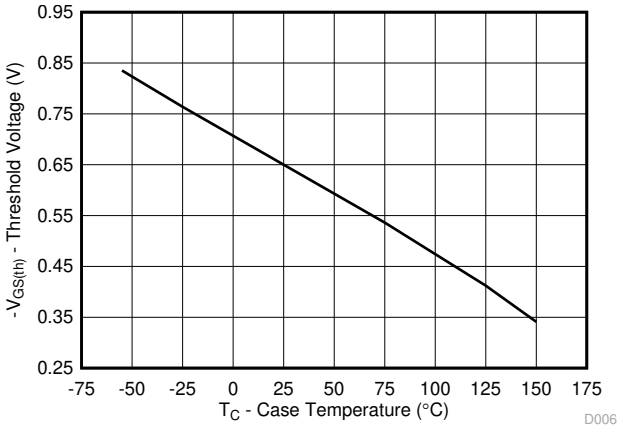


图 5-5. Capacitance



I_D = –250 µA

图 5-6. Threshold Voltage vs Temperature

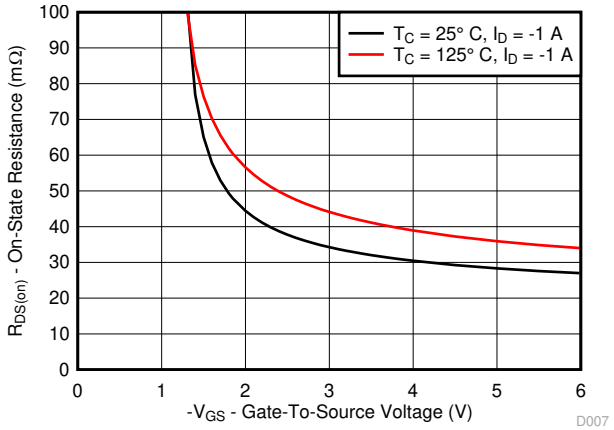
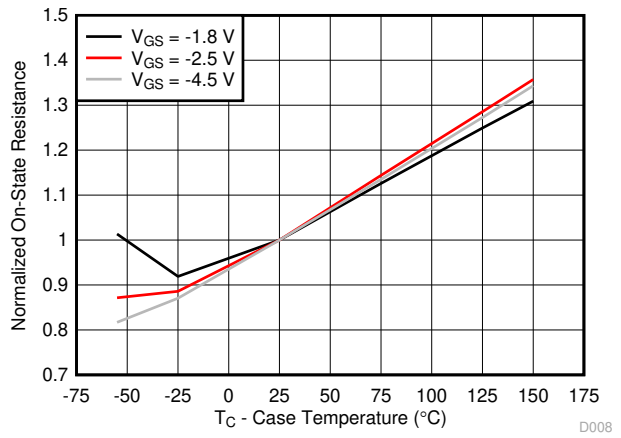


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –1 A

图 5-8. Normalized On-State Resistance vs Temperature

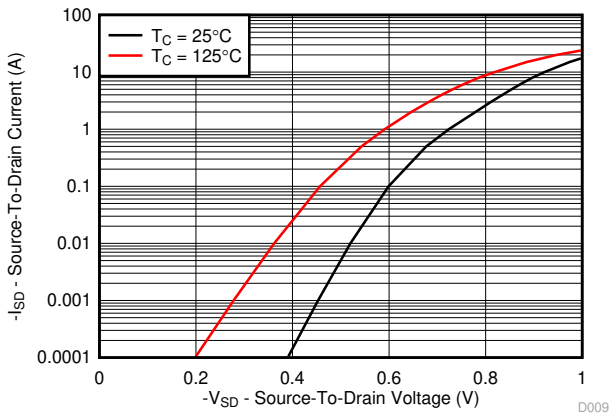
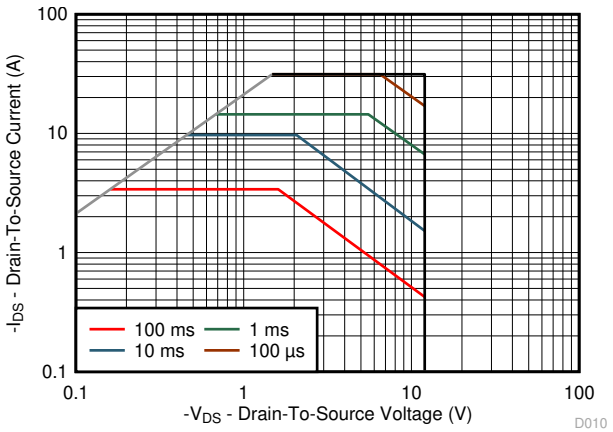


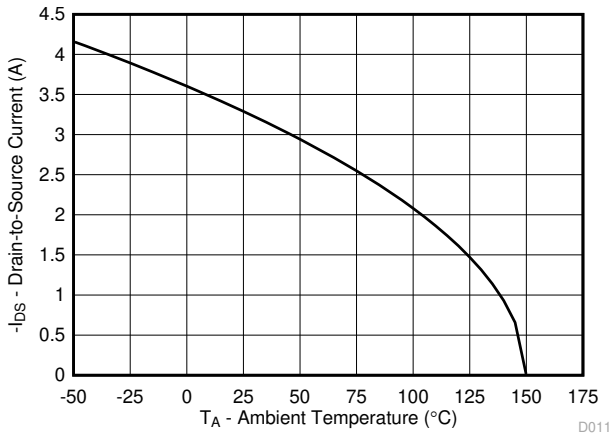
图 5-9. Typical Diode Forward Voltage

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Single pulse, typ $R_{\theta JA}$ = 245°C/W

图 5-10. Maximum Safe Operating Area (SOA)



Min Cu $R_{\theta JA}$ = 245°C/W

图 5-11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

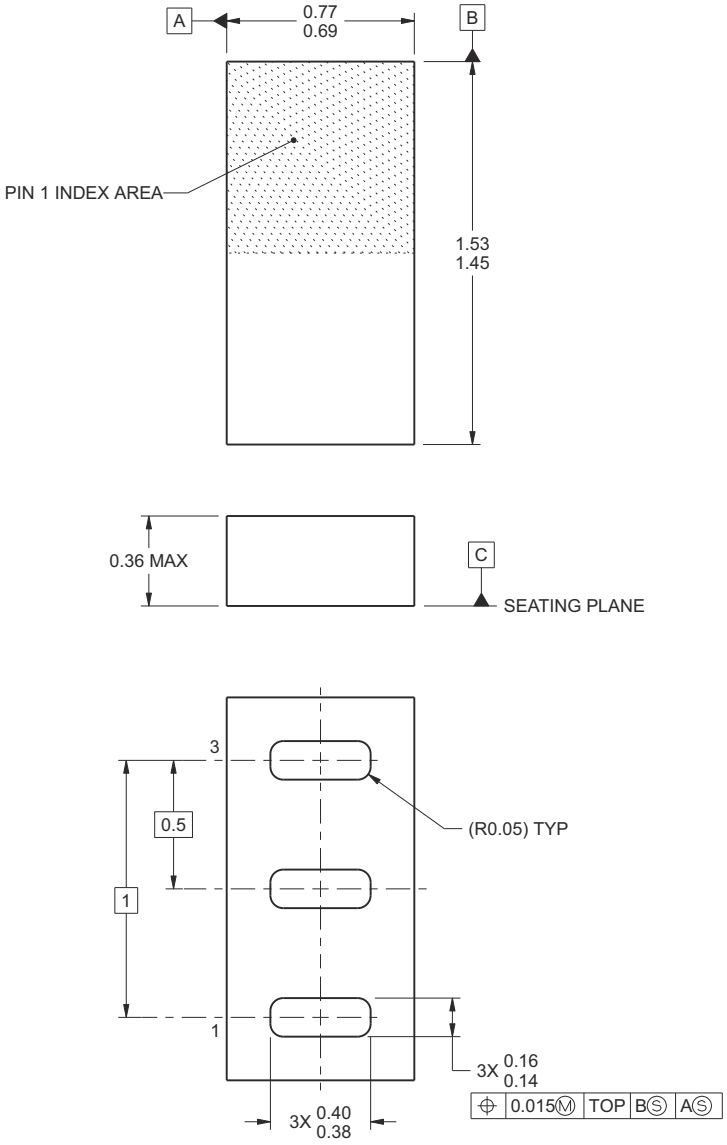
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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



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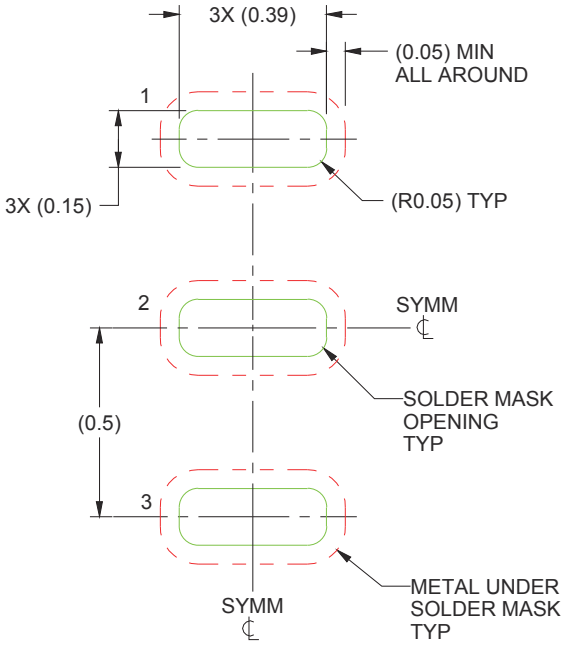
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

表 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

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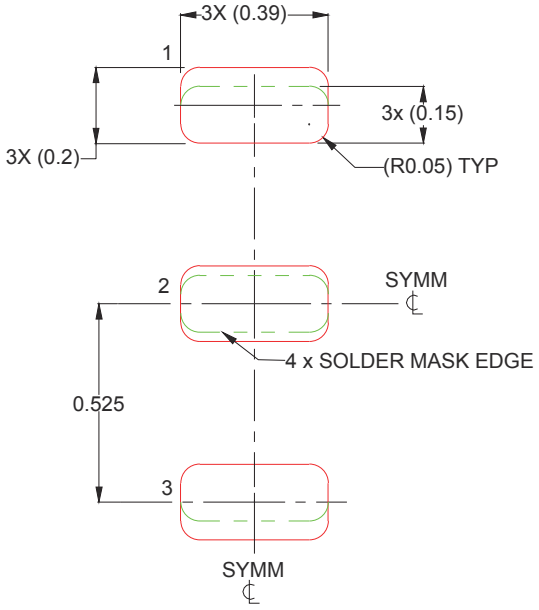
7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.

A. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23285F5	ACTIVE	PICOSTAR	YJK	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4S	Samples
CSD23285F5T	ACTIVE	PICOSTAR	YJK	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

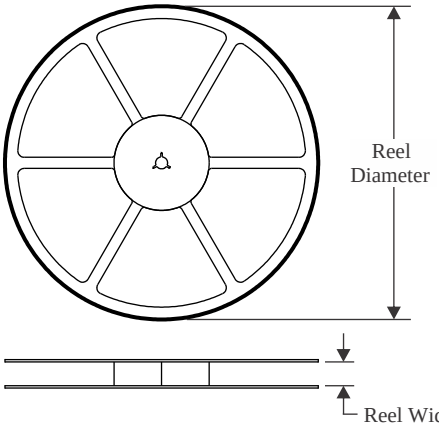
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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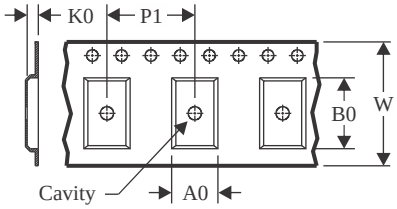
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

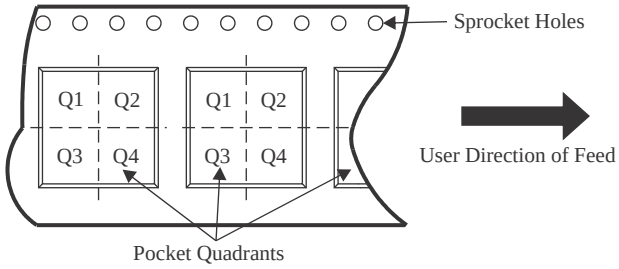


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

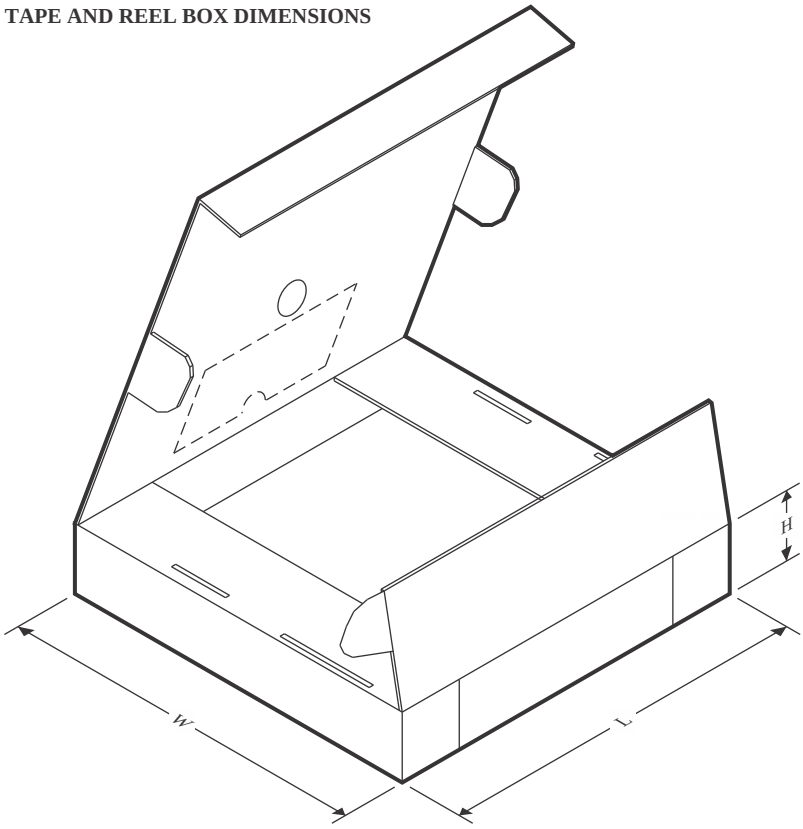
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

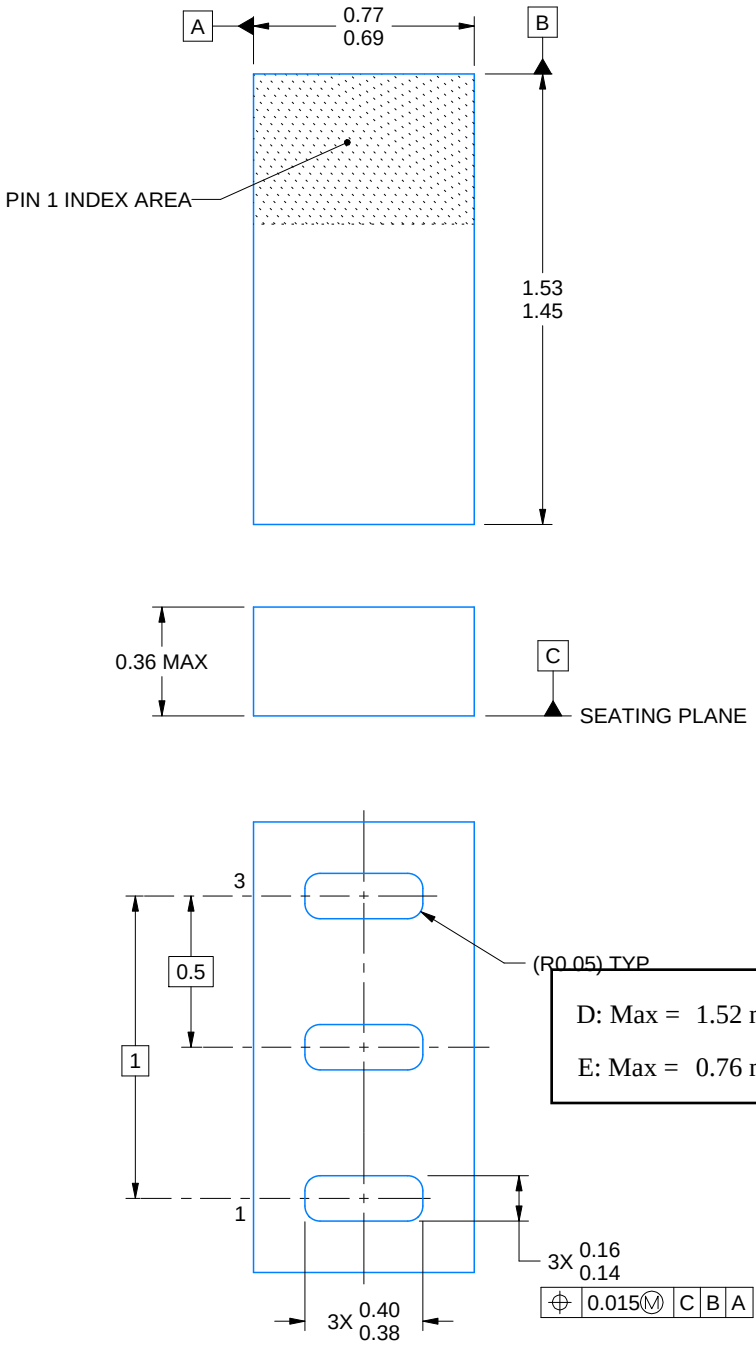
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23285F5	PICOSTAR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD23285F5T	PICOSTAR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD23285F5T	PICOSTAR	YJK	3	250	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23285F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD23285F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0
CSD23285F5T	PICOSTAR	YJK	3	250	220.0	220.0	35.0

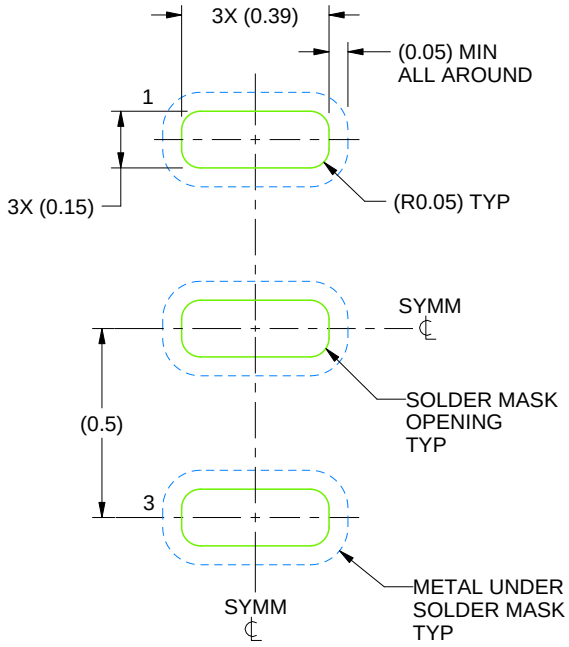


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PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

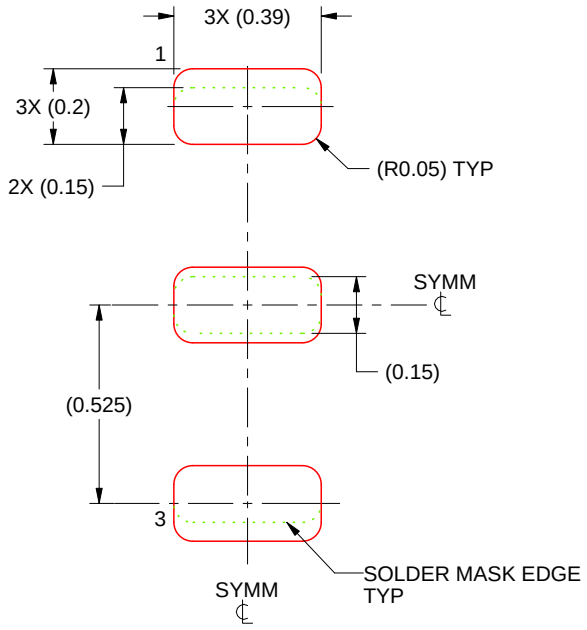


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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