

# CSD22205L -8V P 沟道 NexFET™ 功率 MOSFET

## 1 特性

- 低电阻
- 1.2mm × 1.2mm 小尺寸封装
- 0.36mm 厚，超薄型
- 无铅
- 栅源电压钳位
- 栅极 ESD 保护
- 符合 RoHS
- 无卤素

## 2 应用

- 电池管理
- 负载开关
- 电池保护

## 3 说明

这款 -8V、8.2mΩ、1.2mm × 1.2mm 基板栅格阵列 (LGA) NexFET™ 器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内提供更低的导通电阻和栅极电荷。基板栅格阵列 (LGA) 封装是一种带有金属接触板 (而非焊球) 的器件芯片级封装。

### 产品概要

| T <sub>A</sub> = 25°C |                | 值                       | 单位   |
|-----------------------|----------------|-------------------------|------|
| V <sub>DS</sub>       | 漏源电压           | -8                      | V    |
| Q <sub>g</sub>        | 栅极电荷总量 (-4.5V) | 6.5                     | nC   |
| Q <sub>gd</sub>       | 栅极电荷 (栅极到漏极)   | 1.0                     | nC   |
| R <sub>DS(on)</sub>   | 漏源导通电阻         | V <sub>GS</sub> = -1.5V | 30   |
|                       |                | V <sub>GS</sub> = -1.8V | 20   |
|                       |                | V <sub>GS</sub> = -2.5V | 11.5 |
|                       |                | V <sub>GS</sub> = -4.5V | 8.2  |
| V <sub>GS(th)</sub>   | 阈值电压           | -0.7                    | V    |

### 器件信息(1)

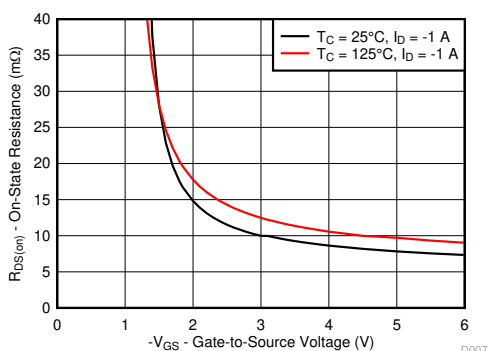
| 器件         | 数量   | 介质     | 封装                       | 配送   |
|------------|------|--------|--------------------------|------|
| CSD22205L  | 3000 | 7 英寸卷带 | 1.20mm × 1.20mm 基板栅格阵列封装 | 卷带包装 |
| CSD22205LT | 250  |        |                          |      |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

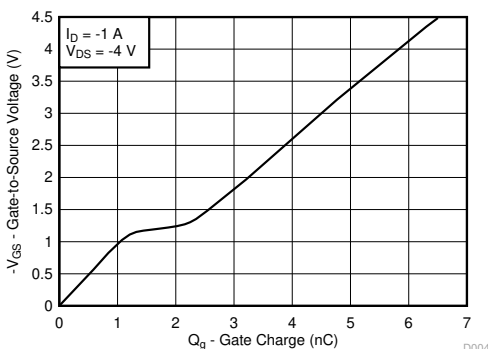
### 绝对最大额定值

| T <sub>A</sub> = 25°C            |           | 值         | 单位 |
|----------------------------------|-----------|-----------|----|
| V <sub>DS</sub>                  | 漏源电压      | -8        | V  |
| V <sub>GS</sub>                  | 栅源电压      | -6        | V  |
| I <sub>D</sub>                   | 持续漏极电流(1) | -7.4      | A  |
| I <sub>DM</sub>                  | 脉冲漏极电流(2) | -71       | A  |
| P <sub>D</sub>                   | 功率耗散(1)   | 0.6       | W  |
| T <sub>J</sub> 、T <sub>stg</sub> | 工作结温，贮存温度 | -55 至 150 | °C |

- (1) R<sub>θJA</sub> = 225°C/W (覆铜面积最小时的值)。  
 (2) 脉宽 ≤ 100 μs，占空比 ≤ 1%。



R<sub>DS(on)</sub> 与 V<sub>GS</sub> 之间的关系



R<sub>DS(on)</sub> 与 V<sub>GS</sub> 之间的关系

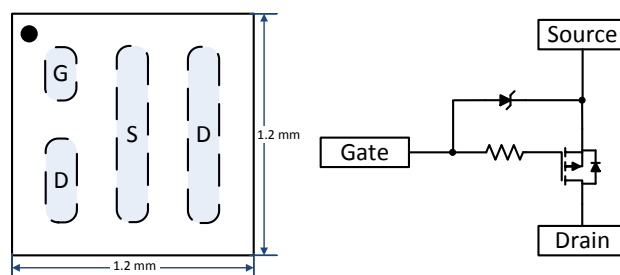


图 3-1. 顶视图和电路配置

## Table of Contents

|                                         |          |                                                                |          |
|-----------------------------------------|----------|----------------------------------------------------------------|----------|
| <b>1 特性</b> .....                       | <b>1</b> | <b>6 Device and Documentation Support</b> .....                | <b>7</b> |
| <b>2 应用</b> .....                       | <b>1</b> | 6.1 Receiving Notification of Documentation Updates.....       | 7        |
| <b>3 说明</b> .....                       | <b>1</b> | 6.2 Trademarks.....                                            | 7        |
| <b>4 Revision History</b> .....         | <b>2</b> | <b>7 Mechanical, Packaging, and Orderable Information</b> .... | <b>8</b> |
| <b>5 Specifications</b> .....           | <b>3</b> | 7.1 CSD22205L Package Dimensions.....                          | 8        |
| 5.1 Electrical Characteristics.....     | 3        | 7.2 Land Pattern Recommendation.....                           | 9        |
| 5.2 Thermal Information.....            | 4        | 7.3 Stencil Recommendation.....                                | 9        |
| 5.3 Typical MOSFET Characteristics..... | 4        |                                                                |          |

## 4 Revision History

| <b>Changes from Revision A (August 2017) to Revision B (February 2022)</b>       | <b>Page</b> |
|----------------------------------------------------------------------------------|-------------|
| • 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm.....                                           | 1           |
| • Changed CSD22205L Package Dimensions image height from 0.35 mm to 0.36 mm..... | 8           |

| <b>Changes from Revision * (May 2017) to Revision A (August 2017)</b>                                                | <b>Page</b> |
|----------------------------------------------------------------------------------------------------------------------|-------------|
| • Changed the units for timing parameters from $\mu$ s : to ns (nanoseconds) in the <a href="#">节 5.1</a> table..... | 3           |

## 5 Specifications

### 5.1 Electrical Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)

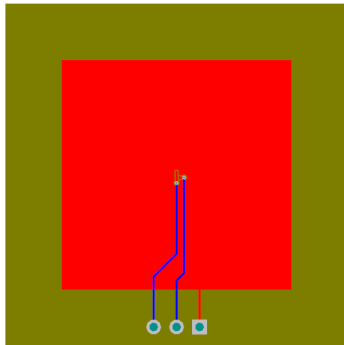
| PARAMETER                      |                                  | TEST CONDITIONS                                                                                  | MIN  | TYP   | MAX   | UNIT |
|--------------------------------|----------------------------------|--------------------------------------------------------------------------------------------------|------|-------|-------|------|
| <b>STATIC CHARACTERISTICS</b>  |                                  |                                                                                                  |      |       |       |      |
| B <sub>V</sub> DSS             | Drain-to-source voltage          | V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA                                                  | -8   |       |       | V    |
| I <sub>DSS</sub>               | Drain-to-source leakage current  | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -6.4 V                                                  |      |       | -100  | nA   |
| I <sub>GSS</sub>               | Gate-to-source leakage current   | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -6 V                                                    |      |       | -100  | nA   |
| V <sub>GS(th)</sub>            | Gate-to-source threshold voltage | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA                                     | -0.4 | -0.7  | -1.05 | V    |
| R <sub>DS(on)</sub>            | Drain-to-source on-resistance    | V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -0.2 A                                                |      | 30    |       | mΩ   |
|                                |                                  | V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -1 A                                                  |      | 20    | 40    |      |
|                                |                                  | V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1 A                                                  |      | 11.5  | 15.0  |      |
|                                |                                  | V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1 A                                                  |      | 8.2   | 9.9   |      |
| g <sub>fs</sub>                | Transconductance                 | V <sub>DS</sub> = -0.8 V, I <sub>D</sub> = -1 A                                                  |      | 10.4  |       | S    |
| <b>DYNAMIC CHARACTERISTICS</b> |                                  |                                                                                                  |      |       |       |      |
| C <sub>ISS</sub>               | Input capacitance                | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -4 V, f = 1 MHz                                         |      | 1070  | 1390  | pF   |
| C <sub>OSS</sub>               | Output capacitance               |                                                                                                  |      | 560   | 730   | pF   |
| C <sub>RSS</sub>               | Reverse transfer capacitance     |                                                                                                  |      | 190   | 250   | pF   |
| R <sub>G</sub>                 | Series gate resistance           |                                                                                                  |      | 30    |       | Ω    |
| Q <sub>g</sub>                 | Gate charge total (-4.5 V)       | V <sub>DS</sub> = -4 V, I <sub>D</sub> = -1 A                                                    |      | 6.5   | 8.5   | nC   |
| Q <sub>gd</sub>                | Gate charge gate-to-drain        |                                                                                                  |      | 1.0   |       | nC   |
| Q <sub>gs</sub>                | Gate charge gate-to-source       |                                                                                                  |      | 1.2   |       | nC   |
| Q <sub>g(th)</sub>             | Gate charge at V <sub>th</sub>   |                                                                                                  |      | 0.7   |       | nC   |
| Q <sub>OSS</sub>               | Output charge                    | V <sub>DS</sub> = -4 V, V <sub>GS</sub> = 0 V                                                    |      | 4.1   |       | nC   |
| t <sub>d(on)</sub>             | Turnon delay time                | V <sub>DS</sub> = -4 V, V <sub>GS</sub> = -4.5 V,<br>I <sub>D</sub> = -1 A, R <sub>G</sub> = 0 Ω |      | 30    |       | ns   |
| t <sub>r</sub>                 | Rise time                        |                                                                                                  |      | 14    |       | ns   |
| t <sub>d(off)</sub>            | Turnoff delay time               |                                                                                                  |      | 70    |       | ns   |
| t <sub>f</sub>                 | Fall time                        |                                                                                                  |      | 32    |       | ns   |
| <b>DIODE CHARACTERISTICS</b>   |                                  |                                                                                                  |      |       |       |      |
| V <sub>SD</sub>                | Diode forward voltage            | I <sub>S</sub> = -1 A, V <sub>GS</sub> = 0 V                                                     |      | -0.68 | -1.0  | V    |
| Q <sub>rr</sub>                | Reverse recovery charge          | V <sub>DS</sub> = -4 V, I <sub>F</sub> = -1 A,                                                   |      | 16    |       | nC   |
| t <sub>rr</sub>                | Reverse recovery time            | di/dt = 200 A/μs                                                                                 |      | 38    |       | ns   |

### 5.2 Thermal Information

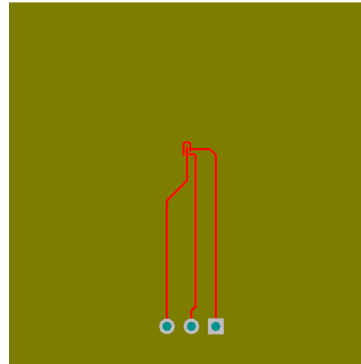
T<sub>A</sub> = 25°C (unless otherwise stated)

| THERMAL METRIC   |                                                       | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------------------------|-----|-----|-----|------|
| R <sub>θJA</sub> | Junction-to-ambient thermal resistance <sup>(2)</sup> |     | 75  |     | °C/W |
|                  | Junction-to-ambient thermal resistance <sup>(1)</sup> |     | 225 |     |      |

- (1) Device mounted on FR4 material with minimum Cu mounting area.
- (2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.



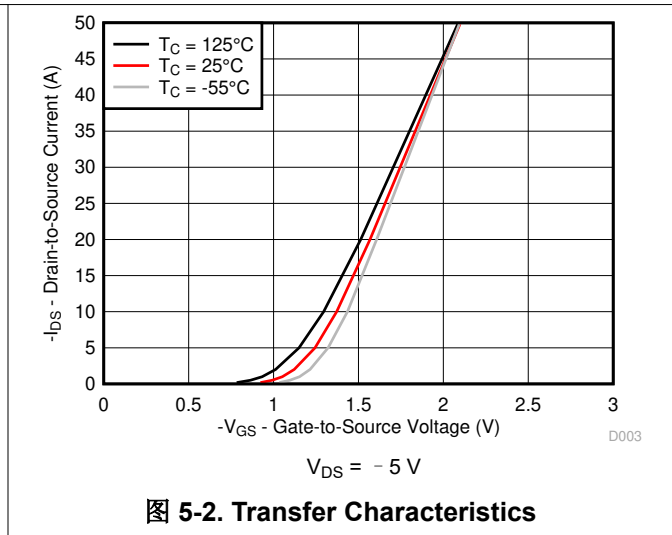
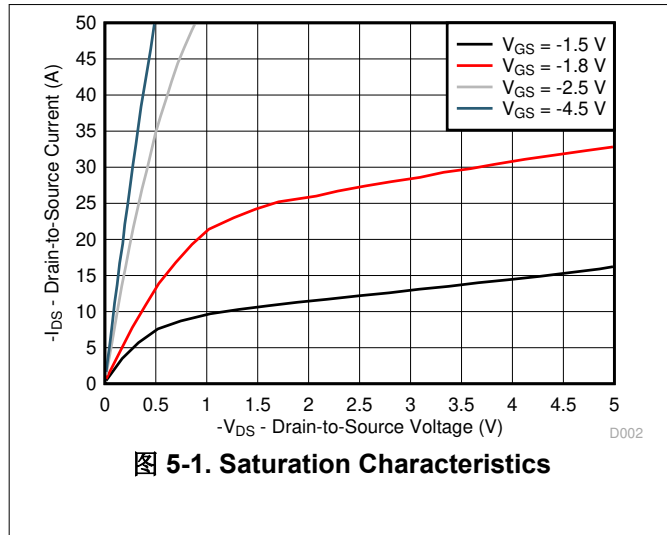
Typ R<sub>θJA</sub> = 75°C/W when mounted on 1 in<sup>2</sup> of 2-oz Cu.



Typ R<sub>θJA</sub> = 225°C/W when mounted on minimum pad area of 2-oz Cu.

### 5.3 Typical MOSFET Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)



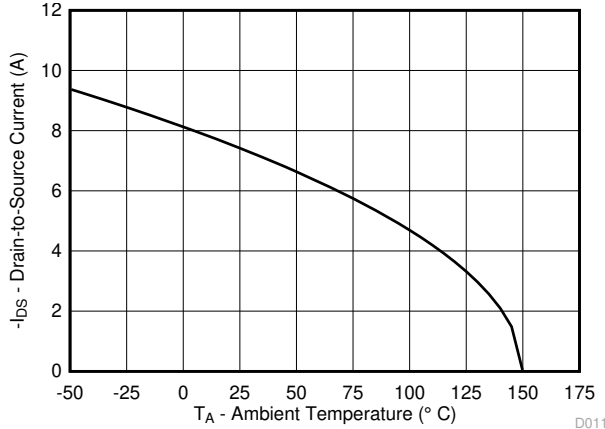


图 5-3. Maximum Drain Current vs Temperature

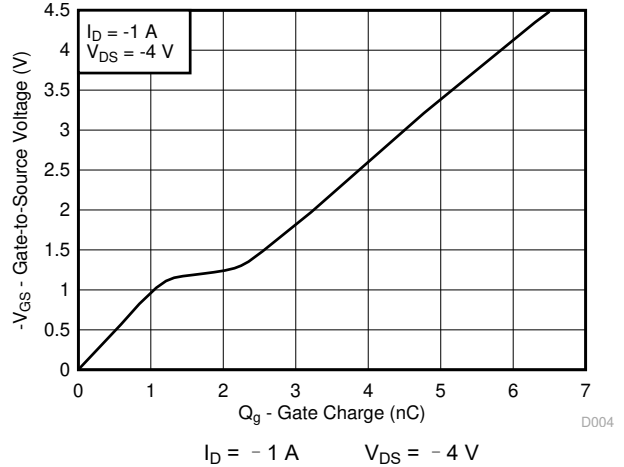


图 5-4. Gate Charge

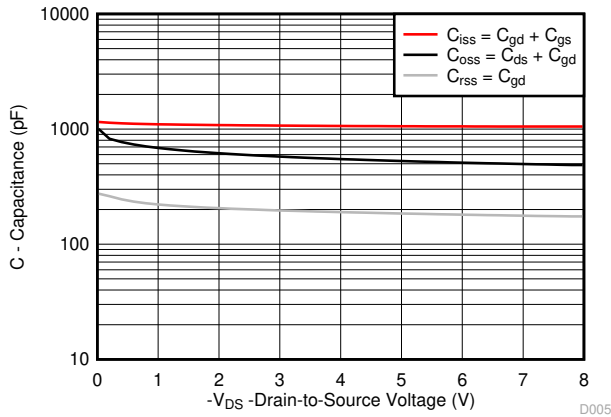


图 5-5. Capacitance

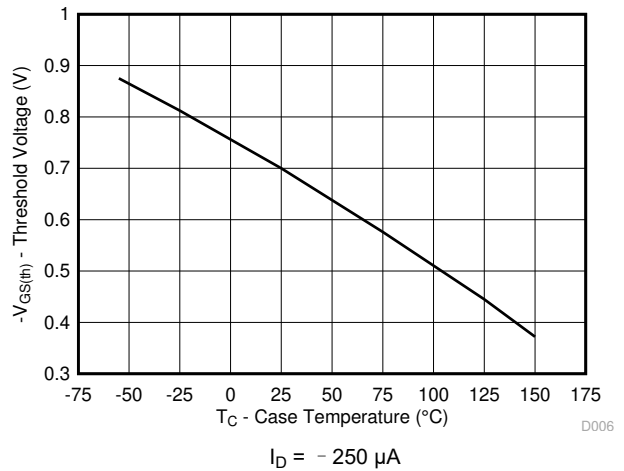


图 5-6. Threshold Voltage vs Temperature

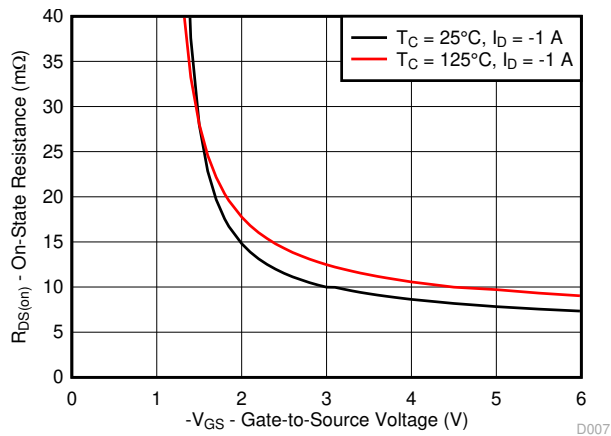


图 5-7. On-State Resistance vs Gate-to-Source Voltage

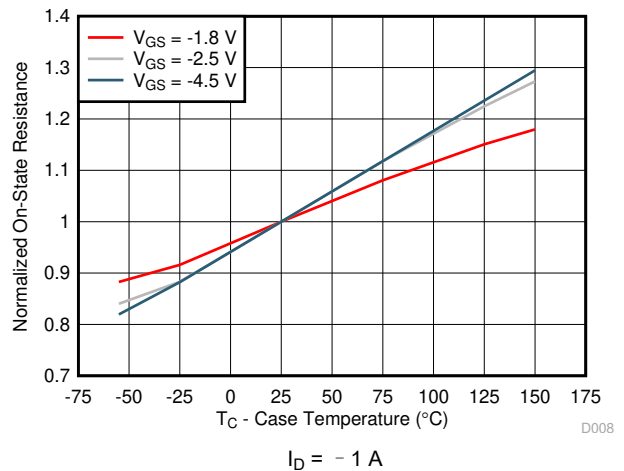


图 5-8. Normalized On-State Resistance vs Temperature

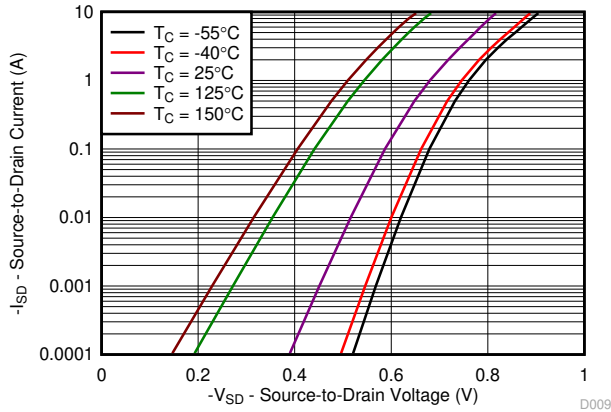


图 5-9. Typical Diode Forward Voltage

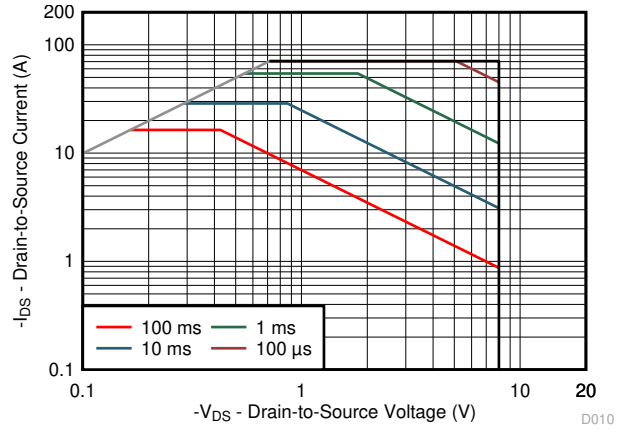


图 5-10. Maximum Safe Operating Area

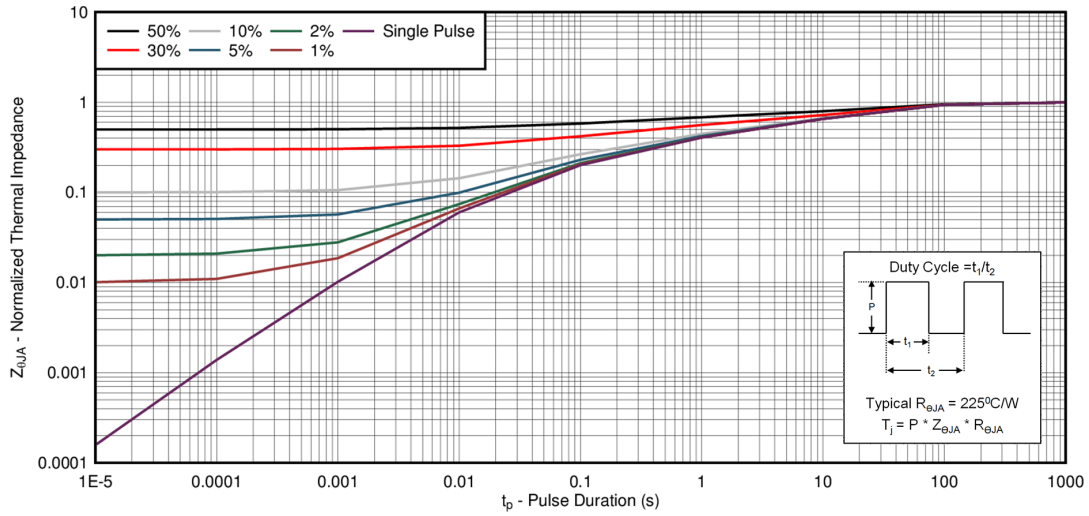


图 5-11. Transient Thermal Impedance

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Trademarks

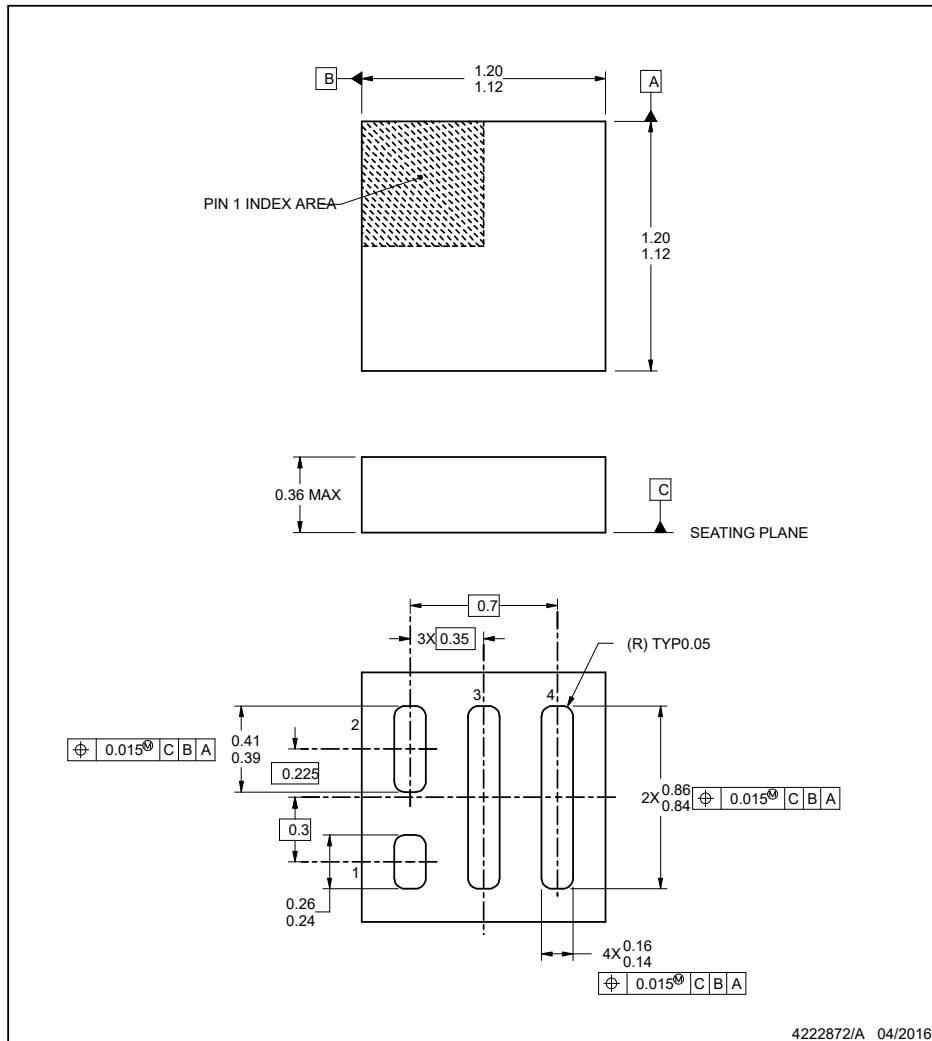
NexFET™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 CSD22205L Package Dimensions



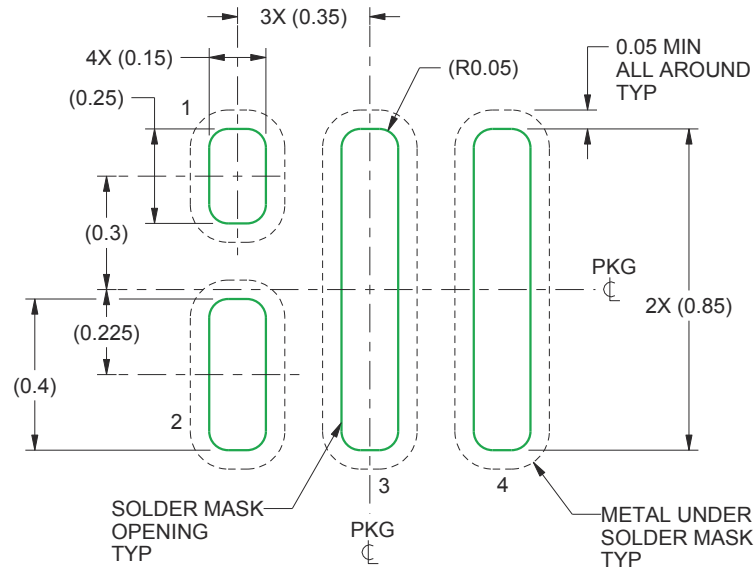
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is a lead-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

表 7-1. Pin Configuration Table

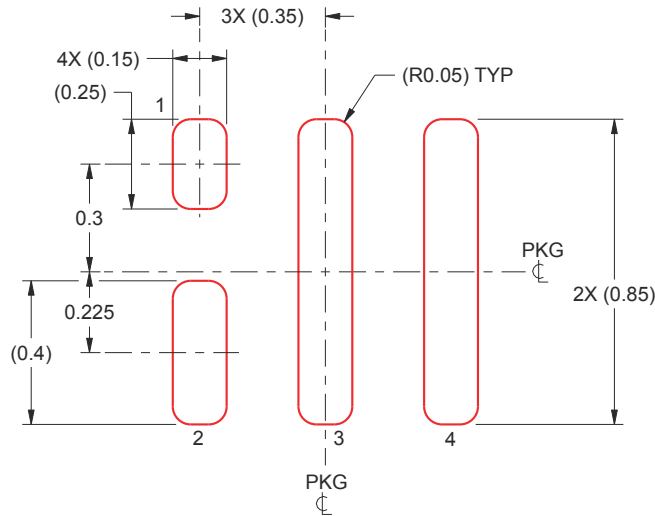
| POSITION | DESIGNATION |
|----------|-------------|
| 1        | Gate        |
| 2        | Drain       |
| 3        | Source      |
| 4        | Drain       |



## 7.2 Land Pattern Recommendation



## 7.3 Stencil Recommendation



- A. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins     | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|--------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CSD22205L</a>  | Active        | Production           | PICOSTAR (YMG)   4 | 3000   LARGE T&R      | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 205                 |
| CSD22205L.B                | Active        | Production           | PICOSTAR (YMG)   4 | 3000   LARGE T&R      | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 205                 |
| <a href="#">CSD22205LT</a> | Active        | Production           | PICOSTAR (YMG)   4 | 250   SMALL T&R       | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 205                 |
| CSD22205LT.B               | Active        | Production           | PICOSTAR (YMG)   4 | 250   SMALL T&R       | Yes         | NIAU                                 | Level-1-260C-UNLIM                | -55 to 150   | 205                 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD22205L  | PICOSTAR     | YMG             | 4    | 3000 | 180.0              | 8.4                | 1.26    | 1.26    | 0.42    | 4.0     | 8.0    | Q1            |
| CSD22205LT | PICOSTAR     | YMG             | 4    | 250  | 180.0              | 8.4                | 1.26    | 1.26    | 0.42    | 4.0     | 8.0    | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CSD22205L  | PICOSTAR     | YMG             | 4    | 3000 | 182.0       | 182.0      | 20.0        |
| CSD22205LT | PICOSTAR     | YMG             | 4    | 250  | 182.0       | 182.0      | 20.0        |

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月