N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

查询样品: CSD13303W1015

特性

- 超低接通电阻
- 超低栅极电荷 **(Qg)** 和栅漏电荷 **(Qgd)**
- 小封装尺寸
- 低高度（高度为 **0.62mm**）
- 无铅
- 符合 **RoHS** 标准
- 无卤素
- 芯片级封装 **(CSP) 1 x 1.5mm** 晶圆级封装

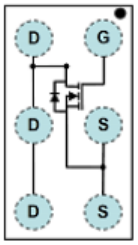
应用范围

- 电池管理
- 负载开关
- 电池保护

说明

此器件设计用于在超低高度并具有出色散热特性的尽可能小外形尺寸封装内产生最低的接通电阻和栅极电荷。

顶视图



产品概述

除非额外注明，否则 T_A=25°C		典型值		单位
V_{DS}	漏源电压	12		V
Q_g	栅极电荷总量 (4.5V)	3.9		nC
Q_{gd}	栅漏栅极电荷	0.4		nC
R_{DS}（接通）	漏源导通电阻	V_{GS}=2.5V	18	mΩ
		V_{GS}=4.5V	16	mΩ
$V_{GS(th)}$	电压阀值	0.85		V

订购信息

器件	封装	介质	数量	出货
CSD13303W1015	1 × 1.5 晶圆级封装	7 英寸卷带	3000	卷带封装

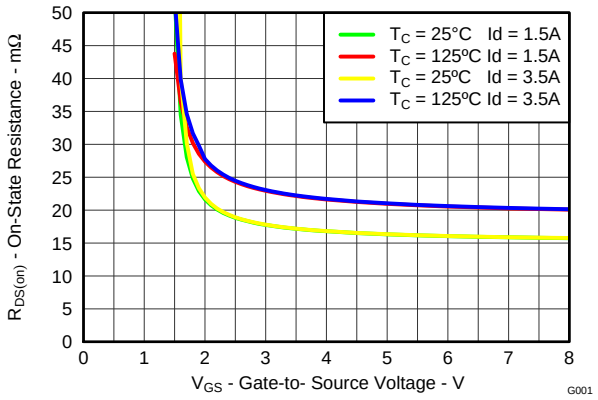
绝对最大额定值

T_A=25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	±8	V
I_D	持续漏极电流，T_C=25°C 时测得(1)	3.5	A
I_{DM}	脉冲漏极电流，T_A=25°C 时测得(2)	31	A
P_D	功率耗散(1)	1.65	W
T_{STG}	储存温度范围	-55 至 150	°C
T_J	工作结温范围		

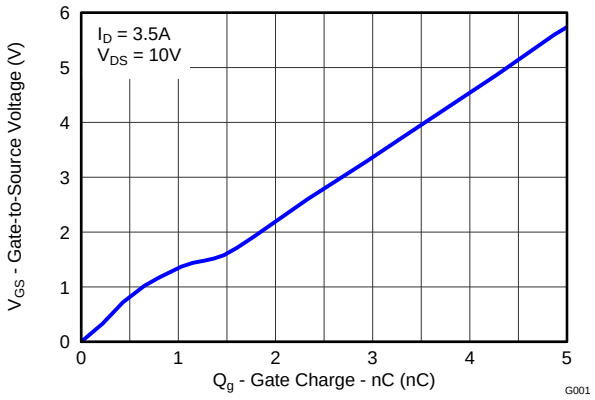
(1) 在 1 in^2 2 盎司纯铜 (Cu) (2 oz.) 且厚度为 0.060" 的环氧板 (FR4) 印刷电路板 (PCB) 上，$R_{\theta JA}$ = 75.7°C/W （典型值）。

(2) 脉宽 ≤ 1ms，占空比 ≤ 2%

R_{DS}（接通）与 V_{GS}间的关系



栅极电荷



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

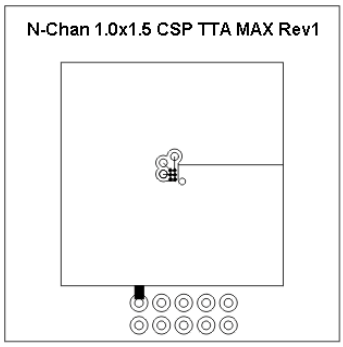
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	12			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 9.6V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.65	0.85	1.2	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 2.5V, I_D = 1.5A		18	23	mΩ
		V_{GS} = 4.5V, I_D = 1.5A		16	20	mΩ
g_{fs}	Transconductance	V_{DS} = 6V, I_D =1.5A		14		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 6V, f = 1MHz		550	715	pF
C_{OSS}	Output Capacitance			400	480	pF
C_{RSS}	Reverse Transfer Capacitance			29	36	pF
R_g				3	4.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 6V, I_D = 1.5A		3.9	4.7	nC
Q_{gd}	Gate Charge Gate to Drain			0.4		nC
Q_{gs}	Gate Charge Gate to Source			1		nC
$Q_{g(th)}$	Gate Charge at Vth			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = 6V, V_{GS} = 0V		4.9		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 6V, V_{GS} = 4.5V, I_D = 1.5A R_G = 4Ω		4.6		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			14.7		ns
t_f	Fall Time			3.2		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 1.5A, V_{GS} = 0V		0.7	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 6V, I_F = 1.5A, di/dt = 200A/µs		14		nC
t_{rr}	Reverse Recovery Time			38.7		ns

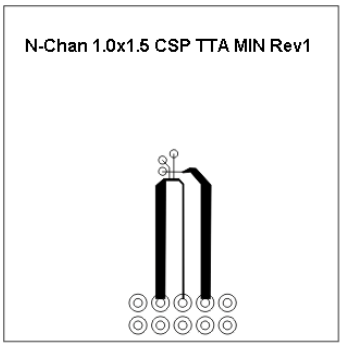
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			295.5	°C/W
	Thermal Resistance Junction to Ambient (1 in^2 Cu area)			94.6	°C/W



Max $R_{\theta JA}$ = 94.6°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 295.5°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

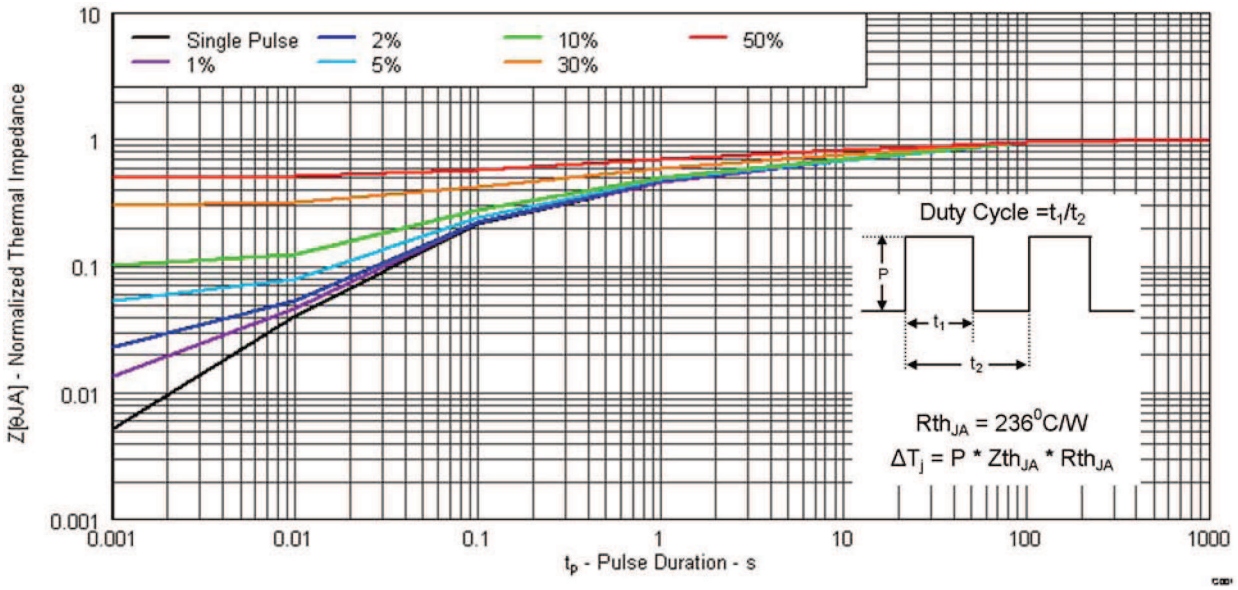


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

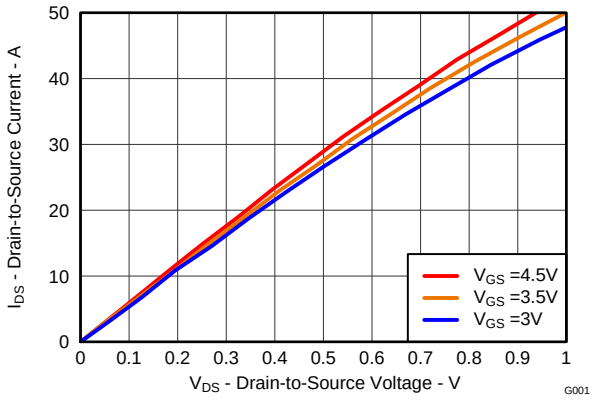


Figure 2. Saturation Characteristics

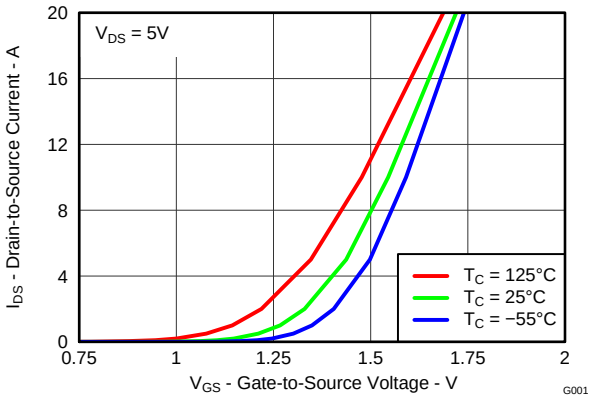


Figure 3. Transfer Characteristics

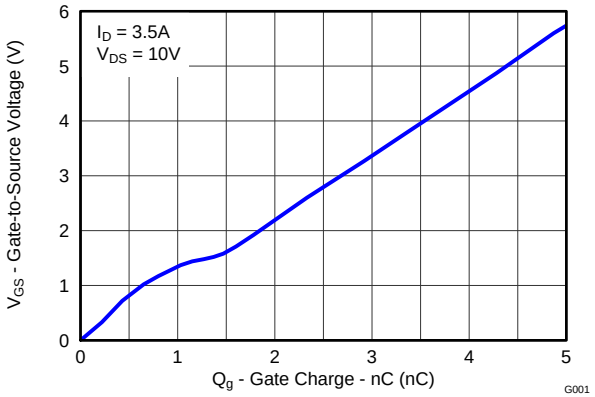


Figure 4. Gate Charge

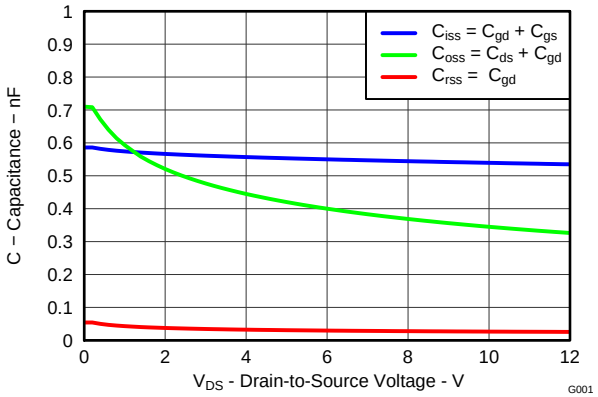


Figure 5. Capacitance

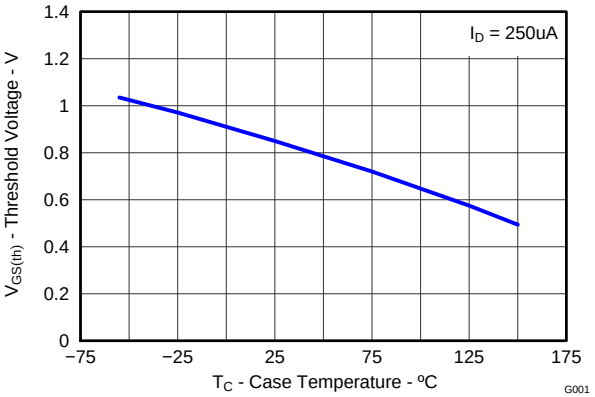


Figure 6. Threshold Voltage vs. Temperature

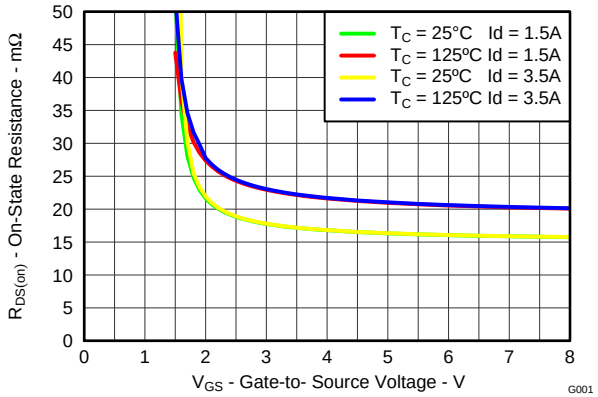


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

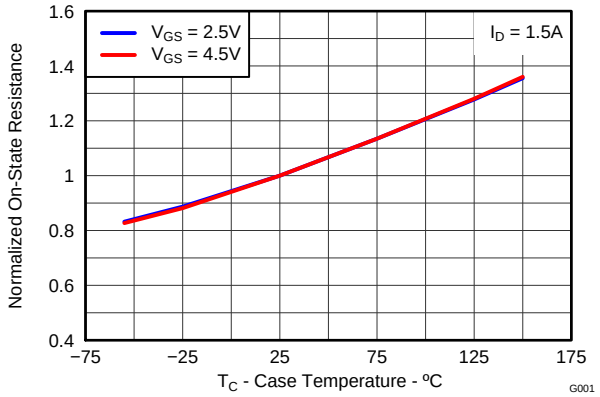


Figure 8. Normalized On Resistance vs. Temperature

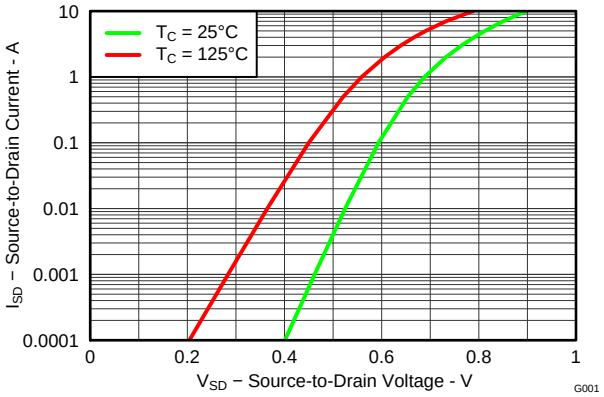


Figure 9. Typical Diode Forward Voltage

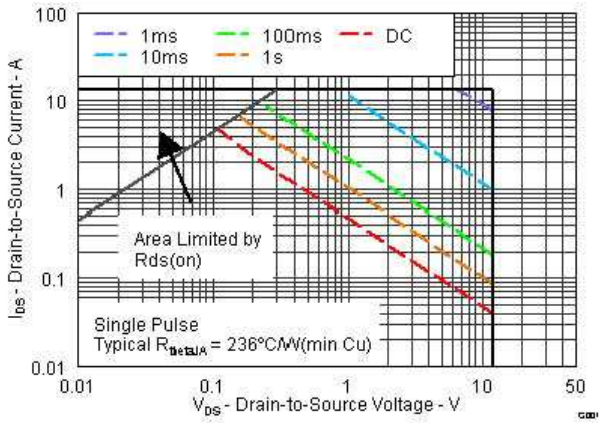


Figure 10. Maximum Safe Operating Area

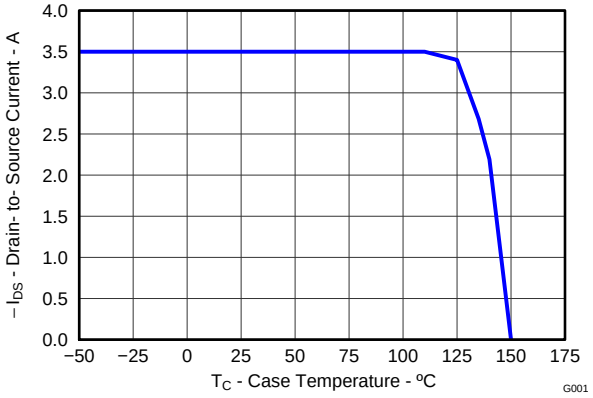


Figure 11. Maximum Drain Current vs. Temperature

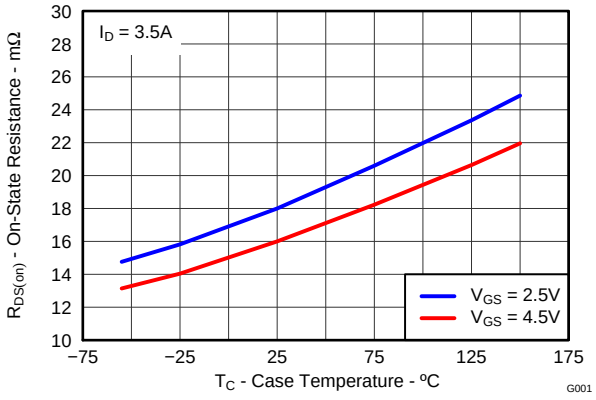
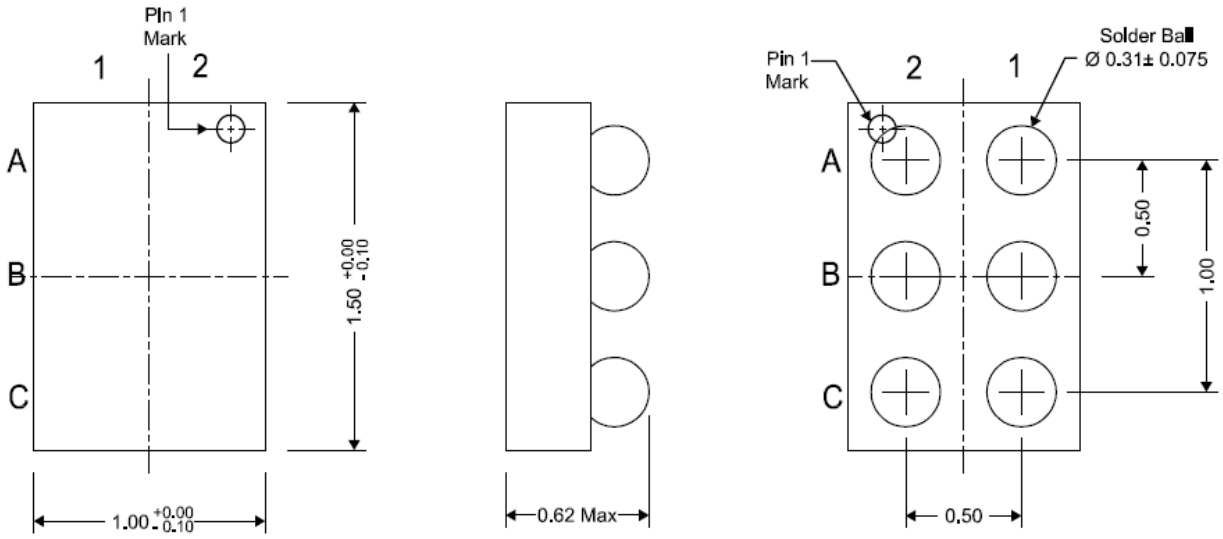
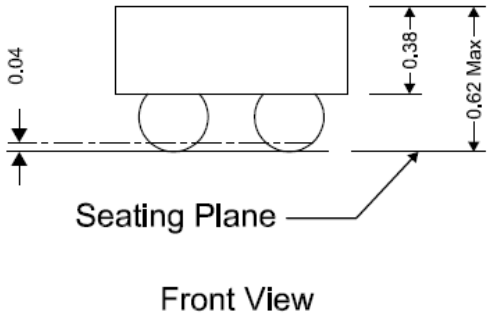


Figure 12. On Resistance vs. Temperature

MECHANICAL DATA

CSD13303W1015 Package Dimensions



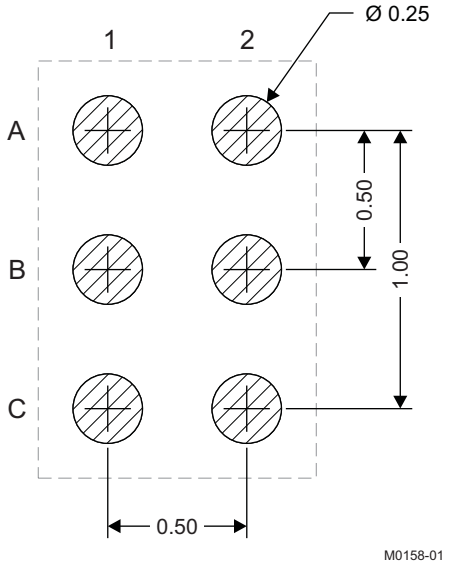


NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

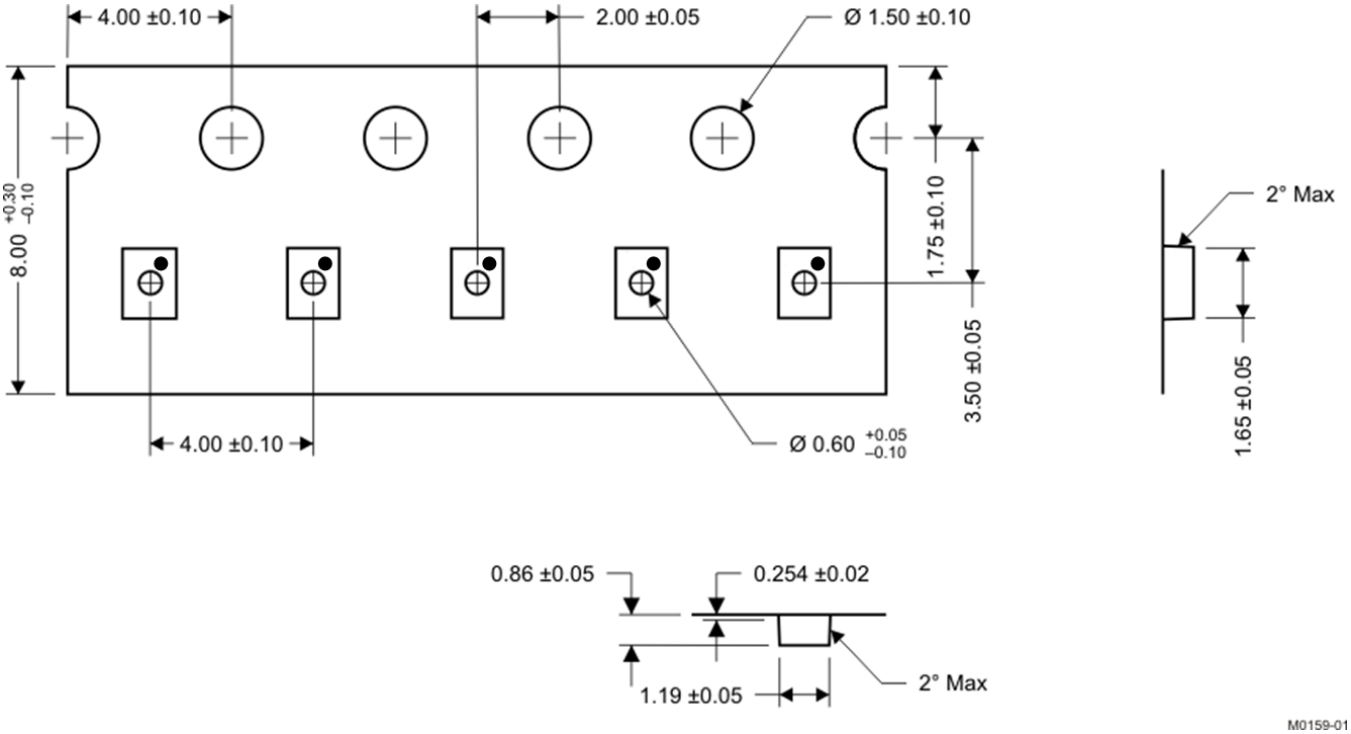
POSITION	DESIGNATION
C2, B2	Source
A2	Gate
A1, B1, C1	Drain

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (May 2012) to Revision A	Page
• Changed the Tape and Reel Information section	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13303W1015	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	13303	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

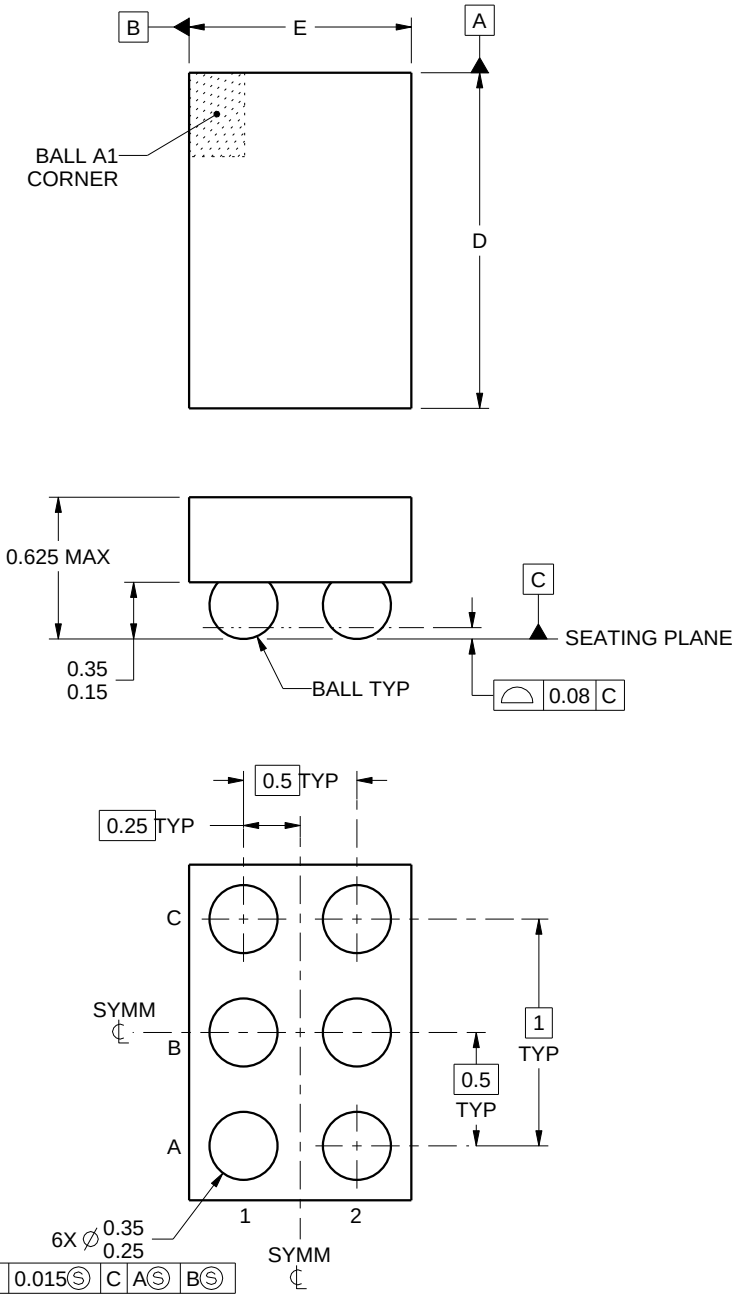
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

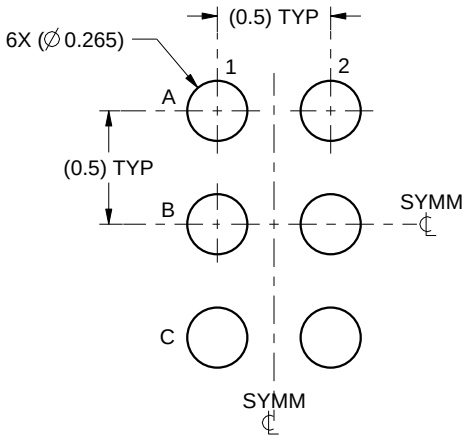


4219522/A 02/2015

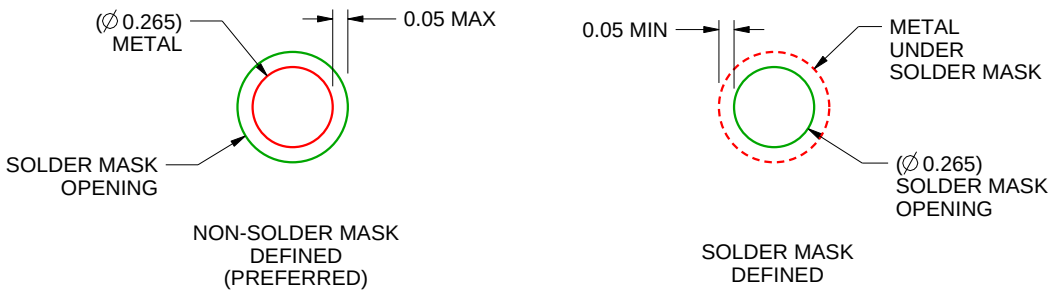
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:30X

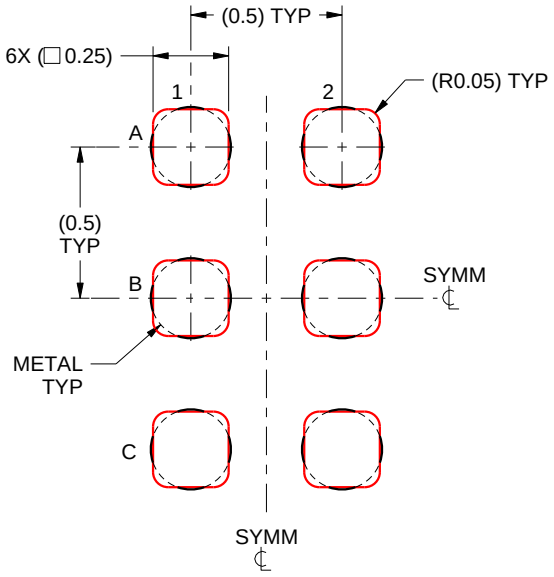


SOLDER MASK DETAILS
NOT TO SCALE

4219522/A 02/2015

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219522/A 02/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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