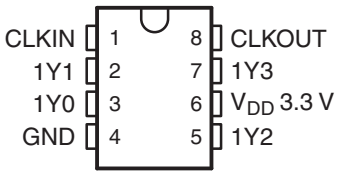
3.3-V CLOCK PHASE-LOCKED LOOP CLOCK DRIVER

FEATURES

- **Qualified for Automotive Applications**
- **Phase-Locked Loop Clock Driver for Synchronous DRAM and General-Purpose Applications**
- **Spread-Spectrum Clock Compatible**
- **Operating Frequency: 24 MHz to 200 MHz**
- **Low Jitter (Cycle-to-Cycle): <150 ps Over the Range 66 MHz to 200 MHz**
- **Distributes One Clock Input to One Bank of Five Outputs (CLKOUT Is Used to Tune the Input-Output Delay)**
- **Three-States Outputs When There Is No Input Clock**
- **Operates From Single 3.3-V Supply**
- **Available in 8-Pin SOIC Package**
- **Consumes Less Than 100 μA (Typically) in Power Down Mode**
- **Internal Feedback Loop Is Used to Synchronize the Outputs to the Input Clock**
- **25-Ω On-Chip Series Damping Resistors**
- **Integrated RC PLL Loop Filter Eliminates the Need for External Components**

D PACKAGE
(TOP VIEW)



DESCRIPTION

The CDCVF2505 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks (1Y[0–3] and CLKOUT) to the input clock signal (CLKIN). The CDCVF2505 operates at 3.3 V. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs provides low-skew, low-jitter copies of CLKIN. Output duty cycles are adjusted to 50 percent, independent of duty cycle at CLKIN. The device automatically goes in power-down mode when no input signal is applied to CLKIN.

Unlike many products containing PLLs, the CDCVF2505 does not require an external RC network. The loop filter for the PLLs is included on-chip, minimizing component count, space, and cost.

Because it is based on the PLL circuitry, the CDCVF2505 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, and following any changes to the PLL reference.

The CDCVF2505 is characterized for operation from –40°C to 85°C.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Reel of 2500	CDCVF2505IDRQ1	CKV05Q

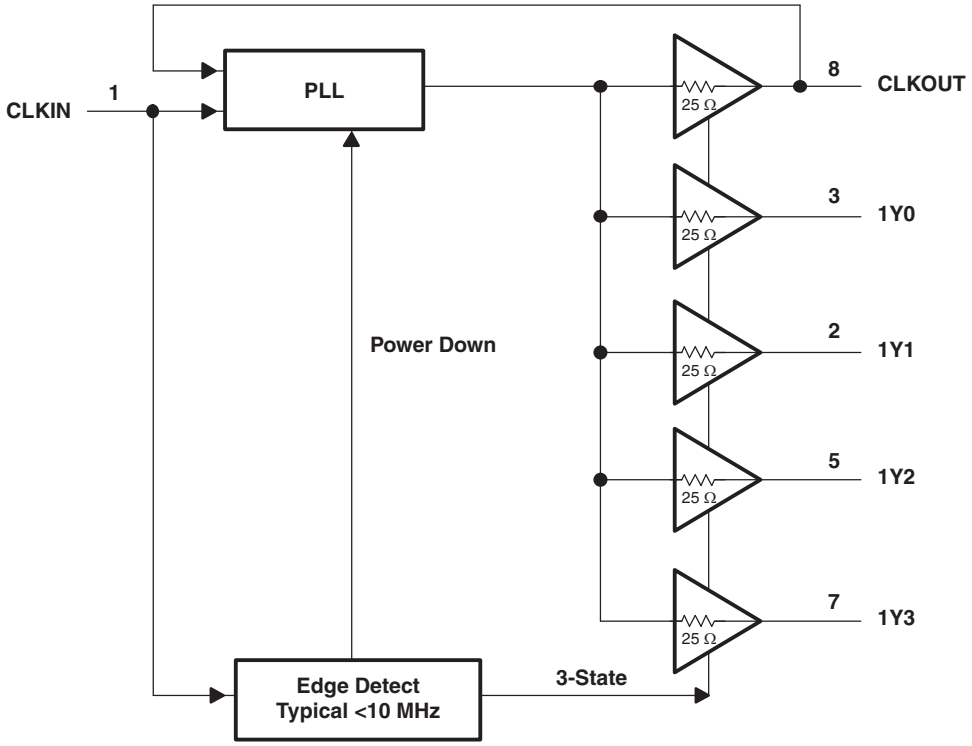
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUT	OUTPUTS	
CLKIN	1Y[0–3]	CLKOUT
L	L	L
H	H	H
<10 MHz(1)	Z	Z

(1) Below 2 MHz (typical) the device goes into power-down mode, during which the PLL is turned off and the outputs enter into Hi-Z mode. If a >10-MHz signal is applied at CLKIN, the PLL turns on, reacquires lock, and stabilizes after approximately 100 µs. The outputs are then enabled.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
1Y0	3	O	Clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series damping resistor.
1Y1	2		
1Y2	5		
1Y3	7		
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF2505 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid signal is applied, a stabilization time (100 µs) is required for the PLL to phase lock the feedback signal to CLKIN.
CLKOUT	8	O	Feedback output. CLKOUT completes the internal feedback loop of the PLL. This connection is made inside the chip and an external feedback loop should NOT be connected. CLKOUT can be loaded with a capacitor to achieve zero delay between CLKIN and the Y outputs.
GND	4	Power	Ground
V_{DD}3.3V	6	Power	3.3-V supply

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage range		–0.5 V to 4.3 V
V_I	Input voltage range(2)(3)		–0.5 V to V_{DD} + 0.5 V
V_O	Output voltage range(2)(3)		–0.5 V to V_{DD} + 0.5 V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{DD}	±50 mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{DD}	±50 mA
I_O	Continuous total output current	V_O = 0 to V_{DD}	±50 mA
θ_{JA}	Package thermal impedance(4)		97.1°C/W
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.3 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTROSTATIC DISCHARGE INFORMATION

	ESD MODEL	LIMIT
HBM	Human-Body Model	2000 V
MM	Machine Model	300 V
CDM	Charged-Device Model	1000 V

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	0.7 × V_{DD}			V
V_{IL}	Low-level input voltage			0.3 × V_{DD}	V
V_I	Input voltage	0		V_{DD}	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–40		85	°C

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency		24		200	MHz
	Input clock duty cycle	24 MHz to 85 MHz(1)	30		85	%
		86 MHz to 200 MHz	40	50	60	
	Stabilization time(2)				100	µs

(1) Specified by design.
(2) Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input voltage		I_I = –18 mA	3 V			–1.2	V
V_{OH}	High-level output voltage		I_{OH} = –100 µA	MIN to MAX	V_{DD} – 0.2			V
			I_{OH} = –12 mA	3 V	2.1			
			I_{OH} = –6 mA	3 V	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 100 µA	MIN to MAX			0.2	V
			I_{OL} = 12 mA	3 V			0.8	
			I_{OL} = 6 mA	3 V			0.55	
I_{OH}	High-level output current		V_O = 1 V	3 V	–27			mA
			V_O = 1.65 V	3.3 V		–36		
I_{OL}	Low-level output current		V_O = 2 V	3 V	27			mA
			V_O = 1.65 V	3.3 V		40		
I_I	Input current		V_I = 0 V or V_{DD}				±5	µA
C_i	Input capacitance		V_I = 0 V or V_{DD}	3.3 V		4.2		pF
C_o	Output capacitance	Yn	V_I = 0 V or V_{DD}	3.3 V		2.8		pF
		CLKOUT				5.2		

(1) All typical values are at nominal V_{DD} and T_A = 25°C.

SWITCHING CHARACTERISTICS(1)

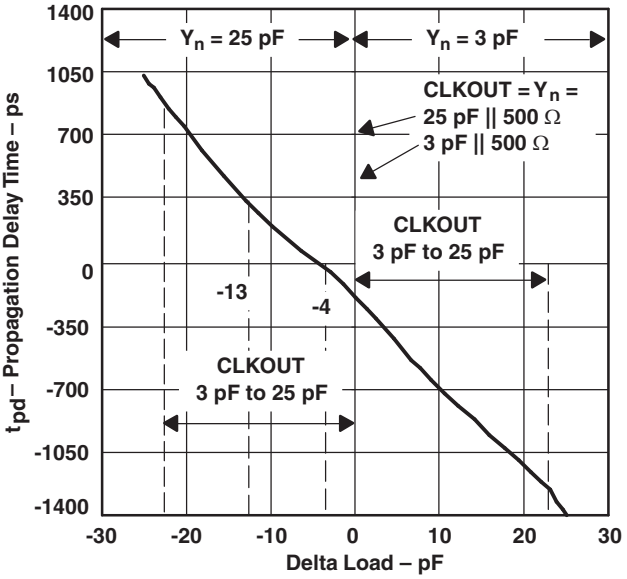
over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{pd}	Propagation delay, normalized (see Figure 1)	CLKIN to Yn, f = 66 MHz to 200 MHz	–150		150	ps
$t_{sk(o)}$	Output skew(3)	Yn to Yn			150	ps
$t_{c(jit\_cc)}$	Jitter (cycle to cycle) (see Figure 5)	f = 66 MHz to 200 MHz		70	150	ps
		f = 24 MHz to 50 MHz		200	400	
odc	Output duty cycle (see Figure 4)	f = 24 MHz to 200 MHz at 50% V_{DD}	45		55	%
t_r	Rise time	V_O = 0.4 V to 2 V	0.5		2	ns
t_f	Fall time	V_O = 2 V to 0.4 V	0.5		2	ns

(1) Not production tested
(2) All typical values are at nominal V_{DD} and T_A = 25°C.
(3) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

TYPICAL CHARACTERISTICS

t_{PD}, PROPAGATION DELAY TIME
vs
DELTA LOAD (TYPICAL VALUES at 3.3 V, 25°C)
CLOCK FREQUENCY, f = 100 MHz



NOTE: Delta Load = CLKOUT Load – Yn Load

Figure 1.

t_{pd}, PROPAGATION DELAY TIME
vs
FREQUENCY (TYPICAL VALUES at 3.3 V, 25°C)

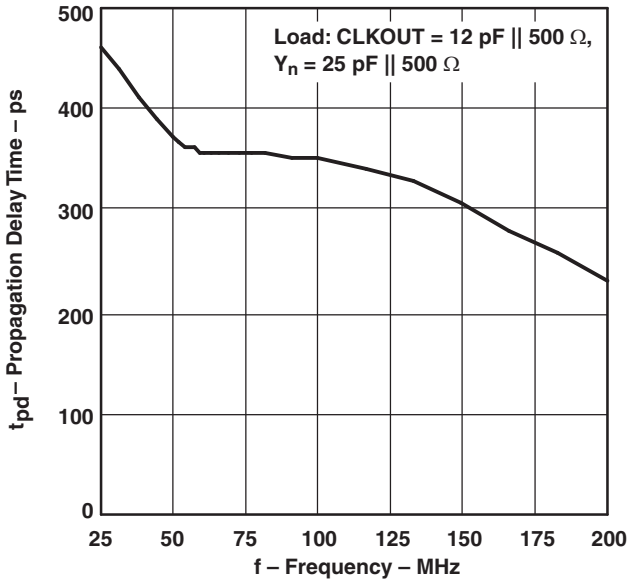


Figure 2.

t_{pd}, TYPICAL PROPAGATION DELAY TIME
vs
FREQUENCY (TUNED FOR MINIMUM DELAY)

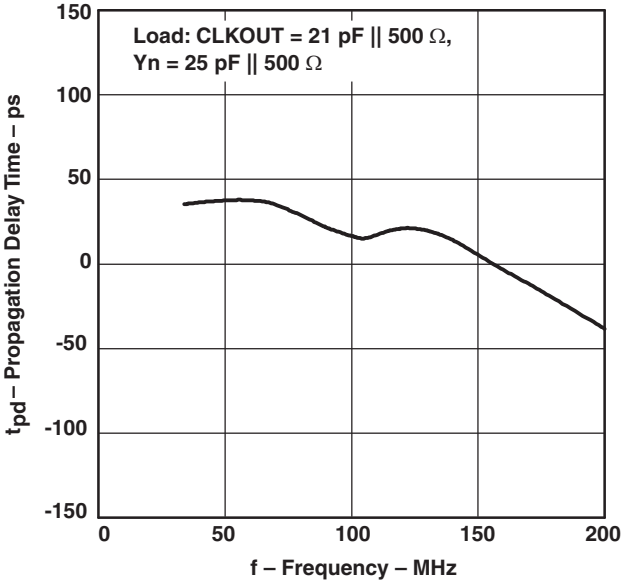


Figure 3.

DUTY CYCLE
vs
FREQUENCY

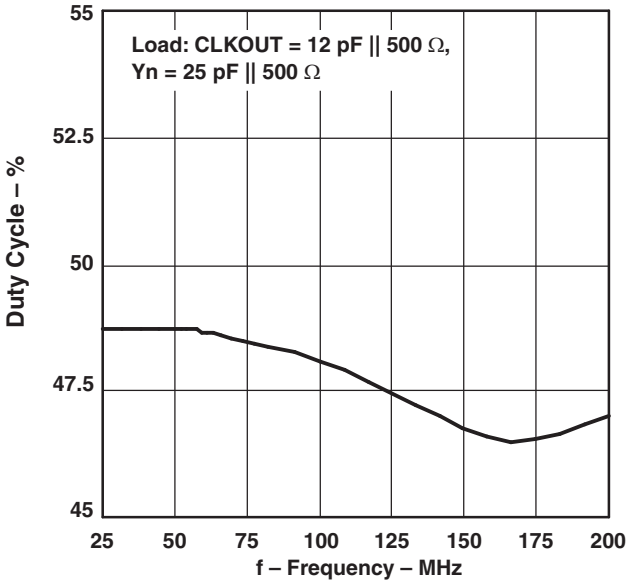


Figure 4.

TYPICAL CHARACTERISTICS (continued)

CYCLE-to-CYCLE JITTER vs FREQUENCY

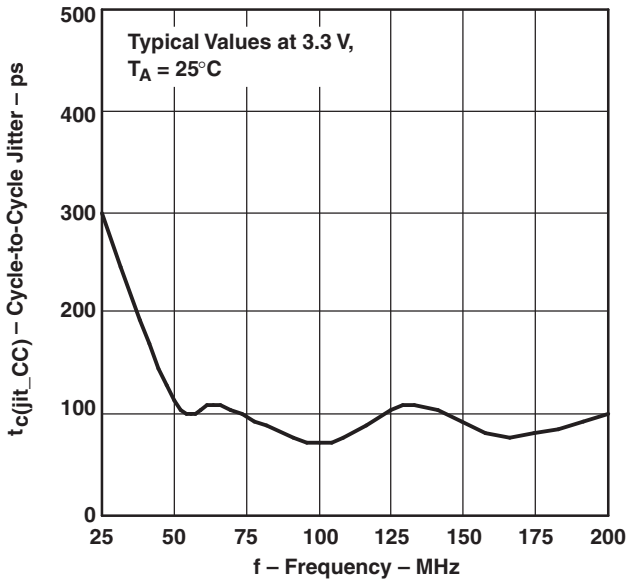


Figure 5.

I_{CC}, SUPPLY CURRENT vs FREQUENCY

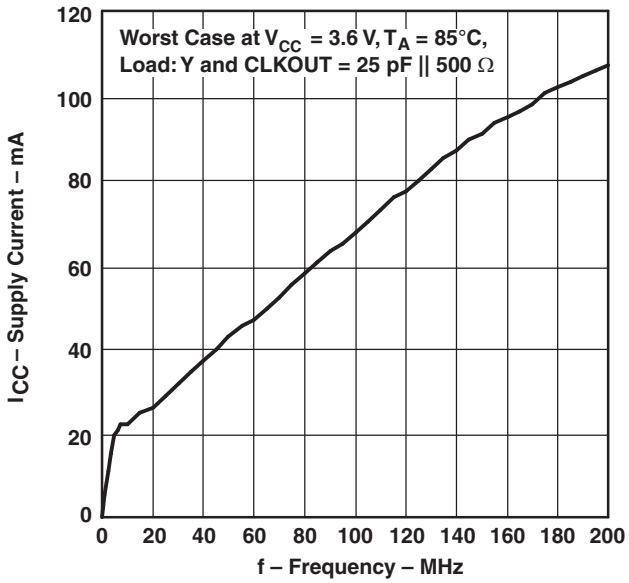


Figure 6.

PARAMETER MEASUREMENT INFORMATION

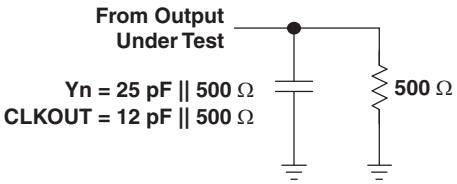


Figure 7. Test Load Circuit

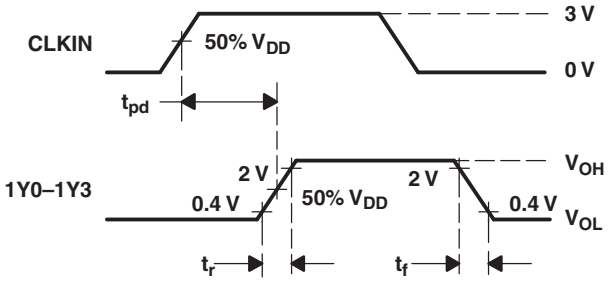


Figure 8. Voltage Threshold for Measurements, Propagation Delay (t_{pd})

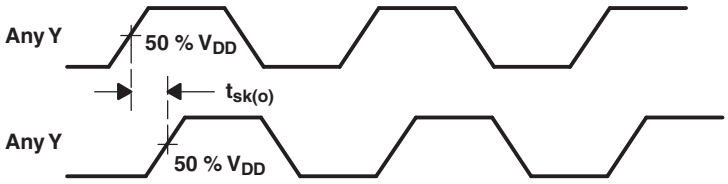


Figure 9. Output Skew

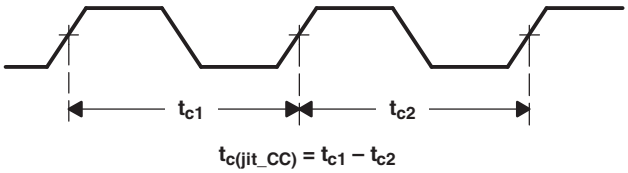


Figure 10. Cycle-to-Cycle Jitter

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCVF2505IDRQ1	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05Q
CDCVF2505IDRQ1.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CDCVF2505-Q1 :

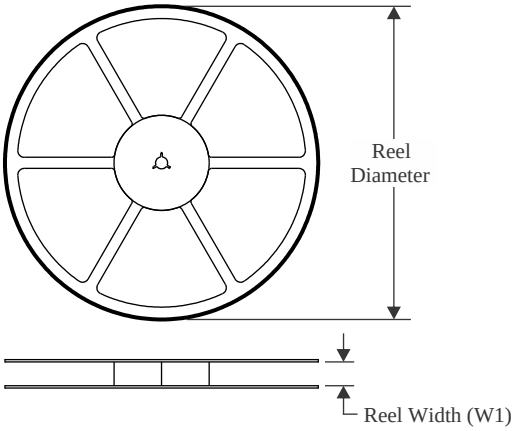
- Catalog : CDCVF2505

NOTE: Qualified Version Definitions:

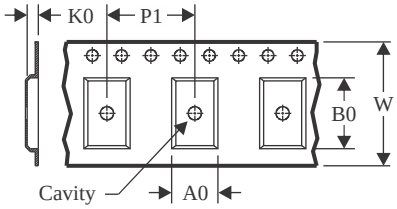
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

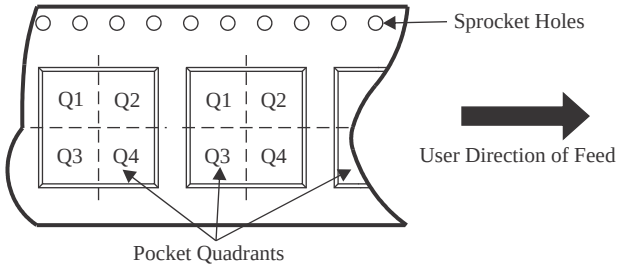


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

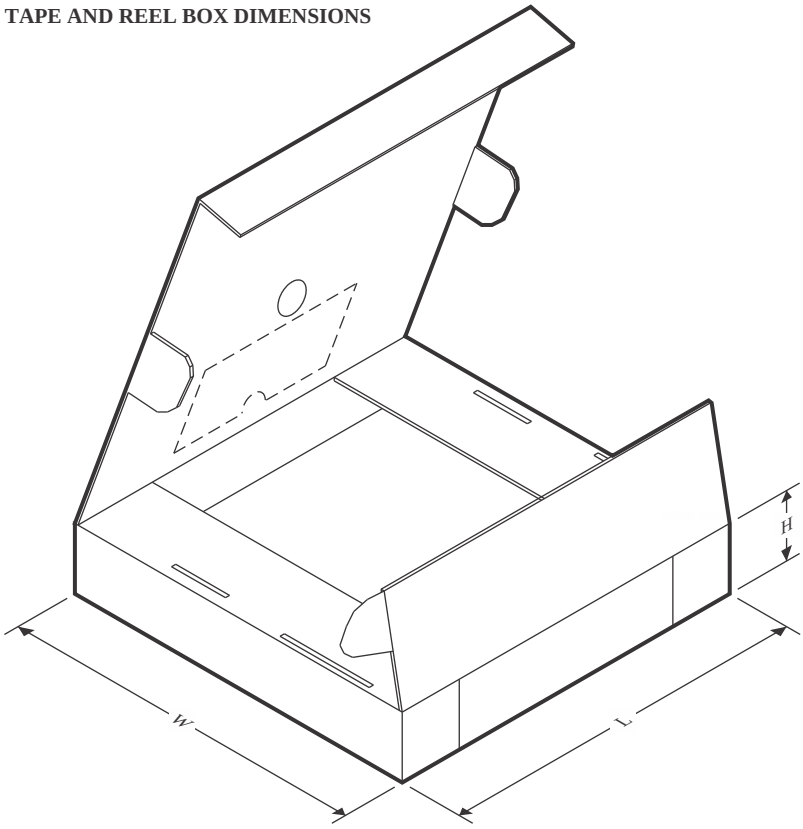
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

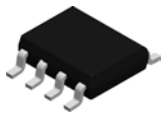
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2505IDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2505IDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

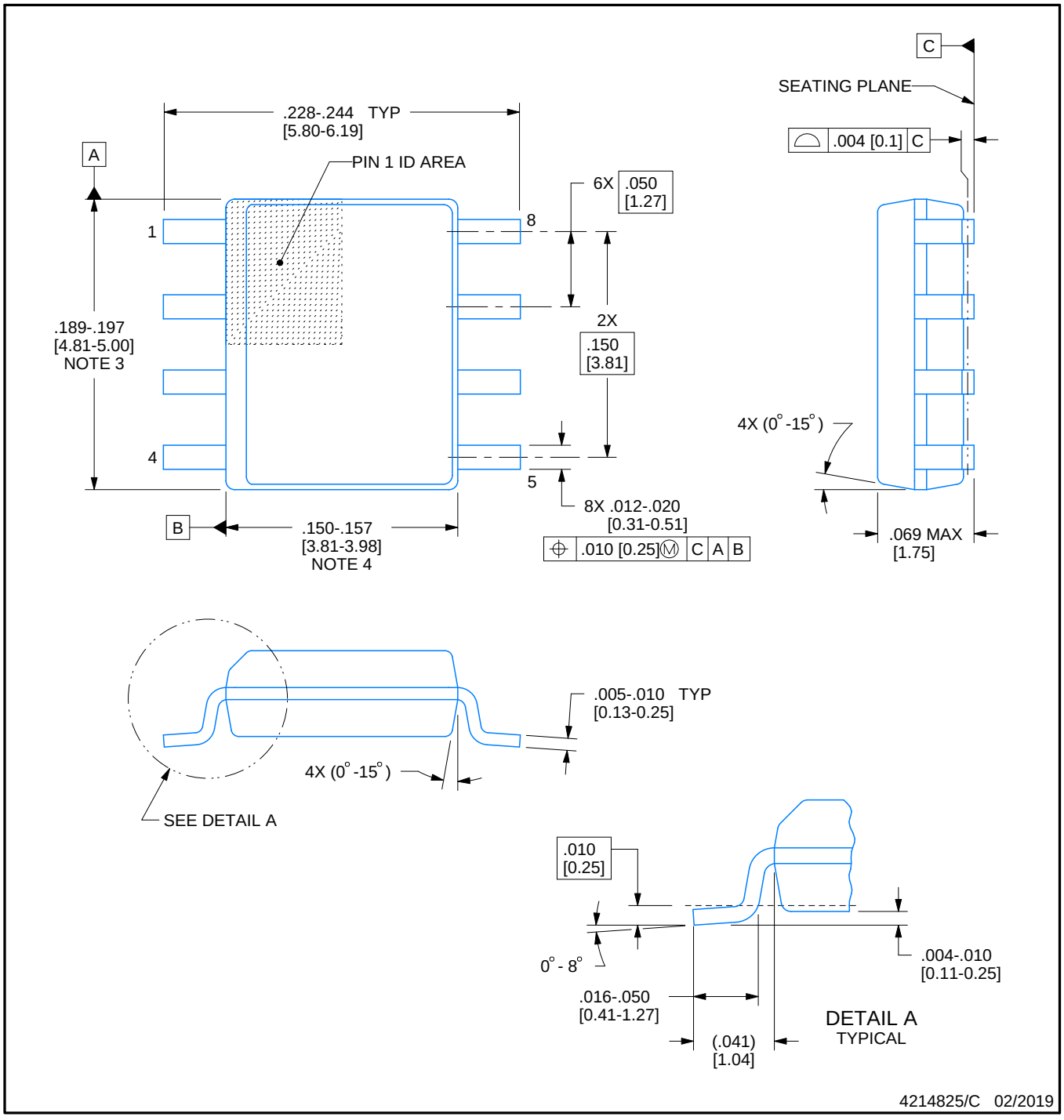


PACKAGE OUTLINE

D0008A

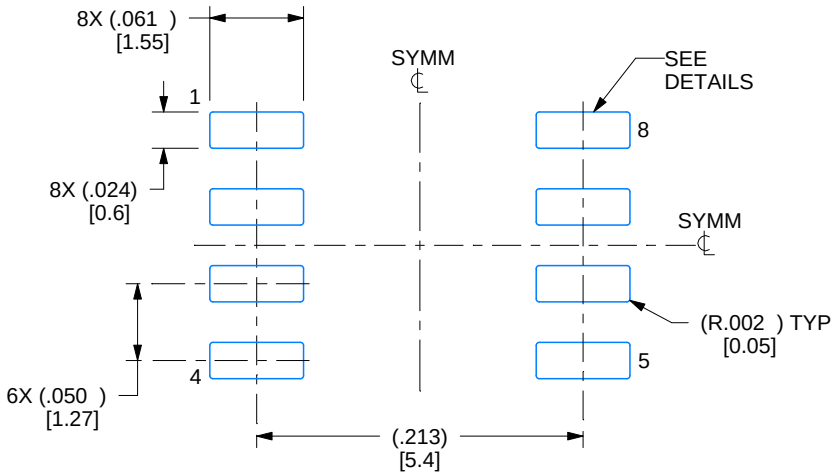
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

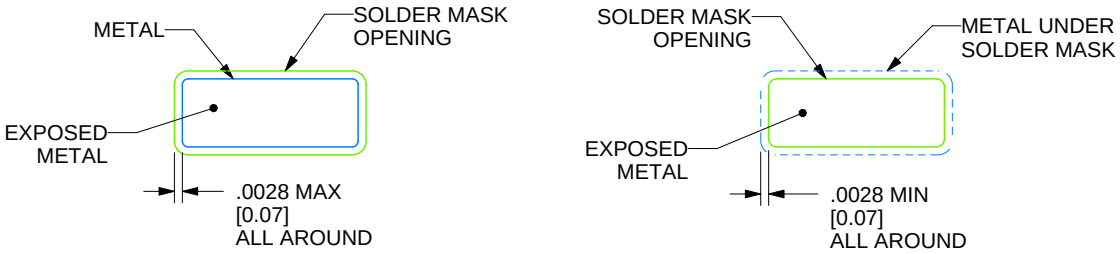


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

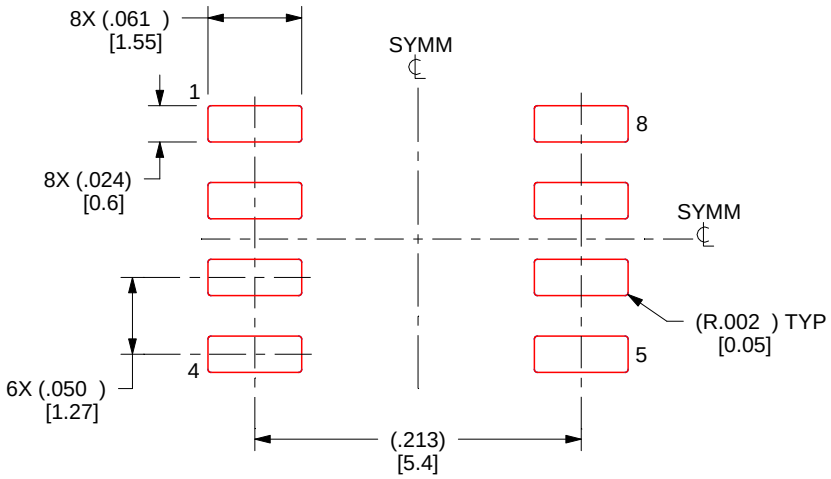
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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