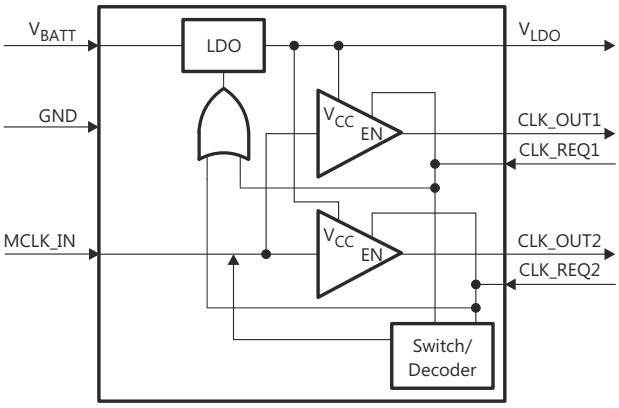
CDC3RL02 低相位噪声双通道时钟扇出缓冲器

1 特性

- 低附加噪声：
  - –149dBc/Hz（10kHz 偏移相位噪声时）
  - 0.37ps (RMS) 输出抖动
- 受限输出压摆率可降低 EMI（对于 10pF 至 50pF 的负载，上升/下降时间为 1ns 至 5ns）
- 自适应输出级控制反射
- 稳压 1.8V 外部可用 I/O 电源
- 超小型 8 凸点 YFP 0.4mm 间距 WCSP（0.8mm × 1.6mm）
- ESD 性能超过 JESD 22
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型（JESD22-C101-A III 级）

2 应用

- 手机
- 全球定位系统 (GPS)
- 无线 LAN
- FM 无线电
- WiMAX
- W-BT



简化版方框图

3 说明

CDC3RL02 是一款双通道时钟扇出缓冲器，适用于需要时钟缓冲以及超低附加相位噪声和扇出功能的便携式终端设备（如手机）。该器件将温度补偿晶体振荡器 (TCXO) 等单个时钟源缓冲至多个外设。该器件具有两个时钟请求输入（CLK_REQ1 和 CLK_REQ2），每个输入均支持单个时钟输出。

CDC3RL02 在主时钟输入 (MCLK_IN) 处接受方波或正弦波，无需交流耦合电容器。可接受的最小正弦波为 0.3V 信号（峰峰值）。CDC3RL02 旨在提供极小的通道间偏斜，附加输出抖动和附加相位噪声。自适应时钟输出缓冲器可在宽电容负荷范围内提供受控的转换率，从而更大限度地降低 EMI 辐射、保持信号完整性，并更大限度地减少由时钟分配线上的信号反射造成的振铃效应。

CDC3RL02 具有集成的低压降 (LDO) 稳压器，该稳压器可接受 2.3V 至 5.5V 的输入电压，可输出 1.8 V、50mA。该 1.8V 电源可从外部获得，从而为 TCXO 等外设提供稳定电源。

CDC3RL02 采用 0.4mm 间距 Die Size Ball Grid Array (DSBGA) 封装 (0.8mm× 1.6mm)，也称为 Wafer-level Chip-scale (WCSP) 封装，并经过优化可实现超低待机电流消耗。

封装信息

器件型号(1)	封装	封装尺寸(2)
CDC3RL02	YFP（DSBGA，8）	0.80mm × 1.60mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

Table of Contents

4 Device Comparison

表 4-1. Device Comparison

T_A	PACKAGE (1)	ORDERABLE PART NUMBER	BACKSIDE COATING (2)
-40°C to 85°C	YFP	CDC3RL02BYFPR	Yes
-40°C to 85° C	YFP	CDC3RL02YFPR	No

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) CSP (DSBGA) devices manufactured with backside coating have an increased resistance to cracking due to the increased physical strength of the package. Devices with backside coating are highly encouraged for new designs.

5 Pin Configuration and Functions

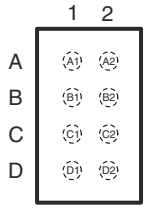


图 5-1. YFP Package 8-Pin DSBGA Top View

表 5-1. Pin Functions

PIN		Type(1)	DESCRIPTION
NAME	NO.		
V_{BATT}	A1	I	Input to internal LDO
CLK_OUT1	A2	O	Clock output 1
V_{LDO}	B1	O	1.8V I/O supply for CDC3RL02 and external TCXO
CLK_REQ1	B2	I	Clock request 1 (from peripheral) for Clock output 1
MCLK_IN	C1	I	Master clock input
CLK_REQ2	C2	I	Clock request 2 (from peripheral) for Clock output 2
GND	D1	–	Ground
CLK_OUT2	D2	O	Clock output 2

(1) I = Input, O = Output

表 5-2. YFP Package Pin Assignments

	1	2
A	V_{BATT}	CLK_OUT1
B	V_{LDO}	CLK_REQ1
C	MCLK_LIN	CLK_REQ2
D	GND	CLK_OUT2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted. (1)

			MIN	MAX	UNIT
V_{BATT}	Voltage range(2)		– 0.3	7	V
	Voltage range(3)	CLK_REQ_1/2, MCLK_IN	– 0.3	V_{BATT} + 0.3	V
		V_{LDO}, CLK_OUT_1/2(2)	– 0.3	V_{BATT} + 0.3	
I_{IK}	Input clamp current at V_{BATT}, CLK_REQ_1/2, and MCLK_IN	V_I < 0		– 50	mA
I_O	Continuous output current	CLK_OUT1/2		±20	mA
	Continuous current through GND, V_{BATT}, V_{LDO}			±50	mA
T_J	Operating virtual junction temperature		– 40	150	°C
T_A	Operating ambient temperature range		– 40	85	°C
T_{stg}	Storage temperature range		– 55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
(3) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{BATT}	Input voltage to internal LDO		2.3	5.5	V
V_I	Input voltage	MCLK_IN, CLK_REQ1/2	0	1.89	V
V_O	Output voltage	CLK_OUT1/2	0	1.8	V
V_{IH}	High-level input voltage	CLK_REQ1/2	1.3	1.89	V
V_{IL}	Low-level input voltage	CLK_REQ1/2	0	0.5	V
I_{OH}	High-level output current, DC current		– 8		mA
I_{OL}	Low-level output current, DC current			8	mA

(1) All unused inputs of the device must be held at V_{CC} or GND to verify proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application note.

6.4 Thermal Information

THERMAL METRIC[1]		CDC3RL02 YFP (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LDO							
V_{OUT}	LDO output voltage	I_{OUT} = 50mA		1.71	1.8	1.89	V
C_{LDO}	External load capacitance			1		10	µF
$I_{OUT(SC)}$	Short circuit output current	R_L = 0Ω			100		mA
$I_{OUT(PK)}$	Peak output current	V_{BATT} = 2.3V, V_{LDO} = V_{OUT} – 5%				100	mA
PSR	Power supply rejection	V_{BATT} = 2.3V, I_{OUT} = 2mA,	f_{IN}= 217Hz and 1kHz	60			dB
			f_{IN}= 3.25MHz	40			
t_{su}	LDO startup time	V_{BATT} = 2.3V, C_{LDO} = 1 µF, CLK_REQ_n to V_{IH} = 1.71V			0.2		ms
		V_{BATT} = 5.5V, C_{LDO} = 10 µF, CLK_REQ_n to V_{IH} = 1.71V				1	
POWER CONSUMPTION							
I_{SB}	Standby current	Device in standby (all $V_{CLK\_REQ\_n}$ = 0V)			0.2	1	µA
I_{CCS}	Static current consumption	Device active but not switching			0.4	1	mA
I_{OB}	Output buffer average current	f_{IN} = 26MHz, C_{LOAD} = 50pF			4.2		mA
C_{PD}	Output power dissipation capacitance	f_{IN} = 26MHz				44	pF
MCLK_IN INPUT							
I_I	MCLK_IN, CLK_REQ_1/2 leakage current	V_I = V_{IH} or GND				1	µA
C_I	MCLK_IN capacitance	f_{IN} = 26MHz			4.75		pF
R_I	MCLK_IN impedance	f_{IN} = 26MHz			6		kΩ
f_{IN}	MCLK_IN frequency range			10	26	100	MHz
MCLK_IN LVCMOS SOURCE							
	Additive phase noise	f_{IN} = 26MHz, $t_r/t_f \leqslant$ 1ns	1kHz offset		–140		dBc/Hz
			10kHz offset		–149		
			100kHz offset		–153		
			1MHz offset		–148		
	Additive jitter	f_{IN} = 26MHz, V_{PP} = 0.8V, BW = 10MHz to 5MHz			0.37		ps (rms)
t_{DL}	MCLK_IN to CLK_OUT_n propagation delay				11		ns
DC_L	Output duty cycle	f_{IN} = 26MHz, DC_{IN} = 50%		45%	50%	55%	

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MCLK_IN SINUSOIDAL SOURCE							
V_{MA}	Input amplitude			0.3		1.8	V
	Additive phase noise	f_{IN} = 26MHz, V_{MA} = 1.8V_{PP}	1kHz offset		–141		dBc/Hz
			10kHz offset		–149		
			100kHz offset		–152		
			1MHz offset		–148		
		f_{IN} = 26MHz, V_{MA} = 0.8V_{PP}	1kHz offset		–139		
			10kHz offset		–146		
			100kHz offset		–150		
			1MHz offset		–146		
	Additive jitter	f_{IN} = 26MHz, V_{MA} = 1.8V_{PP}, BW = 10MHz to 5MHz			0.41		ps (RMS)
t_{DS}	MCLK_IN to CLK_OUT_1/2 propagation delay				12		ns
DC_s	Output duty cycle	f_{IN} = 26MHz, V_{MA} > 1.8V_{PP}		45%	50%	55%	
CLK_OUT_N OUTPUTS							
t_r	20% to 80% rise time	C_L = 10pF to 50pF		1		5.2	ns
t_f	20% to 80% fall time	C_L = 10pF to 50pF		1		5.2	ns
t_{sk}	Channel-to-channel skew	C_L = 10pF to 50pF (C_{L1} = C_{L2})		–0.5		0.5	ns
V_{OH}	High-level output voltage	I_{OH} = –100 µA, reference to V_{LDO}		–0.1			V
		I_{OH} = –8mA		1.2			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA				0.2	V
		I_{OL} = 8mA				0.55	

6.6 Typical Characteristics

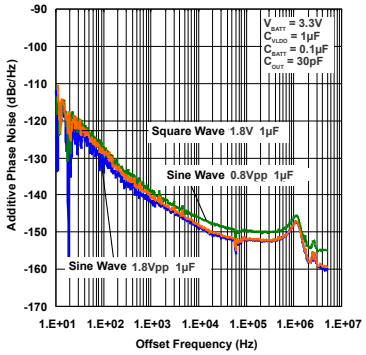


图 6-1. Additive Phase Noise vs Offset Frequency

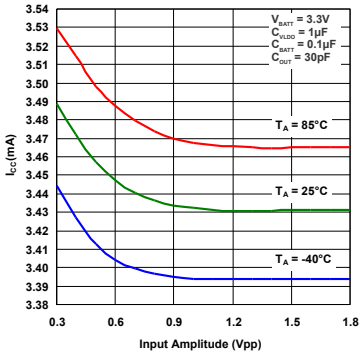


图 6-2. Supply Current vs Input Amplitude

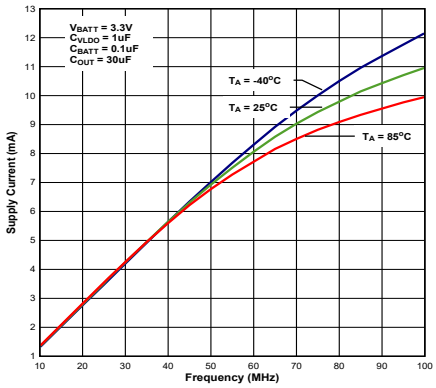


图 6-3. Supply Current vs Input Frequency

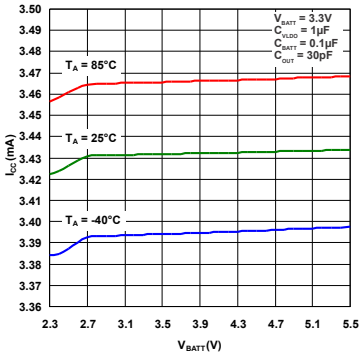


图 6-4. Supply Current vs Supply Voltage

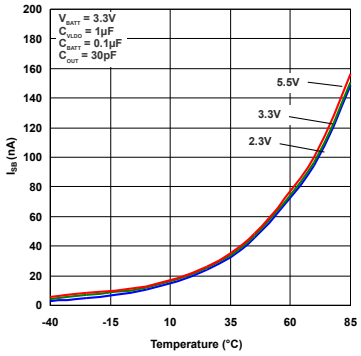


图 6-5. Standby Current vs Temperature

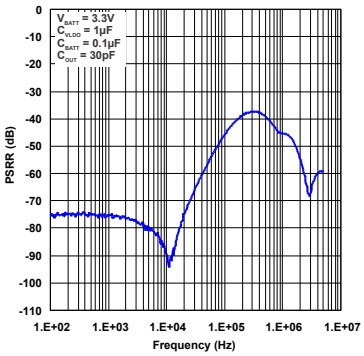


图 6-6. Power Supply Rejection vs Input Frequency

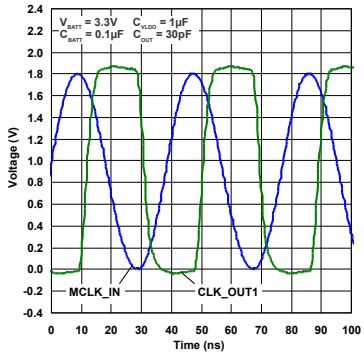


图 6-7. Sine-Wave Input vs Square-Wave Output

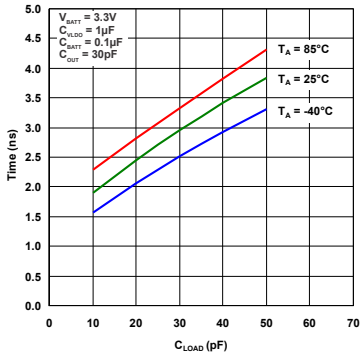


图 6-8. Rise Time vs Load

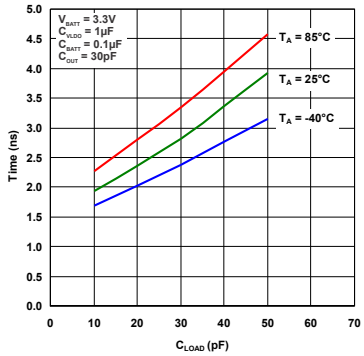


图 6-9. Fall Time vs Load

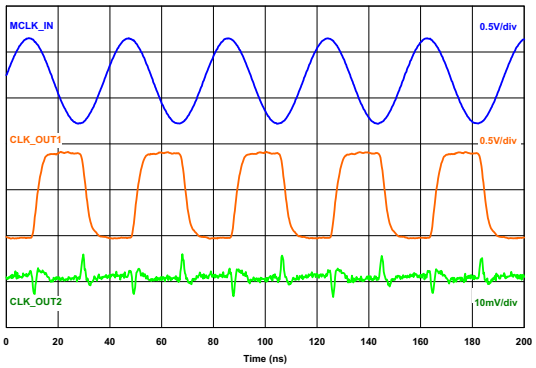


图 6-10. Digital Cross-Talk Scope Shot

7 Detailed Description

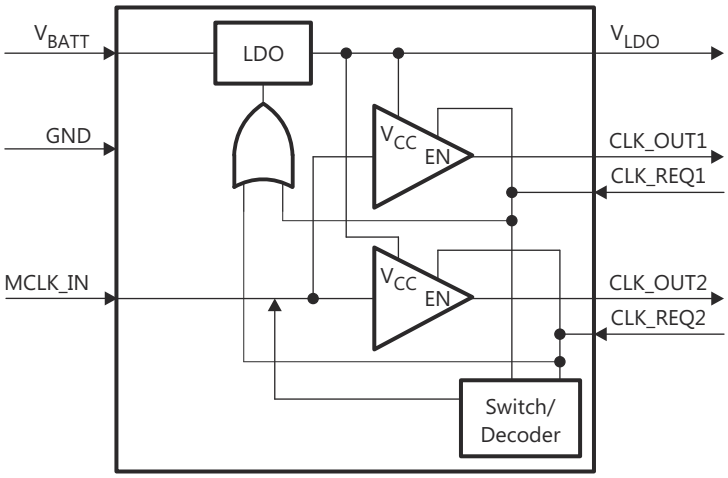
7.1 Overview

The CDC3RL02 is a two-channel clock fan-out buffer and is designed for use in portable end-equipment, such as mobile phones, that require clock buffering with minimal additive phase noise and fan-out capabilities. The device buffers a single master clock, such as a temperature compensated crystal oscillator (TCXO) to multiple peripherals. The device has two clock request inputs (CLK_REQ1 and CLK_REQ2), each of which enable a single clock output.

The CDC3RL02 accepts square or sine waves at the master clock input (MCLK_IN), eliminating the need for an AC coupling capacitor. The smallest acceptable sine wave is a 0.3V signal (peak-to-peak). CDC3RL02 is designed to offer minimal channel-to-channel skew, additive output jitter, and additive phase noise. The adaptive clock output buffers offer controlled slew-rate over a wide capacitive loading range which minimizes EMI emissions, maintains signal integrity, and minimizes ringing caused by signal reflections on the clock distribution lines.

The CDC3RL02 has an integrated Low-Drop-Out (LDO) voltage regulator which accepts input voltages from 2.3V to 5.5V and outputs 1.8V, 50mA. This 1.8V supply is externally available to provide regulated power to peripheral devices such as a TCXO.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low Additive Noise

The CDC3RL02 features –149dBc/Hz at 10kHz offset phase noise and 0.37ps (RMS) of output jitter, to provide low noise buffered signals.

7.3.2 Regulated 1.8V Externally Available I/O Supply

The CDC3RL02 allows users to connect to the output of the internal LDO, for providing power to other ICs. For more information, refer to *LDO*.

7.3.3 Ultra-Small 8-bump YFP 0.4mm Pitch WCSP Package

Using the ultra-small YFP package, the CDC3RL02 is very small and allows the device to be placed on a board with minimum work.

7.4 Device Functional Modes

表 7-1 is the function table for CDC3RL02.

表 7-1. Function Table

INPUTS			OUTPUTS	
CLK_REQ1(1)	CLK_REQ2(1)	MCLK_IN	CLK_OUT1	CLK_OUT2
L	L	X	L	L
L	H	CLK	L	CLK
H	L	CLK	CLK	L
H	H	CLK	CLK	CLK

(1) If a CLK_OUT is always enabled, tying the CLK_REQ pin to an external 1.8V source (not VLDO) is acceptable.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Input Clock Squarer

图 8-1 shows the input stage of the CDC3RL02. The input signal at MCLK_IN can be a square wave or sine wave. C_{MCLK} is an internal AC coupling capacitor that allows a direct connection from the TCXO to the CDC3RL02 without an external capacitor.

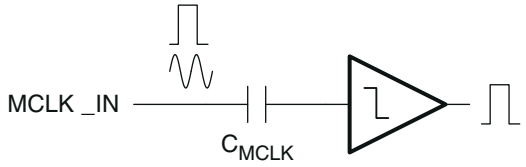


图 8-1. Input Stage With Internal AC Coupling Capacitor

Any external component added in the series path of the clock signal potentially adds phase noise and jitter. The error source associated with the internal decoupling capacitor is included in the specification of the CDC3RL02. The recommended clock frequency band of the CDC3RL02 is 10MHz to 80MHz for specified functionality. All performance metrics are specified at 26MHz. The lowest acceptable sinusoidal signal amplitude is $0.8V_{PP}$ for specified performance. Amplitudes as low as $0.3V_{PP}$ are acceptable but with reduced phase-noise and jitter performance.

8.1.2 Output Stage

Each output drives 1.8V LVCMOS levels. Adaptive output buffers limit the rise/fall time of the output to within 1ns to 5ns with load capacitance between 10pF and 50pF. Fast slew rates introduce EMI into the system. Each output buffer limits EMI by keeping the rise/fall time above 1ns. Slow rise/fall times can induce additive phase noise and duty cycle errors in the load device. The output buffer limits these errors by keeping the rise/fall time below 5ns. In addition, the output stage dynamically alters impedance based on the instantaneous voltage level of the output. This dynamic change limits reflections keeping the output signal monotonic during transitions. Each output is active low when not requested to avoid false clocking of the load device.

8.1.3 LDO

A low noise 1.8V LDO is integrated to provide the I/O supply for the output buffers. The LDO output is externally available to power a clock source such as a TCXO. A clean supply is provided to the clock buffers and the clock source for optimum phase noise performance. The input range of the LDO allows the device to be powered

directly from a single cell Li battery. The LDO is enabled by either of the CLK_REQ_N signals. When disabled, the device enters a low power shutdown mode consuming less than 1 µA from the battery. The LDO requires an output decoupling capacitor in the range of 1 µF to 10 µF with an equivalent series resistance (ESR) of at least 0.1 Ω for compensation and high-frequency PSR. This capacitor must stay within the specified range for capacitance and ESR over the entire operating temperature range. A ceramic capacitor can be used if a small external resistance is added in series with the capacitor to increase the effective ESR. An input bypass capacitor of 1 µF or larger is recommended.

8.2 Typical Application

The CDC3RL02 is designed for use in mobile applications as shown in 图 8-2. In this example, a single low noise TCXO system clock source is buffered to drive a mobile GPS receiver and WLAN transceiver. Each peripheral independently requests an active clock by asserting a single clock request line (CLK_REQ_1 or CLK_REQ_2). When both clock request lines are inactive, the CDC3RL02 enters a low current shutdown mode. In this mode, the LDO output, CLK_OUT_1, and CLK_OUT_2 are pulled to GND and the TCXO is not powered.

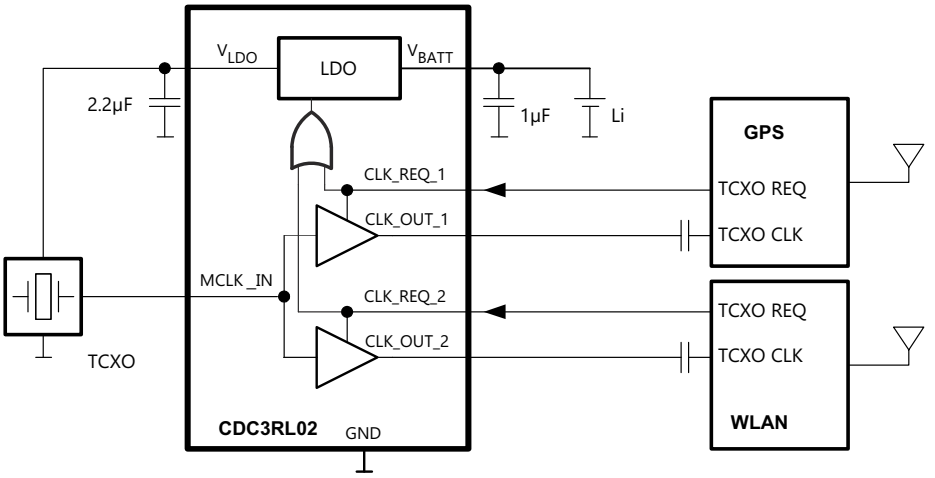


图 8-2. Mobile Application

When either peripheral requests the clock, the CDC3RL02 enables the LDO and powers the TCXO. The TCXO output (square wave, sine wave, or clipped sine wave) is converted to a square wave and buffered to the requested output.

8.2.1 Design Requirements

For the typical application, the user must know the following parameters.

表 8-1. Design Parameters

PARAMETER	DESCRIPTION	EXAMPLE VALUE
V_{BATT}	Input voltage from battery or power supply	3.7V
MCLK_IN	Input frequency from a TCXO	26MHz

8.2.2 Detailed Design Procedure

The designer must verify that all parameters are within the ranges specified in *Recommended Operating Conditions.*

Each device which receives a clock output from the CDC3RL02 must have the CLK request pin connected to the appropriate CLK_REQ pin on the CDC3RL02. This pin enables the output buffer when a device requests the clock signal.

Control of the clock outputs is possible by using a GPIO from a controller to control the CLK_REQ pins.

If one of the outputs is unused, then tie the CLK_REQ and CLK_OUT pins to ground. If the user wants a CLK_OUT pin always enabled, tie the paired CLK_REQ pin to an external 1.8V source (not V_{LDO} because the LDO output is not enabled until at least one CLK_REQ pin is high).

8.2.3 Application Curve

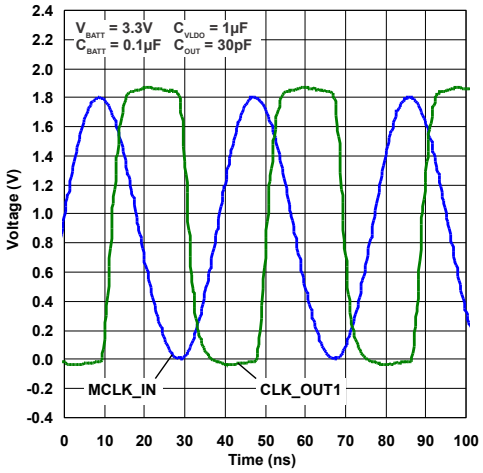


图 8-3. Sine Wave Input vs Output

8.3 Power Supply Recommendations

General power supply recommendations are to be considered for the CDC3RL02. These include:

- Decoupling capacitors placed close to the V_{BATT} pin of typical values (1 µ F)
- V_{BATT} be within the recommended voltage range

8.4 Layout

8.4.1 Layout Guidelines

To provide reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies and must be placed as close as possible to the V_{BATT} pin
- Short trace-lengths must be used to avoid excessive loading
- For improved performance on the clock output lines, use a ground trace on the sides of the clock trace to minimize crosstalk and EMI

8.4.2 Layout Example

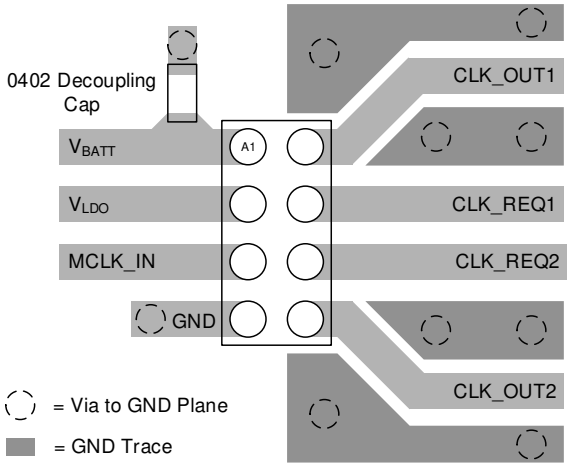


图 8-4. Example Layout for YFP Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, AN-2028 LMH2191 Evaluation Board, compatible EVM user's guide

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (November 2022) to Revision H (October 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated the Electrical Characteristics for increased 100MHz MCLK_IN maximum frequency	5

Changes from Revision F (August 2019) to Revision G (November 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed MCLK_IN frequency maximum value from: 54MHz to: 80MHz	5
• Changed the x-axis range in 图 6-3	7
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	13

Changes from Revision E (August 2018) to Revision F (August 2019) **Page**

- Changed MCLK_IN frequency maximum value from: 52MHz to: 54MHz..... 5

Changes from Revision D (April 2017) to Revision E (August 2018) **Page**

- Changed V_{LDO} test conditions to V_{IH} conditions in the *Electrical Characteristics* table 5
- Added a tablenote to the *Function Table* 10
- Added content to the *LDO* section 10
- Changed the last sentence in the *Detailed Design Procedure* section 12

Changes from Revision C (January 2016) to Revision D (April 2017) **Page**

- Updated clock request descriptions in the *Pin Functions* table..... 3
- Added *Receiving Notification of Documentation Updates* section.....14

Changes from Revision B (December 2015) to Revision C (January 2016) **Page**

- Added the *Device Comparison* 3

Changes from Revision A (September 2015) to Revision B (November 2015) **Page**

- 添加了*热性能信息* 表、*概述*、*特性说明* 部分、*电源相关建议* 部分和*布局* 部分.....1

Changes from Revision * (November 2009) to Revision A (September 2015) **Page**

- 根据新标准更新了文档格式..... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC3RL02BYFPR	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02BYFPR.A	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02BYFPR.B	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02YFPR	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02YFPR.A	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02YFPR.B	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

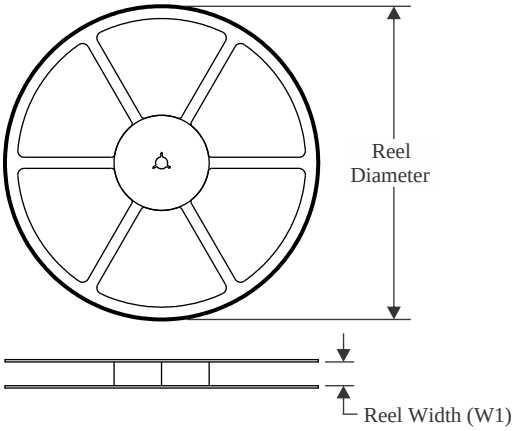
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

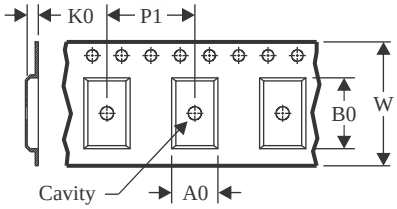
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

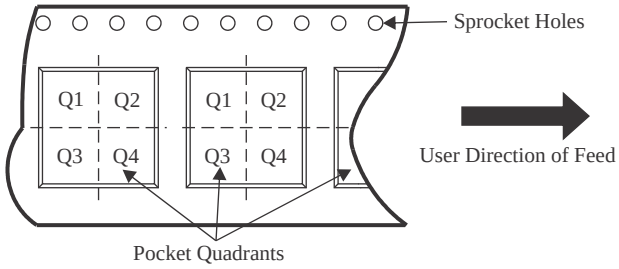


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

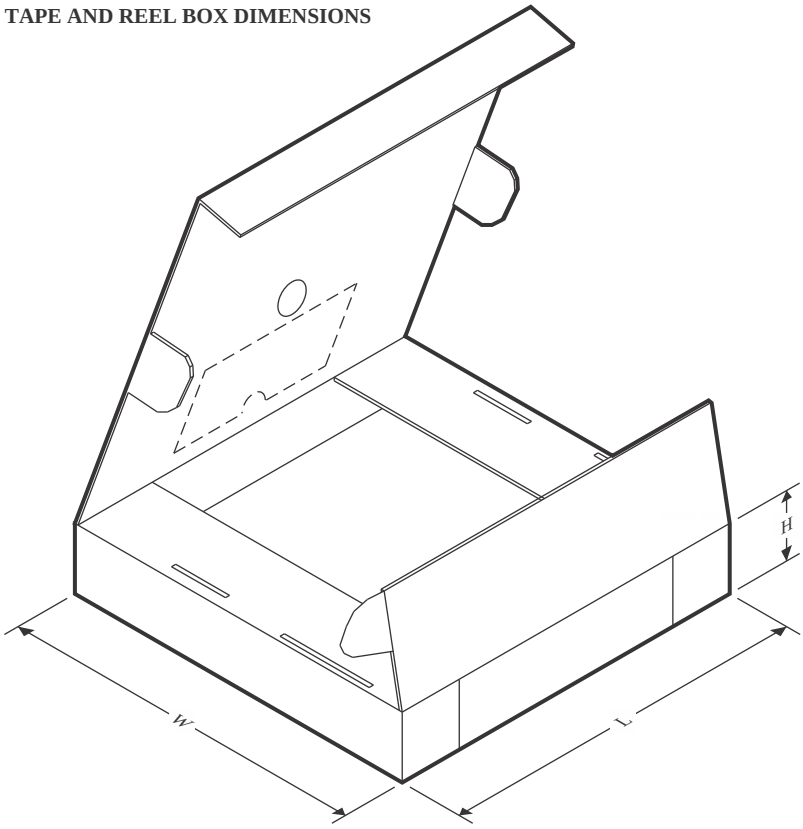
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

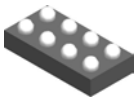
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC3RL02BYFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
CDC3RL02YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC3RL02BYFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
CDC3RL02YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

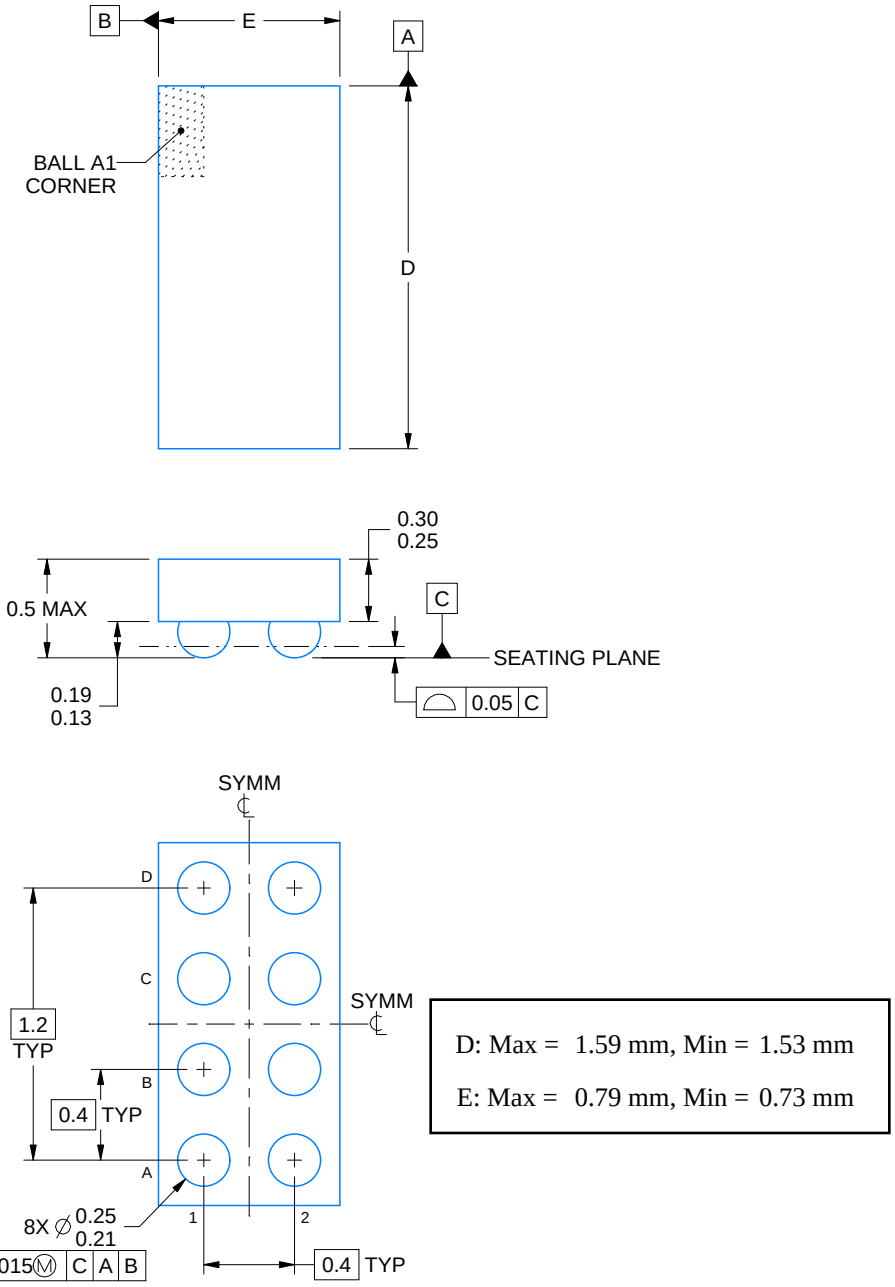


PACKAGE OUTLINE

YFP0008

DSBGA - 0.5 mm max height

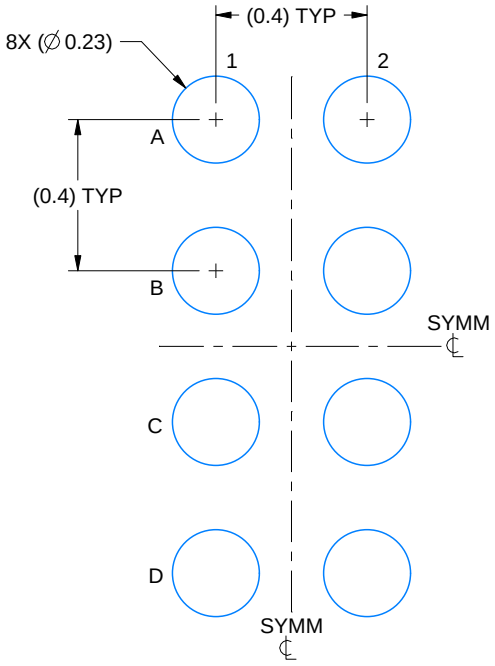
DIE SIZE BALL GRID ARRAY



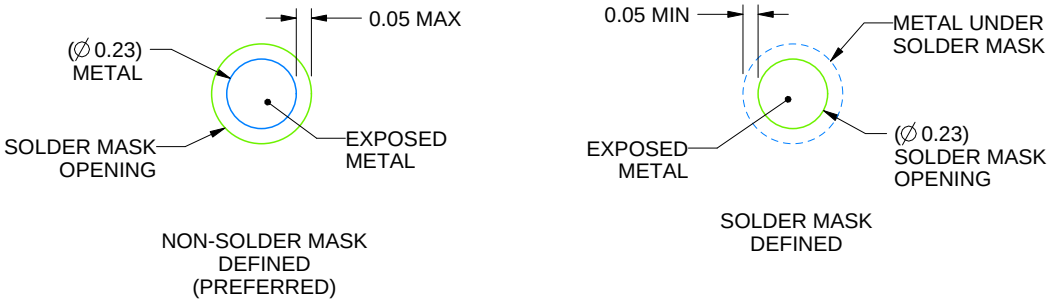
4225242/A 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

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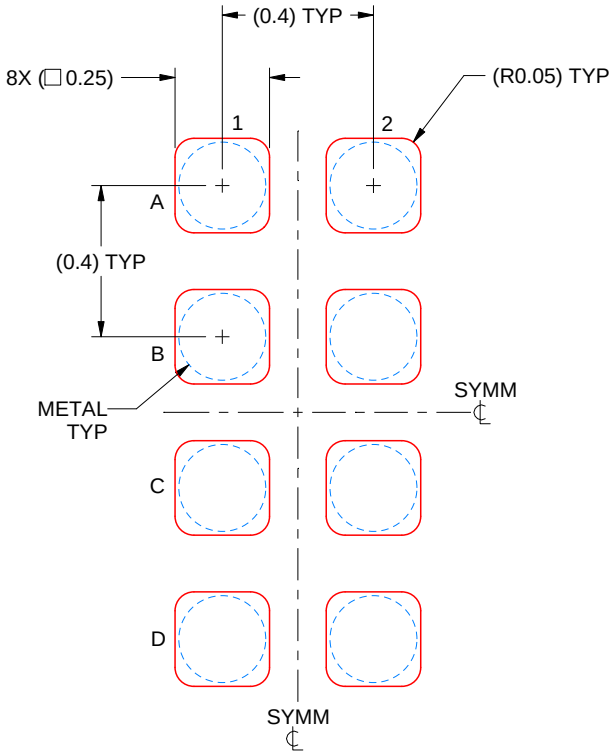
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最后更新日期：2025 年 10 月