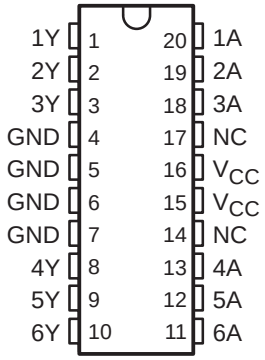
- **CDC204 Replaces 74AC11204**
- **Low-Skew Propagation Delay Specifications for Clock-Driver Applications**
- **CMOS-Compatible Inputs and Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Package (DW))**

DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

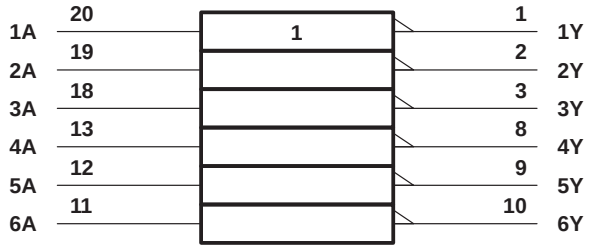
The CDC204 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$. It is designed specifically for applications requiring low skew between switching outputs.

The CDC204 is characterized for operation from T_A = 25°C to 70°C.

FUNCTION TABLE

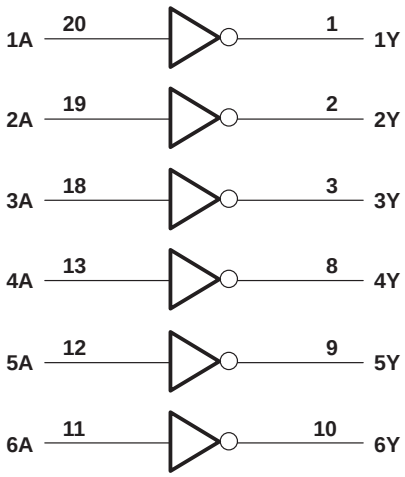
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±150 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.6 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	V_{CC} = 4.75 V	3.3			V
		V_{CC} = 5.25 V	3.7			
V_{IL}	Low-level input voltage	V_{CC} = 4.75 V			1.4	V
		V_{CC} = 5.25 V			1.6	
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.75 V			–24	mA
		V_{CC} = 5.25 V			–24	
I_{OL}	Low-level output current	V_{CC} = 4.75 V			24	mA
		V_{CC} = 5.25 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
f_{clock}	Input clock frequency				80	MHz
T_A	Operating free-air temperature		25		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level voltage output	I_{OH} = – 50 µA	V_{CC} = 4.75 V	25°C	4.65			V
				Full range	4.65			
			V_{CC} = 5.25 V	25°C	5.15			
				Full range	5.15			
		I_{OH} = – 24 mA	V_{CC} = 4.75 V	25°C	4.19			
				Full range	4.05			
			V_{CC} = 5.25 V	25°C	4.68			
				Full range	4.55			
		I_{OH} = –75 mA‡,	V_{CC} = 5.25 V	Full range	3.6			
V_{OL}	Low-level voltage output	I_{OL} = 50 µA	V_{CC} = 4.75 V	25°C			0.1	V
				Full range			0.1	
			V_{CC} = 5.25 V	25°C			0.1	
				Full range			0.1	
		I_{OL} = 24 mA	V_{CC} = 4.75 V	25°C			0.36	
				Full range			0.44	
			V_{CC} = 5.25 V	25°C			0.36	
				Full range			0.44	
		I_{OL} = 75 mA‡,	V_{CC} = 5.25 V	Full range			1.65	
I_I	Input current	V_I = V_{CC} or GND	V_{CC} = 5.25 V	25°C			±0.1	µA
				Full range			±1	
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 5.25 V,	25°C			4	µA
				Full range			40	
C_i	Input capacitance	V_I = V_{CC} or GND,	V_{CC} = 5 V	25°C		4		pF

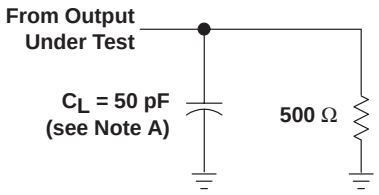
† Full range is T_A = 25°C to 70°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.25 V (see Note 3 and Figures 1 and 2)

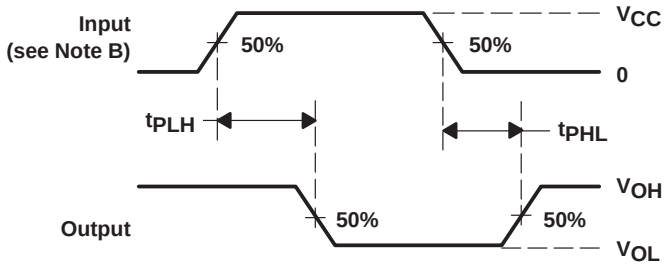
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level (see Figure 1)	A	Y	3.7	5.7	ns
t_{PHL}	Proagation delay time, high-to-low level (see Figure 1)			2.9	5.7	
$t_{sk(o)}$	Output skew time (see Figure 2)	A	Y		1	ns

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

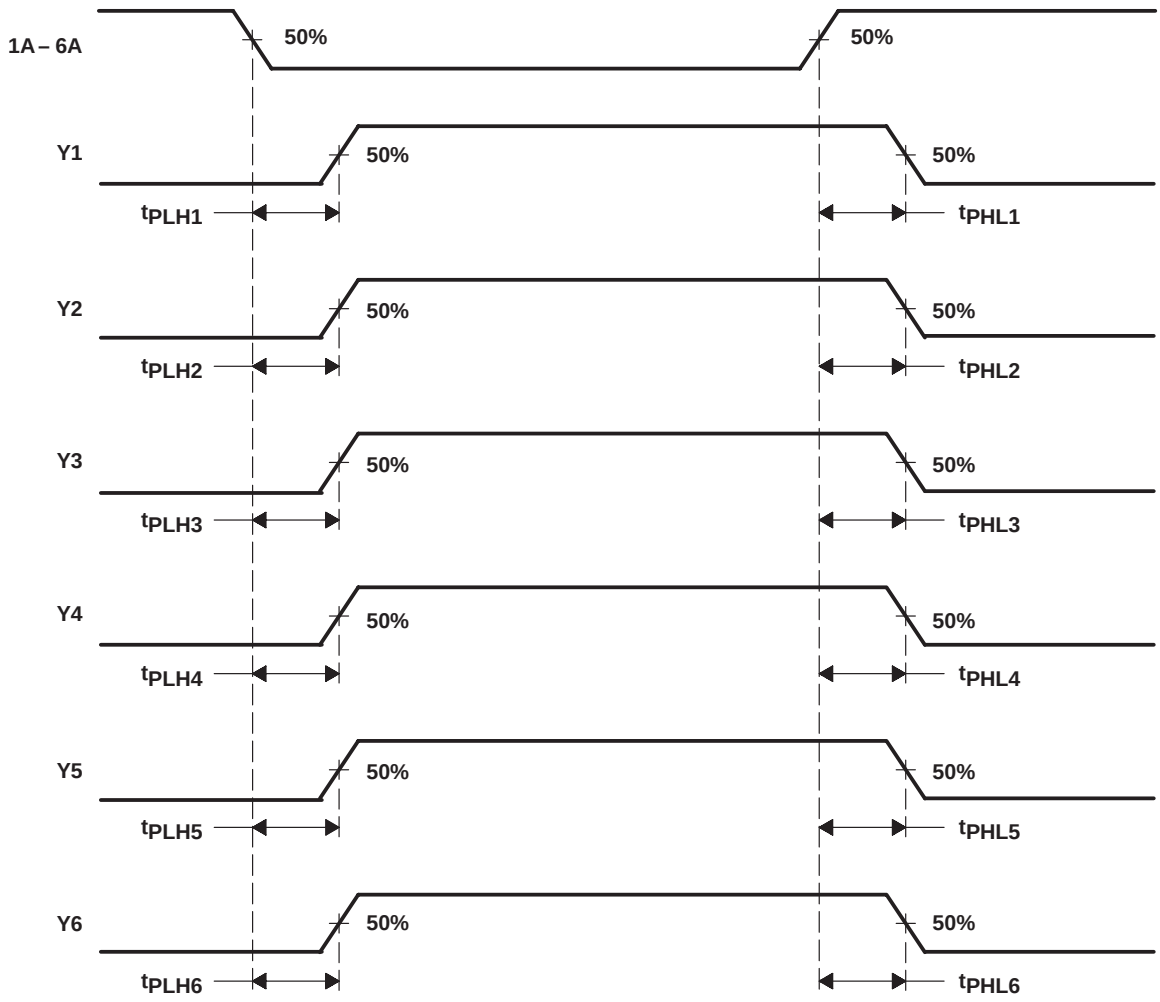


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 6)
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 6)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC204DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	25 to 70	CDC204
CDC204DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	25 to 70	CDC204
CDC204DWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	25 to 70	CDC204

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

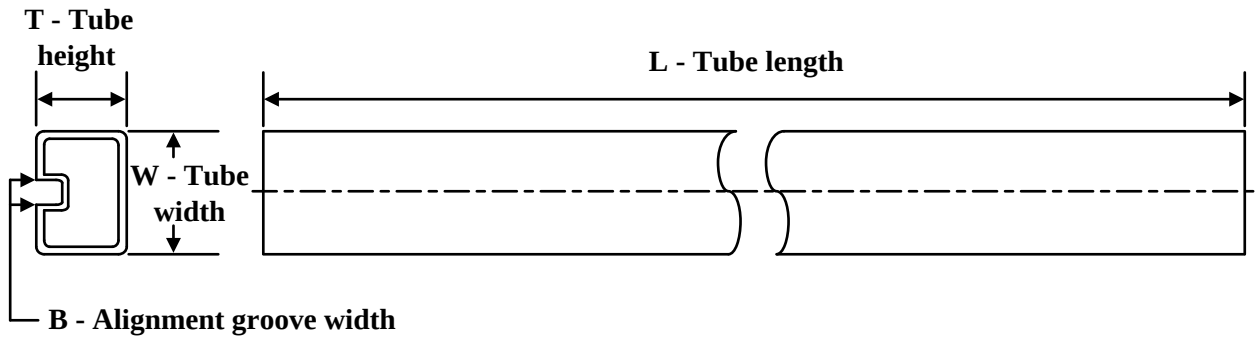
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC204DW	DW	SOIC	20	25	507	12.83	5080	6.6
CDC204DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
CDC204DWG4	DW	SOIC	20	25	507	12.83	5080	6.6

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